UCL Université catholique de Louvain

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Engineered Si-based substrate for RF applications

Dissertation presented by
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Contents

Acronyms

3G	Third generation mobile networks
4G	Fourth generation mobile networks
5G	Fifth generation mobile networks
AAO	Anodic aluminum oxide
BOX	Buried oxide
CMOS	Complementary metal–oxide–semiconductor
CPW	Coplanar waveguide
DI	De-ionized
DRIE	Deep reactive-ion etching
HF	Hydrofluoric acid
HR	High-resistivity
HR-SOI	High-resistivity silicon-on-insulator
IC	Integrated circuit
IPA	Isopropanol
LP	Large pattern
LPCVD	Low-pressure chemical vapor deposition
LTE	Long-Term Evolution
MACE	Metal-assisted chemical etching
MOS	Metal–oxide–semiconductor
NO	Native oxide
NP	Nanoparticle
NSL	Nanosphere lithography
NW	Nanowire
POx	Plasma oxide
PSC	Parasitic surface conduction
PSi	Porous silicon
PVD	Physical vapor deposition
RF	Radio frequency
RFFE	Radio frequency front-end

RIE Reactive-ion etching
SCP Small continuous pattern
SEM Scanning electron microscope
SoC System-on-chip
SOI Silicon-on-insulator
SOQ Silicon-on-quartz
SOS Silicon-on-sapphire
SRF Self-resonant frequency
SSP Small separate pattern
TR Trap-rich
TSV Through silicon via
VNA Vector network analyzer

Symbols

D_{it}	Interface traps density	[cm^{-2}]
d_{NP}	Mean nanoparticle diameter	[nm]
d_{pore}	Pore depth	[µm]
ε_{eff}	Effective relative permittivity of the substrate	[$-$]
$\varepsilon_{\text{pore}}$	Relative permittivity of the pores	[$-$]
ε_r	Bulk relative permittivity of the substrate	[$-$]
f	Frequency	[Hz]
N_D	Donor atoms concentration	[cm^{-3}]
p_{pore}	Pore pitch	[µm]
Q_{OX}	Fixed oxide charge density	[cm^{-2}]
ρ_{eff}	Effective resistivity of the substrate	[Ω·cm]
ρ	MACE electrolyte molar ratio	[%]
ρ_0	Bulk resistivity of the substrate	[Ω·cm]
r_{ind}	Inductor radius	[µm]
r_{sub}	Substrate radius	[µm]
t_{BOX}	Buried oxide thickness	[µm]
T	Temperature	[°C]
t_{ind}	Inductor thickness	[µm]
t_{PSC}	PSC layer thickness	[µm]
t_{sub}	Substrate thickness	[µm]
w_{ind}	Inductor width	[µm]
w_{pore}	Pore width	[µm]

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Chapter 1

Introduction

In today's world, connectivity represents an important aspect of our everyday life. We are all surrounded with a growing number of connected electronic devices – smartphones, portable computers and soon various objects linked to the Internet of Things. They are providing a wide range of useful features such as instant access to information, world-wide audio and video calls, and multimedia streaming services. However, the evolution of consumer electronics is headed in one general direction: faster devices with higher data rates. In addition to the growing number of devices, this creates an exponential growth of the global network's bandwidth [1].

To accommodate for growing demands in network speed, mobile telecommunication standards are evolving quickly: third generation (3G), fourth generation (4G) and Long-Term Evolution (LTE) mobile networks. However, the spectral efficiencies are already close to the theoretical limits of the sub-3 GHz spectrum [1]. At the current state, millimeter-wave communications are investigated for high-data-bandwidth applications. Millimeter-wave bands ($3-60$ GHz) are considered for future fifth generation (5G) cellular networks [2] and multi-gigabit wireless LAN networks (IEEE 802.11ad [3]). The semiconductor industry must follow the trend and provide telecommunication systems able to respond to those demands with higher data rates, better spectral efficiency, and improved coverage [4].

1.1 RF circuits

A typical example of radio frequency (RF) integrated circuit (IC) is the radio frequency front-end (RFFE) module, found on any wireless communication device. The module connects the transceiver to the antenna and is optimized with respect to the device's RF performances. A RFFE block diagram for the LTE standard is shown in Figure 1.1. The system is composed of several key components, active and passive: switches, amplifiers and filters. The main specifications for those components are: linearity, insertion losses, power efficiency, tunability, quality factor and temperature stability [5].

Originally, gallium arsenide (GaAs) was used as the semiconductor of choice for RF applications. Its advantages over silicon (Si) are higher mobility, low RF losses and high linearity. However, with the scaling down of transistor sizes, Si-based ICs have become competitive for RF applications as well [7]. Especially in consumer electronics, the lower fabrication and wafer costs of Si technology, and compatibility with CMOS processing are the main advantages.

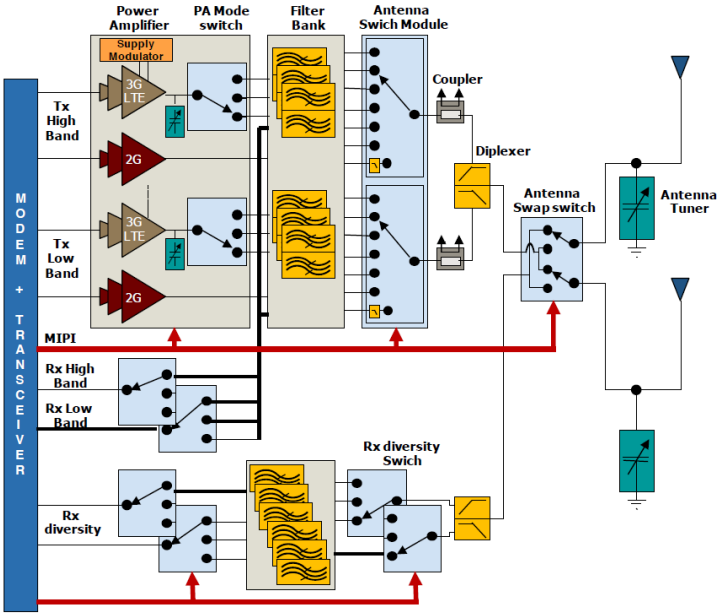

Figure 1.1: Front-end module block diagram for LTE [6].

1.2 RF substrates

With the decrease of GaAs-based RF-ICs, Si-based substrates became mainstream in the last several years in the RF domain (see Figure 1.2). The substrates need to posses the following main characteristics to be compatible with RF systems: high resistivity, linearity and good thermal conductivity. Bulk silicon has poor RF properties such as linearity and signal loss. Bulk Si substrates are therefore mostly used for systems requiring low RF performances or high integration with digital circuits. Several Si-based substrates have thus been introduced during the last 20 years with enhanced RF properties: silicon-on-insulator (SOI) [9], high-resistivity (HR) SOI [10], and finally trap-rich (TR) HR-SOI [11]. Another type of oxide-based substrates – silicon-on-sapphire (SOS) and silicon-on-quartz (SOQ) have also been used for their great electrical

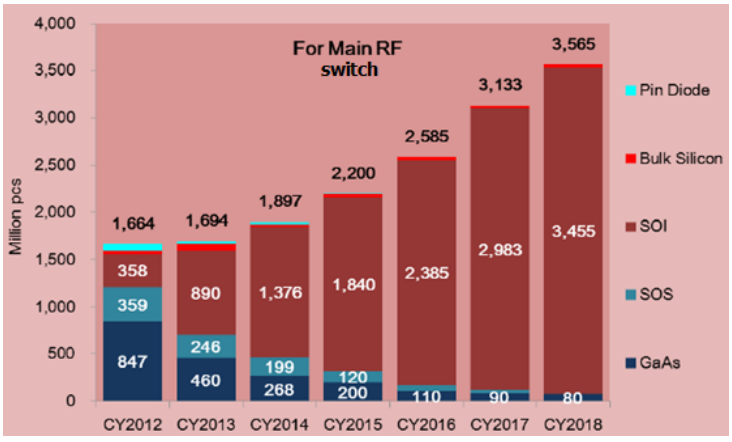

Figure 1.2: Rapid adoption of trap-rich SOI substrate for RF switches [8].

and thermal properties [12]. However, despite being perfect for RF applications, the fabrication and the integration costs are much higher than Si-based substrates.

Recently, porous silicon (PSi) has gained interest as a low-cost material for future RF substrates. Extracted parameters from measurements of coplanar waveguide (CPW) lines fabricated by Belaroussi et al. [13] on thick porous Si layers are shown in Figure 1.3. PSi presents great RF characteristics in comparison to other Si-based substrates. The effective resistivity, attenuation losses and linearity are better than TR HR-SOI. Moreover, PSi substrates possess inherent low dielectric constant, ranging between 2 and 4 with varying porosities [14]. The low permittivity, not achievable for SOI-like substrates, increases the operating frequency range of passive inductors. Similar results were also reported by Sarafis et al. [15].

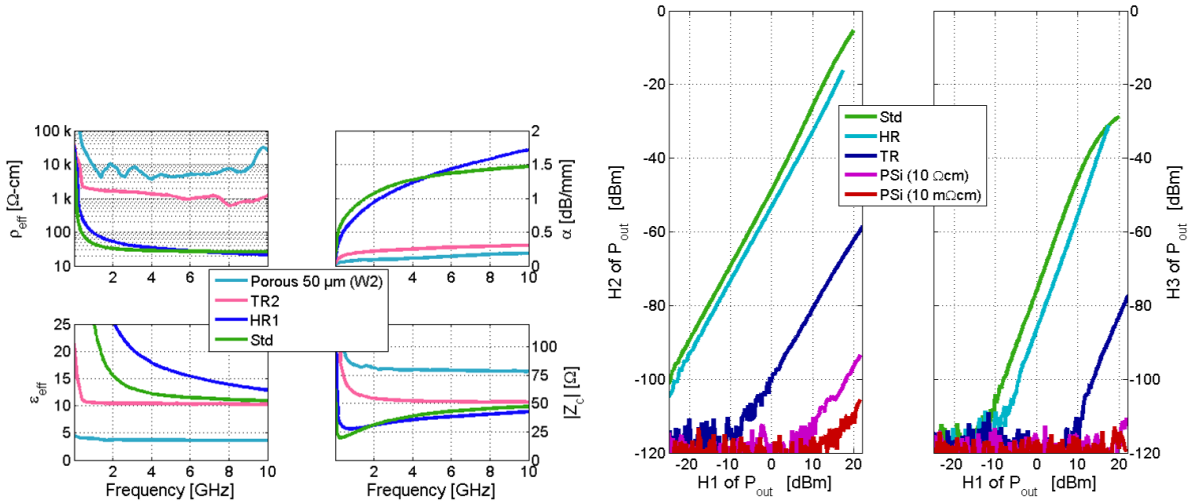

Figure 1.3: Extracted small-signal and large-signal parameters of CPW lines fabricated on different Si-based substrates. Adapted from [13].

The current challenge of PSi substrates lies in the integration with standard CMOS processes. On the one hand, porosification can be done before the fabrication of RF devices [15, 16]. Typically, a bulk silicon substrate is partially porosified by anodization, an insulating SiO_2 layer is deposited and the devices fabricated above. However, porous Si does not withstand high temperature treatments. Internal stresses appear and induce strains that can lead to undesired buckling of the substrate [17]. The approach is therefore not compatible with CMOS processes.

On the other hand, porosification can be done as a post-CMOS process [18, 19]. PSi is grown selectively from the font-side in bulk Si substrates, forming porous islands under critical areas. However, the approach is design-dependent and no techniques have yet been reported for the porosification of SOI substrates from the back-side as a post-CMOS process.

1.3 Scope of the work

The characteristics of the different RF substrates are summarized in Table 1.1. Porous silicon has been demonstrated as an excellent RF substrate candidate in all aspects, except for the integration with CMOS technology. This issue is addressed in this work by elaborating several fabrication procedures. The processes consist of post-CMOS porosification of Si-based, SOI-like substrates by electroless etching techniques. The experimental part of this work was done at WINFAB[1], the micro- and nanofabrication platform of UCL.

In the following chapters, the trenched substrate design is presented first. Chapter 2 and Chapter 3 are devoted to semiconductor and electromagnetic simulations. In Chapter 2, effective parameters are extracted from CPW line simulations as function of the trenches' morphology and substrate's characteristics. The impact of parasitic oxide charges and interface traps is studied. In Chapter 3, an integrated inductor is simulated on the trenched substrate. The inductor's quality factor is extracted as function of the substrate's characteristics. A homogeneous substrate with effective parameters, and a heterogeneous substrate with actual trench geometry are compared. Finally, in Chapter 4 the fabrication process for the trenched substrate by metal-assisted chemical etching is described. The numerous etching parameters are studied with their impact on the etching results.

The second process, described in Chapter 5, was designed for the substrate's porosification by metal-assisted chemical etching with gold nanoparticles. First, the deposition of the nanoparticles is detailed with the selection of the most suited technique for this application. And second, the actual etching results are presented and compared to similar results found in literature.

The third and last process is described in Chapter 6. The techniques of galvanic etching and lateral porosification are combined into an innovative fabrication process. The two main steps of trench formation by DRIE and porous silicon formation by galvanic etching are explained in detail. The feasibility of the process is demonstrated with the first fabrication results.

Finally, a general conclusion about the design and fabrication of trenched and porous Si-based substrates for RF applications is proposed, in addition to future research perspectives.

[1] Wallonia Infrastructure Nano FABrication – http://www.uclouvain.be/en-winfab

Table 1.1: List of substrate's parameters to fulfil for the integration of RFFE in SoCs. Question mark indicates the possibility to fulfil the specified characteristic under certain conditions. Inspired from [7].

	SOI	HR-SOI	SOS SOQ	Trap-rich HR-SOI	PSi
Compatibility with CMOS technology	✔	✔	✔	✔	?
Low RF losses ($\rho > 3\,\mathrm{k\Omega{\cdot}cm}$)	✗	✗	✔	✔	✔
Low crosstalk ($f < 10\,\mathrm{GHz}$)	✗	✗	✔	✔	✔
Linearity ($< -70\,\mathrm{dBc}$ @ $35\,\mathrm{dBm}$)	✗	✗	✔	✔	✔
High quality passive devices ($\rho > 1\,\mathrm{k\Omega{\cdot}cm}$)	✗	?	✔	✔	✔
Large-bandwidth passive devices (low ε_r)	✗	✗	✔	✗	✔
Availability (mainstream production, wafer size)	✔	✔	?	✔	✔
Low cost	✔	✔	✗	✔	✔

Chapter 2

CPW Transmission Line Simulations

2.1 Introduction

Typical quality factors, used for characterization of RF substrates are the effective resistivity (ρ_{eff}) and the effective permittivity (ε_{eff}). The effective parameters permit easy comparison of substrates with different morphologies. The original substrate is modelled by a homogeneous substrate with effective parameters ρ_{eff} and ε_{eff}, as shown in Figure 2.1. The effective parameters are set so that both substrates have identical RF losses. They can be extracted either from semiconductor device simulations, or from wafer RF measurements with a vector network analyzer (VNA) [20, 21]. Usually CPW lines are used for measurements/simulations, as basic building blocks for RF systems. In order to suppose that the substrate is lossless compared to the conductor losses, a typical value of $\rho_{\text{eff}} \geq 3\,\text{k}\Omega\cdot\text{cm}$ is required [10]

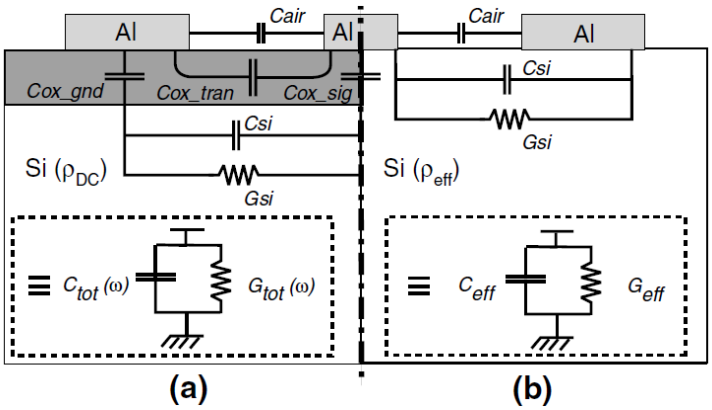

Figure 2.1: CPW structure on (a) a passivated Si substrate, and (b) an effective homogeneous substrate used for ρ_{eff} modeling. Adapted from [21].

In the following sections, first the simulation model is presented. Then, the effect of different substrate parameters is studied: oxide interface charges, pores geometry and interface defect traps.

2.2 Simulation model

The simulations in this chapter were performed with Atlas, a 2D simulation software for semiconductor devices [22]. The simulation model of the CPW line on passivated trenched substrates is shown in Figure 2.2. The CPW line is designed for a characteristic impedance of $50\,\Omega$ on bulk silicon. The substrate and buried oxide (BOX) thicknesses are respectively $t_{\text{sub}} = 400\,\mu\text{m}$ and $t_{\text{BOX}} = 400\,\text{nm}$. The trenches (also called pores here) are placed under the BOX, distributed for the whole width of the transmission line.

The substrate's bulk resistivity (ρ_0) is varied from $10\,\Omega\cdot\text{cm}$ to $8\,\text{k}\Omega\cdot\text{cm}$ to encompass a wide range of substrates from standard resistivity to HR. The bulk relative permittivity of the substrate is kept at $\varepsilon_r = 11.7$, as only silicon substrates are treated in this work. The relative permittivity of the pores ($\varepsilon_{\text{pore}}$), however, is set to the permittivity of the dielectric filling the pore (Air or SiO_2).

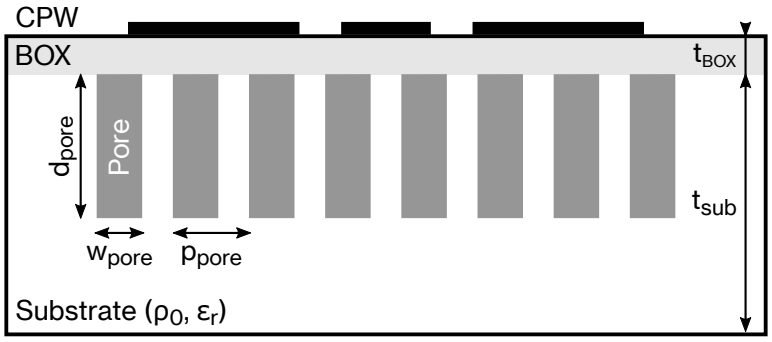

Figure 2.2: Atlas model of the CPW line simulation on porous substrates.

2.3 Oxide interface charges

The metal–oxide–semiconductor (MOS) and SOI structures have already been thoroughly studied with respect to the relation of the oxide charges (Q_{OX}) at the BOX–substrate interface and the presence of a parasitic surface conduction (PSC) layer for HR substrates. The greater sensitivity of substrates with higher resistivity to the oxide charges was also demonstrated [7]. In this section, the impact of Q_{OX} presence is analysed for the porous substrate model presented in Figure 2.2.

Three simulation cases are distinguished here:

- No Q_{OX} — no oxide interface charges are modelled.
- Q_{BOX} — charges are added only at the BOX–substrate interface (see Figure 2.3a).
- Q_{pore} — charges are added at the BOX–substrate and pore–substrate interfaces (see Figure 2.3b).

A typical value of $Q_{\text{OX}} = 10^{11}\,\text{cm}^{-2}$ is used in simulations, assuming the total charge is mainly due to fixed interface charges[1] [23].

[1] From the four types: fixed, mobile ionic, oxide trapped and interface trapped charges [7]

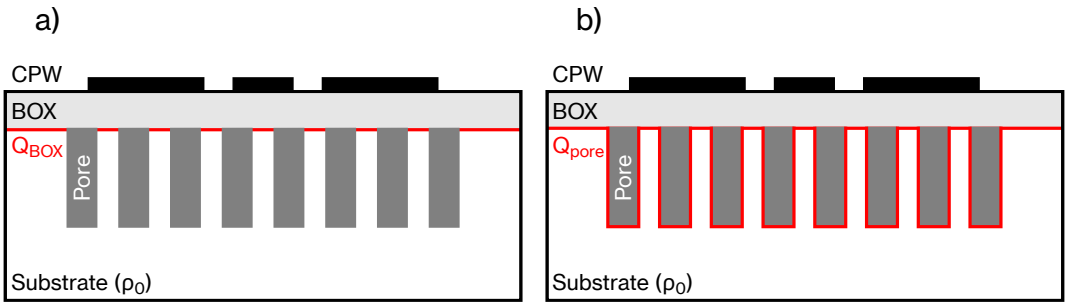

Figure 2.3: Simulation model with oxide charges: (a) at the BOX–substrate interface, and (b) at the BOX–substrate and pore–substrate interfaces.

The result of the simulation is shown in Figure 2.4 in the form of the effective resistivity as function of the frequency. The three cases described above are simulated with $\rho_0 = 8\,\mathrm{k\Omega\cdot cm}$. The typical curves can be observed, with the resistivity decreasing with the frequency where capacitive coupling effects are dominating. The limit value of the resistivity at high frequency ($10\,\mathrm{GHz}$ in this work) is the one that matters for RF applications and will, from now on, be simply called effective resistivity (ρ_{eff}).

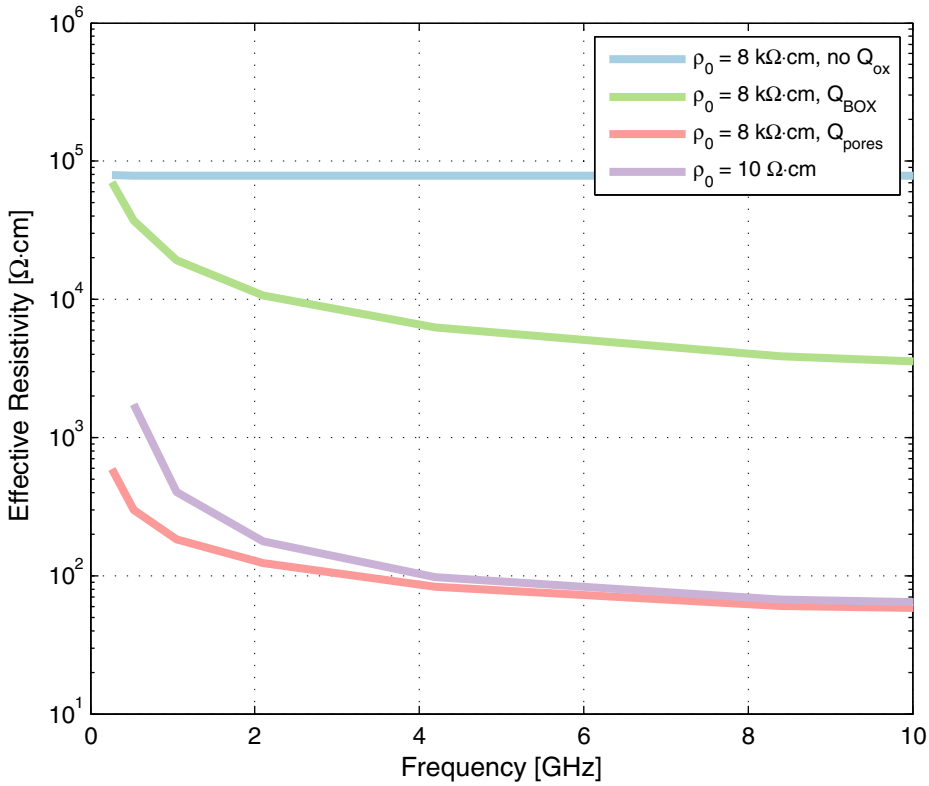

Figure 2.4: Simulated effective resistivity of the substrate with oxide interface charges as a function of the frequency. Model parameters: $d_{\mathrm{pore}} = 400\,\mu\mathrm{m}$, $p_{\mathrm{pore}} = 20\,\mu\mathrm{m}$, $w_{\mathrm{pore}} = 16\,\mu\mathrm{m}$.

The absolute values of ρ_{eff} extracted from the simulations in Figure 2.4 are not important here, they are defined by the geometrical pore parameters and will be discussed in Section 2.4.

Instead, the relative magnitudes characterize the impact of the addition of fixed oxide charges Q_{BOX} and Q_{pore} to the interfaces (as defined in Figure 2.3), and can be analysed.

- The addition of Q_{BOX} decreases ρ_{eff} by more than an order of magnitude. This is explained by the presence of a PSC layer in Si near the BOX interface, formed by a strong inversion zone as shown in Figure 2.5a.

- The addition of Q_{pore} decreases ρ_{eff} by another order of magnitude compared to Q_{BOX}. This can be explained by the appearance of an in-volume inversion region in the remaining silicon structure. The result can be observed from the extracted resistivity distribution in Figure 2.5b.

The 2D resistivity in Figure 2.5 was extracted from the simulation results by using the definition:

$$\rho = \frac{1}{q\left(\mu_n n + \mu_p p\right)}$$

where q is the elementary charge, n and p are the electron and hole concentrations, and, μ_n and μ_p the corresponding mobilities.

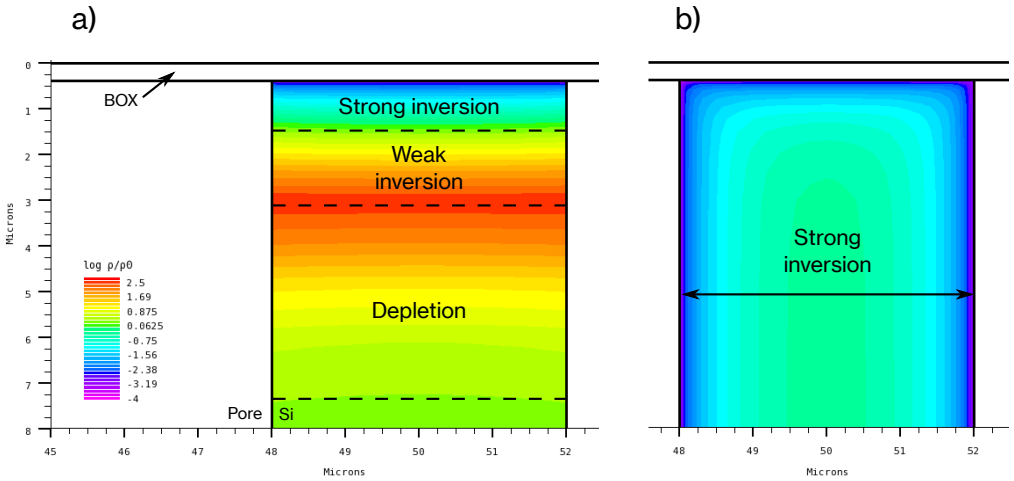

Figure 2.5: Resistivity distribution extracted from Atlas simulations for substrates with fixed oxide charges: (a) Q_{BOX} and (b) Q_{pore}. Model parameters: $d_{\text{pore}} = 400\,\mu\text{m}$, $p_{\text{pore}} = 20\,\mu\text{m}$, $w_{\text{pore}} = 16\,\mu\text{m}$, $\rho_0 = 8\,\text{k}\Omega\cdot\text{cm}$, $Q_{\text{BOX}} = Q_{\text{pore}} = 10^{11}\,\text{cm}^{-2}$.

The simulation result of a porous substrate with a standard bulk resistivity $\rho_0 = 10\,\Omega\cdot\text{cm}$ is also included in Figure 2.4. In this case, as mentioned earlier, the impact of the fixed oxide charges is negligible and only one curve is represented. A more comprehensive plot is given in Figure 2.6, showing ρ_{eff} as a function of the substrate's bulk resistivity. Several observations can be established from those results.

- The presence of pores increases the resistivity of the substrate by approximately an order of magnitude when no oxide charges are taken into account.

- The effect of Q_{BOX} appears around $\rho_0 = 1\,\text{k}\Omega\cdot\text{cm}$, saturating the maximum value of ρ_{eff}. To attain higher resistivity, techniques such as TR layer fabrication combined with HR substrates are necessary to counteract the PSC at the BOX interface.

- The effect of Q_{pore} is present for the whole range of bulk resistivities and does not permit ρ_{eff} higher than $100\,\Omega\cdot\text{cm}$, not sufficient for RF applications. Therefore, minimizing the Q_{pore} value or compensating it with fabrication techniques is necessary.

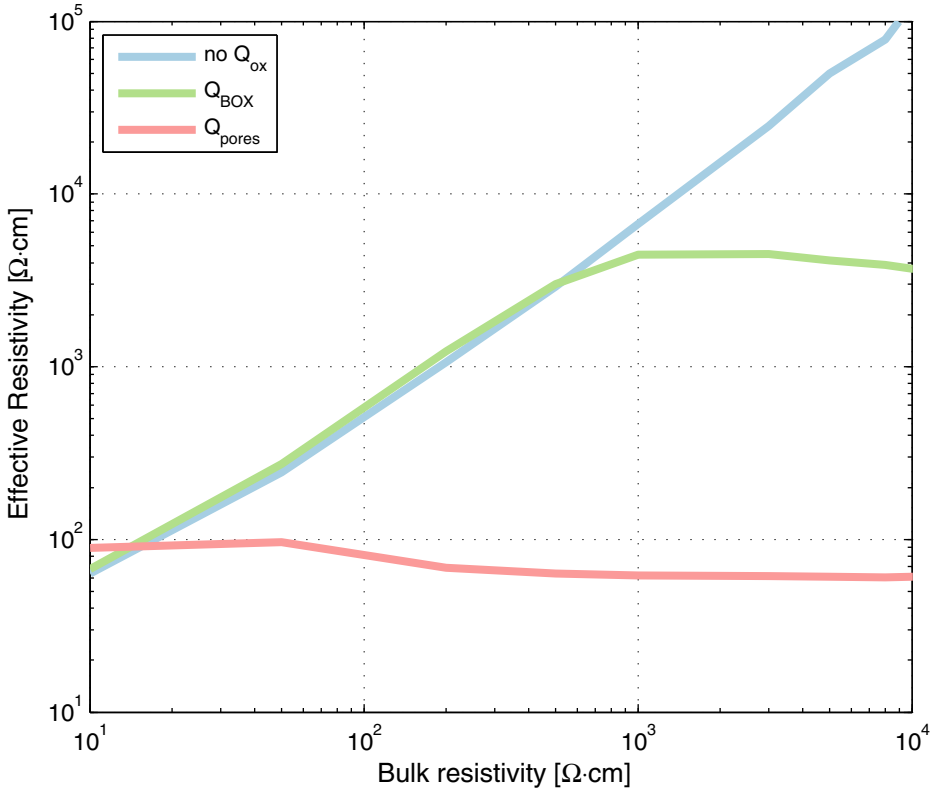

Figure 2.6: Simulated effective resistivity of the substrate as a function of the bulk resistivity. Model parameters: $d_{\text{pore}} = 400\,\mu\text{m}$, $p_{\text{pore}} = 20\,\mu\text{m}$, $w_{\text{pore}} = 16\,\mu\text{m}$, $f = 10\,\text{GHz}$.

2.4 Pore geometry

In this section, the geometrical parameters of the pores (shown in Figure 2.2) are studied with respect to the effective parameters of the substrate. In particular, the impact of the pore depth and pore width on the effective resistivity and permittivity is analysed. The dimensions are kept in the possible fabrication ranges for 3 inch, $200-400\,\mu\text{m}$ thick wafers in the Winfab cleanroom facilities, for the process described in Chapter 4.

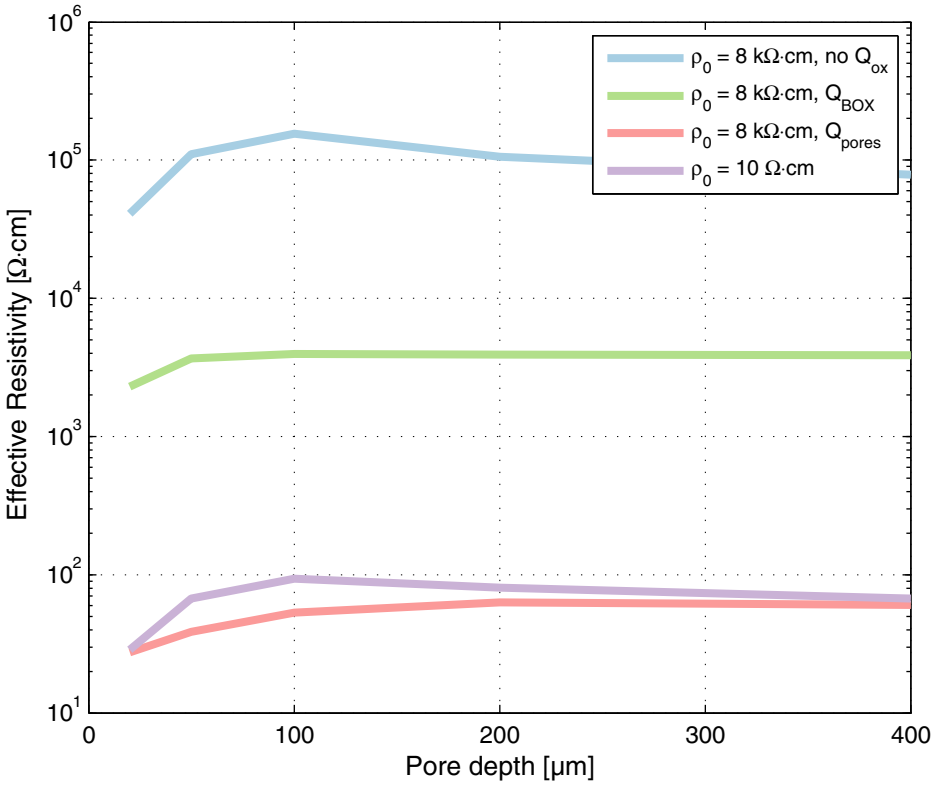

Figure 2.7: Simulated effective resistivity of the substrate as a function of the pore depth. Model parameters: $p_{\text{pore}} = 20\,\mu\text{m}$, $w_{\text{pore}} = 16\,\mu\text{m}$, $f = 10\,\text{GHz}$.

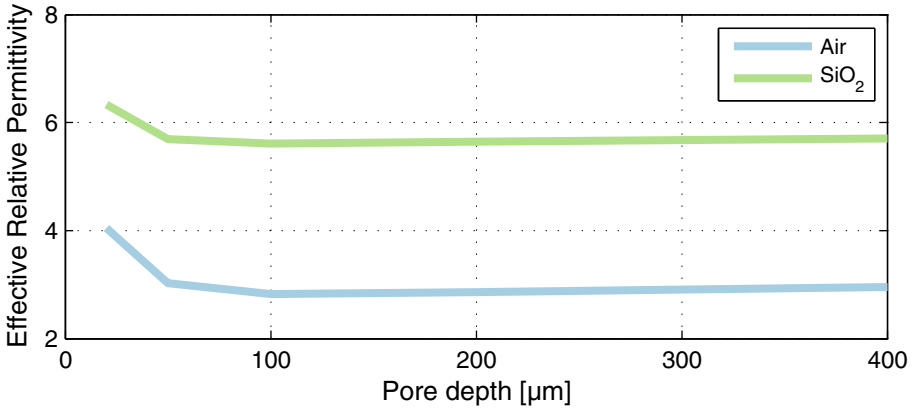

Figure 2.8: Simulated effective relative permittivity of the substrate as a function of the pore depth. Model parameters: $p_{\text{pore}} = 20\,\mu\text{m}$, $w_{\text{pore}} = 16\,\mu\text{m}$, $f = 10\,\text{GHz}$.

2.4.1 Pore depth

At first, the pore depth (d_{pore}), measured from the BOX, is varied while the other dimensions are kept fixed. The simulation results are represented in Figure 2.7 and Figure 2.8. The effective resistivity is simulated for standard and HR bulk resistivities, and for the three Q_{OX} cases explained in the previous section. The effective permittivity is given for the case where the pores

are filled with air or with SiO_2.

Both parameters show a trend where they are mostly impacted by the first $100\,\mu m$ of pore depth, and stabilize past this point. This is explained by the fact that the electromagnetic fields in the substrate are mainly located close to the BOX interface in the case of CPW lines. While this means that for the current simulation model, only the first $100\,\mu m$ need to be porosified to reach the maximum ρ_{eff} and ε_{eff}, the proposed fabrication process involves etching through the whole substrate from the back side. A pore depth of $d_{pore} = 400\,\mu m$ is therefore used for the rest of the simulations.

2.4.2 Pore width

Second, the pore width impact is studied by varying w_{pore}. As the pore pitch is kept constant at $20\,\mu m$, the remaining Si structure width is changing as $p_{pore} - w_{pore}$. The results of the simulations, with the same model parameters as in the previous section, are presented in Figure 2.9 in the form of effective resistivity and in Figure 2.10 in the form of effective relative permittivity.

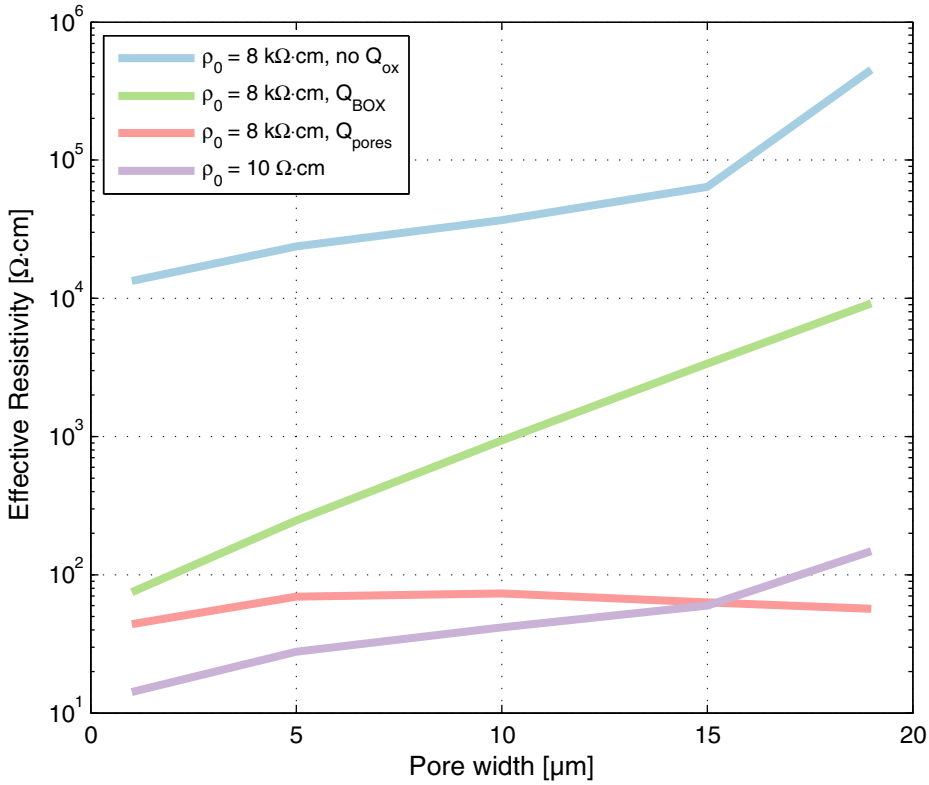

Figure 2.9: Simulated effective resistivity of the substrate as a function of the pore width. Model parameters: $d_{pore} = 400\,\mu m$, $p_{pore} = 20\,\mu m$, $f = 10\,GHz$.

By analysing the results in Figure 2.9, a trend for the most ρ_{eff} curves can be observed. The effective resistivity is at its minimum value when no pores are present ($w_{pore} \approx 0\,\mu m$) and increases as expected with the pore width by one to two orders of magnitude, until almost no Si substrate is left ($w_{pore} \approx 20\,\mu m$).

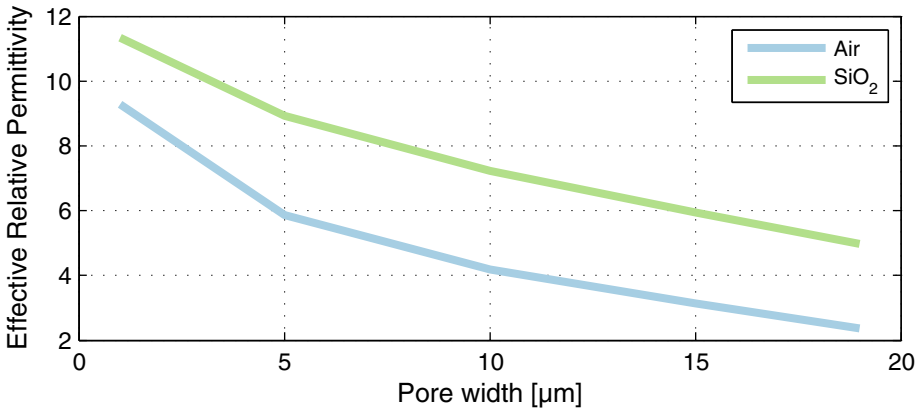

Figure 2.10: Simulated effective relative permittivity of the substrate as a function of the pore width. Model parameters: $d_{\text{pore}} = 400\,\mu\text{m}$, $p_{\text{pore}} = 20\,\mu\text{m}$, $f = 10\,\text{GHz}$.

An exception is the case where fixed oxide charges Q_{pore} are used with $\rho_0 = 8\,\text{k}\Omega\cdot\text{cm}$. The effective resistivity rises from a width of $1\,\mu\text{m}$ to $5\,\mu\text{m}$, but then remains constant or even decreases. This can be explained by observing the resistivity distribution shown in Figure 2.11. For $w_{\text{pore}} = 1\,\mu\text{m}$ (see Figure 2.11a), a weak inversion/depletion region is in the center of the remaining Si with a strong inversion region around, creating a PSC layer at the interfaces. By increasing the pore width up to $5\,\mu\text{m}$ and higher, and thus decreasing the Si width, the whole volume becomes a strong inversion region (see Figure 2.11b). The conductivity rises and dominates for larger pore widths, saturating ρ_{eff}.

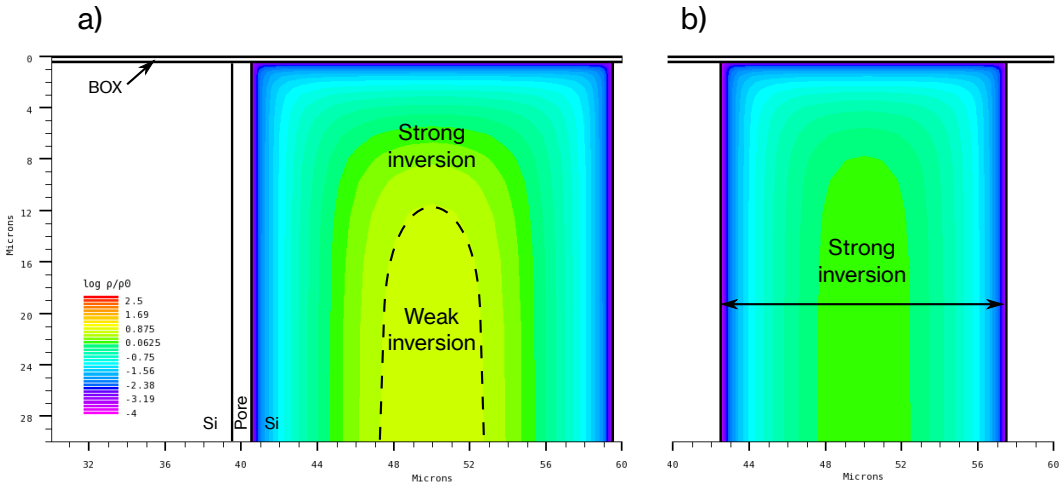

Figure 2.11: Resistivity distribution extracted from Atlas simulations for substrates with different pore widths: (a) $w_{\text{pore}} = 1\,\mu\text{m}$ and (b) $w_{\text{pore}} = 5\,\mu\text{m}$. Model parameters: $d_{\text{pore}} = 400\,\mu\text{m}$, $p_{\text{pore}} = 20\,\mu\text{m}$, $\rho_0 = 8\,\text{k}\Omega\cdot\text{cm}$, $Q_{\text{pore}} = 10^{11}\,\text{cm}^{-2}$.

The effective relative permittivity on the other hand, shown in Figure 2.10, behaves as expected. By increasing the pore width, ε_{eff} decreases from the bulk Si value to the dielectric constant of the material filling the pore. The decrease is linear, expressed as a weightened mean of the pore and the remaining silicon widths by their relative permittivities. This shows that

for the best/lowest ε_{eff}, pores as big as possible should be realised and if they are filled, low-k materials should be used.

A comparable analysis could be done for the pore pitch parameter, but was not realized in this work due to time constraints. Although, similar results are to be expected, where the proportion of the pore dielectric material to the remaining silicon is of importance for the effective resistivity and permittivity, and not the actual pore dimensions.

2.5 Interface traps

The deliberate addition of interface defect traps such as in TR-HR substrates, has been shown to reduce the PSC and increase the RF performances of the substrates [7]. In this final section about CPW transmission lines simulations, the impact of interface traps on the effective parameters of porous substrates is briefly studied.

The simulation model with fixed oxide charges at the BOX–substrate and pore–substrate interfaces ($Q_{\text{pore}} = 10^{11}\,\text{cm}^{-2}$, see Figure 2.3b) is reused. In addition, traps are added to pore–substrate interfaces as shown in Figure 2.12, representing intrinsic or intentionally fabricated interface defects. Those can, for example, be due to the formed porous silicon layer during metal-assisted chemical etching (MACE) (see Section 4.5.1). The simulated traps are uniformly distributed within the bandgap of the semiconductor with typical trap density D_{it} between $10^{9}\,\text{cm}^{-2}$ and $10^{12}\,\text{cm}^{-2}$.

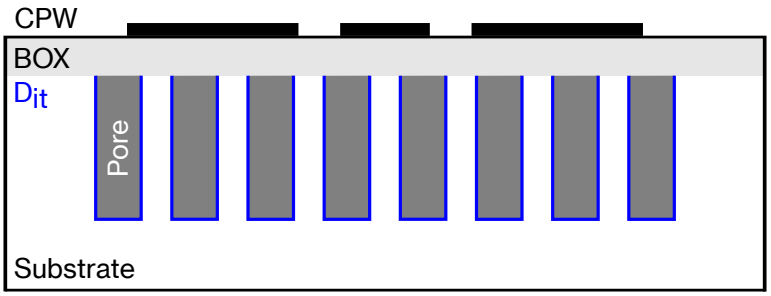

Figure 2.12: Simulation model with pore–substrate interface traps.

The simulation results are given in Figure 2.13, in the form of extracted effective resistivity as function of the trap density for two porous HR substrates. The results indicate that the low ρ_{eff} due to the PSC and the in-volume inversion region, can be improved by adding defects at the interfaces to trap the free carriers. At low trap densities, the impact is insufficient and the inversion region is maintained as shown in Figure 2.14a. But when the defect density is equal or higher than the density of carriers attracted by the fixed oxide charges, a depletion region is formed at those interfaces as shown in Figure 2.14b. The effective resistivity is thus improved by more than two orders of magnitude, when the density of traps is sufficient to counterbalance the fixed oxide charges.

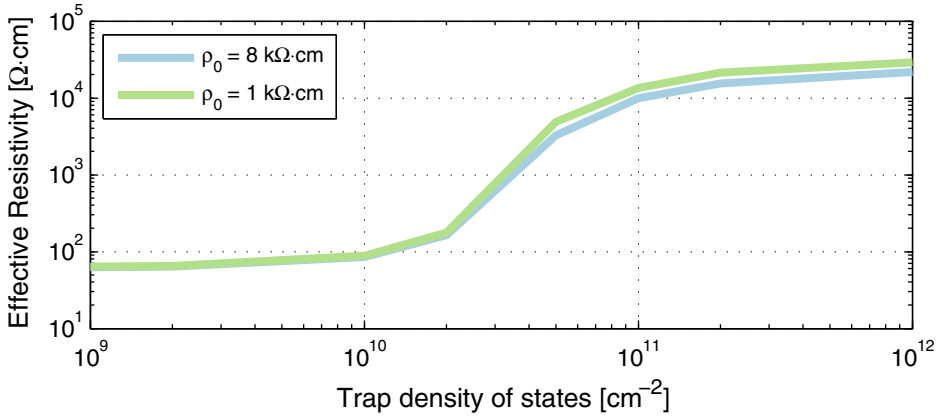

Figure 2.13: Simulated effective resistivity of the substrate as a function of the trap density. Model parameters: $d_{\text{pore}} = 400\,\mu\text{m}$, $p_{\text{pore}} = 20\,\mu\text{m}$, $w_{\text{pore}} = 16\,\mu\text{m}$, $f = 10\,\text{GHz}$, $Q_{\text{pore}} = 10^{11}\,\text{cm}^{-2}$.

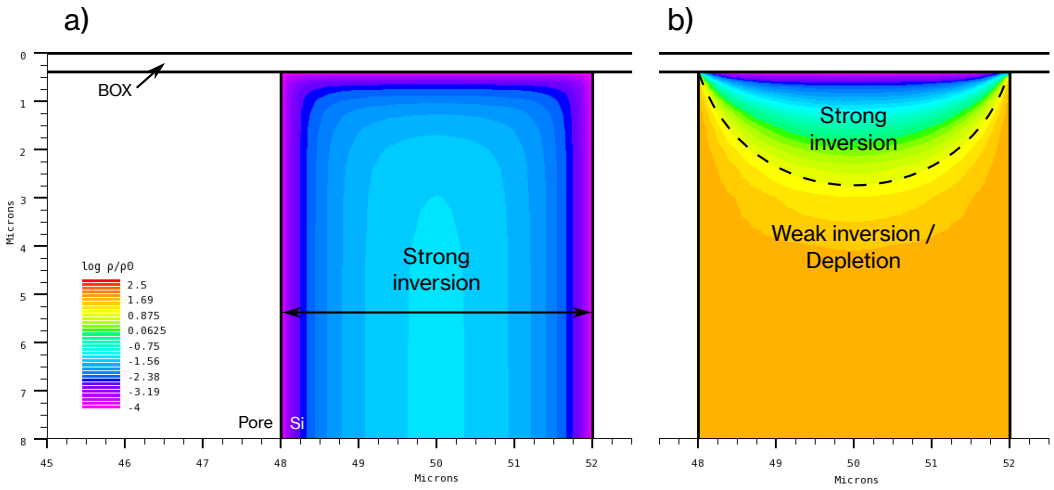

Figure 2.14: Resistivity distribution extracted from Atlas simulations for substrates with interface traps: (a) $D_{\text{it}} = 10^{10}\,\text{cm}^{-2}$ and (b) $D_{\text{it}} = 2 \cdot 10^{11}\,\text{cm}^{-2}$. Model parameters: $d_{\text{pore}} = 400\,\mu\text{m}$, $p_{\text{pore}} = 20\,\mu\text{m}$, $w_{\text{pore}} = 16\,\mu\text{m}$, $\rho_0 = 8\,\text{k}\Omega\cdot\text{cm}$, $Q_{\text{pore}} = 10^{11}\,\text{cm}^{-2}$.

2.6 Conclusion

Atlas simulations of CPW lines were realized to extract the effective parameters of trenched silicon substrates. In the best case, the addition of trenches increased the substrate's effective resistivity by up to two orders of magnitude and reduced the relative permittivity down to 3. From the geometrical point of view, only the $100\,\mu m$ closest to the BOX impact the effective parameters, where the electromagnetic fields are concentrated. Whereas, wider pores improved the RF characteristics overall, as less of the lossy Si structure remains.

In the case of substrates with standard bulk resistivity, the addition of trenches does not increase the RF performances in a significant way. The effective resistivity remains below $100\,\Omega cm$ in all cases, which is too low for RF applications. For trenched substrates fabricated from high bulk resistivity, a phenomenon similar to the PSC in HR-SOI is observed. If fixed oxide charges are present at the pore−substrate interfaces, an in-volume strong inversion region is created in the remaining Si. Due to the inversion zone, the effective resistivity drops below $100\,\Omega \cdot cm$ regardless of the bulk resistivity.

Finally, the addition of interface traps to the simulation improved the RF performances of the substrate. With a sufficient trap density to "catch" all free carriers, trenched substrates with effective resistivity higher than $3\,k\Omega \cdot cm$ were obtained. Those defects in practice can be either specifically fabricated or intrinsic interface traps.

Two future research perspectives are proposed to assess the possibility of trenched substrates integration with CMOS processes:

- Conceive an experimental setup to get a more precise estimation of the fixed oxide charge and trap densities at the Si−pore interfaces.
- Study of the impact of the pores size in proportion to the simulated devices, as well as the pores position with respect to the device mismatch.

Chapter 3

Integrated Inductor Simulations

3.1 Introduction

In addition to CPW lines, integrated inductors are widely used passive devices in RF circuits. Typical applications requiring inductors are impedance matching and filtering blocks. The main inductors' characteristics are the actual inductance value and the quality factor (Q). In this chapter, the impact of the substrate RF characteristics on the Q factor is studied, which defines the insertion loses, power consumption and bandwidth of the inductor.

The equivalent circuit of spiral inductors is shown in Figure 3.1. On the one hand, the intrinsic properties of the inductor such as the metal conductance and layout define the series elements (L_S, R_S and C_S). The metal losses impact the lower frequency range of the Q factor. On the other hand, capacitive and resistive losses due to the substrate are modelled as shunt elements (C_P and G_P). Those are linked to the substrate's effective parameters and typically define the Q factor at high frequencies [16, 24].

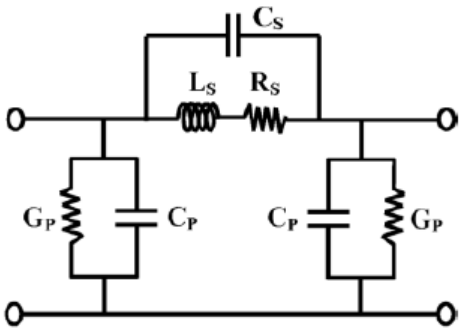

Figure 3.1: Equivalent circuit of spiral inductors. Adapted from [16].

In the following sections, an inductor is first simulated on homogeneous porous substrates with effective parameters. The extracted quality factor is compared to bulk and TR HR-SOI substrates. Second, a heterogeneous substrate is simulated with rectangular trenches. The extracted quality factors of the homogeneous and heterogeneous substrates are compared. All the simulations were performed with HFSS, a high frequency electromagnetic field simulation software [25].

3.2 Homogeneous effective substrates

An inductor was simulated on homogeneous substrates with effective resistivity and effective permittivity (ρ_{eff} and ε_{eff}), extracted from Atlas simulations in Chapter 2. The effective parameters are taken from simulations with the following pore dimensions: $w_{\text{pore}} = 16\,\mu\text{m}$, $p_{\text{pore}} = 20\,\mu\text{m}$ and $d_{\text{pore}} = 400\,\mu\text{m}$, representative of those actually fabricated during this work. The substrate thickness is kept at $t_{\text{sub}} = 400\,\mu\text{m}$ as in Chapter 2. The substrate radius $r_{\text{sub}} = 800\,\mu\text{m}$ (see Figure 3.2b) was chosen as described in Appendix A, and also defines the surrounding air "box" size.

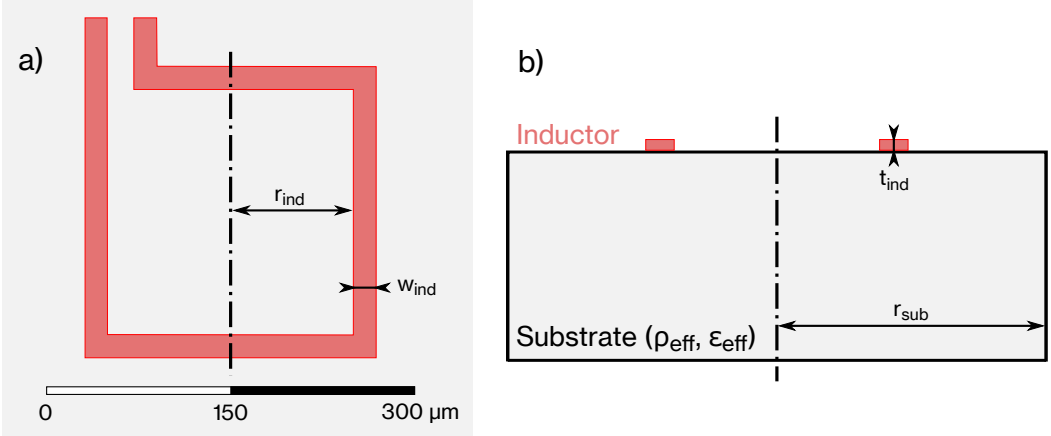

Figure 3.2: HFSS model of the simulated inductor on substrate with effective parameters ρ_{eff} and ε_{eff}: (a) top view, and (b) cross-section.

The inductor is designed as a single-turn metal loop, inspired from the work of Rais-Zadeh et al. [26]. The model is shown in Figure 3.2, with the following geometrical parameters used in the simulation: inductor radius $r_{\text{ind}} = 150\,\mu\text{m}$, metal width $w_{\text{ind}} = 20\,\mu\text{m}$ and metal thickness $t_{\text{ind}} = 10\,\mu\text{m}$. These were not optimized for any particular inductance value or frequency bandwidth, as the purpose of this work is to observe the impact of the substrate rather than the inductor design and/or dimensions on the performance.

The results of the inductor simulations are given in Figure 3.3. The following four substrates were simulated and are compared:

- A bulk silicon substrate with $\rho_0 = 10\,\Omega\cdot\text{cm}$ and $\varepsilon_r = 11.7$.
- A porous substrate fabricated from a standard resistivity wafer ($\rho_0 = 10\,\Omega\cdot\text{cm}$), with $\rho_{\text{eff}} = 100\,\Omega\cdot\text{cm}$ and $\varepsilon_{\text{eff}} = 4$.
- A porous substrate fabricated from a HR wafer ($\rho_0 = 1\,\text{k}\Omega\cdot\text{cm}$), with $\rho_{\text{eff}} = 3\,\text{k}\Omega\cdot\text{cm}$ and $\varepsilon_{\text{eff}} = 4$.
- A trap-rich substrate with $\rho_{\text{eff}} = 3\,\text{k}\Omega\cdot\text{cm}$ and $\varepsilon_{\text{eff}} = 10$.

At low frequencies (below Q_{max}), all the curves share the same shape, where the quality factor is determined by the losses in the metal conductor (unchanged between the designs). At high frequencies, however, the substrate's impact can be observed. First, the increase of the ρ_{eff}

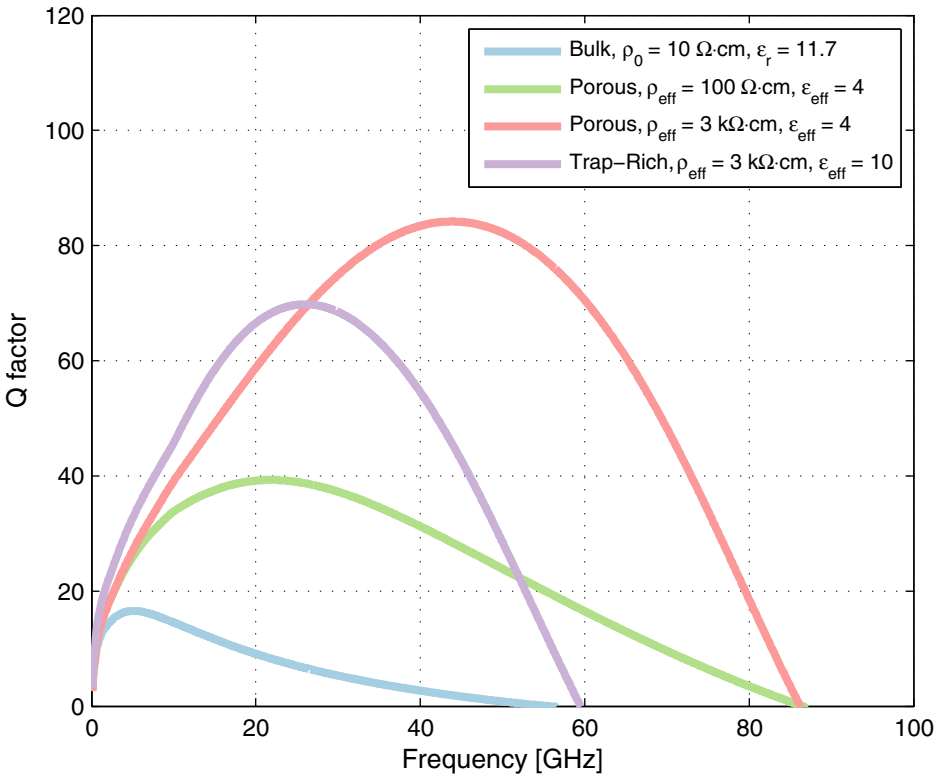

Figure 3.3: Simulated Q factor of an inductor on homogeneous substrates with effective parameters ρ_{eff} and ε_{eff} as a function of the frequency.

shows an improvement of the peak Q factor. The value increases by $2\times$ for $\rho_{\text{eff}} = 100\,\Omega\cdot\text{cm}$, and up to $4\times$ for $\rho_{\text{eff}} = 3\,\text{k}\Omega\cdot\text{cm}$ in comparison to the low-resistivity bulk substrate. Second, the frequency bandwidth is extended. The inductors on bulk and TR substrates exhibit the same self-resonant frequency (SRF) of approximately $60\,\text{GHz}$, as they share similar ε_{eff}. While the inductors on porous substrates have a higher SRF, and thus higher bandwidth, which can be correlated to the low ε_{eff}.

3.3 Heterogeneous porous substrates

In this section, the validity of the previous inductor simulations on effective substrates is analysed by simulations of the same design on heterogeneous porous substrates. Whether or not the effective parameters, extracted from CPW simulations, are accurate factors of merit for substrates for other passive devices (in this case inductors) is examined.

The HFSS software does not perform semiconductor physics simulations. Therefore, the PSC effect due to oxide interface charges is modelled as a separate high conductivity layer between the BOX and the substrate as shown in Figure 3.4. The PSC layer thickness $t_{\text{PSC}} = 100\,\text{nm}$ and doping $N_{D,\text{PSC}} = 10^{16}\,\text{cm}^{-3}$ were set to match the HR substrate characteristics. The oxide charges in pore walls are assumed to be counterbalanced by the presence of interface traps, as explained in Section 2.5.

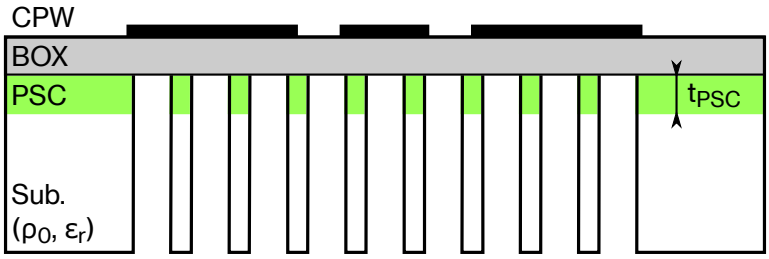

Figure 3.4: Atlas simulation model of a porous heterogeneous substrate with a PSC layer with thickness t_{PSC} and doping $N_{D,\text{PSC}}$.

The comparison of Atlas simulations for those two models is shown in Figure 3.5. The results indicate a quite good approximation of the PSC layer, from the effective resistivity point of view, for the whole bandwidth of the simulated inductor.

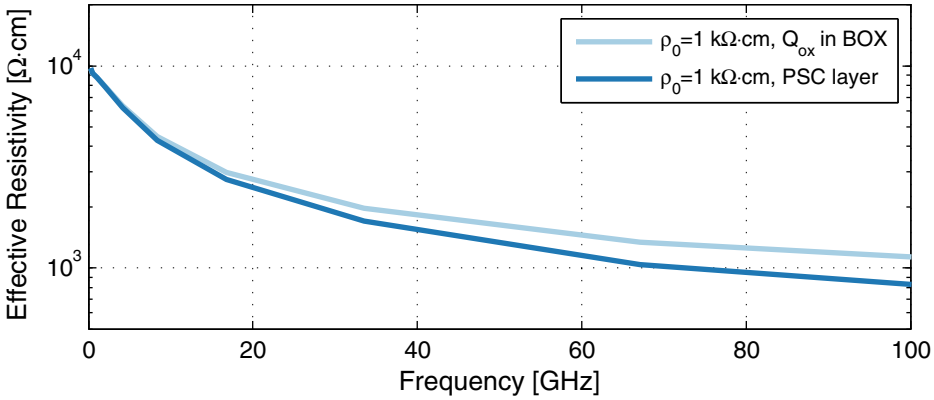

Figure 3.5: Simulated effective resistivity of the substrate with a PSC layer as a function of the frequency.

The inductor with the same design and dimensions as in Section 3.2 is then simulated on three different substrates with:

- a bulk resistivity of $1\,\text{k}\Omega\cdot\text{cm}$, a 400-nm-thick BOX, a PSC layer, without pores (Figure 3.6a);
- a bulk resistivity of $1\,\text{k}\Omega\cdot\text{cm}$, a 400-nm-thick BOX, a PSC layer, with rectangular air-filled pores (Figure 3.6b); and
- effective parameters $\rho_{\text{eff}} = 3\,\text{k}\Omega\cdot\text{cm}$ and $\varepsilon_{\text{eff}} = 4$ (Figure 3.2).

The surrounding air "box" size is again optimized as explained in Appendix A. But in contrast to the previous section, the substrate size is kept constant at $r_{\text{sub}} = 300\,\mu\text{m}$ to minimize the number of mesh points, and the simulation time, while being sufficient to impact the quality factor of the inductor.

The simulation results of the inductor on the three substrates are shown in Figure 3.7. On one hand, the addition of the rectangular pores to the substrate modelled with the PSC layer increases the Q factor by a factor of 2 due to increased effective resistivity. And the frequency bandwidth is improved as well, due to the increased permittivity of the substrate.

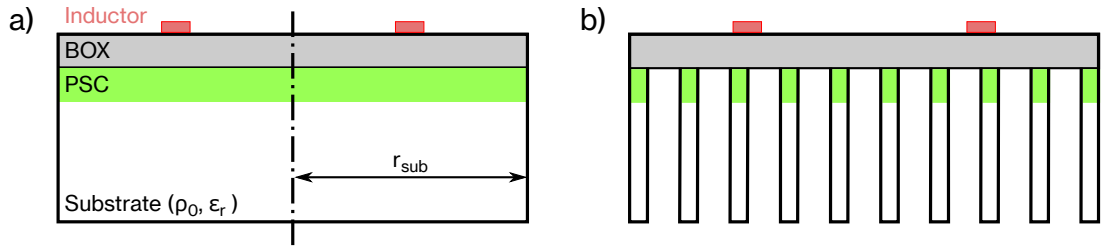

Figure 3.6: HFSS simulation model cross-section of an inductor on heterogeneous substrates: (a) without pores, and (b) with rectangular pores.

On the other hand, the simulations of the substrate with effective parameters and the trenched substrate can be compared. The heterogeneous model does not match exactly with the results of the substrate with effective parameters. An error of approximately 30% is made for the Q factor, and 15% for the SRF. However, the increased accuracy of the trenched substrate comes at the cost of increased number of simulation elements from 30k to 100k tetrahedra. This figures are extracted from the mesh generated by the adaptive meshing algorithm in HFSS. With more in-depth study and configuration of the simulation model, lower complexity can probably be achieved.

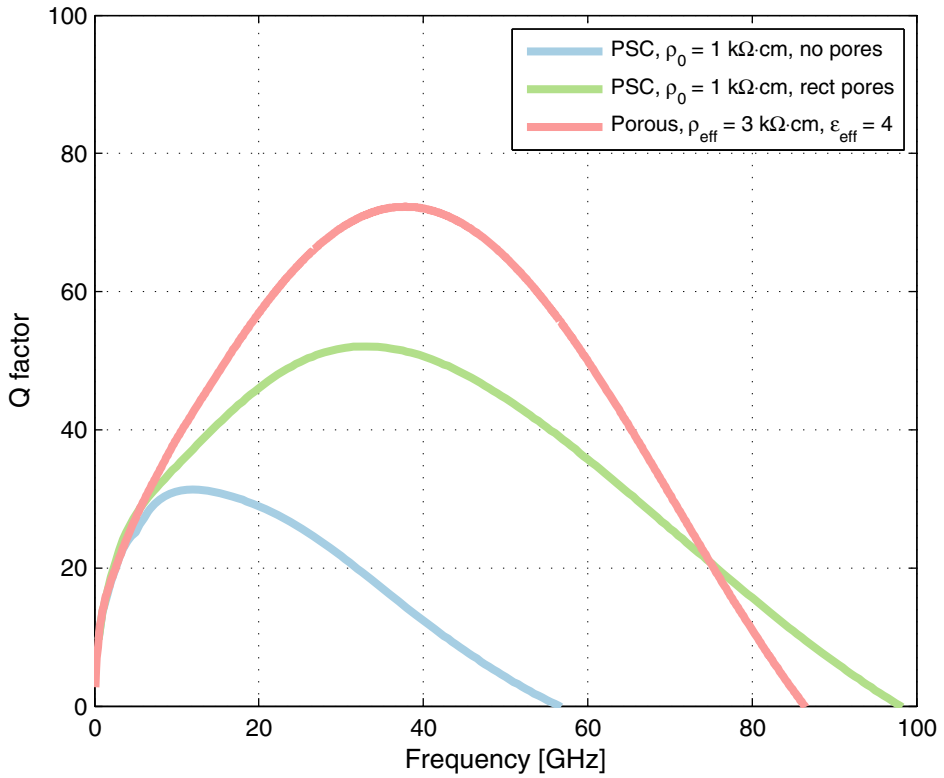

Figure 3.7: Simulated Q factor of an inductor on heterogeneous substrates modelled with a PSC layer, as a function of the frequency.

3.4 Conclusion

The simulation of an inductor design on bulk and trenched Si-based substrates was realised. The higher effective parameters of the porous substrates lead to a significant improvement of the inductor's RF properties. The increase of the quality factor is found to be related to the effective resistivity, while the bandwidth is improved by the low effective permittivity of the substrate.

Homogeneous substrates with effective parameters can be used in fast simulations to get an approximation of the Q factor and the SRF. However, an approximative error of respectively 30% and 15% is obtained for those values, compared to the heterogeneous substrates. The actual trenches geometry can therefore be modelled and simulated in order to obtain a more precise result. Although, this comes at the cost of increased computational complexity, which resulted in four times longer simulation time in this work.

Chapter 4

Trenched Silicon Substrate Fabrication by MACE with Patterned Metal Films

4.1 Introduction

A process is established to improve a substrate's RF characteristics in a post-CMOS process with back-side access only. Deep trench-like pores are created in the Si, as defined in the the model simulated in Chapter 2 and Chapter 3. In the case of DRIE, etch depth becomes extremely non-uniform if the amount of exposed Silicon on a wafer exceeds 20 to 30%. Therefore, metal-assisted chemical etching with a patterned gold film was chosen for the formation of the trenches.

In the following sections, first the process is divided in five fabrication steps. Then in particular, the patterning technique, Au film deposition, MACE parameter optimization and the results are presented in details. A large number of fabrication trials were realized during this work. However, only the best or the most pertinent results are presented here.

4.2 Fabrication steps

This fabrication process can be described by distinguishing five main steps illustrated in Figure 4.1:

(a) The starting SOI substrate includes the RF devices on the front-side. A silicon nitride (Si_3N_4) etch-stop layer is required under the BOX to prevent SiO_2 etching by the HF solution during the process. A standard cleaning is performed on the back-side and a plasma oxide (POx) layer is formed.

(b) The patterned Au film is produced by standard lift-off photolithography and sputtering physical vapor deposition (PVD), and is annealed (see Section 4.3 and Section 4.4).

(c) The substrate is immersed in a HF solution, provoking the metal-assisted chemical etching (see Section 4.5). The patterned Au film "sinks" intro the substrate, creating large trench-like pores. The front-side containing the devices must not be exposed to the electrolyte during this step. A protective layer resistant to HF, such as a hydrocarbon polymer based resist [27] can be used, however a mechanical protection is better suited for mass production. In this work, the wafer was placed in a hermetic sample holder, exposing only the back-side of the substrate to the HF solution.

(d) MACE is stopped when the metal layer reaches the etch-stop nitride surface, resistant to the HF electrolyte (see Section 4.5.6).

(e) The Au is removed from the bottom of the pores by wet-etching (dilute aqua regia [28]). Finally, the sample is rinsed and dried.

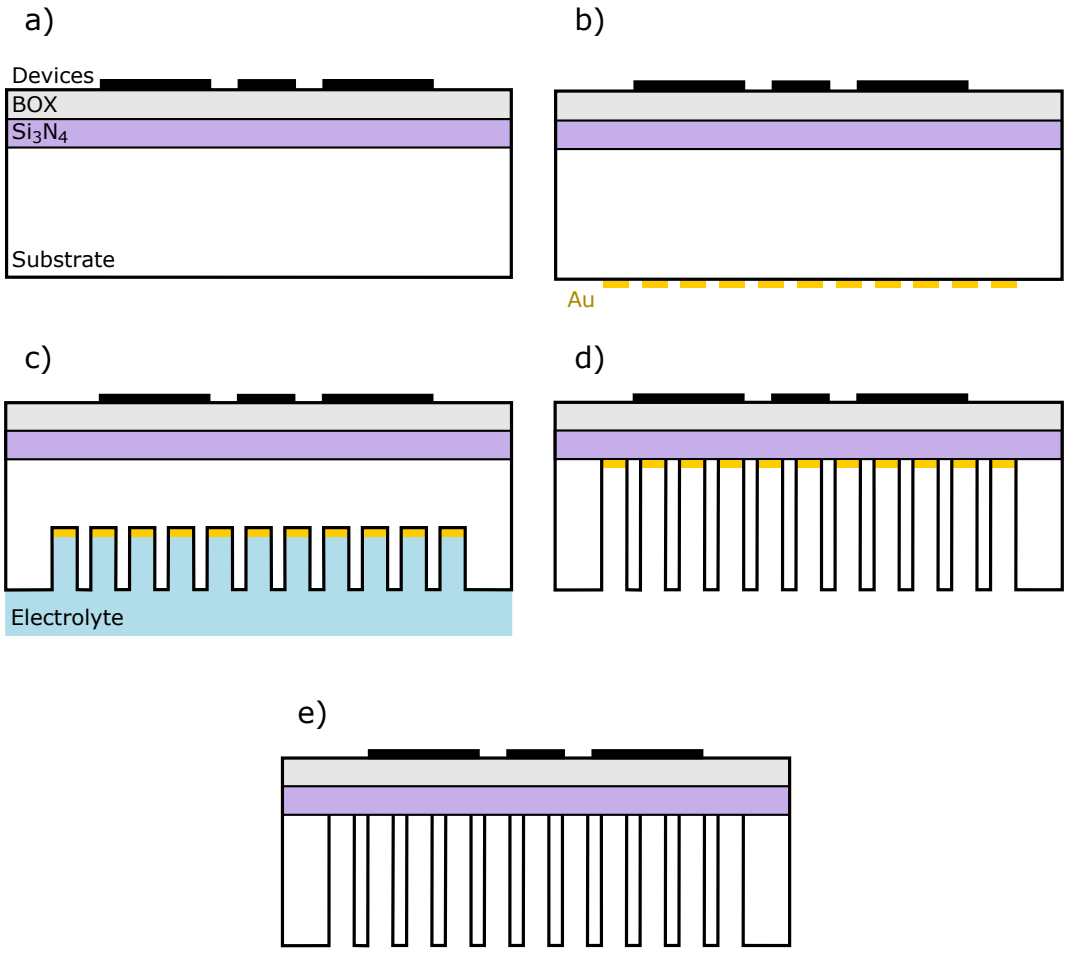

Figure 4.1: Porous substrate fabrication steps by MACE with patterned Au film. (a) Initial substrate with RF devices fabricated on the front-side. (b) Deposition of the patterned porous Au film on the back-side. (c) Etching of the silicon in the electrolyte solution. (d) End of the etching process at the etch-stop layer. (e) Final porous substrate after the Au film removal.

4.3 Metal patterning

The purpose of creating a patterned Au film is to etch as much as possible of the substrate for the best RF performances, as was shown in Chapter 2. At the same time, a sufficient silicon structure must be kept as mechanical support. In this section, the chosen patterning technique and the design of the masks for Au deposition are presented.

4.3.1 Patterning techniques

Two patterning techniques were considered as alternatives to the classic UV photolithography. Nanosphere lithography (NSL), and the use of an ultrathin anodic aluminum oxide (AAO) as patterning mask are both processes attracting growing interest for the generation of periodic and homogeneous nanoscale structures.

Nanosphere lithography NSL is a technique used for the formation of hexagonal patterns by self-assembling of polystyrene sphere layers on a Si surface (see Figure 4.2). The beads are usually deposited from a colloidal solution and are available in different sizes. Once deposited they can be used as a negative or a positive mask for metal deposition [29–31].

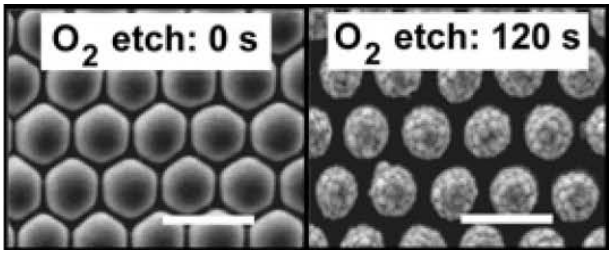

Figure 4.2: SEM top-view images of nanosphere samples on silicon before and after O_2 plasma etching. Scale bars are 750 nm. Adapted from [29].

+ Potential for low-cost mass production with wafer-scale processes
+ Easy nanosphere and thus pattern size variation.
– Limited to hexagonal and triangular geometries.
– Self-assembly large-scale defects are possible.

AAO mask The anodic aluminum oxide is a layer with regular hexagonal-shaped pores, formed by anodization of aluminum films in liquid electrolyte (see Figure 4.3). It can be used as a hard mask for deposition or etching processes, with pore sizes between a few nanometres and several hundreds of nanometres [32, 33]

+ Allows self-assembled, large area porosification.
+ Control of the pore dimensions by varying the anodization conditions.
– Limited hexagonal geometry.
– Requires separate AAO layer fabrication process and a transfer to the Si substrate.

The two alternative patterning techniques present interesting advantages, but are mostly suited for Si-nanowire (NW) fabrication. Whereas in this work sub-micron structures are not necessary. The easier and well-known lift-off process, in combination with UV photolithography, was therefore chosen for the Au film patterning, described in the next section.

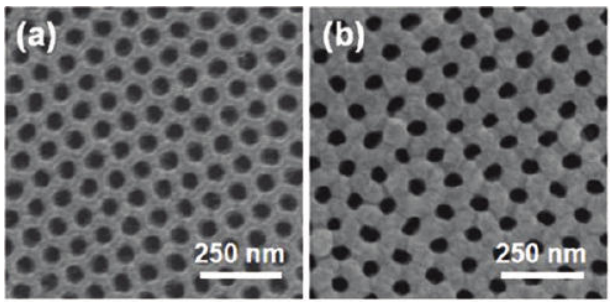

Figure 4.3: SEM top-view images of (a) AAO membrane and (b) metal mesh sputtered on top. Adapted from [33].

4.3.2 Mask design

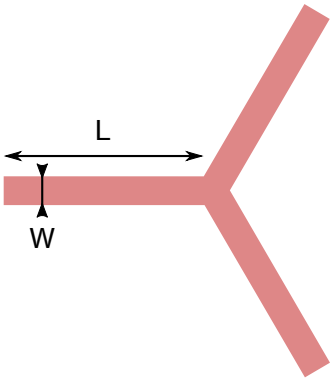

Figure 4.4: Elementary star cell used in mask designs.

W	L
1	7
2	100
5	35
5	100
7	49
7	100
10	70
10	100

Table 4.1: Star pattern dimensions [µm].

The different mask variations are created from the elementary star cell shown in Figure 4.4, with the sizes given in Table 4.1. Different dimensions were used to study their impact, on the one hand, on the remaining Si walls and thus the substrates' mechanical rigidity (out of scope of this work); and on the other hand, on the metal pattern sizes and thus the MACE speed and uniformity (see Section 4.5). The actual masks were designed by G. Scheen, with honeycomb-like shapes typical in applications where low material density and good mechanical properties are required. The star cells are assembled in two distinct patterns shown in Figure 4.5, where:

(a) the metal film forms one semi-continuous pattern; and

(b) the metal film forms separate hexagonal structures.

The type of pattern is significant to the MACE etch quality and is discussed in Section 4.5 as well.

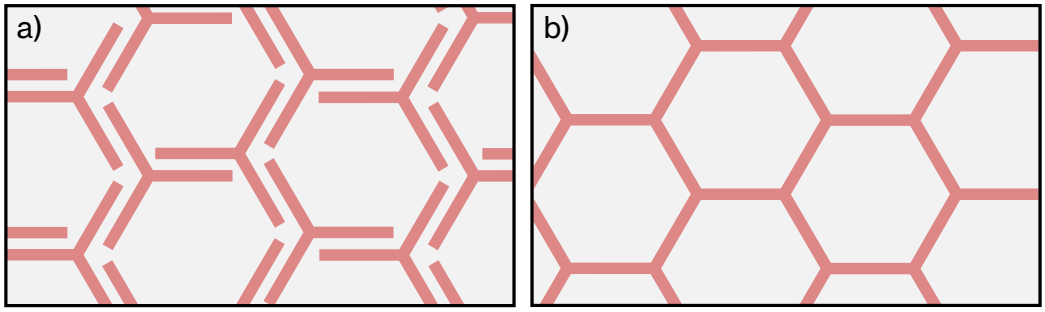

Figure 4.5: Assembly of the star cells to form (a) a semi-continuous pattern, and (b) separate hexagonal shapes, for the Au film deposition mask. The red zones define the area where the photoresist is deposited and grey where the Si will be etched by the metal.

4.4 Porous Au film deposition

The impact of the pattern width on the etching uniformity and speed was demonstrated by Geyer et al. [34]. The etching of a thick (40 nm) non-porous Ag layer was performed for two pattern widths: 390 nm and 710 nm. The results, shown in Figure 4.6, indicate a reduction of the etching speed (20 nm/min vs. 35 nm/min) and a non-uniformity of etching for the large pattern size. This behaviour is supported by the diffusion process of the reactants and the reaction products of MACE to the etching site under the metal layer, explained in Section 4.5.1.

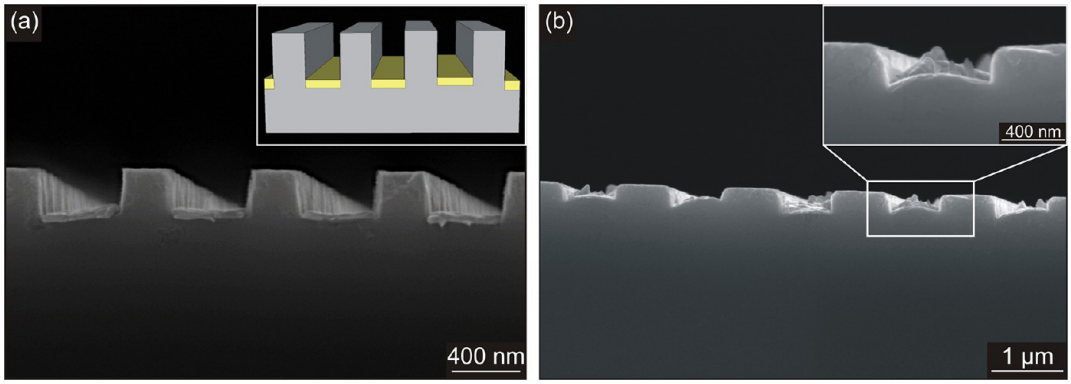

Figure 4.6: SEM cross-section images of etched Ag stripes with a thickness of 40 nm with different lateral sizes: (a) 390 nm and (b) 710 nm. Adapted from [34].

Therefore, in this work, a porous Au layer is fabricated to facilitate the electrolyte diffusion under the metal, and thus to improve the etching speed and uniformity. Several 1 cm × 1 cm Si samples were prepared with a POx surface layer[1]. Gold depositions were performed by sputtering with thicknesses ranging between 11 nm and 24 nm. The deposition technique is described in detail in Section 5.3.1.

The results, given in Figure 4.7, show an increasing coverage of the substrate by the metal. The samples vary with the increasing thickness from a separated metal islands (11 nm), to a porous metal film (18 nm), to an almost completely covered substrate by the Au film (24 nm). A thermal dewetting was done as well at 180°C for 30 min, resulting in a globally more uniform

[1] 1 min at 150 W in a barrel O_2 plasma etcher

film with better defined pores. A metal thickness between 15 nm and 18 nm was selected as the most adapted for MACE, generating a uniform metal layer with evenly-spaced separated pores.

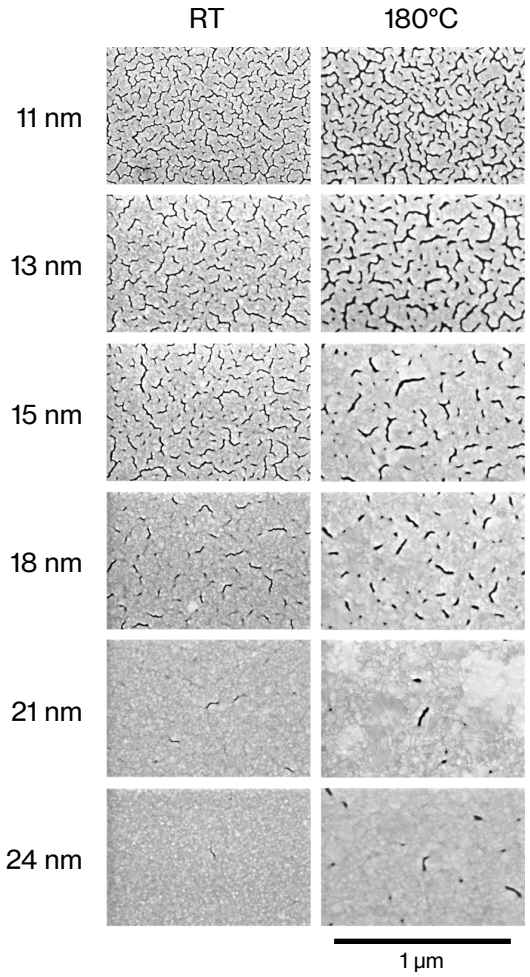

Figure 4.7: SEM images of porous gold films deposited at room temperature (RT) and after 30 minutes of annealing (180°C) for increasing thicknesses.

4.5 Metal-assisted chemical etching

The samples with the patterned Au film deposited on the back-side were then etched in the HF electrolyte. Numerous MACE parameters and etch conditions impact the quality and speed of the process, as well as the morphology of the resulting pores. Several of those, presented in the following sections, were studied in detail: metal layer morphology, pattern shape and size, electrolyte composition, and finally the temperature and illumination conditions.

4.5.1 MACE mechanisms

Metal-assisted chemical etching is based on the principle of Si dissolution in a HF electrolyte. Two conditions are necessary for the etching process: the presence of electronic holes (h^+) and contact with the HF electrolyte. The holes are generated by the H_2O_2 reduction:

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+ \tag{4.1}$$

Without the metal, oxidation occurs but is very slow, resulting in etching speed lower than $10\,\text{nm}$ per hour [35]. The metal, on the other hand, acts as a catalyst and the oxidation occurs mostly at the metal–electrolyte interface. The generated holes are then injected in the Si at proximity of the metal, where the dissolution process occurs:

$$Si + 6H^+ + 6F^- + 4h^+ \rightarrow SiF_6^{2-} + 6H^+ \tag{4.2}$$

However, numerous dissolution models have been proposed, and the exact reaction remains an open question [36, 37]. Accompanying the etching process, formation of gas bubbles is often observed, explained by the generation of hydrogen:

$$2H^+ \rightarrow H_2 \uparrow + 2h^+ \tag{4.3}$$

The most accepted diffusion model of the reactants and reaction products is illustrated in Figure 4.8, valid for both metal films and nanoparticles (NPs). A superficial PSi layer is formed with a thickness depending on the substrate doping and temperature. The layer permits the diffusion of the electrolyte to the metal–silicon interface. The high current density of holes causes electropolishing of Si in contact with the metal, which therefore "sinks" into the substrate [34].

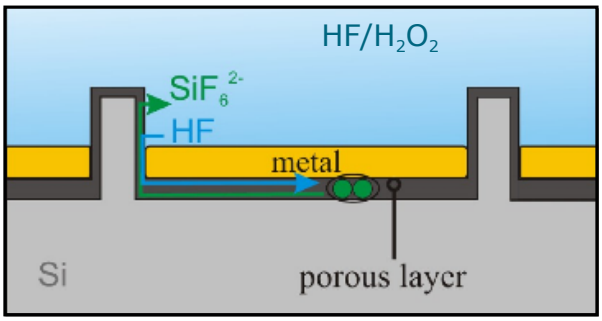

Figure 4.8: Diffusion process model of the reactants and reaction products during metal-assisted chemical etching. Adapted from [34].

Thus, the global etching speed is ruled by the electrochemical reactions and the diffusion rates. Several parameters impact those: metal thickness and lateral size, temperature, doping level and type of the Si substrate, and ρ defined as the ratio $[HF]/([HF] + [H_2O_2])$ [34].

4.5.2 Au layer morphology

The samples with different Au layer thicknesses between 13 nm and 18 nm, described in Section 4.4, were etched in the same conditions ($\rho = 37\%$, $T = 40$°C) for two hours. In the general case, dewetting of the Au film increased the layer's toughness, and therefore, most of the etched samples in this process were annealed. The results are shown in Figure 4.9, where the following observations can be made:

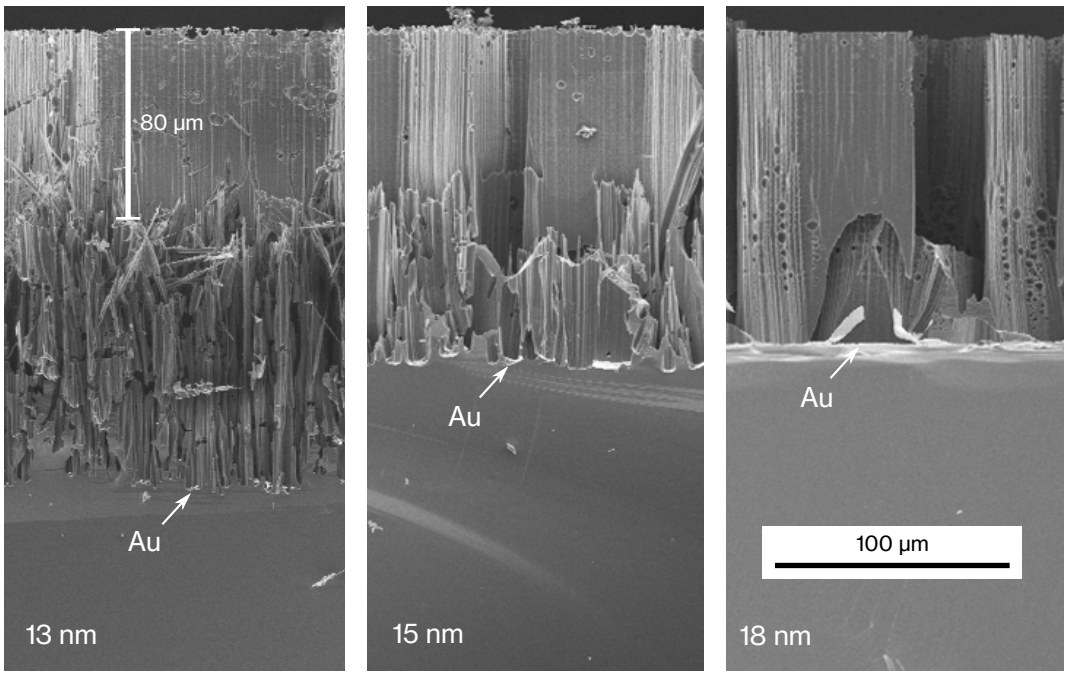

Figure 4.9: SEM cross-section view of samples etched for 120 min with Au film thicknesses of 13 nm, 15 nm and 18 nm.

- 13 nm — The remaining 3D Si structures are correctly defined for the first 80 µm of the etching. Past this depth, the Au layer disintegrates in small separated fragments. This behaviour is observed because of the initial semi-continuous structure of the Au film, which breaks apart due to internal tensile stress during the etching process. The disintegration also leads to a non-uniformity of the etching depth.

- 15 nm — Similar results are observed, where the Au layer disintegrates after an approximative depth of 100 µm. Although, the metal fragments are bigger with a more uniform etching front, meaning that the layer is partially connected. However, the thick Au layer with lower pore density leads to slower etching speed due to reduced electrolyte diffusion to the metal–Si interface.

- 18 nm — The metal layer demonstrates significant improvement in toughness and etch uniformity, with no disintegration observed. The film remained entirely intact up to the largest etch depth tested of 200 µm, with only a slight decrease in the etch rate compared to the 15 nm layer.

The measured etching speeds of the three samples are summarised in Table 4.2

Table 4.2: MACE etch rate as function of Au thickness.

Au thickness [nm]	13	15	18
Etch rate [µm/min]	1.67	1.17	1.11

4.5.3 Pattern configuration

The impact of the pattern design, introduced in Section 4.3.2, on the etch uniformity was studied as well. The designs can be merged in three main groups:

- Small continuous patterns (SCPs) — one uninterrupted metal layer arranged in a honeycomb-like manner (see Figure 4.5a) with a hexagon side length $L = 7\,\mu m$.
- Small separate patterns (SSPs) — detached honeycomb-like metal structures (see Figure 4.5b) with a hexagon side length $L = 7\,\mu m$.
- Large patterns (LPs) — separate or continuous, with a hexagon side length $L = 100\,\mu m$.

For the small patterns, the comparison of the etching results between the continuous and the detached structures is shown in Figure 4.10. The SSP is composed of distinct metal patches, small enough to deviate from the direction perpendicular to the deposition surface. This randomized movement is amplified with the etch time/depth and can be due to imperfections in the metal shape symmetry and thickness, local electrolyte concentration variation and small displacements due to H_2 bubbles generation. The result, illustrated in Figure 4.10a, show the separated metal patches moving in different directions, and thus reaching various etching depths. Whereas, the SCP are all attached to each-other on a large scale. This constraint restricts their movement mostly to only one direction during the etching, i.e. perpendicular to the substrate's surface. This results in well defined pores with a uniform etching depth, as seen in Figure 4.10b.

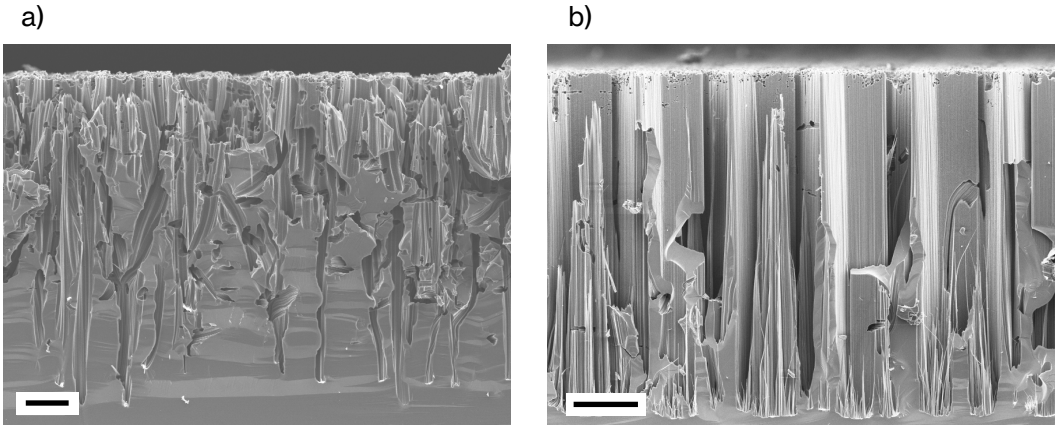

Figure 4.10: SEM cross-section view of etched samples with "small" patterns: (a) SSP and (b) SCP. Scale bars are $10\,\mu m$.

LPs, on the one hand, are big enough by themselves so that small variations in etch rate do not impact the global etching speed and homogeneity. Therefore, both separate and continuous large patterns exhibit similar results with a uniform etch front and well defined remaining Si structures, illustrated in Figure 4.11. On the other hand, the width of created pores/trenches impacts the diffusion rate of the electrolyte from the substrate's surface to the bottom of the pores. This affected the etching speed, so that the pores generated in samples with large patterns were up to two times deeper than in samples with small patterns, for similar etching conditions.

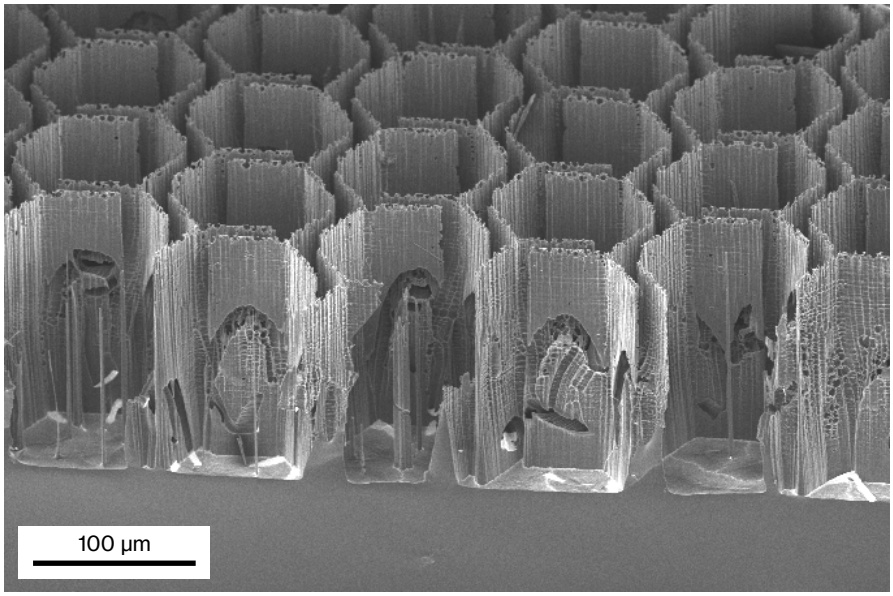

Figure 4.11: SEM bird's-eye view image of an etched sample with "large" patterns.

In the case of SSP, some solutions have already been proposed in literature to improve the directional etch profile, perpendicular to the surface:

- Carrying the etching out in a centrifuge, so that the centrifugal force is perpendicular to the surface, forcing the directional etch [38].
- Magnetically guiding the patterns, composed for example of a Au/Fe/Au trilayer, with an external permanent magnet to accelerate and impose the etching direction [39].

However, this would complicate the process, and in this work, the problem was avoided by focusing on the etching of LPs and SCPs instead of the separated ones.

4.5.4 Electrolyte

Molar ratio The composition of the electrolyte has a strong influence on the speed and resulting pore morphology of metal-assisted etched Si [40]. The molar ratio ρ, used as a unified notation for comparing etching conditions published in literature, is defined as:

$$\rho = [\mathrm{HF}]/([\mathrm{HF}] + [\mathrm{H_2O_2}])$$

The different regimes of Si dissolution as function of ρ were studied by Chartier et al. [41]. The result, illustrated in Figure 4.12, shows an evolution of the etching regimes from electropolishing and crater creation ($\rho < 20\%$), to cone-shaped pores with a microporous layer covering the walls ($20\% < \rho < 70\%$), to cylindrical macro-pores defined by the metal size and shape ($\rho > 70\%$).

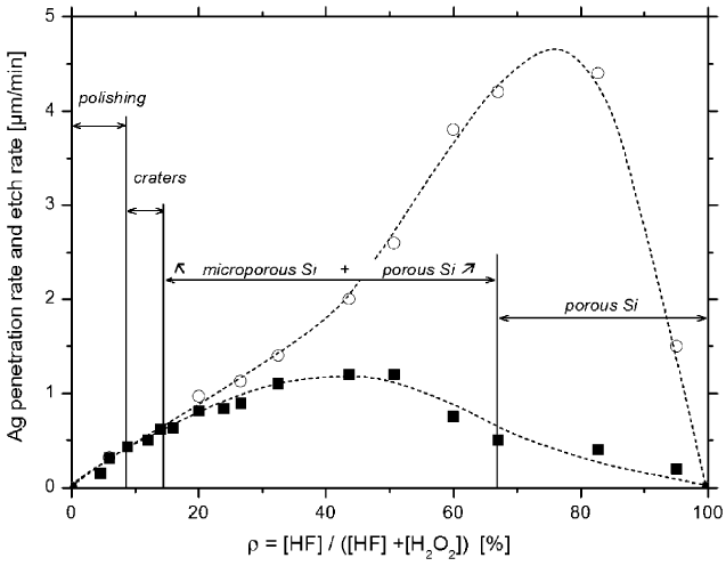

Figure 4.12: Etching rates and morphology as a function of the molar ratio ρ. Open circles: before NaOH treatment, penetration rate of Ag NPs. Filled squares: after NaOH treatment, etch rate. Adapted from [41].

In this work, etching was done with two molar ratios $\rho = 37\%$ and $\rho = 83\%$, while keeping the HF concentration constant at $[\mathrm{HF}] = 3.9\,\mathrm{M}$. The results, given in Table 4.3, indicate a higher etching rate for the low ρ value, accompanied by a larger underetch. The underetch distance is defined as the size reduction of the top of the remaining walls after two hours of etching. That means that for a large underetch, the remaining structures become fine and thus fragile; while with a small underetch, the structure sizes remains as defined by the pattern.

Table 4.3: MACE etch rate and underetch distance as a function of ρ, for constant $[\mathrm{HF}] = 3.9\,\mathrm{M}$.

Molar ratio ρ [%]	37	83
Etch rate [µm/min]	2	0.7
Underetch [nm]	215	100

On the sample with $\rho = 83\%$, the low underetch resulted also in the formation of nanograss at the bottom of the pores, shown in Figure 4.13. The nanograss consists of unetched Si passing through the pores in the Au layer, and is possibly partially responsible for the lower etch rate by obstructing the diffusion of the electrolyte. This type of structures were not observed for low values of ρ .

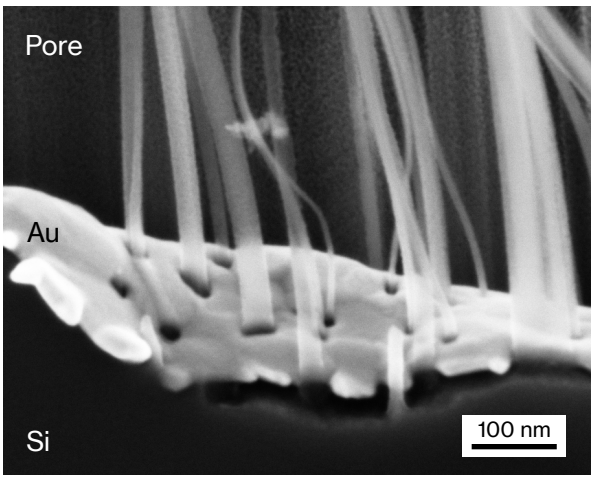

Figure 4.13: SEM cross-section view of Si nanograss formation for $\rho = 83\%$.

Molar concentration of HF Not only the ratio of the concentrations but also the actual molarity of HF (and $[H_2O_2]$ related to [HF] by ρ) has an influence on the etching speed and pore morphology. Samples were etched in two electrolytes with different concentrations $[\mathrm{HF}] = 3.4\,\mathrm{M}$ and $[\mathrm{HF}] = 7.9\,\mathrm{M}$, while keeping a constant $\rho = 60\%$. The results, given in Table 4.4, show a considerable increase in the etching speed and underetch distance with the HF molarity.

Table 4.4: MACE etch rate and underetch distance as a function of HF molarity for constant $\rho = 60\%$.

HF molarity [M]	3.4	7.9
Etch rate [µm/min]	0.5	3.1
Underetch [nm]	50	350

The impact of the molar ratio ρ and the HF concentration on SiNWs formation, through the variation of the electrolyte composition was summarized by Kim et al. [33] as well, illustrated in Figure 4.14.

Solvent The addition of a solvent to the electrolyte is often done, usually ethanol for PSi formation by anodization. The solvent acts as a wetting agent, increases the electrolyte diffusion inside the pores, reduces surface tension effects and helps minimizing hydrogen bubbles [42]. Here, several etching were performed with varying volumes of added isopropanol (IPA). The results indicate a decrease in the etch rate with increasing IPA volume, given in Table 4.5. However, even for small percentages, a significant improvement in etch uniformity was observed due to H_2 bubble size reduction and better electrolyte diffusion.

Table 4.5: MACE etch rate as a function of IPA volume.

IPA [vol. %]	0	2.5	7.5	17
Etch rate [µm/min]	5	2.5	2	1.9

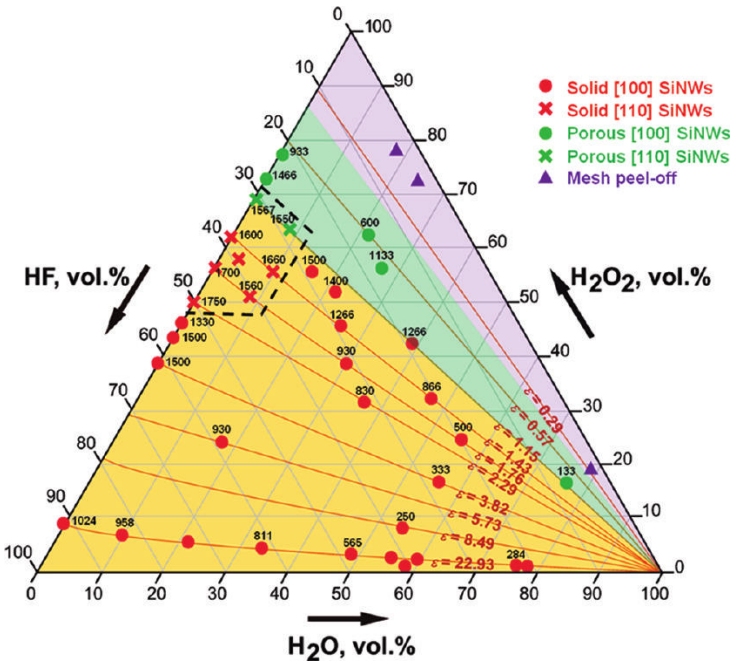

Figure 4.14: Summary graph of the evolution of etching rate (nm/min), etching direction and morphology during MACE of SiNWs as function of ternary mixture of 46 wt. % HF, 35 wt. % H_2O_2 and H_2O at room temperature. Adapted form [33].

4.5.5 Etching conditions

Temperature The impact of the reaction temperature on the etching rate of SiNWs was studied by Cheng et al. [43]. Their results, represented in Figure 4.15, indicated an increased etching speed with increasing temperature between 0°C and 50°C. The improvement of etching speed and uniformity of wide pores for high-aspect ratio through silicon vias (TSVs) was also reported with etching temperatures up to 100°C [44].

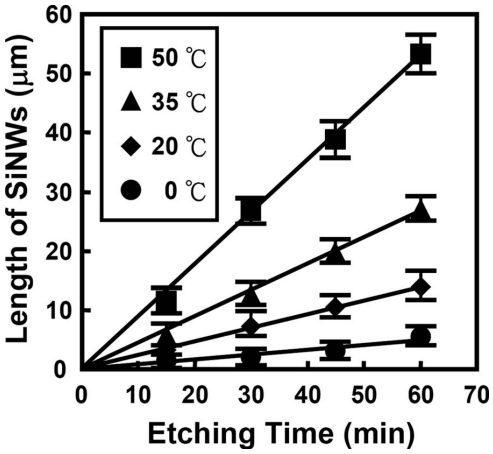

Figure 4.15: Length of SiNWs as a function of etching time at different etching temperatures. Adapted from [43].

In this work, three samples were etched ($\rho = 37\%$) at room temperature and in solutions

heated up to 40°C and 50°C. The results, given in Table 4.6, indicate an approximately linear increase of the etching speed with the temperature as expected. The effect of the improved diffusion was observed as well, with a better etch uniformity at high temperatures.

Table 4.6: MACE etch rate as a function of increasing temperature.

Temperature [°C]	20	40	50
Etch rate [µm/min]	2	4	5.7

Illumination In the case of metal-assisted chemical etching, the reduction of H_2O_2 is fast due to the presence of metal functioning as a catalyst. Therefore, the number of photogenerated holes is usually smaller than the holes injected from the H_2O_2 reduction for room light illumination [37].

In this work, several samples were etched in the dark and under ambient light (no dedicated illumination). The results indicated no visible impact of the illumination on etching speed or pore morphology. Confirming that the Si etching is mostly due to the holes injected from H_2O_2 reduction in proximity of the metal layer.

4.5.6 Etch-stop layer

Silicon nitride is often used as an etch mask due to the slow etch rates in HF-based solutions, depending on the deposition quality [28]. In this work, the nitride is used as an etch-stop layer for the MACE, and to prevent exposing the BOX to the electrolyte. Therefore, a 100-nm-thick layer of Si_3N_4 was deposited by low-pressure chemical vapor deposition (LPCVD) before the growth of the SiO_2 BOX layer. A sample was etched by MACE with the nitride surface exposed to the HF electrolyte. The measured etching speeds were approximately 500 nm/min for the Si and 1 nm/min for the Si_3N_4. This result confirms the high selectivity of Si etching over the nitride with a ratio of 500:1, making the layer suitable as an etch-stop for MACE.

The behaviour of the Au film reaching the etch-stop layer is analysed from a SEM cross-section image, shown in Figure 4.16. From the observed samples was established that the metal patterns do not reach the Si_3N_4 layer during the MACE process. Instead, a thin Si layer (a few hundred of nanometres) remains unetched between the nitride and Au. The morphology and behaviour of this Si layer (possibly depleted of holes), and whether it has an impact on RF performances of the substrate are still to be studied.

4.6 Conclusion

A fast, easy and low-cost process was designed for the fabrication of deep trench-like pores by metal-assisted chemical etching in silicon substrates. The process is aimed at improving the substrates' RF characteristics, while being compatible as a post-CMOS process with RF devices present on the front side. A thin porous gold layer is deposited on the back side, patterned by lift-off photolithography, defining the Si to be removed and the remaining structures. Metal-assisted

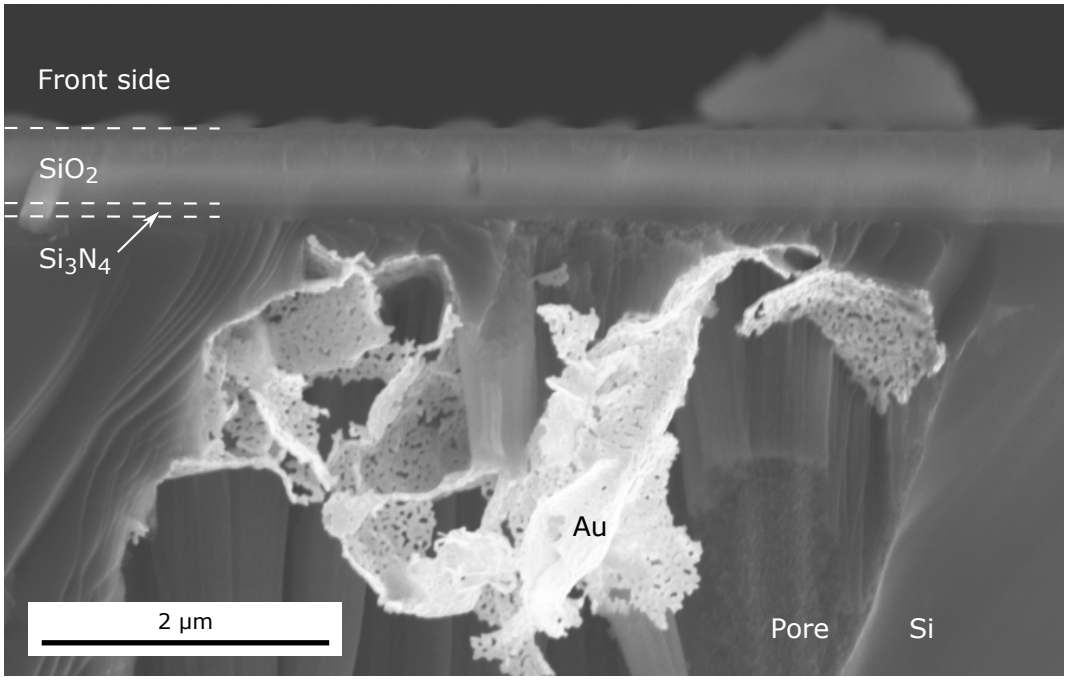

Figure 4.16: SEM cross-section view of a metal patch reaching the nitride etch-stop layer. The nitride layer is colour-highlighted for visibility.

chemical etching is then performed in a HF-based electrolyte, with Au patterns "sinking" into the substrate until reaching the etch-stop Si_3N_4 layer situated under the BOX.

By optimizing the MACE parameters related to the metal layer morphology, the electrolyte composition and the etching conditions, pores with uniform etching profiles are obtained for substrate thicknesses of $200\,\mu m$ in less than an hour. A summary of the impact of each parameter on the relevant MACE etching characteristics is given in Table 4.7.

Table 4.7: MACE parameters summary. The symbols ↗/↘ signify that the parameter increases/decreases the corresponding etch characteristic, and – that no impact or only a negligible impact was observed.

Parameter	Etch uniformity	Etch rate	Underetch
Au thickness	↗	↘	–
Annealing	↗	–	–
Pattern size	↗	↗	–
Molar ratio ρ	–	↘	↘
HF molarity	–	↗	↗
IPA	↗	↘	↘
Temperature	↗	↗	↗
Illumination	–	–	–

Even though the fabrication of the trenches was successful, the rigidity of remaining part of the Si structure turned out very low. The fabricated samples broke too fast to be further processed or to perform any measurements. Therefore, further research to improve the mechanical strength of the substrate has to be performed. The possibility of filling the trenches with a low-k dielectric can be considered, such as polymers with inherent low relative permittivity and dielectric loss factors [45, 46].

Chapter 5

Porous Silicon Formation by MACE with Metal Nanoparticles

5.1 Introduction

In Chapter 4 was determined that removing a large proportion of the substrate is possible by etching wide trench-like pores by MACE. However, the solution is not optimal, as the remaining structure is mechanically weak and the substrate's rigidity is reduced drastically.

Unlike the trench-like wide pores, demonstrated in the previous chapter, this process aims to transform the whole bulk substrate thickness into a macroporous silicon layer. Similar work has been published where measurements of CPW transmission lines, fabricated on microporous silicon substrates, demonstrate enhanced insertion losses and linearity due to the improved effective resistivity and permittivity of the substrate [47]. But for the fabrication steps to be compatible as a post-CMOS process, the most-used anodization technique for PSi manufacturing can not be employed here, as it requires dedicated electric contact with the front-side of the silicon. Instead, MACE with gold NPs deposited on the back-side, is proposed as a low-cost, electroless method of PSi formation.

In the following sections, first the fabrication steps are explained as a whole process. Then, the two main steps to master are detailed: the Au NP deposition technique and the etching process. Finally, the fabrication results are presented and analysed.

5.2 Fabrication steps

The fabrication process can be described by distinguishing four main steps (similar to the process from Section 4.2) illustrated in Figure 5.1:

(a) The same starting SOI substrate is used as in Chapter 4. The RF devices are already present on the front-side, and a nitride etch-top layer is required under the BOX. The back-side surface of the Si can be treated, impacting NP formation. Three different surface states are characterized in this work (see Section 5.3): etched in HF solution, with a native oxide (NO) layer and with a POx layer.

(b) Gold NPs are deposited by sputtering on the whole surface of the wafer's back-side. An annealing can be done to achieve the desired size and distribution of NPs on the surface (see Section 5.3).

(c) The substrate is immersed in a HF solution and the Au NPs penetrate the substrate, creating a porous silicon layer (see Section 5.4). The front-side of the substrate with devices is protected from the electrolyte by placing the wafer in a hermetic sample holder.

(d) The fabrication is finished when the NPs reach the nitride layer, after traversing the substrate. The remaining silicon layer is then ideally completely porous. Finally, the sample is rinsed and dried.

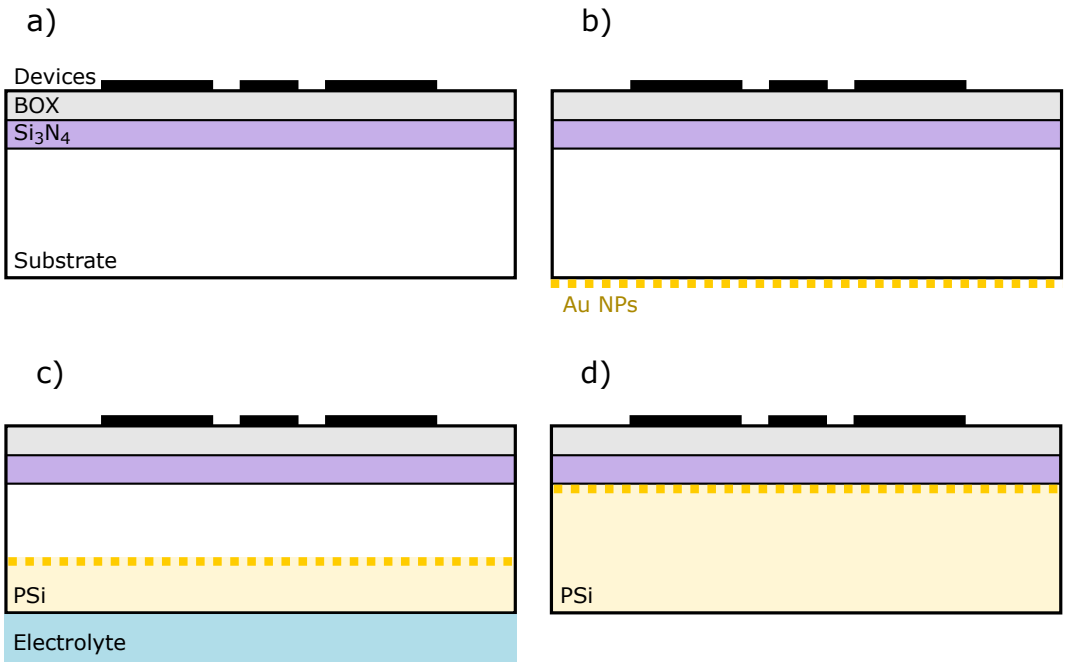

Figure 5.1: Porous substrate fabrication steps by MACE with Au NPs. (a) Initial substrate with RF devices fabricated on the front-side. (b) Deposition of Au NPs on the back-side. (c) Etching of the silicon in the electrolyte solution. (d) End of the etching process at the etch-stop layer.

5.3 Au nanoparticle formation

5.3.1 Deposition techniques

Several deposition techniques exist for the formation of noble metal NPs on silicon substrates. The most common, used for MACE, are:

Electroless deposition Metal ions are dissolved in HF solution. A galvanic reaction reduces the ions to metal, which deposits as nanoparticles [40]. The same solution is often used for the metal deposition and Si etching at the same time. However, the process is more suited for Si NW production from dendrite-like structures [41, 48, 49].

+ Easy and low-cost one-step process.

– Difficult control of the dimensions and homogeneity.

Deposition from colloidal solution NPs suspended in a colloidal solution are deposited on functionalized Si surface [50–52].

+ Possibility of assembly at specific sites by irradiating the surface with charged particle beams.

– Cost and speed: requires multiple steps, i.e. preparation of the solution, preparation of the surface (with or without linker molecules).

Physical vapor deposition In particular, sputtering PVD presents the most advantages for NP deposition in the context of this work [53–56].

+ Well controlled film thickness, coverage and roughness.

+ Can be deposited at relatively low substrate temperature.

In this work, sputtering deposition was chosen and was done with a Cressington 208HR Magnetron Sputter Coater (see Figure 5.2). This technique allows fast operation (a few minutes for the whole process including the vacuum pumping) on a wafer scale or on small samples, and a precise thickness control with a resolution better than $0.1\,\mathrm{nm}$ [57]. Making the setup ideal for easy metal NP deposition on several silicon surfaces and for various thicknesses.

Figure 5.2: Cressington 208HR Magnetron Sputter Coater [57].

5.3.2 Fabrication and results

The $1\,\mathrm{cm} \times 1\,\mathrm{cm}$ Si samples were first prepared by performing a standard cleaning. Three surface states were then achieved before the NP deposition:

HF Hydrogen-terminated silicon surface, obtained by dipping in aqueous HF, followed by deionized (DI) water rinsing.

NO A native oxide layer, grown for 24 hours in a controlled cleanroom environment after the cleaning.

POx A silicon oxide layer, formed by an O_2 plasma[1].

After the surface preparation, Au NPs were sputtered at room temperature with varying layer thickness between 3 nm and 9 nm. Gold was chosen as the most available metal at the moment of fabrication (besides silver, platinum and palladium), while meeting the required characteristics for MACE: [37, 52, 58]

- stable in HF solution;
- relatively high etching speed; and
- straight pore generation.

The deposition results with the different parameters, analysed by scanning electron microscope (SEM), are shown in Figure 5.3. The NO and POx surfaces present the same NP distributions and will be more generally called "oxide surfaces". The following observations can be made:

- All the surfaces present the most circular-shaped NPs for the 3 nm samples, with a mean NP diameter $d_{\text{NP}} \approx 15$ nm.
- For the 6 nm samples, the NPs are more randomly shaped with $d_{\text{NP}} \approx 30$ nm.
- Finally, for the 9 nm samples, the metal coverage of the substrate increases drastically and the shapes can not be called nanoparticles, but rather a partially discontinuous gold film.

In the general case, the NPs on the HF surface are slightly smaller in size than on the oxide surfaces, but remain in the same order of magnitude.

Thermal dewetting of gold films is a known technique for fabrication of Au NPs. The post-growth annealing causes aggregation of nanoparticles, and the formation of discrete single-crystalline islands with various diameter ranges (function of the initial film thickness, the annealing temperature and duration) [54–56, 59]. However, the substrate's temperature must be kept under 360°C to prevent gold-silicide formation, also prevented by the presence of the SiO_2 layer [60]. Moreover, high temperatures are to be avoided in this work, designed as a post-CMOS process. Therefore, a 10-minute annealing of the samples from Figure 5.3 was done at 300°C in N_2 atmosphere, and the results are given in Figure 5.4.

The nanoparticles post-annealing are globally more circular and better defined at 3 nm and 6 nm, with a slight increase in mean size. Whereas at 9 nm, the discontinuous film before annealing transformed into randomly shaped separated Au islands with dimensions ranges from less than 100 nm to several hundreds of nanometres. Important size deviations were observed, mostly seen here for the 6 nm POx sample compared to the hydrofluoric acid (HF) and NO ones. These were found to be due to thickness non-uniformity between the samples after the sputtering, most likely caused by the positioning in the deposition chamber with varying distances from the sputtering target. Since no fundamental differences were observed for the NP formation between the clean Si and the oxide surfaces, POx samples are used for the rest of this work.

[1] 1 min at 150 W in a barrel plasma etcher

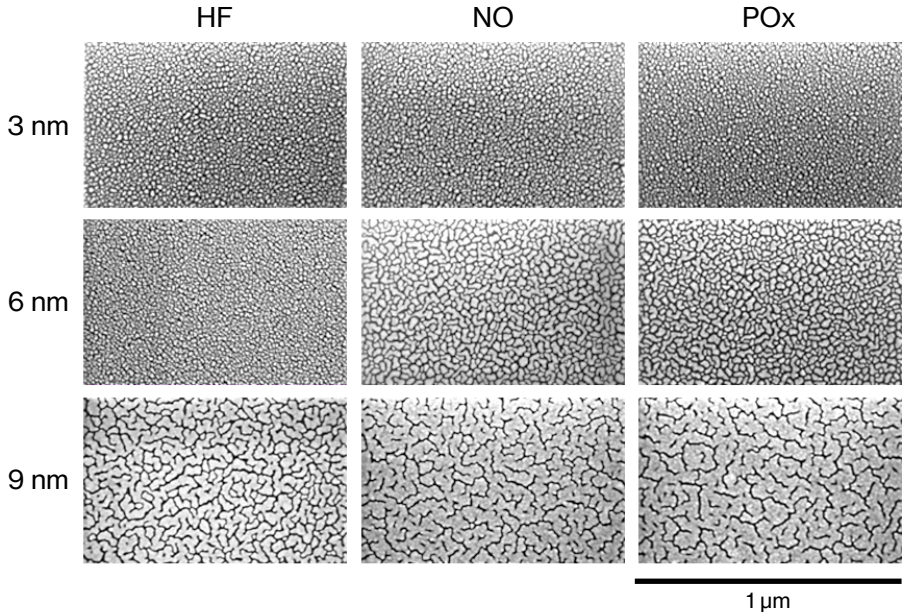

Figure 5.3: SEM top-view images of gold NPs deposited at room temperature on silicon substrates for increasing thicknesses.

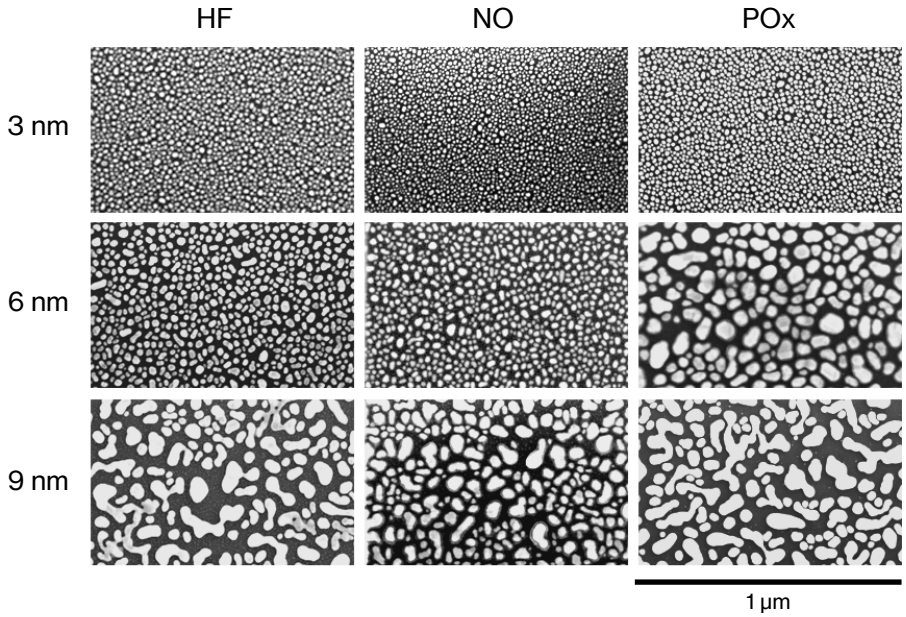

Figure 5.4: SEM top-view images of annealed (10 minutes at 300°C) gold NPs deposited on silicon substrates for increasing thicknesses.

5.4 Metal-assisted chemical etching

After the NP deposition, the samples were immersed in the HF electrolyte ($\rho = 83\%$) for two hours at room temperature (25°C). After the etching, the porous substrates were carefully rinsed in DI water and dried with N_2.

SEM images of the 6 nm POx non-annealed and the 3 nm POx annealed etched samples are

shown in Figure 5.5 and Figure 5.6. The samples with similar NP sizes were chosen for the etching process, and the illustrated images are representative references for comparison between non-annealed and annealed results.

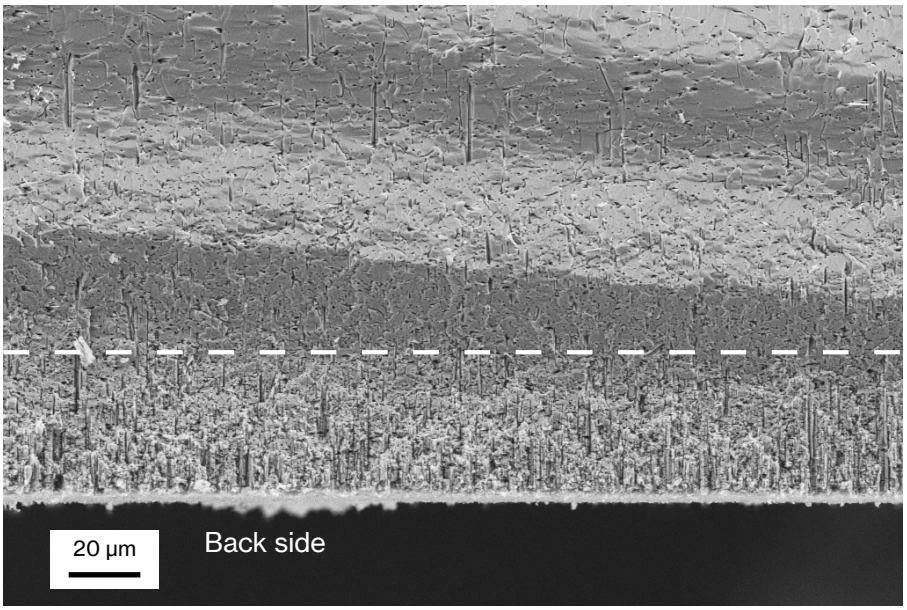

Figure 5.5: SEM cross-section view of the 6 nm POx non-annealed etched sample. Etching parameters: $\rho = 83\%$, $t = 120$ min, $T = 25$°C.

The sample prepared by MACE of the non-annealed NPs displays a varying porosity with the etching depth. Close to the back-side surface, for a depth smaller than approximately $50\,\mu$m (below the white dashed line in Figure 5.5), a high porosity is observed. Deeper into the substrate, the density of the pores decreases progressively with the NPs "disappearing". Only a few wide pores are still visible, similar to the annealed sample discussed later. In literature, similar results have been reported for small metal particle sizes (under 100 nm), showing that well defined pores perpendicular to the surface are rarely observed [38, 61, 62]. Instead, the substrate is etched in a highly disordered fashion in the surface-near region, confirming the results of this work.

The sample etched with the annealed NPs exhibits different results. Wide and well defined pores are visible with varying depths. The measured maximum depth of the pores is around $200\,\mu$m, corresponding to a maximum etch rate of approximately $1.7\,\mu$m/min. At the bottom of the pores, clusters of Au NPs in the micrometre range can be observed (indicated with white arrows and the inset in Figure 5.6), defining the etched shape and size. However, the pores are spread out and the most nanoparticles remained at the surface of the sample, creating trenches by etching in directions parallel to the surface.

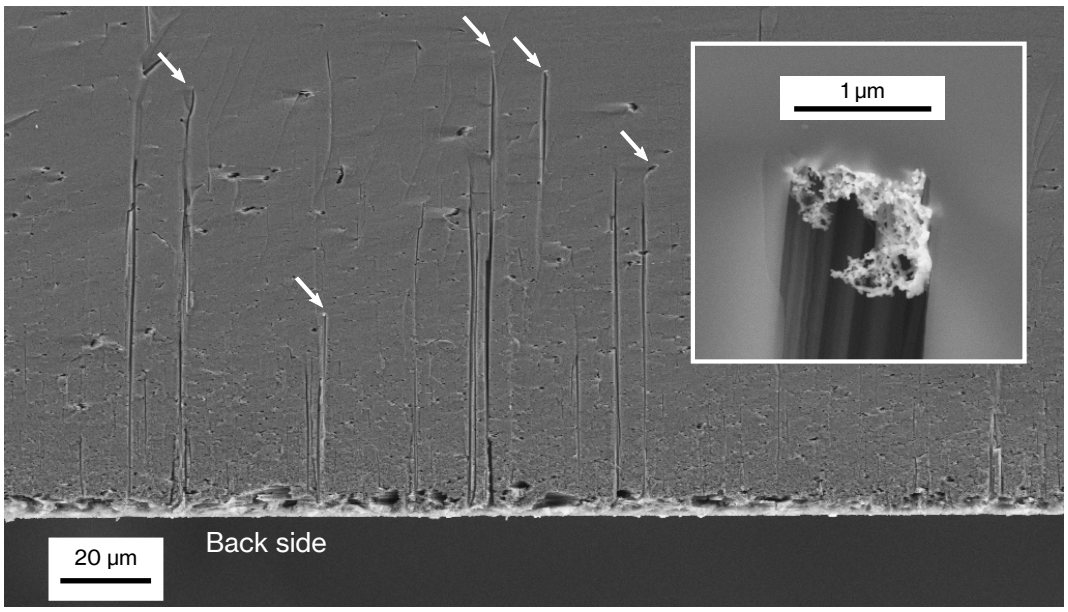

Figure 5.6: SEM cross-section view of the 3 nm POx annealed etched sample. Etching parameters: $\rho = 83\%$, $t = 120$ min, $T = 25$°C. Inset: magnification of NP clusters marked with white arrows.

5.5 Conclusion

The possibility of porosifying a Si-based substrate, as a post-CMOS process, by metal-assisted chemical etching with Au nanoparticles was studied. The sputtering PVD was found to be a well-suited Au deposition technique. In combination with thermal dewetting, fabrication of ordered nanostructures ranging from NPs to porous films was achieved.

However, the etching results of the samples with annealed or non-annealed NPs demonstrated non-uniform porous layer, with a maximum depth of 50 µm. This indicates that this fabrication process is not adapted for thick substrate porosification. Instead, wider metal structures (larger than 100 nm) seem to be more suited for deep pore formation, as was shown in Chapter 4.

Chapter 6

Lateral Porous Silicon Formation by Galvanic Etching

6.1 Introduction

In the previous chapter, porosification of thick substrates by MACE with nanoparticles was demonstrated to be unsuccessful. Therefore, in this chapter, a novel process is proposed for the electroless fabrication of porous Si substrates from the back-side. The galvanic etching and lateral porosification techniques are combined into one post-CMOS compatible process, with high potential for fast and low-cost integration. In the following sections, first the global fabrication steps are outlined. Then, the trench formation by DRIE and the galvanic porosification phases are detailed and illustrated with results.

6.2 Fabrication steps

The fabrication process can be described by five main steps, illustrated in Figure 6.1. The schematic represents one hexagonal trench pattern, whereas the actual mask is composed of periodic hexagons forming a honeycomb-like structure.

(a) The same starting SOI starting is used as in the first two fabrication processes (Chapter 4 and Chapter 5). As a post-CMOS process, the RF devices are present on the front-side. A Si_3N_4 layer is required here as well, to protect the BOX from HF electrolyte.

(b) A silicon nitride layer is deposited on the back-side, with the purpose of electrically insulating a part of the metal from the substrate. LPCVD is preferred for better resistance to HF [28]. The layer is then patterned by reactive-ion etching (RIE) in SF_6 plasma to create hexagonal openings. A platinum thin film is deposited above with good step coverage, providing electrical connection of the whole Pt layer with the substrate. A titanium adhesion layer is used between Si_3N_4 and Pt [63].

(c) Deep hexagonal trenches are etched in two steps. First, Pt and Si_3N_4 layers are etched by RIE in SF_6 plasma. Second, the Si substrate is etched by deep reactive-ion etching (DRIE) with a typical Bosch process [28] (see Section 6.3). A thick patterned photoresist is used as mask for the whole etching process.

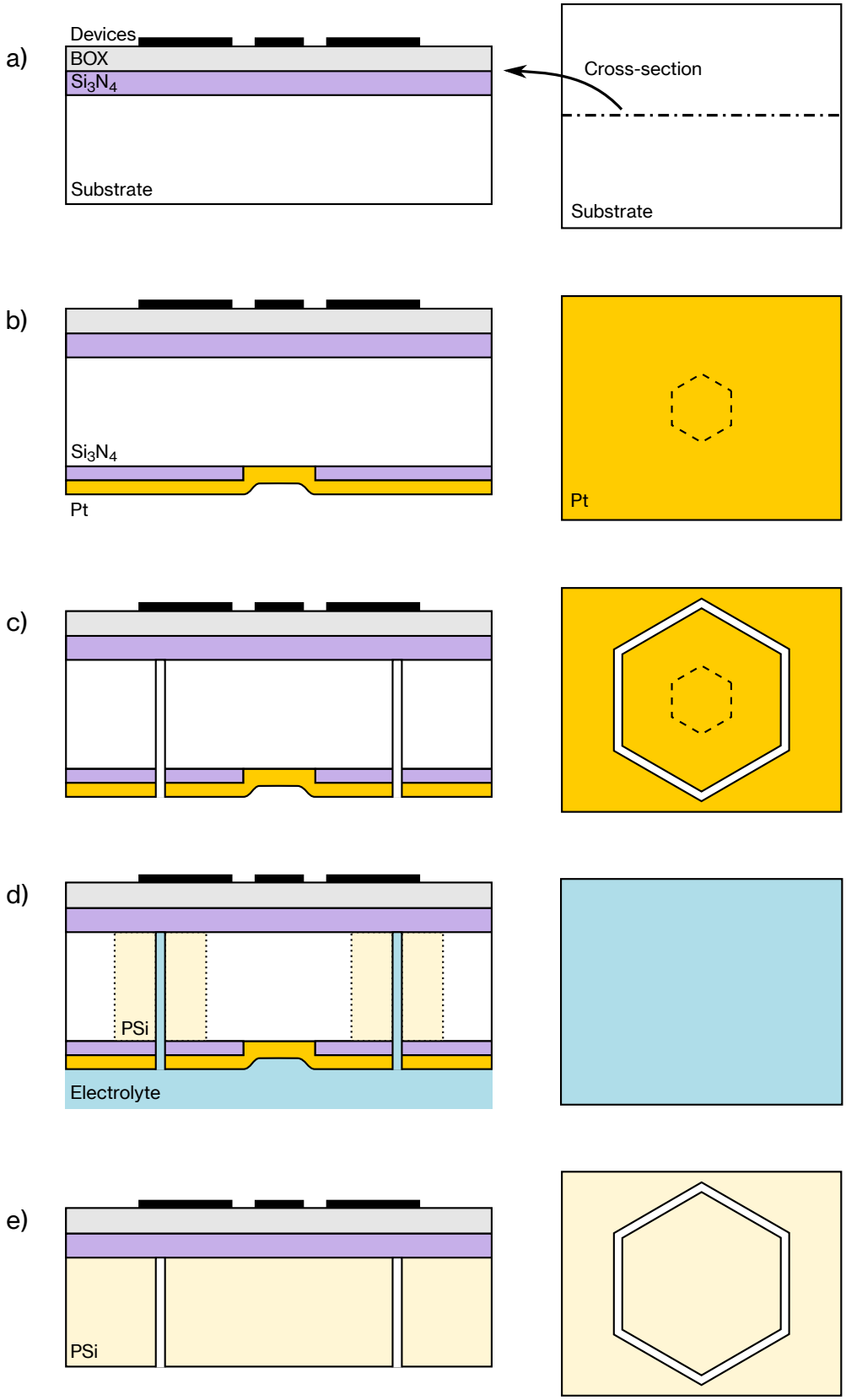

Figure 6.1: Lateral PSi fabrication steps by galvanic etching: cross-section view on the left with the corresponding bottom view on the right. (a) Initial substrate with RF devices fabricated on the front-side. (b) Deposition of a nitride layer patterned with a hexagonal opening, and a thin platinum film with step coverage. (c) Etching of hexagonal trenches by DRIE. (d) Galvanic PSi formation by immersion in an electrolyte solution. (e) Completely porous substrate after an eventual removal of the back-side layers.

(d) The substrate is immersed in a HF-based electrolyte, inducing a galvanic lateral PSi formation. The porosification progresses from the trench walls into the substrate's depth (see Section 6.4). Front-side devices are protected from the electrolyte by placing the wafer in a hermetic sample holder.

(e) Once the whole substrate is porous, the surface is rinsed with DI water and dried. Finally, the back-side Si_3N_4 and Pt layers can be removed if required.

6.3 Trench formation

The trenches in this process are etched by DRIE, a widely used anisotropic etch process for the fabrication of high-aspect-ratio trenches and microstructures in Si. Although the process is slow and costly, it is well documented in literature, enabling easy optimization of the etching parameters to achieve the desired features.

Metal-assisted chemical etching was considered as an alternative process to DRIE for the trench creation. As was shown in Chapter 4, MACE is also suited for the fabrication of uniform high-aspect-ratio structures, with the advantage of being fast and low-cost. However, more fabrication steps would be needed for the patterning and deposition of a metal layer for the trench etching (separate from the Pt), and thus adding complexity to the total process. DRIE was therefore the preferred choice, with short implementation time, to demonstrate the process's concept.

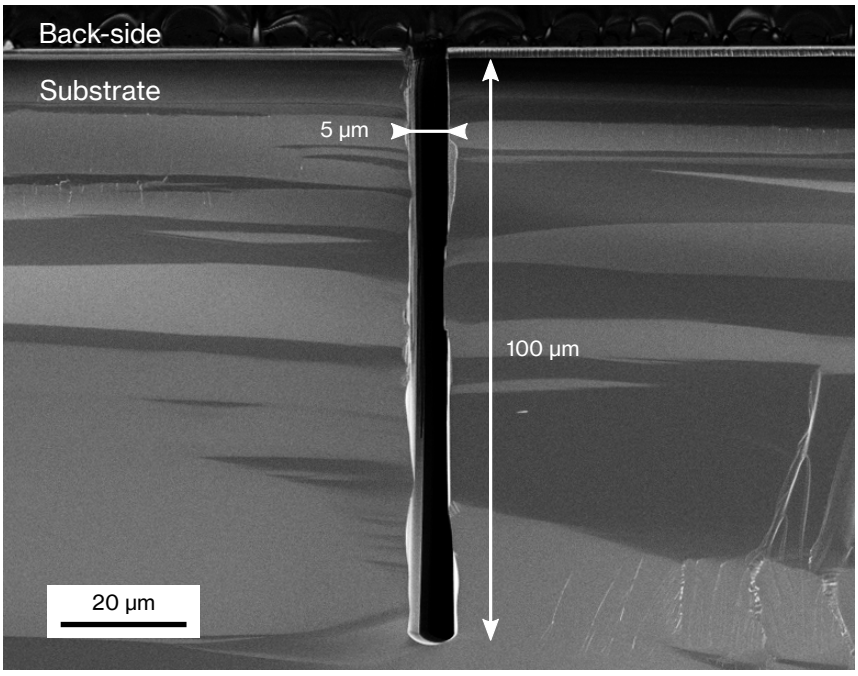

Figure 6.2: SEM cross-section view of a trench etched by DRIE.

The process takes advantage of self-alignment by using the same 30-µm-thick photoresist[1]

[1] AZ 9260 by MicroChemicals

mask for the Pt/Si_3N_4 layers etching with SF_6, and Si etching done by DRIE. The result of the DRIE, after 220 cycles of a typical Bosch process, is shown in Figure 6.2. A 100-µm-deep trench is observed with a very uniform etch profile, although larger depths (depending on the substrate's thickness) can be achieved be increasing the number of etching cycles. The measured trench width is 5 µm, as defined by the mask pattern.

6.4 Galvanic etching

Galvanic etching of Si is a process similar to metal-assisted chemical etching. Electronic holes are generated by H_2O_2 reduction in presence of a metal, and are injected in silicon. However, in contrast with MACE, the semiconductor is etched remotely from the initial site of hole injection [64]. Becker et al. [65] managed to fabricate thick uniform nanoporous layers by galvanic etching of Si. On one side of the wafer, Pt is deposited as H_2O_2 reduction site. On the other side, PSi is formed in locations not masked by Si_3N_4, as shown in Figure 6.3.

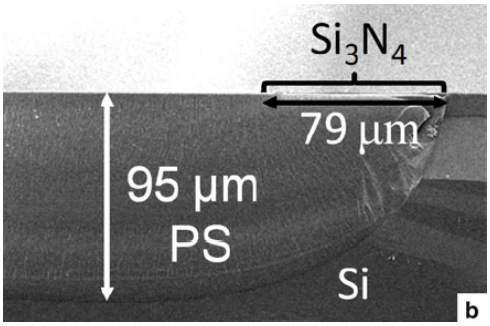

Figure 6.3: SEM cross-section view of a galvanic PSi layer. Adapted from [65].

However, in a post-CMOS process, the front-side can not be used, making the "classical" implementation of galvanic etching impossible. The possibility of lateral porosification was thus explored. Lateral PSi fabrication schemes have been proposed in literature, mostly for the production of porous membranes in microfluidic devices [66, 67]. The processes are, however, usually based on the anodization approach, requiring an external power supply.

In this work, an innovative PSi substrate fabrication technique is proposed. Electroless galvanic etching is combined with lateral porosification, requiring back-side-only access to the substrate and no external power supply. A schematic of the etching process is given in Figure 6.4. The reduction of H_2O_2 occurs at the electrolyte–metal interface, generating electronic holes. The carriers are injected in Si through the opening in the Si_3N_4 layer, where Pt is in contact with the substrate. The holes migrate to the etching site, where the silicon is in contact with the HF electrolyte, generating porous Si. By Comsol simulations was shown that with correct dimensioning of the structure, an even distribution of the hole current can be achieved throughout the substrate depth (see Appendix B) [68]. Thus, leading to a uniform etch progression from the trench walls to the center of the substrate.

The fabricated samples were immersed for one hour in the electrolyte composed of 15:5:2 (vol) of 48 wt. % HF, ethanol and 30 wt. % H_2O_2. The ethanol is used as a surfactant to enable wetting of the Si during the etching process [65]. The results were then observed by SEM,

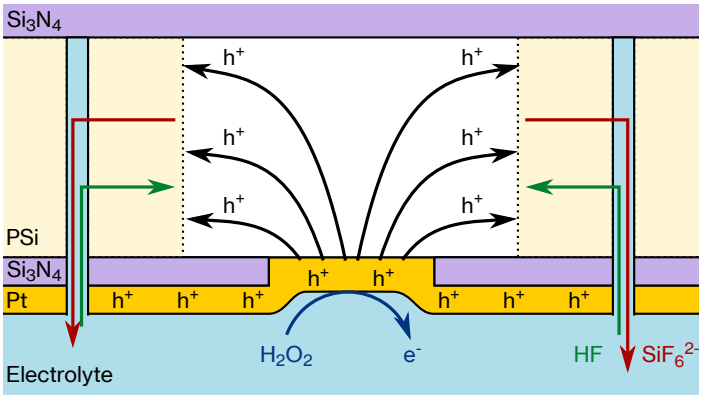

Figure 6.4: Schematic of lateral Si porosification process by galvanic etching.

illustrated in Figure 6.5. The formed PSi layer is found on all sides of the trench and measures 15 µm. The presence of PSi at the bottom could indicate that the trenches do not need to be formed for the whole substrate depth. From the fabricated samples, porous Si formation under the nitride layer was observed. This phenomenon is explained by unintended openings in Pt/Si_3N_4, indicated by red arrows in Figure 6.5, allowing the electrolyte to penetrate and etch the substrate underneath. Further tests to porosify the whole substrate have still to be performed.

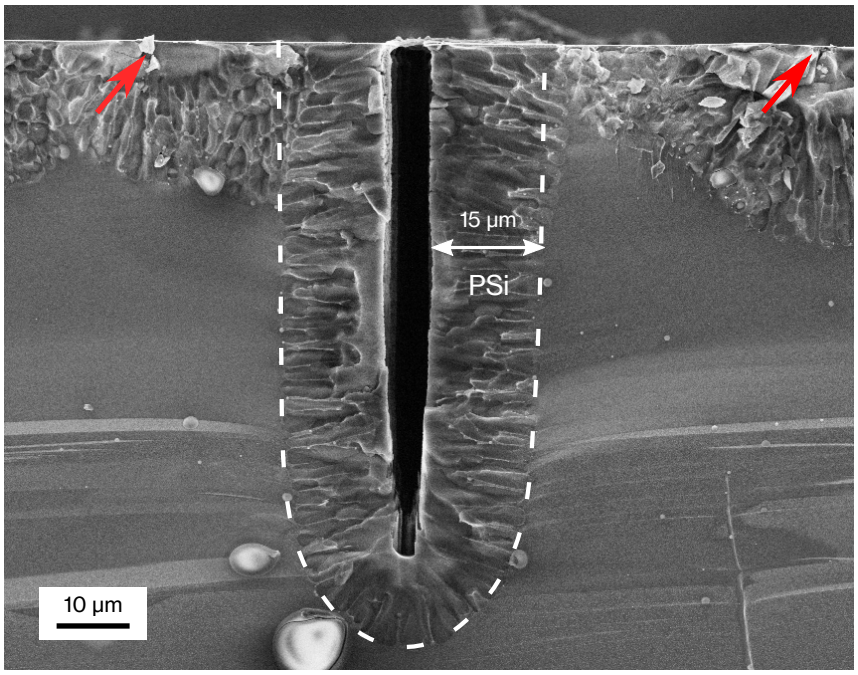

Figure 6.5: SEM cross-section view of a lateral PSi layer formed by galvanic etching.

6.5 Conclusion

An innovative fabrication scheme was conceived for the porosification of silicon substrates as a post-CMOS compatible process. The design regroups galvanic etching and lateral porosification approaches to achieve PSi formation from the back-side with no external power supply requirement. Fabrication of deep trenches in the substrate by DRIE and the early stage of uniform PSi formation by galvanic etching are demonstrated.

However, further development must be done to validate the fabrication process. The following points are the most important to accomplish:

- Achieve complete porosification of the substrate.
- Enhance the etching rate by optimizing the etching parameters, similar to the work done in Chapter 4.
- Integrate trench fabrication by MACE, in order to potentially improve the process's cost and throughput.

Conclusions

The main purpose of this master thesis was to design and fabricate Si-based RF substrates. A particular attention was given to the integration of the fabrication as a post-CMOS compatible process. Whereas recent results in literature are found for porous silicon substrates with great RF characteristics, their complete CMOS process integration and design-independence has not been achieved yet.

The first part of this work focusses on trenched Si substrates. In Chapter 2 semiconductor simulations are realised in order to prove the substrates' RF performances. The effective parameters are extracted from CPW simulations for different trench morphologies and bulk substrate characteristics. A degradation of the effective resistivity is observed due to fixed oxide charges, similar to the parasitic surface conduction effect, observed in HR-SOI substrates. With the addition of interface traps to the trench interfaces, the defects are shown to capture the free carriers and counteract the oxide charges. The trenched substrates then demonstrate high effective resistivity – above $3\,\mathrm{k\Omega\cdot cm}$. An improvement of the effective permittivity is observed as well, with values down to 3 due to the addition of air- or SiO_2-filled pores.

In Chapter 3 an integrated inductor is simulated on trenched substrates. The increase of the effective resistivity and the decrease of the permittivity demonstrate an improvement of the inductor's Q factor and frequency bandwidth. The Q factor is increased by a factor 4 and the bandwidth by approximately 50% with the transition from a bulk substrate to a HR trenched substrate.

In Chapter 4, metal-assisted chemical etching is demonstrated as a fast and low-cost fabrication process for the formation of deep trenches in Si substrates. A gold porous layer sputtering deposition technique is implemented that allows uniform etching of the trenches with a directional etch profile, perpendicular to the deposition surface. MACE etching parameters are studied thoroughly and are optimized to enable fast and uniform etching.

The second part of this work consists in the porosification of silicon substrates without external power supply or front-side access, required by the classical anodization techniques. In Chapter 5 a process is defined for porous Si formation be MACE with metal nanoparticles. Metal NP formation is obtained by sputtering of ultra-thin gold films, followed by thermal annealing. The correlation between deposited metal thickness and nanoparticle size and surface coverage is illustrated. Porosification with NPs by MACE was performed. The results indicate a non-uniform etching rate and direction with a maximum etch depth of approximately $50\,\mu\mathrm{m}$, not suitable for thick substrate porosification. The observations are supported by similar results found in literature.

In Chapter 6, an innovative fabrication process is proposed combining lateral porosification and galvanic etching of silicon. Deep trenches are etched by DRIE, however integration of MACE can be envisioned to improve the process' cost and throughput. By engineered patterned deposition of Si_3N_4 and platinum layers, the substrate can be laterally and uniformly porosified by immersion in HF-based solution.

Suggested future research perspectives include:

- Improving the mechanical strength of trenched substrates from Chapter 4 by filling the trenches with a low-k dielectric material.
- Completing the galvanic porosification process from Chapter 6 for the full wafer thickness and perform RF measurements on the resulting porous substrate.

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Appendix A

HFSS — Inductor Substrate Size Impact

In order to take into account the integration of all electromagnetic fields, the size of the substrate and the surrounding "air box" must be sufficiently large. The radius of the simulated substrate was progressively increased, until the variation of the inductor's Q factor between two iterations became smaller than 1%. This condition was satisfied for all substrates at $r_{\text{sub}} = 600\,\mu\text{m}$ (see Figure A.1), value therefore used in the simulations.

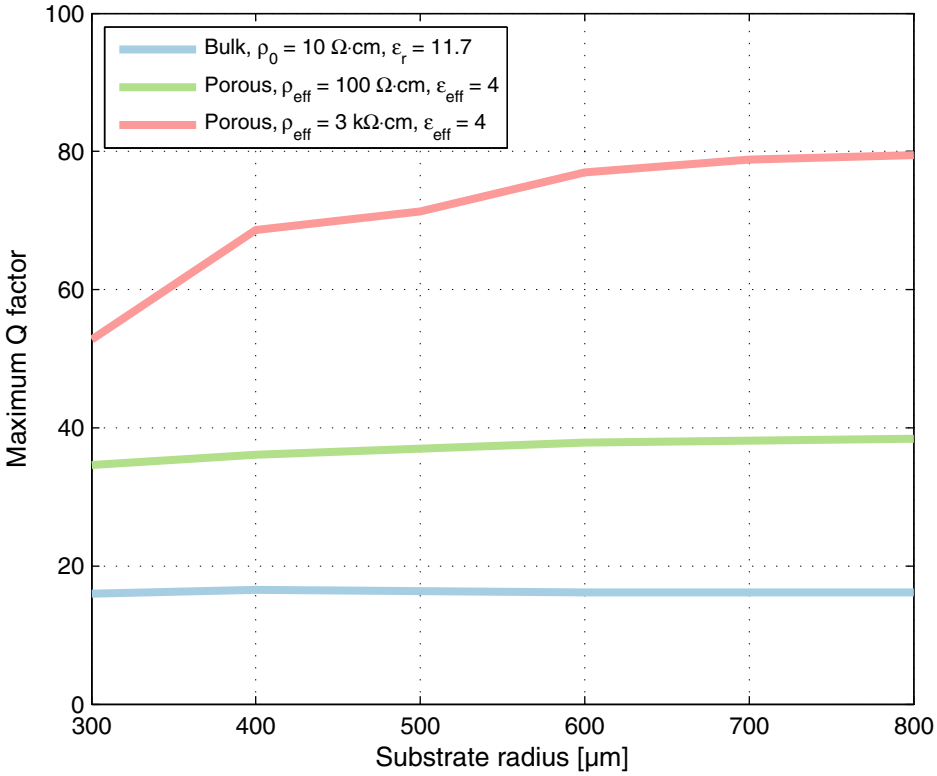

Figure A.1: Maximum Q factor of the inductor as a function of the simulated substrate size.

Appendix B

Galvanic Etching — Current Distribution

Comsol simulations were performed by Scheen [68] to get an insight into the current distribution inside the substrate during the lateral galvanic etching of Si. The simulated model is illustrated in Figure B.1. The metal contact with generated holes due to H_2O_2 reduction is represented by the ohmic contact with a variable width w_c. The silicon–electrolyte interfaces form Schottky contacts on the walls of the trenches. Other interfaces are electronic insulators, representing the Si_3N_4 layers.

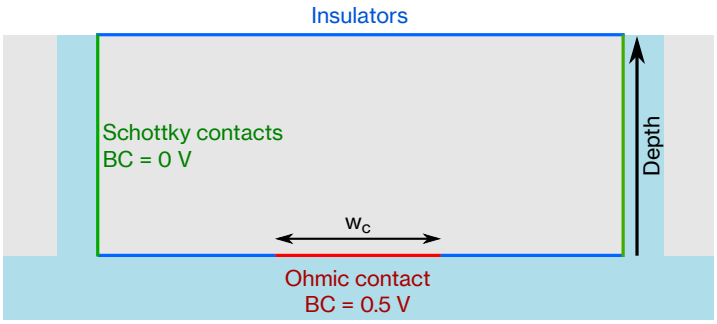

Figure B.1: Comsol simulation model for current distribution during galvanic etching.

The result of the simulation is given in Figure B.2. The hole current density exiting the substrate through the Schottky contacts is shown along the depth of the trench, for different w_c values. The result indicates that an even distribution of the current is possible to achieve, when w_c is much smaller than the depth of the substrate ($200\,\mu m$ here).

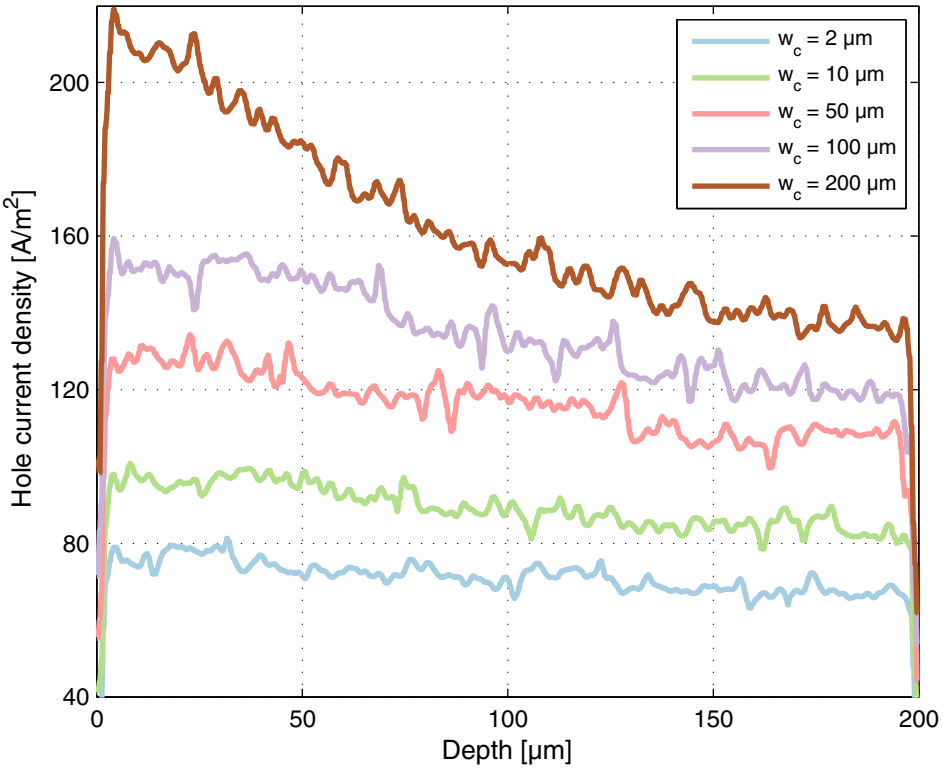

Figure B.2: Hole current distribution as a function of the trench depth.

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