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Power Quality of Smart Grids: study of supraharmonics (disturbing phenomena in the frequency range 2-150 kHz)

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Abstract

Disturbing phenomena in the frequency range 2-150kHz, known as supraharmonics are gaining more and more interest in the recent year. In this master thesis an experimental setup is built to assess the supraharmonic emissions of an Active Power Factor Corrector circuit. The goal is to test a specific control and to asses the behaviour of the converter as a supraharmonic current or voltage source. To do so, we put an inductance (L_s) in serie with the grid and measure the voltage and current at the input of the device under test for different values of the serie inductance. By looking at the 50kHz voltage and current variation in function of the serie inductance we can deduce the supraharmonic current or voltage source behaviour. We use 800Hz band grouping around the 50kHz switching frequency.

This setup is composed of a Texas instrument development kit connected to an auto transformer. The TI kit is the masterpiece and permits to implement the desired control using Matlab Simulink.

The complete measurement method is detailed and digital filtering is used to mitigate the side effects of the Discrete Fourier Transform (DFT).

Two main measurements are presented. First the effectiveness of the APFC in reducing the low frequency harmonics (up to 2kHz) is shown. Secondly, the supraharmonic voltage source behaviour of the converter is confirmed.

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Acronyms

ADC analog-to-digital converter. 23, 28, 36

APFC Active Power Factor Corrector. i, 2, 15, 24, 30, 40, 42, 46, 47, 52

DAC Digital-to-analog converter. 22

DFT Discrete Fourier Transform. i, 3, 13, 31, 52

DTFT Discrete Time Fourier Transform. 31

EMI electromagnetic interference. 26

EUT equipment under test. 16, 50

EV Electric Vehicle. 2, 52

FFT Fast Fourier Transform. 31

hf High Frequency. 7–9, 11

HP high-pass. 32

IBC Interleaved Boost Converter. 2, 3, 15, 28, 30, 41–43, 53

IEA International Energy Agency. 11

IPM Interior permanent magnet machine. 22

IRR Infinite Impulse Response. 32

MPPT Maximum Power Point Tracking. 7, 8

PFC Power Factor Corrector. 2, 3, 20, 24, 40

PV photovoltaic. 4, 8

PWM Pulse Width Modulation. 4, 22, 23, 27, 62

SSA Sate Space Averaging. 28

SSL Small-Signal Linearization. 28

THD Total Harmonic Distortion. 35, 41–43

Introduction

Context

Supraharmonics are gaining more and more attention in the years due to the increasing use of switching power electronics. All kinds of power electronic converters are connected to the grid, such as electrical vehicles, solar inverters, LED lamps and small converters to charge portable devices. The nonlinear characteristics of such loads will lead to the increase of supraharmonic emission between 2 and 150 kHz [1].

To facilitate the efficient conversion of power from DC to AC and vice versa, power electronics devices, particularly converter-based devices, are widely used and especially for higher power applications. Active PFC circuits are often used in EV chargers in order to meet the requirements with respect to harmonics given by standards[2].

However, the use of these devices at a larger scale introduces both known and unknown effects on the grid. One significant effect is the generation of "supraharmonic" disturbances, which occur in the frequency range 2 to 150 kHz and are primarily caused by self-commutated converters. These supraharmonic disturbances can lead to component degradation, excessive heating, malfunctioning, interference with other devices, and even equipment damage [3],[4].

Objectives

The main objective is to study supraharmonic emissions with a focus on the emission of an Interleaved Boost Converter (IBC) used as Active Power Factor Corrector (APFC). We are looking at the impact of the control loop on the high frequencies emissions. The goal is to identify experimentally

the behaviour of the converter as a supraharmonic voltage source or current source. To do so, we put an inductance (L_s) in serie with the grid and measure the voltage and current at the input of the TI kit for different values of the serie inductance. By looking at the 50kHz voltage and current variation in function of the serie inductance we can deduce the supraharmonic current or voltage source behaviour. We use 800Hz band grouping around the 50kHz switching frequency.

Methodology

The methodology is experimental. A test bench as been developed based on a Texas Instrument development kit. This kit is equipped with PFC stage composed of an IBC and is programmable using Matlab Simulink. A frequency domain analysis is proposed using Discrete Fourier Transform, digital filtering and specific band grouping.

Chapter 1

State of the art

1.1 Sources of supraharmonics

1.1.1 Solar inverters

The photovoltaic energy production has dramatically increased in the past decade (Figure 1.1). Moreover, an average annual generation growth of 25% in the period 2022-2030 is needed to follow the Net Zero Emissions by 2050 Scenario [5]. But solar energy can't be used on the AC grid without inverters. In this section we will discuss the supraharmonic emission of small inverters (<10kVA).

Most of the single-phase PV inverters available on the market today are self-commutated and uses various modulation techniques such as Pulse Width Modulation (PWM). There are several PWM strategies in existence, but their underlying principles are generally similar. Self-commuted inverters connected to the grid can control both current as well as voltage waveforms to adjust the power factor and suppress harmonics [6]. However, this PWM switching unintentionally introduces high-frequency (supraharmonics) emissions into the grid.

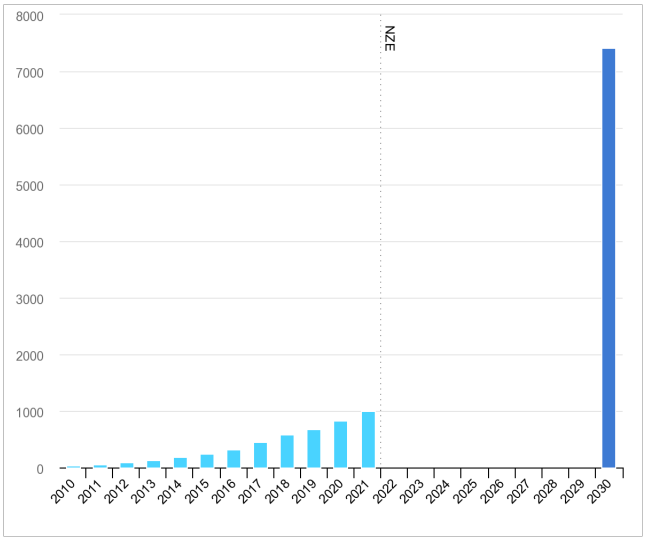
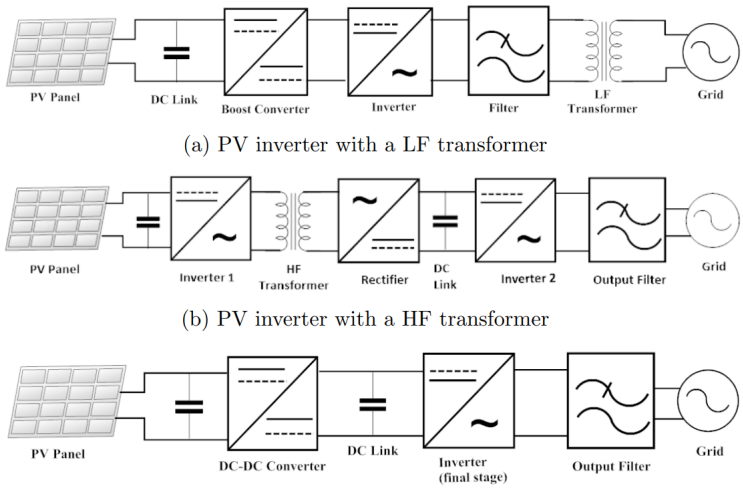


Figure 1.1: Solar PV power generation in TWh in the Net Zero Scenario, 2010-2030

[5]



(a) PV inverter with a LF transformer

(b) PV inverter with a HF transformer

(c) Transformer-less PV inverter

Figure 1.2: Topologies of small-scale, grid-tied, single-phase PV inverters

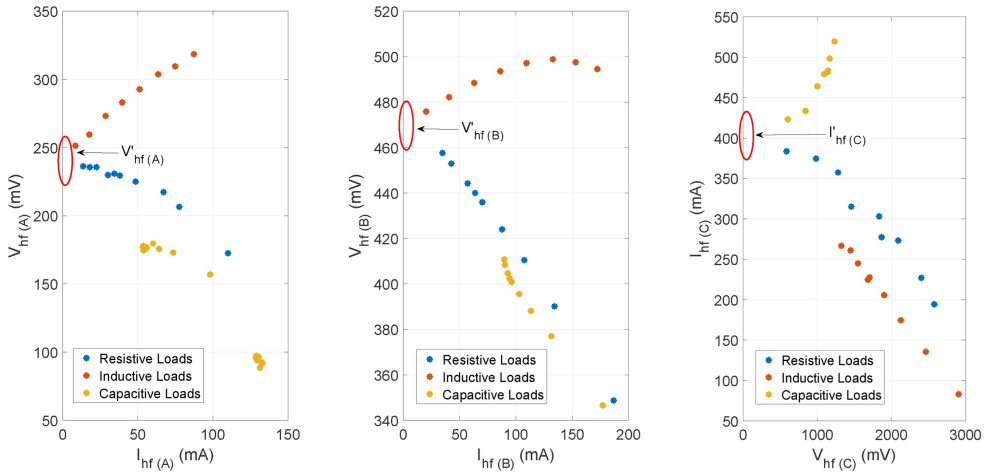
Almost all grid-tie, small-scale, single-phase inverters can fall into one of those three topologies: low frequency inverters, high frequency inverters and

transformer-less inverters [7]. Those topologies are represented on Figure 1.2.
In [8], a comparison is made between three types of single-phase inverters with their specifications on 1.3.

	Inverter A	Inverter B	Inverter C
Nominal output power	2.6kW	2.5kW	3.6kW
MPPT voltage range	230–500V	175–570V	200–530V
Inverter topology	HF inverter	HF inverter	TL inverter
Centre frequency (f_c)	20kHz	16kHz	25kHz

Figure 1.3: Technical specifications of the selected PV inverters

The article highlights that we can clearly identify two behaviours, The inverter is either a high frequency voltage sources (Thevenin's equivalent circuit) or current source (Norton's equivalent circuit). To find the source type, a V_{hf} versus I_{hf} graph is plotted for various grid impedances.



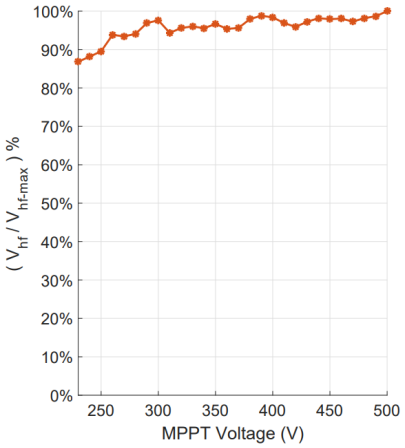
(a) Inverter A (b) Inverter B (c) Inverter C

Figure 1.4: Characteristic curves of the selected PV inverters at reference operating conditions under varying Z_grid values

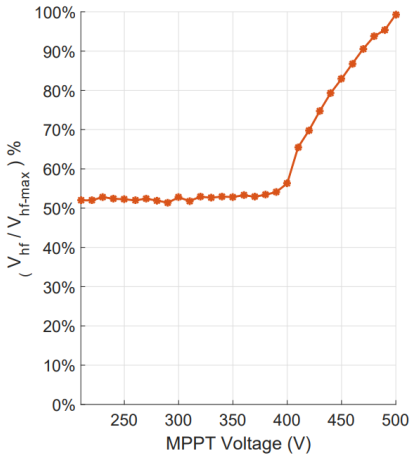
The phd thesis [7] goes deeper in the comparison by looking at the link between the topologies, the harmonic voltages, the output power and the

MPPT voltage.

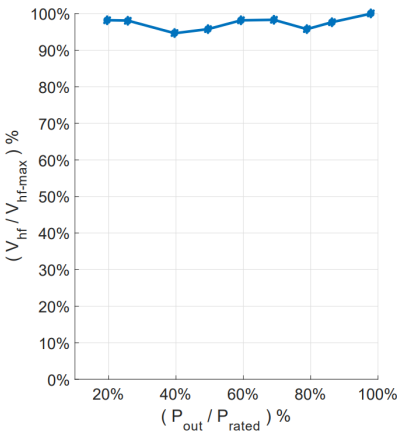
A clear relation is shown between MPPT voltage, hf emission and transformer topology on Figure 1.5. For transformer inverters the curve is flat (Figure 1.5a), the supraharmonic emission is constant meaning it shows no dependence with MPPT voltage. For transformer-less inverters we can clearly see a dependence (Figure 1.5b). When the MPPT voltage reaches 400V, the hf emission starts to increase with it.



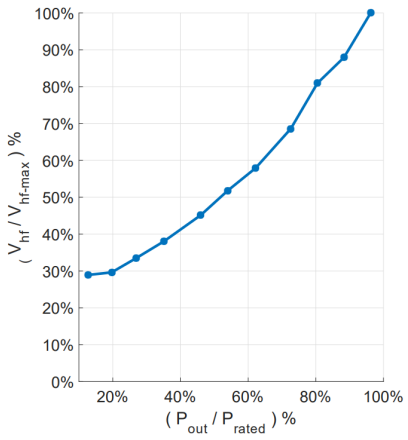
(a) Transformer inverter



(b) Transformer-less inverter



(c) type A behaviour



(d) Type B behaviour

Figure 1.5: hf emissions from PV inverters

Concerning the variation of hf emission in function of the output power

of the inverter no clear correlation with the inverter type is observed but the inverter can still be dissociated in two types. Type A, the inverters hf emission shows no dependence with the power output as we can see on Figure 1.5c. Type B, the hf emission is proportional to the output as we can see on Figure 1.5d.

This result is interesting because, as a first intuition we could think that the hf emission are always correlated with the output power but it is not. The fact we cannot observe clear correlation with transformer topology is also noteworthy because it suggests that the different controls might be the reason of type A and B distinction.

In [9], an analysis is made on three PV inverters. For one of the inverters tested, detailed results are presented. A similar behaviour as Figure 1.5b is observed concerning the hf emission in function of the MPPT voltage but no precision is given on the use of transformer or transformer-less inverter. The article summarises the results for the three inverters in a more qualitative analysis, represented on Figure 1.6.

Factor	PVI A	PVI B	PVI C
$\lvert\underline{U}^{(1)}_{\mathrm{POC}}\rvert$	-	--	+
U_{DC}	++	--	++
$\underline{U}^{(h)}_{\mathrm{POC}}$	-	-	--
P_{POC}	+	++	++
f_{N}	--	--	

(a) Qualitative analysis

Impact	none	low	medium	high
Maximum changes	<1%	1%…10%	10%...50%	>50%
	--	-	+	++

(b) Categorization symbols - Percent of maximum changes in suprahamonic emission

Figure 1.6: Qualitative analysis of influencing factors of supraharmonic emission of different PVIs

with

- $|U^{(1)}_{POC}|$ the AC fundamental voltage amplitude.

- U_{DC} the MPPT voltage.

- $|U_{POC}^{(h)}|$ the amplitude of the harmonic of order h added to the fundamental voltage to measure the impact of wave distortion.

- P_{POC} Output power

- f_N Frequency of the fundamental voltage of the inverter (set between 48Hz and 51.5Hz)

The analysis of Figure 1.6 shows that the impact of the influencing factors changes within different manufacturers. According to [9] this is mainly due to the control strategies resulting in different switching patterns for the inverter bridge.

To conclude we can say that inverter supraharmonic rejection varies from one device to another but there is still a clear distinction between transformer and transformer-less inverters. The control strategy seems to be the other reason of the variety of behaviours regarding hf emissions.

1.1.2 EV chargers

The number of electric vehicles (EVs) has been increasing for the past few years (Figure 1.7) and will keep on increasing for at least the next decade. In Fact the European Parliament approved on 14 February 2023 the new CO2 emission reduction targets for new passenger cars and light commercial vehicles, part of the "Fit for 55" package. It means that by 2035 every new car will no longer be allowed to emit CO2 [10].

In this context more and more people are installing small EV chargers to charge their car at home. In this section we will focus on those small AC EV chargers, those use the on-board AC-DC converter. We will not discuss high power DC charging stations.

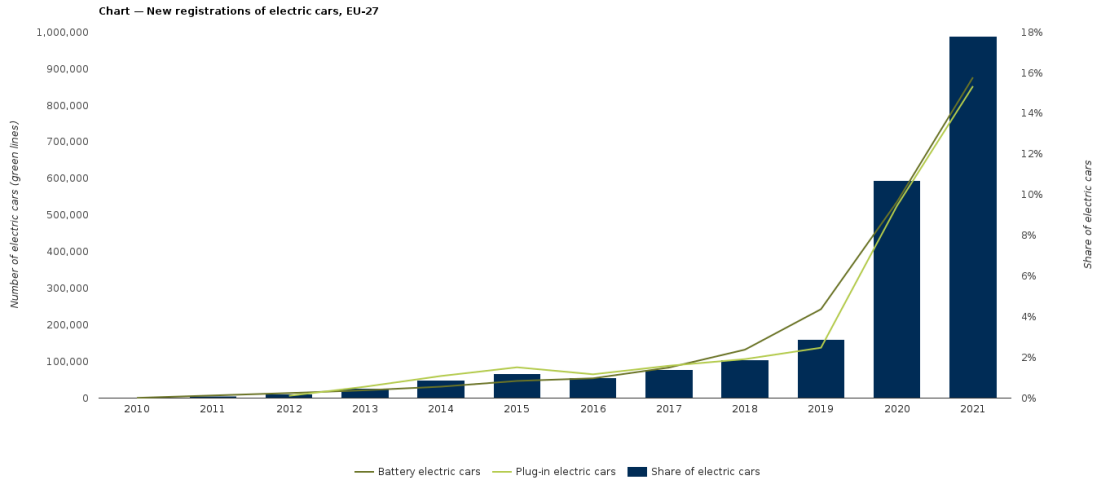


Figure 1.7: New registrations of electric cars, EU-27 [11]

In [12] a study of the propagation of supraharmonic currents of four EV chargers in a normal grid and in a microgrid is proposed. The experiment shows that the supraharmonic emissions mostly stay within the local installation due to the absorption of nearby devices.

This article also highlights the phenomenon of frequency beating as we can see on Figure 1.8. Beating appears when two sin waves with a slight frequency difference are added. This results in the multiplication of a sin wave whose frequency is half of the frequency difference of the two waves by a sin wave whose frequency is the mean of the two (see eq 1.1).

$$sin(a) + sin(b) = sin(\frac{a+b}{2})sin(\frac{a-b}{2}) \tag{1.1}$$

It is clear that when frequencies are close, the second therm of equation 1.1 ($sin(\frac{a-b}{2})$ has a much lower frequency and this will create a sort of amplitude modulation, known as beating.

This beating emphasises the fact that in presence of multiple EV chargers we cannot simply add their respective supraharmonic emissions.

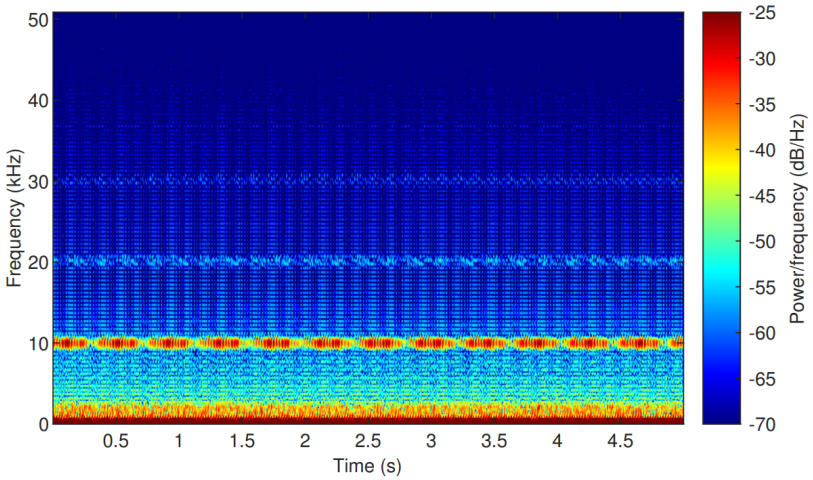


Figure 1.8: Time–frequency analysis of the measured beating effect around 10 kHz [12]

1.1.3 LED lamps

The LED lights are everywhere in our daily life, from public street lamps to household lightning. The LED has rapidly replaced the other classical lamps (fluorescent, filament,..). According to [13], "The global LED use has increased substantially in recent years, rising from a market share of 5% in 2013 to nearly half of global lighting sales in 2019". This is represented on Figure 1.9 and the market penetration will keep rising. In fact, the International Energy Agency (IEA) is targeting a switch of the lightning market to 100% LED by 2025 [14]

But every LED lamp needs a driving circuit and those converters can interact with supraharmonics. Household appliances malfunctions, notably LED lamps have been documented both in the United States and Europe, particularly when they are linked to photovoltaic inverters and other power electronic devices [15]. In [16], 24 LED lamps are tested and variations of light intensity is observed because of interaction with supraharmonics. According to [17] the effect of hf distortion on the flicker of LED lamps is clear. It can increase up to 10 times due to hf voltage distortion and can even become observable and potentially problematic for human beings.

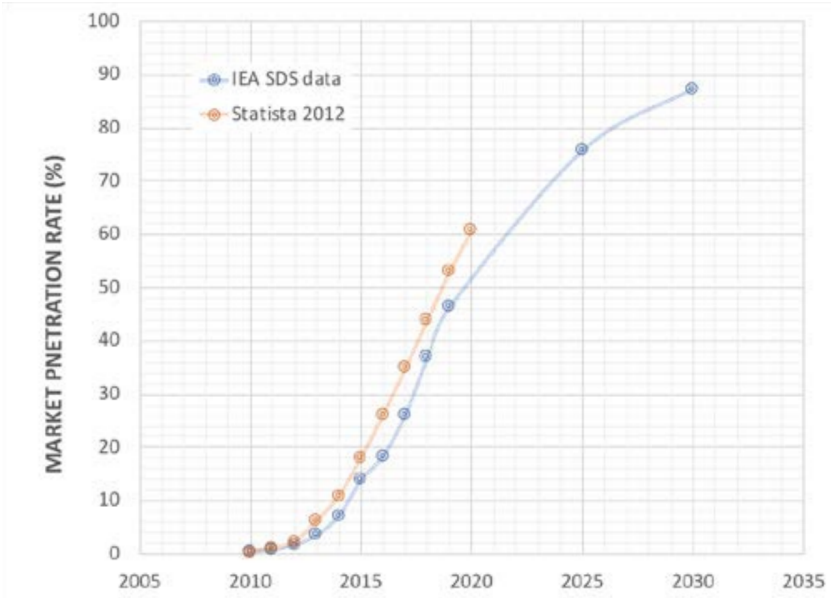


Figure 1.9: LED penetration rate projected by Statista (data from [IEA-19] and [STA-12]).[13]

1.2 Supraharmonics standards

Standards related to 2-150kHz unintentional emission are still being discussed. The range 0-2kHz is well documented in IEC 61000-4-7. Concerning the upper bound, beyond 150kHz, CISPR 16-2-1 documents radio disturbances up to 30Mhz. Actually, there are three standards overlapping for the frequency range we are interested in.

1.2.1 CISPR 16-2-1

This standard explains the measurement method of disturbance phenomena in general in the frequency range 9 kHz to 18 Ghz and especially of disturbances conducted along leads in the range 9kHz to 30MHz.

It provides guidelines and procedures for testing the susceptibility of electronic equipment to conducted disturbances and for measuring the emissions of such disturbances from the equipment itself. It aims to ensure that electronic devices can function properly in the presence of various radio frequency disturbances, and also that they do not emit excessive interference that could

affect other nearby devices.

CISPR standards are essential for maintaining electromagnetic compatibility (EMC) in electronic devices, ensuring that they can operate reliably in the presence of electromagnetic interference and do not cause undue interference to other devices.

CISPR 16 focuses on emissions from equipment under test (EUT), it does not directly address power quality investigation. According to [18] who analyses the suitability of the CISPR 16 method for measuring conducted emissions in the 2–150kHz range in low voltage grids, the method presented in this standard has important limitations in terms of accuracy requirements and reproducibility.

1.2.2 IEC 61000-4-7

Part 4-7 provide a general guide on harmonics and interharmonics measurements. It gives the measurements standards for assessing harmonics up to the 40th, so up to 2kHz for a 50Hz grid.

Compliance with IEC 61000-4-7 helps in assessing the harmonic performance of devices, ensuring that they meet acceptable levels of electromagnetic compatibility and do not cause disruptions or damage to the power supply system or other connected equipment. The standard contributes to the overall goal of creating a harmonious and interference-free environment for electrical and electronic devices.

Annex B of the standard is the point of interest here. In fact it fills the gap between 2kHz of IEC and the 9kHz of CISPR. The idea is to modify the discrete Fourier transform already used for harmonics up to 2kHz. The same 200ms rectangular data acquisition window is used, giving a 5 Hz frequency resolution. But the raw DFT is then grouped in bands of 200Hz.

$$Y_{B,b} = \sqrt{\sum_{f=b-95Hz}^{b+100Hz} Y_{C,f}^2} \tag{1.2}$$

The centre frequency is b, starts at 2.1kHz and ends at 8.9kHz. The grouping is graphically represented on Figure 1.10.

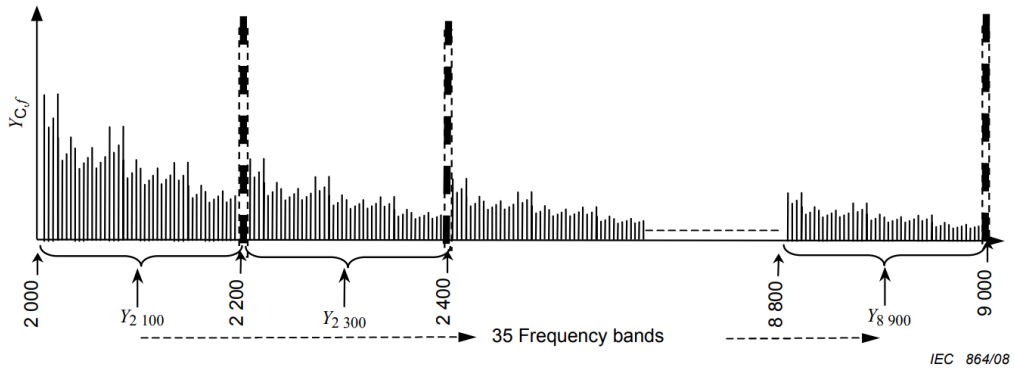


Figure 1.10: frequency bands for measurement in the range above the 40th harmonic order for 50 Hz power system up to 9 kHz [19]

1.2.3 IEC 61000-4-30

IEC 61000-4-30 provides guidelines and methods for testing and measuring power quality in electrical systems.The standard specifies measurement methods to measure various parameters related to power quality, including voltage fluctuations, flicker, harmonic content, and interharmonics. Compliance with IEC 61000-4-30 is crucial to assess the performance of electrical systems and ensuring that they meet acceptable standards for power quality.

Annex C of the standard discuss methods for assessing disturbance from 9kHz to 150kHz. It suggests extending the method proposed in IEC 61000-4-7 Annex B up to 150kHz. Therefore, the method used in this master thesis is the 200Hz grouping from 2kHz to 150kHz.

Chapter 2

Experimental setup

The experiment consists of studying the behaviour of an Active Power Factor Corrector (APFC). The goal is to measure the supraharmonic emission in various scenarios. The APFC used is part of a programmable Texas Instrument kit.

In this chapter we go through the different parts of the experimental setup. A focus is made on the Interleaved Boost Converter (IBC) which is the converter used for power factor correction. Figure 2.1 represents a simplified schematic of the test bench. The parts framed in colour are described in the sections of this chapter.

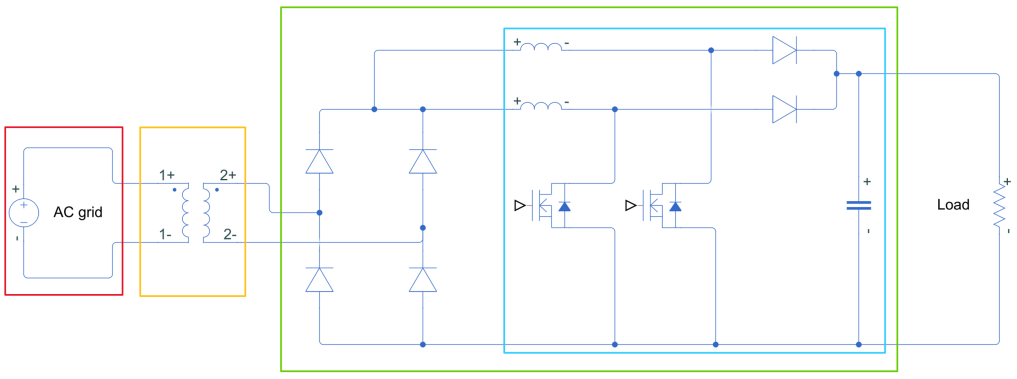


Figure 2.1: Simplified circuit representation of the experimental setup

2.1 Grid

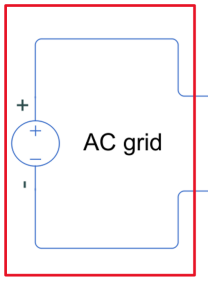


Figure 2.2: Grid - Simplified circuit representation

The device under test is connected to the grid through a transformer but the grid is not a perfect source as represented on Figure 2.2. No LISN (Line Impedance Stabilization Network) is used, A LISN would allow to have a known and precise impedance at the power input of the equipment under test (EUT). Therefore we need to measure the grid impedance. We used two methods:

Voltage drop with a load

The idea here is quite simple, we deduce the grid impedance by measuring the voltage drop when a 20A load is connected, this is represented on Figure 2.3. By measuring the difference in voltage between the case with and without the load, we can deduce the value of the grid impedance. For this first approximation we will neglect the inductive part, in fact we are connected to the low voltage grid and the inductive part of the impedance is expected to be much smaller than the resistive one.

$$R_g = \frac{V_{grid} - V_{load}}{I_{load}} = \frac{8.48}{20.70} = 0.41\Omega \tag{2.1}$$

This method allows us to have a first idea of the grid impedance. It is, of course, not precise enough and we will confirm our measurement with a grid impedance meter.

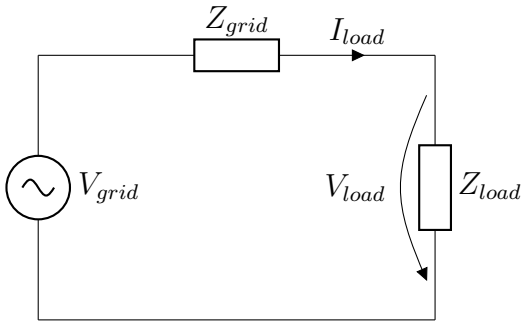


Figure 2.3: Grid impedance measurement

Grid impedance meter

We used the Solar 200 and the IMP57 from HT-instrument to measure the grid impedance, doing so we find:

$$Z = 456m\Omega$$

$$X = 27.4m\Omega$$

$$R = 455m\Omega$$

Detailed explanations on this impedance meter and the connection are given in section 3.4.3.

2.2 Auto transformer

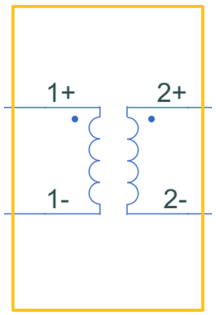


Figure 2.4: Transformer - Simplified circuit representation

As for the grid, we need to determine the impedance of the transformer. We cannot just consider an ideal transformer as represented on Figure 2.4 because the impedance of the transformer has an impact on supraharmonic emission. A better representation is the equivalent circuit of a single phase transformer on Figure 2.5.

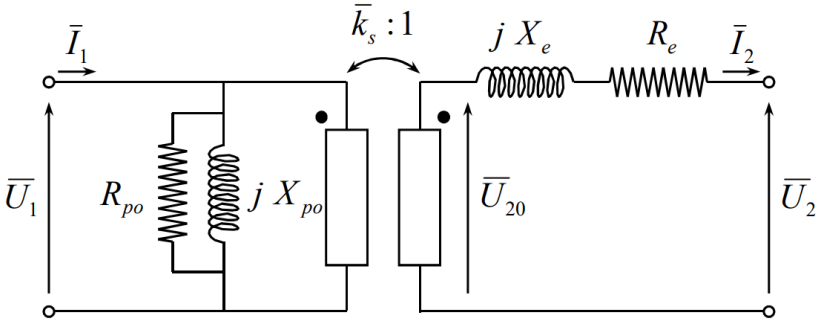


Figure 2.5: Simplified equivalent circuit of a single phase transformer [20]

To find the equivalent circuit elements of the transformer, we conduct the classical short circuit and open circuit tests.

Open circuit test

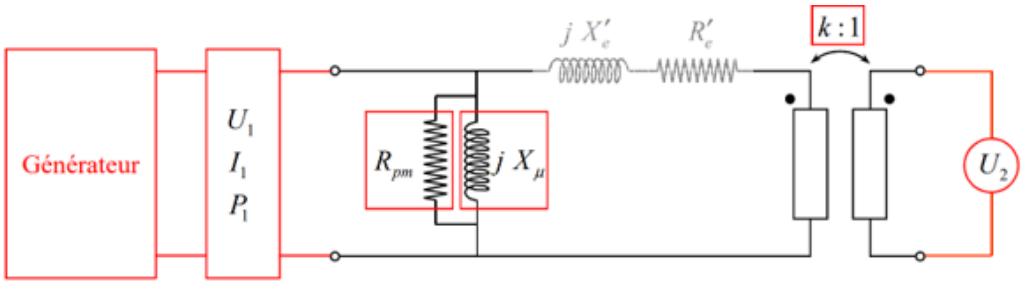


Figure 2.6: Open circuit test configuration [20]

The open circuit test allows us to find the parallel element of the equivalent circuit. The primary winding is connected to the grid and the secondary stays open. By measuring the input power (P_1), the input current (I_1), the primary voltage (U_1) and the secondary voltage (U_2) we can deduce the parallel elements.

- $U_1 = 228.8\text{V}$
- $U_2 = 35.0\text{V}$
- $P_1 = 10.6W$
- $cos(\phi) = 0.69$
- $I_1 = 0.067A$

$$Z_\mu = \frac{|\overline{U_2}|}{|\overline{I_1}|}$$

$$X_\mu = \frac{Z_\mu}{sin\phi} = 4715\Omega$$

$$R_{pm} = \frac{Z_\mu}{cos\phi} = 4949\Omega$$

Short circuit test

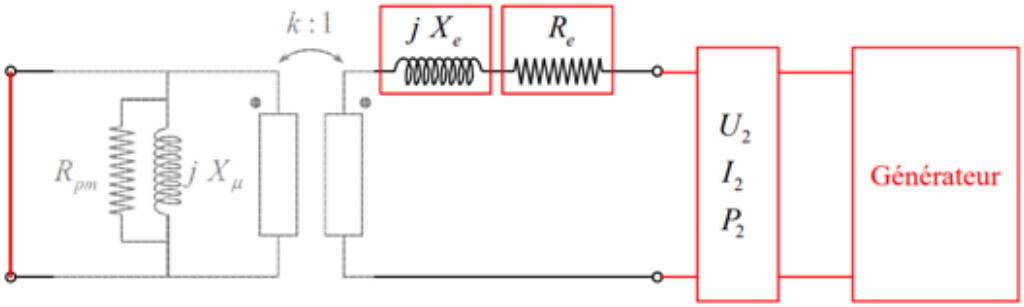


Figure 2.7: Short circuit test configuration [20]

The short circuit allows to find the series elements. The primary is shorted while the voltage is increased at the secondary until it reaches a current close to the nominal current.

- $U_2 = 2.62V$
- $I_2 = 4.3A$

- $\phi = 25.86°$

$$\overline{Z_e} = \frac{\overline{U_2}}{\overline{I_2}}$$
$$X_e = 0.266\Omega$$
$$R_e = 0.548\Omega$$

2.3 Texas instruments kit

Figure 2.8: TMDSHVMTRPFCKIT

The High Voltage Digital Motor Control (DMC) and Power Factor Correction (PFC) kit (TMDSHVMTRPFCKIT) is the masterpiece of the experimental setup. It is equipped with a C2000 micro controller unit (MCU) that allows to program the PFC and the inverter, this is explained more in detail in section 2.3.1.

This kit is typically used to control 3-phase motors as represented on the diagram 2.9. But in our case we do not use it to control a motor, we are just interested in the APFC stage. Therefore we disconnect the Inverter stage and put a load directly at the APFC output as represented on 2.10. This load is a variable resistor that will dissipate energy in the form of heat.

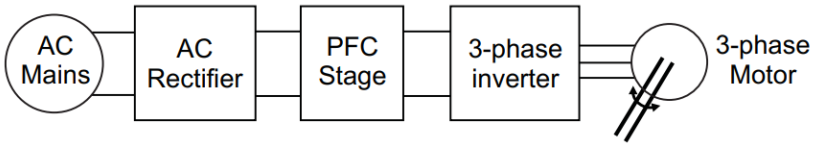


Figure 2.9: Block diagram for a typical motor drive system using power factor correction

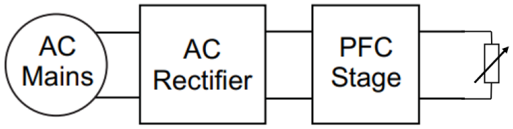


Figure 2.10: Block diagram for our use of the TI kit

One of the most time-consuming parts of this master thesis was programming this kit with Simulink and make it work as wanted. In fact, it is easy to find documentation on how to control the transistors of the inverters stage and what parameters need to be used in Simulink. But the Simulink parameters to control the PFC stage are much less described in the documentation available. Therefore I explained it in Appendix B.

The kit has multiple features:

- A 3-phase inverter Stage
- Power Factor Correction
- AC Rectifier
- Aux Power Supply Module

- Isolated CAN interface, Onboard Isolated JTAG emulation, Isolated UART
- Four PWM DACs generated by low pass filtering the PWM signals to observe the system variables on an oscilloscope to enable easy debug of control algorithms.
- Over-current protection for PFC stage (both phases) and the inverter stage, PWM trip zone protection for IPM faults

Figure 2.11 shows the main blocks of the TI kit. We will take a closer look at those blocks.

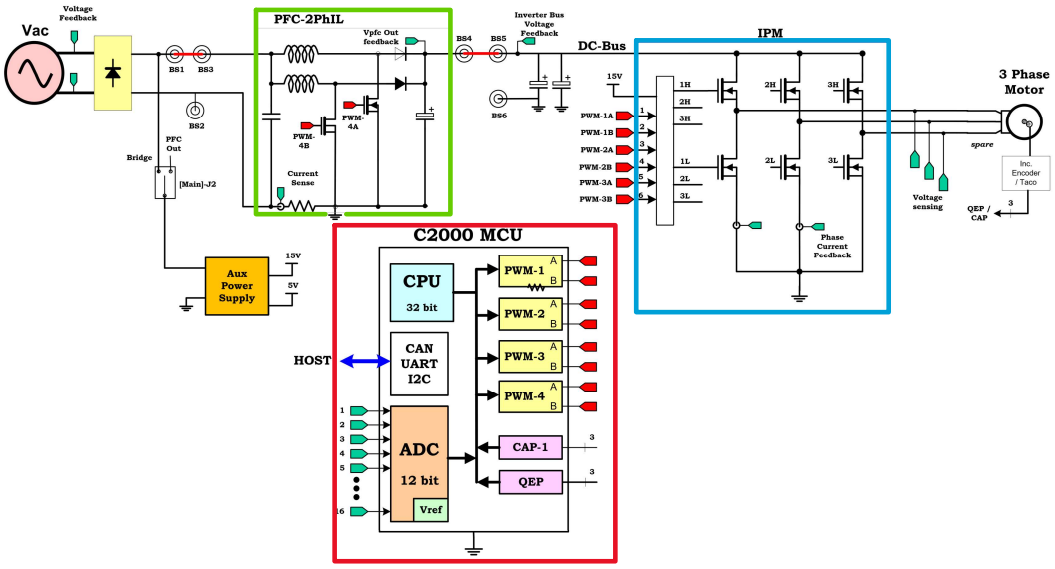


Figure 2.11: Block diagram for our use of the TI kit

2.3.1 C2000 MCU

C2000™ real-time microcontrollers are optimized for processing, sensing, and actuation to improve closed-loop performance in real-time control applica-

tions such as industrial motor drives; solar inverters and digital power; electrical vehicles and transportation; motor control; and sensing and signal processing. [21]

In our TI kit we use the TMS320F28335 microcontroller. This C2000 MCU offers a 16 channels 12-bit analog-to-digital converter (ADC) with a 12.5 mega samples per second sampling rate and has a 150-Mhz CPU. It has 12 PWM outputs used to control the PFC and the Inverter. The ADC and PWM ports are selected by specific Simulink blocks.

2.3.2 Two phase PFC stage

More information on working principle of PFC's is given in 2.4, here we will focus and the specification of the PFC stage.

Table 2.1: PFC stage specifications

Two phase interleaved topology, capable of phase shedding
85-132VAC/ 170-250VAC rectified input
400V DC Max output voltage
750W* max power rating
Up to 96% efficiency
200Khz switching frequency for the power stage
Up to 100Khz PFC control loop frequency
Uses Texas Instruments UCC27324, high speed dual MOSFET drivers

2.3.3 3-Phase Inverter Stage

This inverter stage can be used to control high voltage motors. We will not go into a detailed explanation of this part of the kit because this stage is disconnected and not used is this master thesis. As explained before, we focus the experiment on the PFC stage.

2.4 Active Power Factor Corrector

In this section we make first an introduction with the definition and working principles of a Power Factor Corrector. After that we look closer to the interleaved boost converter used as APFC of the TI kit and its control.

Many applications, including power converters, often uses diode rectifiers alongside DC capacitors. This configuration results in a low power factor. The introduction of a Power Factor Corrector (PFC) offers a solution to meet regulatory requirements and to bring the power factor closer to 1 [22]. The distribution network's efficiency is compromised by the presence of reactive power and distortion power, which generate additional RMS currents. These additional losses lead to an oversizing of the cross-sectional area of the copper power wires used for distribution. Both user and electricity company take advantage from unity factor [23].

The power factor is the ratio between the active power (P) and the apparent power (S)

$$powerfactor = \frac{P}{S} \tag{2.2}$$

This equation is easy to use when we are working with linear loads and the waveforms are still sinusoidal.

$$P = VIcos(\phi) \tag{2.3}$$

$$S = VI \tag{2.4}$$

In this case we can use equations 2.3 and 2.4. The power factor becomes just the displacement factor: $cos(\phi)$ with ϕ the phase angle between the voltage and the current.

But when loads are nonlinear, the voltage and especially the current can have other weveforms than a sine wave. In this case the equations 2.3 and 2.4 are not valid. The power factor is expressed in function of the displacement factor and the harmonic content. The complete expression of the power factor is,

$$pf_{true} = \frac{P_{avg}}{V_{1,rms}I_{1,rms}} \frac{1}{\sqrt{1+(THD_V/100)^2}\sqrt{1+(THD_I/100)^2}} \tag{2.5}$$

This equation can be simplified using two assumptions:

- Contributions of harmonics above the fundamental to average power is small: $P_{avg} \approx P_{1,avg}$
- THD_V is usually less than 10%, $V_{rms} \approx V_{1,rms}$

Equation 2.5 finally becomes,

$$pf_{true} = \frac{P_{1,avg}}{V_{1,rms} I_{1,rms}} \frac{1}{\sqrt{1 + (THD_I/100)^2}} \tag{2.6}$$

With the first part of the equation being the displacement factor ($cos\phi$) and the second one being the harmonic distortion factor. Complete mathematical development is given in [24]. The main contributors to a poor power factor are the phase displacement angle and harmonic distortion [23] [22]. There are two methods for power correction, active and passive.

Passive power factor correction: Capacitor and inductor can be used to mitigate the impact of the bridge rectifier on the power factor. Adding an inductor at the AC side is the simplest approach but an effective way is to add tuned harmonic filters at the AC side the reduce the main harmonic components and thereby reducing the power factor. One alternative method consists in putting an inductor on the DC side of the bridge. This inductor serves to increase the conduction angles of the diodes, consequently lowering the peak current drawn from the power source [23]. Figure 2.12 shows those types of passive filters.

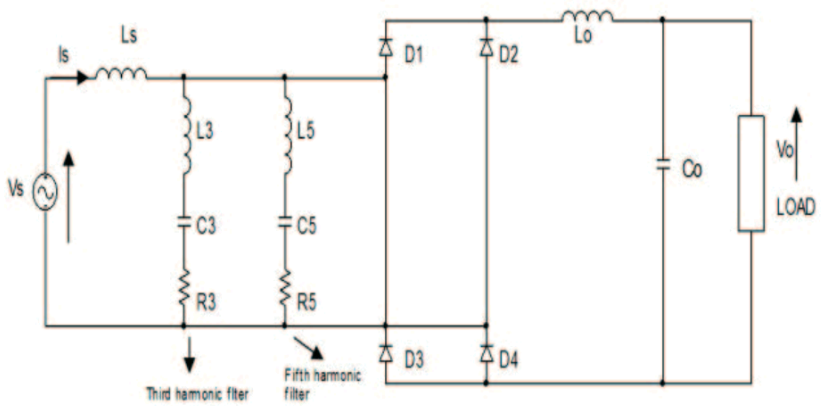


Figure 2.12: Full bridge rectifier with passive filters [23].

Active power factor correction: Active power factor correction uses an electronic converter after the rectifier bridge. This converter has three tasks, maintaining a defined voltage at the DC side, correct the current distortion by controlling its sinusoidal waveform and keeping the current in phase with the voltage. The main converter topologies used for active power factor correction are boost, buck, buck-boost and fly-back converters. In the Texas Instrument kit an Interleaved Boost Converter (IBC) is used, therefore we will look closer at this converter topology.

2.4.1 Interleaved boost converter

As said in Section 2.3.2, the kit is equipped with an interleaved boost PFC. So let us look deeper into this topology. Boost power factor converter topologies as represented on Figure 2.13 are mainly used because of their simplicity, performance and efficiency. Other PFC topologies like buck and buck-boost have also more electromagnetic interference (EMI) [25].

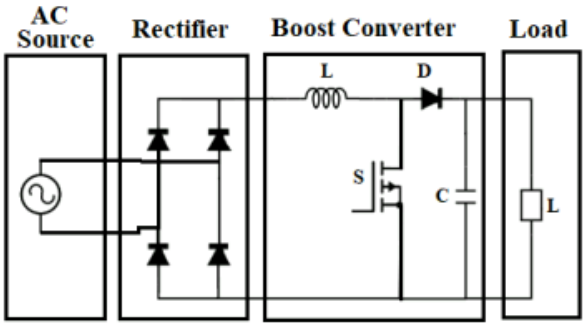


Figure 2.13: Diagram of active PFC with boost converter [22].

The interleaved topology is mostly used for high power applications. In fact this topology permits to reduce the size of the component. The inductor size is reduced by four compared to classical boost topology, the transistor current is reduced by two and the input current ripple is also reduced [26].

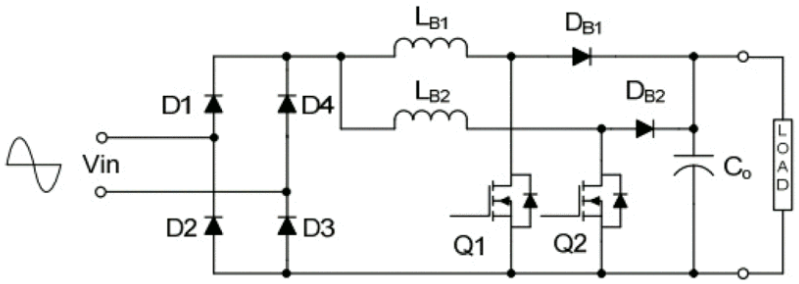


Figure 2.14: Interleaved boost PFC topology [25].

In this topology the two transistors are connected in parallel as represented on Figure 2.14. Their PWM signals have a 180°phase shift resulting in a switching frequency two times bigger than the PWM frequency. In our case the switching frequency is 50kHz so the PWM one is 25kHz. We can observe the two PWM signals on figure 2.15. The phase shift is $20\mu s$ which corresponds to a half period at a frequency of 25kHz. We can also see that the PWM period is $40\mu s$ which corresponds well to the 25kHz frequency.

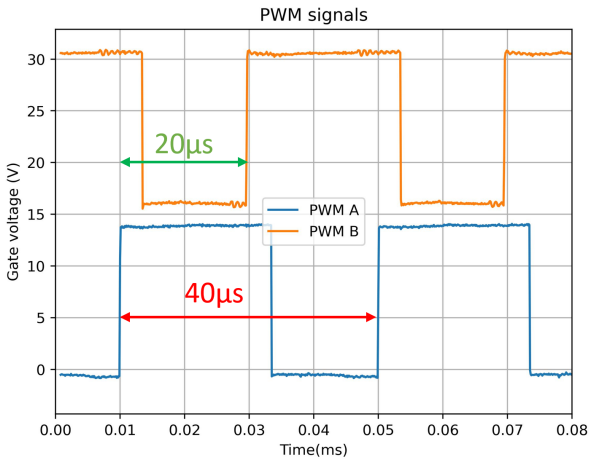


Figure 2.15: PWM signals of the IBC. An offset is applied to PWM B for better readability.

2.4.2 Control strategy of the IBC

The used control has been provided by Erzen Muharemi who is doing a PHD thesis at the UCLouvain on supraharmonics. The measurements in this mas-

ter thesis are closely related to Erzen's work. He has shown the influence of the control structure on the behaviour of the IBC as a supraharmonic current or voltage source. His results are theoretical and proven by simulation. The goal here is to emphasise (or not) those results by measurements on the TI kit.

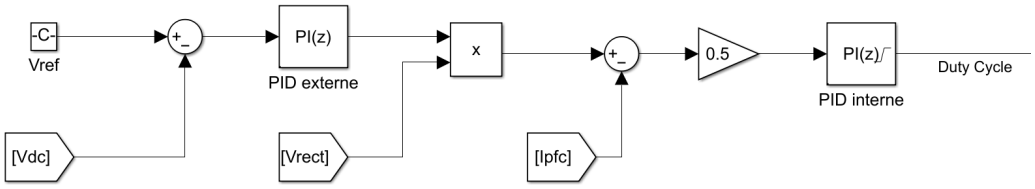


Figure 2.16: Control loop of the IBC

The control structure used is represented on Figure 2.16 with,

- V_{dc}: the output voltage of the PFC stage.
- V_{rect}: the rectifier voltage. In practice we take the AC input voltage and rectify it with an absolute value block in Simulink. In fact as we can see on Figure 2.11 we do not have access to the rectifier voltage with the ADC but only to the AC voltage
- I_{pfc}: the current passing through the PFC stage.

The determination of the transfer functions was carried out through Sate Space Averaging (SSA) and Small-Signal Linearization (SSL) by Erzen and is detailed is his paper [27]. The parameter of the PIs are given in table 2.2.

External loop gain (P_e)	$3.5e^{-4}$
External loop intergral factor(I_e) (	0.01
Internal loop gain (P_i)	0.35
Internal loop intergral factor(I_i)	1

Table 2.2: Parameter of the control given by [27].

Chapter 3

Measurement method

This chapter resumes all the practical aspects of the measurements. From the electrical component used and measurement equipment to the computation of the Fourier transform and the digital filters applied to the measurement data.

3.1 Set Point

In this section we explain the operating point and detail the operating voltage, current, measurement points, resistance and impedance values as well as control parameters.

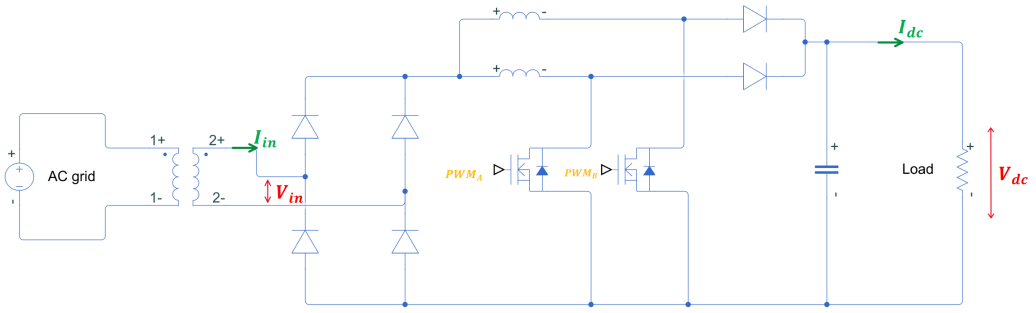


Figure 3.1: Simplified circuit representation of the experimental setup - measurement points

Figure 3.1 shows the global setup with the measurement points in colour. V_{in} and I_{in} are the input voltage and current of the TI kit. Those are the

points where the supraharmonic content is measured. PWM_A and PWM_B are measured at the gate voltage of the transistor of the Interleaved Boost Converter. V_{dc} and I_{dc} are the voltage and current at the dc link, so at the output of the APFC and at the load terminals. The load is a variable resistor able to dissipate the generated heat without reaching more than 80°C.

Here are the value of the components, voltage, current and control parameters.

V_{dc}	250	V
I_{dc}	0.75	A
V_{in}	70	Vrms
I_{in}	2.5	Arms
R_{dc}	710	Ω
P_i	0.1	
P_e	$3.5e^{-4}$	
I_i	1	
I_e	0.01	

Inductors are used in Section 4.2.2 to modify the grid impedance seen by the TI kit. Two different inductors ($L_{s,1}$ and $L_{s,10}$) are used to produce 4 values in function of their parallel or serie connection.

Inductance value	0.5mH	1mH	2mH	5mH
Inductor used	2*$L_{s,1}$ in //	1*$L_{s,1}$	2*$L_{s,10}$ in serie	2*$L_{s,10}$ in //

The values of the resistive and inductive part measured with an LCR meter are given in Table 3.1.

	L[mH]	R[Ω]
$L_{s,1}$	1.15	0.64
$L_{s,10}$	10.36	7.37

Table 3.1: L and R of the used inductors measured at 1kHz

3.2 Discrete Fourier Transform

The Fourier Transform is the first mathematical tool we think of for spectral content analysis. We are dealing with sampled signals, therefore we need

to use the Discrete Fourier Transform (DFT). The DFT transforms a finite sequence of points in the time domain (a discrete signal) into a finite sequence of points in the frequency domain. It is a sampled version of the Discrete Time Fourier Transform (DTFT).

The DFT of a sequence $x(n)$ with $0 \leq n \leq N-1$, is defined by:

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j\frac{2\pi}{N}kn} \tag{3.1}$$

Where:

- $X(k)$ is the kth component of the DFT, a complex number representing the amplitude and phase of the corresponding frequency component.
- $x(n)$ is the nth sample of the input sequence (time domain).
- N is the number of samples.

To compute the DFT, we use the Fast Fourier Transform (FFT). This algorithm is widely used and allows for faster computation than the classical DFT formula. The complexity goes from N^2 down to $Nlog_2N$.

For the measurement, a time window of 200ms is chosen in accordance with the recommendations in IEC 61000-4-7 and IEC 61000-4-30.

3.2.1 Spectral leakage

Applying the DFT can have unwanted effects like spectral leakage. To measure a signal with the oscilloscope, we need to define a finite time window on which we make the acquisition. Spectral leakage is more likely to occur when the signal being analysed is not exactly periodic within the given observation window.

The leakage manifests as energy spreading. Instead of seeing sharp peaks in the frequency domain representing the true frequencies of the signal, we might observe smeared or spread-out peaks. In this case it is challenging to precisely identify the true frequency components of the signal. Figure 3.2 shows an example of spectral leakage. We can clearly see that for N=128 there is spectral leakage. In fact, for 128 sample, the window does not take an integer number of cycles (20 samples per cycle so 128 samples correspond to 6.4 cycles), the signal in the window is no more periodic leading to spectral leakage.

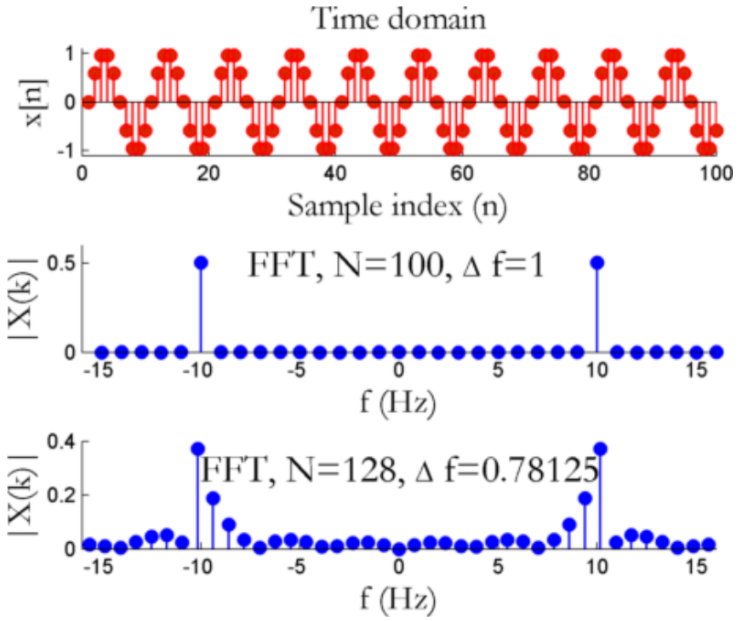


Figure 3.2: Spectral leakage example

Spectral leakage can be mitigated using specific window function like Hann window or Hamming window. Nevertheless IEC 61000-4-7 recommend the use of rectangular window so we use a rectangular window in our measurements. This window does not contribute to spectral leakage mitigation. However, we can mitigate leakage with other methods.

The thesis [7] recommend the use of a digital high-pass (HP) filter with a passband at 2kHz. This filter eliminates the 50Hz main frequency and with it its temporal variation which is the main cause of non periodicity leading to spectral leakage. The filter proposed is a digital, offline, Infinite Impulse Response (IRR), zero-phase HP filter. First we design an elliptic filter with:

- 1MHz sampling rate
- 60dB stopband attenuation
- 0.005dB passband ripple
- 1.7kHz stopband frequency
- 2kHz passband frequency

The resulting filter is of order 10 and is represented on Figure 3.3.

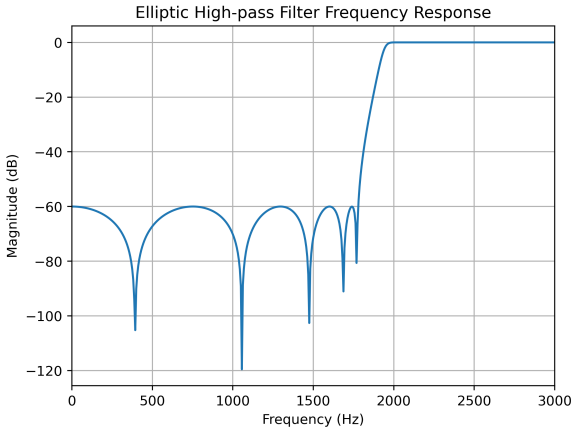


Figure 3.3

After the filter has been built, we apply the digital filter on the acquired data twice, once forward and once backward. The combined filter has zero phase and a filter order twice that of the original. This is achieved using the "filtfilt" function of SciPy in Python.

3.2.2 Aliasing

Aliasing is a phenomenon that occurs when a signal is sampled at a too low sampling rate compared to its frequency. The signal will overlap in the frequency domain causing distortion and loss of information.

Nyquist-Shannon theorem states that if a signal has no frequency components above half of the sampling rate, then the original signal can be perfectly reconstructed from its discrete samples. Therefore we can say that aliasing occurs only if the sampling frequency is smaller than twices the maximum frequency of the signal, this is also represented on Figure 3.4. So to avoid it, we just need to respect:

$$f_s \geq 2f_{max} \tag{3.2}$$

In our case we want to measure frequency up to 150kHz and we have a sampling frequency of 1MHz. So the Nyquist frequency is 500kHz, meaning we can measure frequency up to 500kHz without distortion due to aliasing.

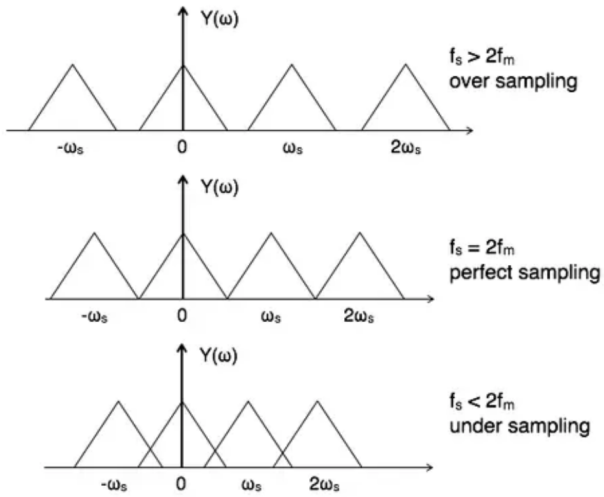


Figure 3.4: Effect of aliasing

But the frequency above will cause aliasing and this frequency overlapping could impact the lower frequency measurements. Therefore we still need an antialiasing filter, this filter is simple and is just a low-pass filter that will cut the frequencies above the Nyquist frequency.

The frequency response of classical Butterworth filter is given by:

$$G_n(\omega) = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_c}\right)^{2n}}} \tag{3.3}$$

with ω_c the cut-off frequency and n the filter order.

The Butterworth filter exhibits a gradual roll-off beyond its cutoff frequency, providing a good attenuation of higher frequencies while maintaining a relatively flat response in the passband. The roll-off rate increases with the filter order (n) and is equal to $20 * n$ dB/decade.

Here we used a 4th order filter with a cut-off frequency of 300kHz. The frequency response of the filter is represented on Figure 3.5.

3.2.3 Grouping in 200Hz bands (IEC 61000-4-7)

The 200Hz frequency grouping is already explained in 1.2.2. We used this grouping for all measurements in the frequency range 2kHz to 150kHz.

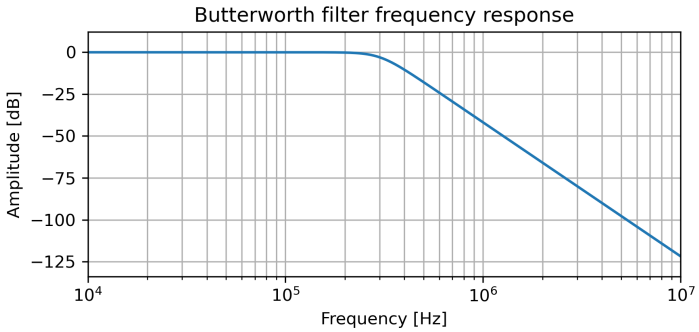


Figure 3.5

3.3 Total Harmonic Distortion

Total Harmonic Distortion (THD) is a measurement that quantifies the level of harmonic distortion present in a signal compared to its fundamental frequency. It assesses how much the harmonics (integer multiples of the fundamental frequency) contribute to the overall signal distortion.

The THD of some measurements is given in Chap 4. Here we will introduce how the computation of the THD is done. IEC 61000-4-7 define the THD as the ratio of the r.m.s. value of the sum of all the harmonic components ($Y_{H,h}$) up to a specified order (h_{max}) to the r.m.s. value of the fundamental component ($Y_{H,1}$):

$$THD_Y = \sqrt{\sum_{h=2}^{h_{max}} \left(\frac{Y_{H,h}}{Y_{H,1}}\right)^2} \tag{3.4}$$

The value of h_{max} is 40 if no other value is defined in a standard concerned with limits (IEC 61000-3 series) and the symbol Y is replaced, as required, by the symbol I for currents or by the symbol U for voltages [19].

3.4 Measurement devices

3.4.1 Oscilloscope

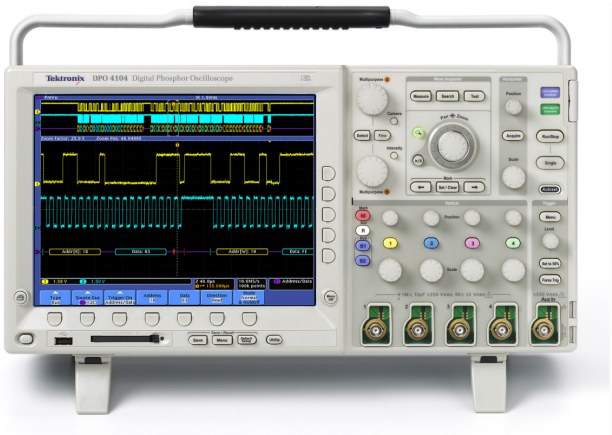


Figure 3.6: DPO4054 oscilloscope from Tektronix

The oscilloscope used for voltage and current measurements is the DPO4054 from Tektronix. The main feature we are interested in here are:

- Up to 2.5GS/s sample rate
- 10MSamples record length
- vertical resolution of 8bits (11 bits in Hi Res mode)
- Max input voltage of 250Vrms

When using Hi Res mode, the record length drops down to 1MSample. For a 200ms acquisition window, it gives us a 5MS/s sampling rate. [7] recommends a 1MHz sampling rates so 5MS/s is more than enough. The biggest limitation here is the vertical resolution of only 11 bits. In fact [28] gives as general guideline the use of a 16 bits analog-to-digital converter when supraharmonics measurements are done using digital filtering. If 12 bits ADC are used, the paper recommends the use of analogue filtering.

But despite those recommendations, we still use digital filters in this master thesis and not analogue. In fact in our case the supraharmonic content has a high amplitude because the measurement point is at the input of the

TI kit so at the secondary of the transformer. Due to its impedance, the transformer is sort of insulating the TI kit from the grid. It acts like a filter and the hf emissions are much lower a the primary than at the secondary. In our measurements we experienced high supraharmonic amplitude, up to 96% of the fundamental voltage and 22%for of the fundamental current for the 50kHz component (see Section 4.2.2). Because of this high amplitude, a 11bits resolution seems enough.

3.4.2 Current probe

The current probe is the TCP312A with the TCPA300. It offers a high bandwidth up to 100MHz. The first probe used has a much lower bandwidth at 200kHz and struggled to measure accurately the frequency content up to 150kHz.

This current probe has an accuracy of ±1.5% of the reading and can measure peak current of 50A. The currents we measure do not exceed 10A peak.

3.4.3 Grid impedance meter

In Section 2.1 we use the Solar200 with the IMP57 from HT Instrument to measure the grid impedance. We expose here the specification of those measurement devices. The Solar200 is a multifunctional meter for safety tests on photovoltaic plants. The feature we are interested in is his ability to measure the phase to neutral impedance. This can be easily done by connecting the meter directly to the outlet as represented on figure 3.7.

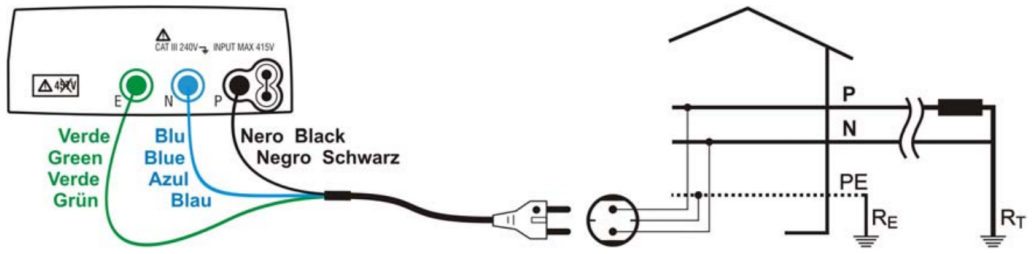


Figure 3.7: Instrument connection for 230V single-phase P-N line impedance measurement through shuko cable

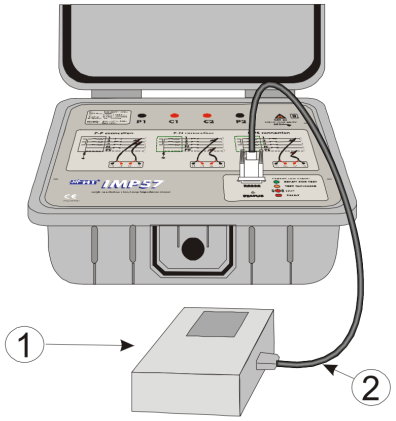
But this method as some drawbacks. First the resolution is really poor. Table 3.2 shows the comparison between the two devices. The IMP57 has a higher resolution and by looking at the range column, it is clear that the Solar200 alone is for higher impedance measurement. As a reminder the grid impedance we measure here is $456m\Omega$.

Table 3.2: Technical specification comparison for line to neutral impedance measurement

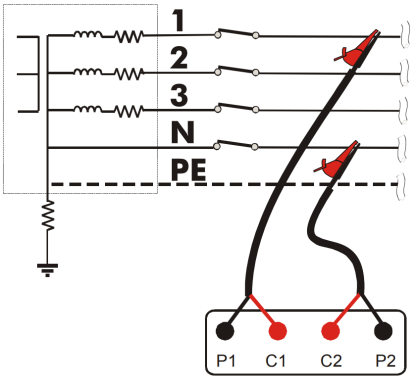
	Range	**Resolution**	**Accuracy**
Solar200 alone	$0.01 \div 9.99\Omega$	0.01Ω	$\pm$(5%rdg+3dgt)
	$10 \div 199.9\Omega$	0.1Ω	
Solar200 + IMP57	$0.0 \div 199.9m\Omega$	$0.1m\Omega$	$\pm$ (5%rdg+$1m\Omega$)
	$200 \div 1999m\Omega$	$1m\Omega$	

Secondly, the IMP57 has the ability to measure the total impedance but also the reactive and the resistive part of the impedance, the Solar200 can only measure the total impedance. The final reason we use the IMP57 is because the current inrush for measuring the short circuit impedance was too high and the Solar 200 alone would not make any measurement. This is why we had no choice but using the IMP57.

The connection instructions of the IMP57 and Solar200 for impedance measurement are represented on Figure 3.8.



(a) IMP57 connection with the Solar200 (1)



(b) Instrument connection for phase to neutral impedance measurement

Figure 3.8: Connection instructions

Chapter 4

Measurements and results

4.1 Harmonics

In this section we focus on the behaviour of our APFC for the "classical" harmonics, so up to 2kHz. Let us remember that one of the purposes of the PFC is to mitigate the harmonic content. We will also compare the waveform with and without PFC stage.

4.1.1 No PFC

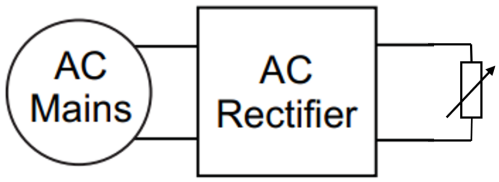
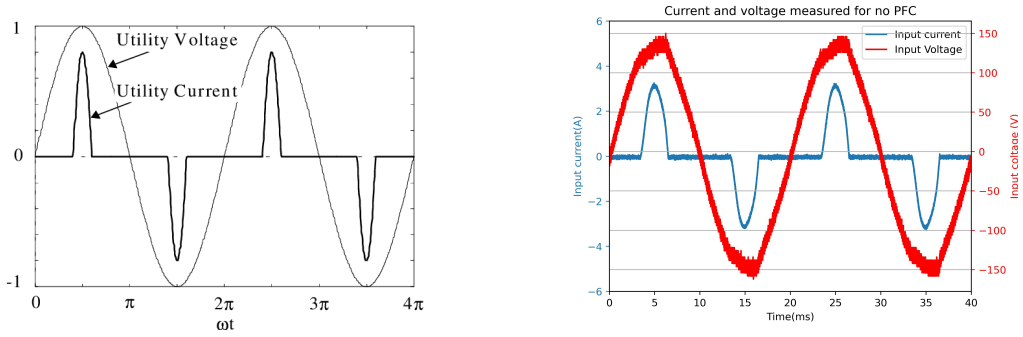


Figure 4.1: Block diagram with no PFC

In this situation we just have the diode bridge and capacitor that are rectifying the voltage to have a DC voltage. The classical voltage and current waveform of rectifier bridge are represented on figure 4.2a.



(a) Typical rectifier waveforms [29] (b) Measured waveforms

Figure 4.2: Typical and measured input current and voltage

To achieve this situation with the TI kit, we just put the duty cycle to 0 in the Simulink file. This will keep to two transistors of the IBC open and the current will flow directly to the load.

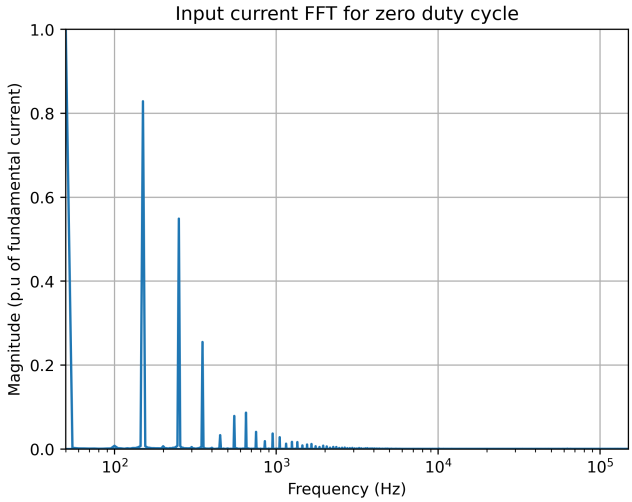


Figure 4.3: Fourier Transform of the input current fo zero duty cycle

Figure 4.3 shows the Fourier Transform of the input current. As expected the odd harmonics have quite a high amplitude. The THD is high and reaches 107.55%.

4.1.2 With the control of the IBC

Achieving a working control was the most important step in this master thesis. In fact it has taken several months to be able to understand and build the Simulink blocks to run the control. The first step was to run the IBC with a fixed duty cycle, so with no control at all. This was a key step because it allows to verify that the simulink blocks were driving the two transistors of the IBC correctly. Achieving two PWM signals in phase opposition as represented on figure 2.15 was the first victory on the road toward a working Active Power Factor Corrector circuit.

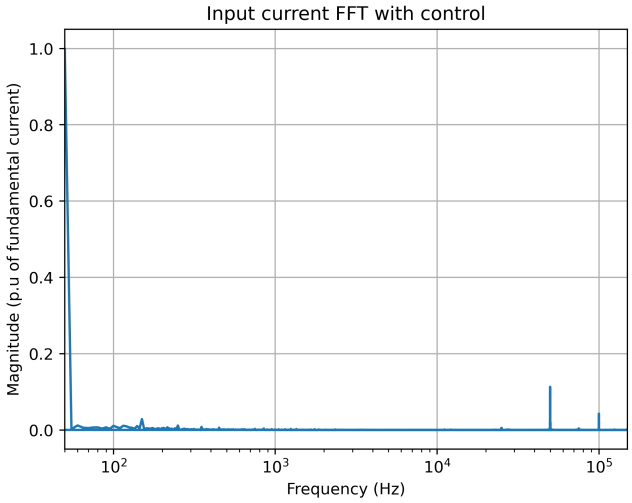


Figure 4.4: Fourier Transform of the input current with control enabled

After that we tested the control and after some tuning, we could finally make it successfully work on the TI kit. The goal of the APFC is to reduce waveform distortion, in other words, limit the low frequency harmonics. By looking to Figure 4.4 and comparing it to figure 4.3 we can clearly see that the IBC works well as an APFC and that the low frequency harmonics are almost suppressed. But it comes at the price of new harmonic distortions at higher frequencies. As we could expected, supraharmonics appears at 50kHz and multiple of 50kHz due to commutation of the IBC, 50kHz being the switching frequency. This supraharmonic rejection is studied in section 4.2.

The current Total Harmonic Distortion is dramatically reduced and is

equal to 0.05% but this results has to be taken with a grain of salt. In fact let us remember how the current THD is computed.

$$THD_I = \sqrt{\sum_{h=2}^{h_{max}} \left(\frac{I_{H,h}}{I_{H,1}}\right)^2} \tag{4.1}$$

The sum of the harmonic components is done up to a specified order, h_{max}. This order is 40 as specified in IEC 6100-4-7 so we are doing the sum only up to 2kHz, not taking into account the energy of the higher supraharmonics. If we compute a new THD by summing up to 150kHz ($h_{max} = 3000$) we have a new higher current THD of 6.04%.

Next we will look at the impact of the proportional parameter of the inner-control loop (P_i) of the IBC.

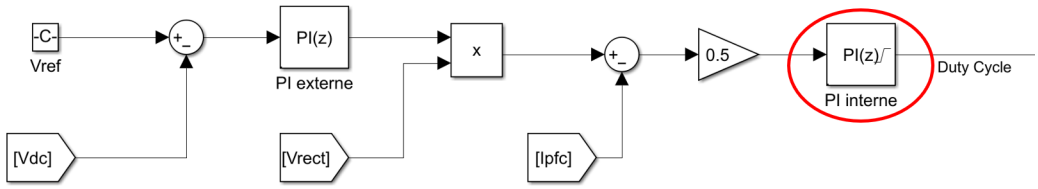


Figure 4.5: Control loop of the IBC with the inner loop PI block circled in red

Figure 4.6 shows the Fourier transform of the input current for a proportional factor of 0.1, 0.2 and 0.3. We can see that the best low frequency harmonics attenuation seems to be achieved with $P_i = 0.1$. This is a bit unexpected. Fist because Erzen's mathematical development find a proportional factor of 0.35. Secondly, because we could expect that a higher gain gives a higher duty cycle amplitude variation so a better aptitude of the control to shape the current waveform as a sinusoidal wave. In the simulation ran by Erzen, the duty cycle follows perfectly the rectifier voltage

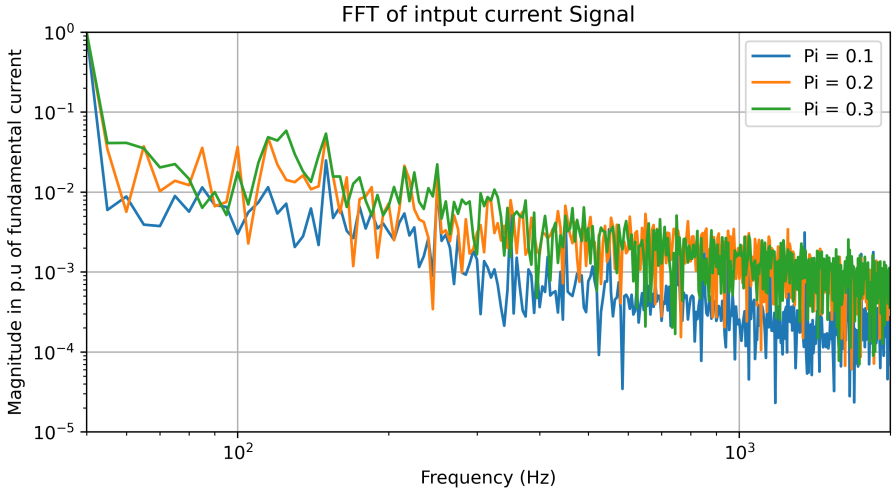


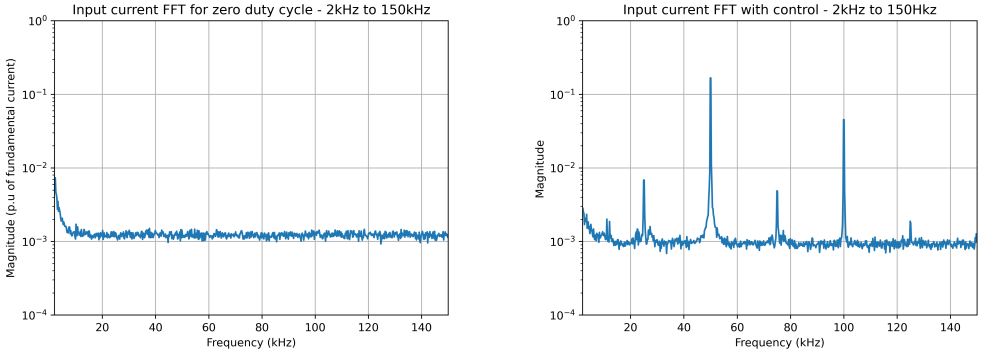
Figure 4.6: Fourier transform of input signal for different value of the proportional parameter of the inner loop.

4.2 Supraharmonics

In this section we focus on the higher frequency components (2-150kHz). The lower frequency components are filtered using the elliptic filter described in section 3.2.1. We first look at the Fourier Transform for a more "visual" analysis. Then we zoom in on the 50kHz component (switching frequency) and apply a quadratic sum on a 800Hz band around it. This is to have a value that represented the power of this signal at the switching frequency, a value we can compare between the different experiences conducted.

4.2.1 Preliminary frequency content observation

First let us compare the signal content of the current with the APFC (Figure 4.7b) and with it disabled (Figure 4.7a). In the previous section we could observe the low frequency harmonic attenuation but here we can clearly see the appearance of new frequencies. The spikes at 50kHz, 100kHz are expected because of the 50kHz switching frequency. The one at 25kHz, 75kHz an 125kHz comes from the 25kHz PWM frequency. Another frequency group is visible around 10kHz, which is not expected at all. One explanation could be



(a) Zero duty cycle (b) With control

Figure 4.7

the presence of another self-commuted device connected near the test bench. Let us look at grid voltage spectral content on Figure 4.8 to see if something is present. Even by zooming on the Y axis, we still don't see any spike at 10kHz. The only explanation I can give is that it is coming from the 12V

DC power supply that is feeding the Texas Instrument 12V, 5V, and 3.3V DC lanes.

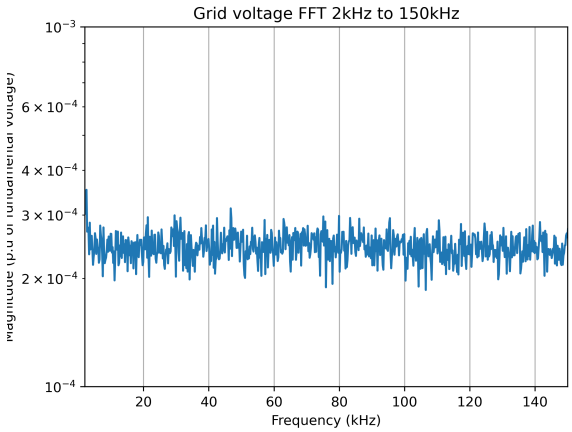


Figure 4.8: h

4.2.2 Supraharmonics source type

We want to find if the PFC circuit with our control acts like a supraharmonic current or voltage source. To do so, we put an inductance (L_s) in serie with the grid and measure the voltage and current at the input of the TI kit for different values of the serie inductance. By looking at the voltage and current variation in function of L_s we can deduce the current or voltage source behaviour.

Figure 4.9 represents the situation where the APFC acts like a supraharmonic **voltage source**. In this case V_{sh}, the 50kHz component of the voltage is constant. If we change the value of L_s we will measure a **different current and the same voltage**.

$$I_{sh} = \frac{V_{sh} - V_{grid}}{jwL_s + Z_{g,e}} \tag{4.2}$$

The simplified circuit equation 4.2 shows this. If L_s increases and V_{sh} is constant (voltage source), I_{sh} will decrease.

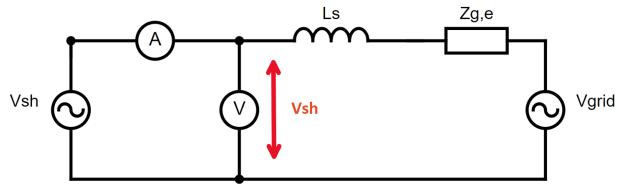


Figure 4.9: Supra harmonic voltage source - simplified representation

Figure 4.10 represents the situation where the APFC acts like a supra-harmonic **current source**. In this case I_{sh}, the 50kHz component of the current is constant, if we change the value of L_s we will measure a **different voltage and the same current**.

$$V_{sh} = V_{grid} + I_{sh}(jwL_s + Z_{g,e}) \tag{4.3}$$

The simplified circuit equation 4.3 shows this. If L_s increases and I_{sh} is constant (current source), V_{sh} will increase.

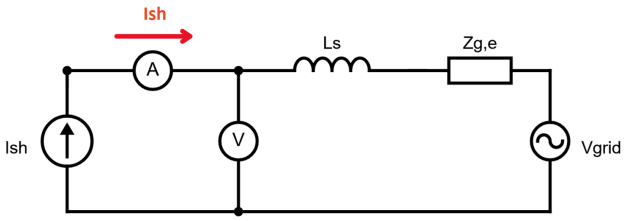


Figure 4.10: Supra harmonic current source - simplified representation

The experiment was lead with 4 inductance values: 0.5mH, 1mH, 2mH, and 5mH.

Grouping in a 800Hz band around 50kHz

To be able to easily compare the 4 situations under study we use grouping around the 50kHz switching frequency. The 200Hz grouping is not sufficient to provide a good estimation of the energy around the switching frequency. As precised by [30], "The 200 Hz bands according to [IEC 61000-4-7] are not optimal, because they don't cover the whole energy of an emission band".

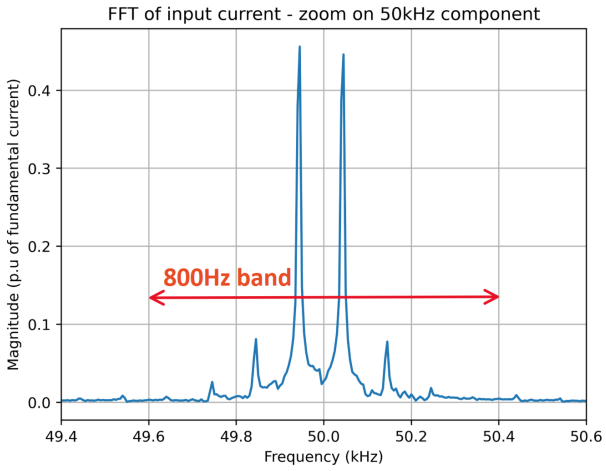


Figure 4.11: Zoom on 50kHz current component

This is in fact verified here. By looking at Figure 4.11 it is obvious that taking only a 200Hz band will not take into account the energy of the side lobes.

$$G_{50kHz} = \sqrt{\sum_{f=50kHz-395Hz}^{50kHz+400Hz} Y_{C,f}^2} \tag{4.4}$$

Equation 4.4 gives the formula used for the grouping. Where $Y_{C,f}$ is the value of the component at the frequency f.

Results

Figure 4.12 shows 12 measurements of the 50kHz current component on one graph. Beside looking at the impact of the serie inductance, we also changed the value of P_i (the proportional factor of the current loop). Each colour represents the measurement for one inductance value and on the X-axis we have the three P_i values used. First, we can observe that the supraharmonic component decreases as the inductance increases. For $P_i = 0.1$ it goes from 22.4% of the fundamental current to 15.4%, which relatively to 22.4 is a 32% decrease. This decrease emphasis the hypothesis of a supraharmonic voltage source.

If we look at the impact of the control, the increase of the proportional factor seems to slightly reduce the 50kHz supraharmonic current. For the

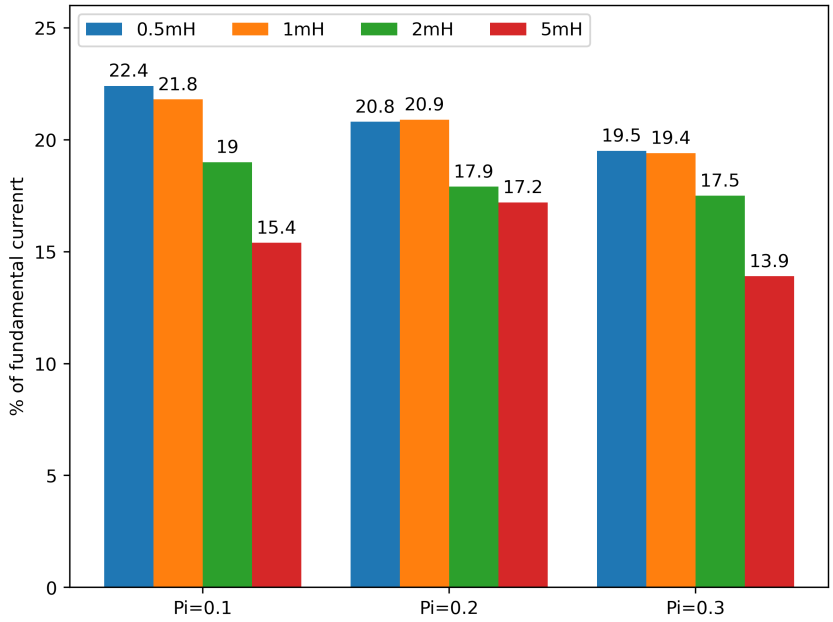


Figure 4.12: 50khz current component amplitude in function of P_i and the serie inductance

0.5mH inductance we have a 2.9% decrease of I_{sh} when P_i goes from 0.1 to 0.3 which is a relative decrease of 13%. With such a small variation we cannot deduce any experimental relation, we can only affirm that there is an impact on the supraharmonic current rejection. We observe still an outsider for 5mH with a value of 17.2% of I_{sh} for $P_i = 0.2$ which is a relative increase of 12% compared to the 15.4% for $P_i = 0.1$.

Figure 4.12 shows measurements of the 50kHz voltage component. The maximum variation we observe is 5% of fundamental voltage (from 91.5% to 96.5%) which relatively to 91.5 is a 5.5% increase. By looking at the graph, we cannot see any significant increase from 0.5mH to 1mH and 2mH. A small increase is observed for 5mH. We can conclude that the harmonic voltage varies very slightly, this emphasis the voltage source behaviour.

Now by looking at the impact of P_i we can see globally a slight decrease but an outsider for 1mH from $P_i = 0.1$ to 0.2 with an increase of the 50kHz voltage component.

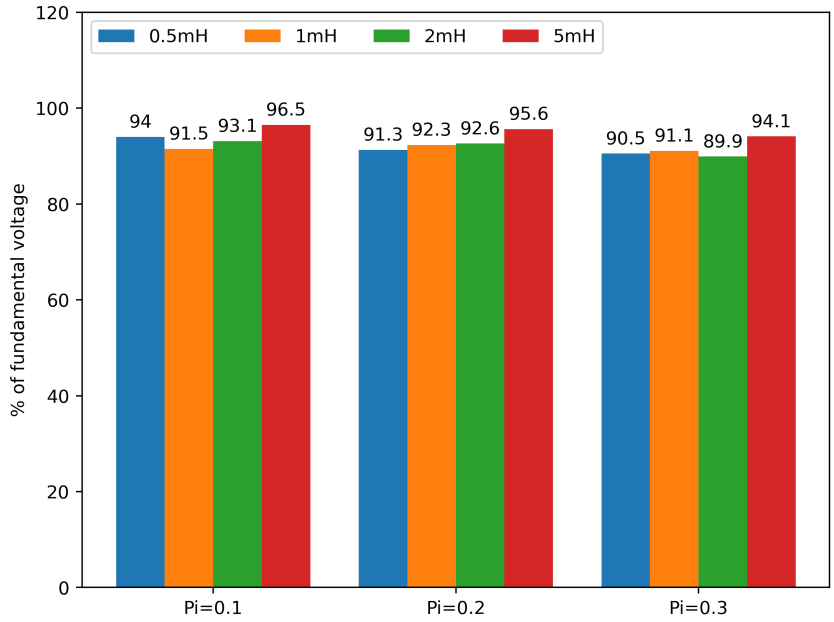


Figure 4.13: 50khz voltage component amplitude in function of P_i and the serie inductance

4.3 Points of attention

The results presented here have to be taken with a grain of salt. In fact the tests experience a lack of precision, the results are poorly reproducible with exactly the same value. The measurement environment can influence the accuracy of the measurement and is difficult to characterise precisely.

The main points of attention are:

- Non-respect of measurement standards. IEC-61000-4-7 requirements on the harmonic content of the test voltage of the EUT are not respected. The lab grid voltage harmonic content exceeds the requirements.
- The Texas Instrument is not connected directly to grid, the transformer has a heavy impact on measurements.
- The input voltage is 70Vrms which is below the recommended working voltage of the TI kit. During the measurements we did not notice any

significant behaviour change when working at a higher voltage. Still the recommended minimum voltage is 85Vrms and a lower voltage could have a hidden impact.

- When increasing P_i, the current waveforms seem to become unstable. A sort of amplitude modulation appears as we can see on Figure 4.14. One possible explanation could come from the saturation parameter of the PI block of the internal control loop. This saturation keeps the duty cycle between 0.5 and 1.

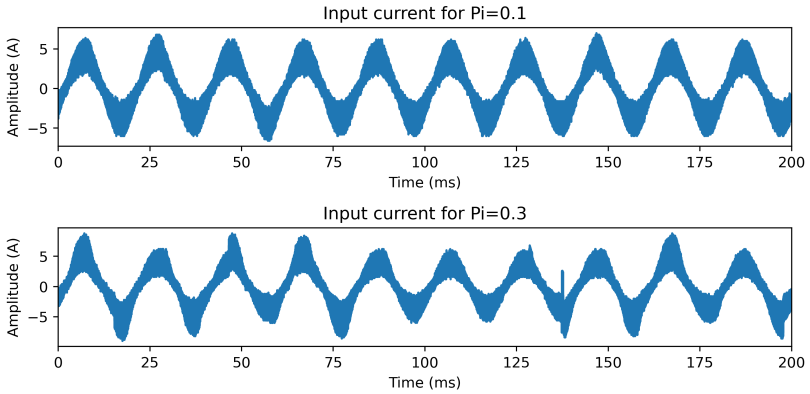


Figure 4.14

Conclusion

4.4 Content overview

The goal of this master thesis was to introduce the power quality issue of supraharmonics with a focus on the emissions of an Active Power Factor Corrector. First the main sources of supraharmonic disturbances are presented with a literature review of solar inverters, EV charger and LED lamps. Then the three measurement standards relevant for the frequency band 2-150kHz are presented, the measurement method used is the 200Hz band grouping proposed in Annex B of IEC61000-4-7 extended to 150kHz.

In the second chapter, a focus is made on the study of an APFC. An experimental setup is built to test a specific control and to determine its behaviour as supraharmonic current or voltage source. This setup is composed of a Texas instrument development kit connected to an auto transformer. The TI kit is the master piece and permits to implement the desired control using Simulink.

The third chapter explains the measurement method. The side effects of the Discrete Fourier Transform are explained and two digital filters are designed to mitigate those. A high-pass elliptic filter is used to filter the frequency up to 2kHz and limit spectral leakage. One Butterworth low-pass filter is used as antialiasing filter.

Finally, the results are presented. Firs the effectiveness of the APFC in reducing the low frequency harmonics (up to 2kHz) is shown. Secondly the supraharmonic voltage source behaviour of the converter is confirmed.

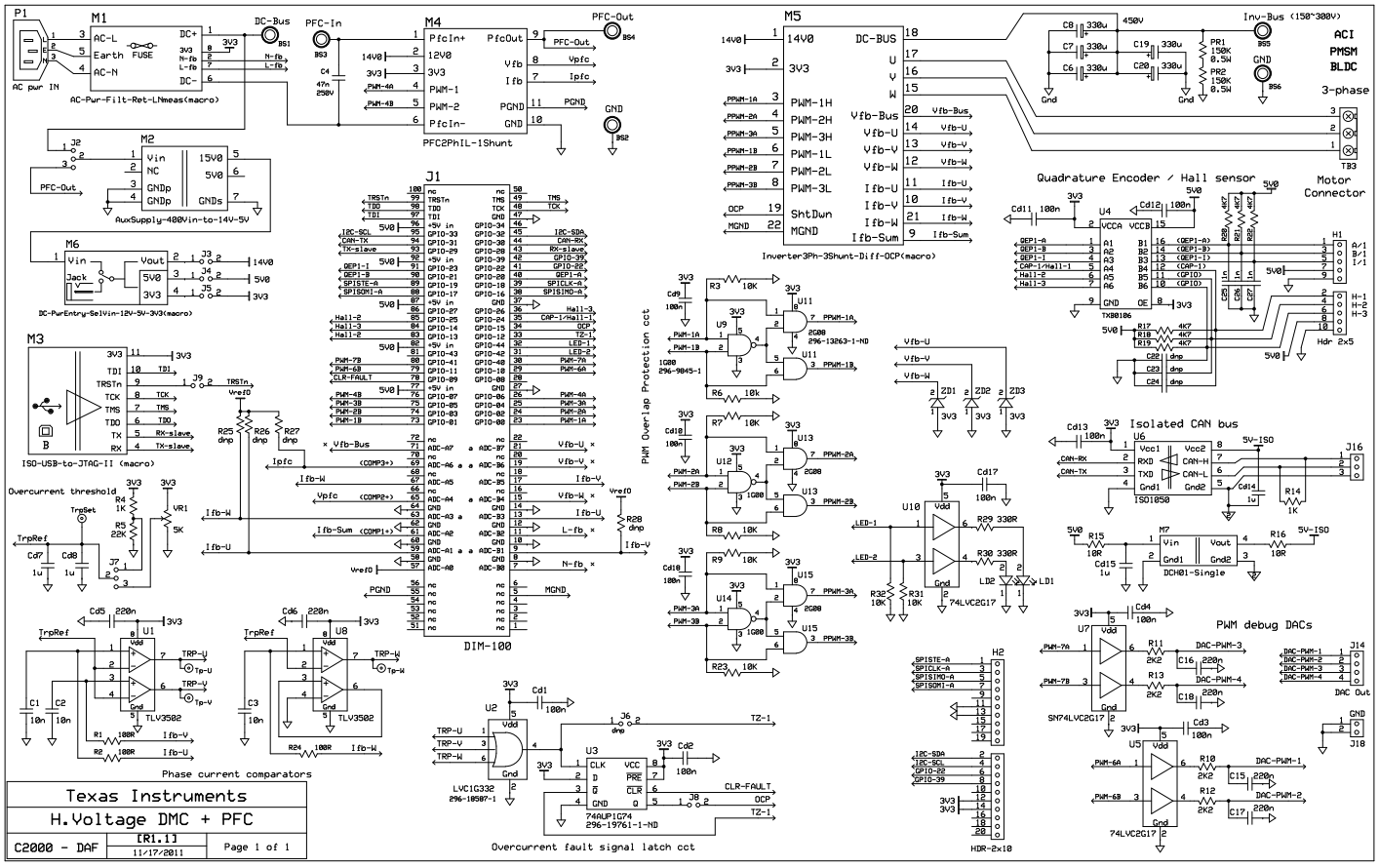
4.5 Recommendations for future work

Here are some recommendations for future work linked to the investigation lead in this master thesis.

- First, it could be interesting to connect the inverter stage of the Texas Instrument kit. It would permit to investigate the impact of this stage on supraharmonic emissions.
- The Interleaved Boost Converter is the converter topology used for power factor correction. As explained in Section 2.4, there exists other topologies. The supraharmonic emissions of those could also be investigated.
- The experimental setup could be extended to multiple TI kit to study the impact of multiple devices connected to the same grid, as done in [12] for EV chargers.
- Other controls could be used with the exact same setup. In fact the investigation of an other control has already started but the first measurements were not relevant and some tuning is necessary. This control comes from the PhD thesis of Caroline Leroi [31] and its supraharmonic current and voltage source behaviour is investigated by Erzen Muharemi in [27] with simulations. It would be really interesting to compare those simulations with experimental measurements.

Appendix A

Texas Instrument kit schematics


P1
M1
AC-Pwr-Filt-Ret-LMmeas(macro)
AC pwr IN
DC-Bus
PFC-In
PFC-Out
PFC2PhIL-1Shunt
M4
M5
Inverter3Ph-3Shunt-Diff-OCP(macro)
Inv-Bus (150~300V)
ACI
PMSM
BLDC
3-phase
Quadrature Encoder / Hall sensor
Motor
Connector
M2
AuxSupply-400Vin-to-14V-5V
M6
DC-PwrEntry-SelVin-12V-5V-3V3(macro)
J1
DIM-100
M3
ISD-USB-to-JTAG-II (macro)
Overcurrent threshold
Isolated CAN bus
ISO1050
DCH01-Single
PWM debug DACs
SN74LVC2G17
LVC1G332
296-10507-1
74AUP1G74
296-19761-1-ND
Overcurrent fault signal latch cct
PWM Overlap Protection cct
Phase current comparators
HDR-2x10
Hdr 2x5
Texas Instruments
H.Voltage DMC + PFC
C2000 - DAF
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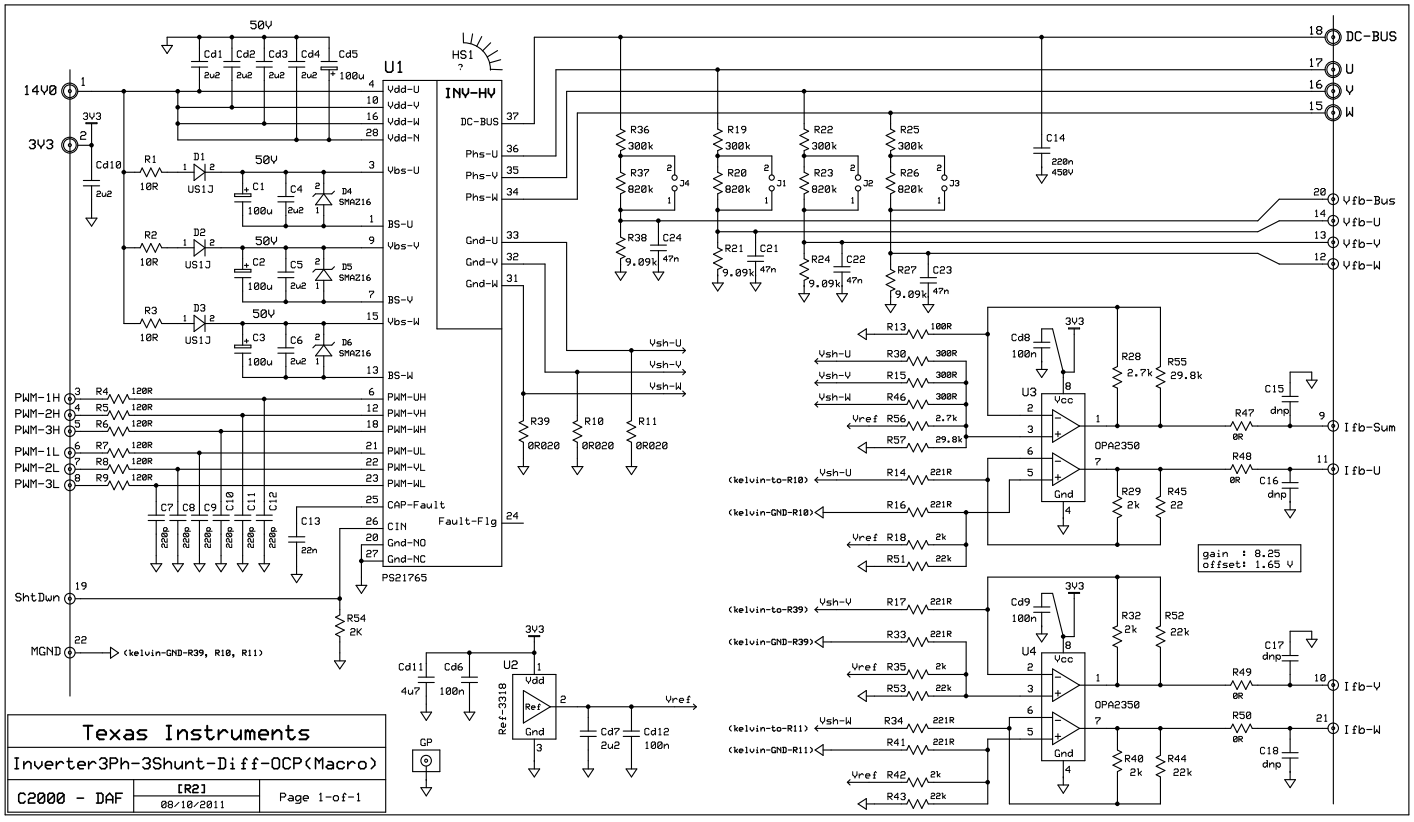
Texas Instruments
Inverter3Ph-3Shunt-Diff-OCP(Macro)
C2000 - DAF
[R2]
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Page 1-of-1
14V0
3V3
50V
U1
INV-HV
HS1
DC-BUS
PWM-1H
PWM-2H
PWM-3H
PWM-1L
PWM-2L
PWM-3L
ShtDwn
MGND
PS21765
Fault-Flg
OPA2350
U2
Ref-3318
U3
U4
gain : 8.25
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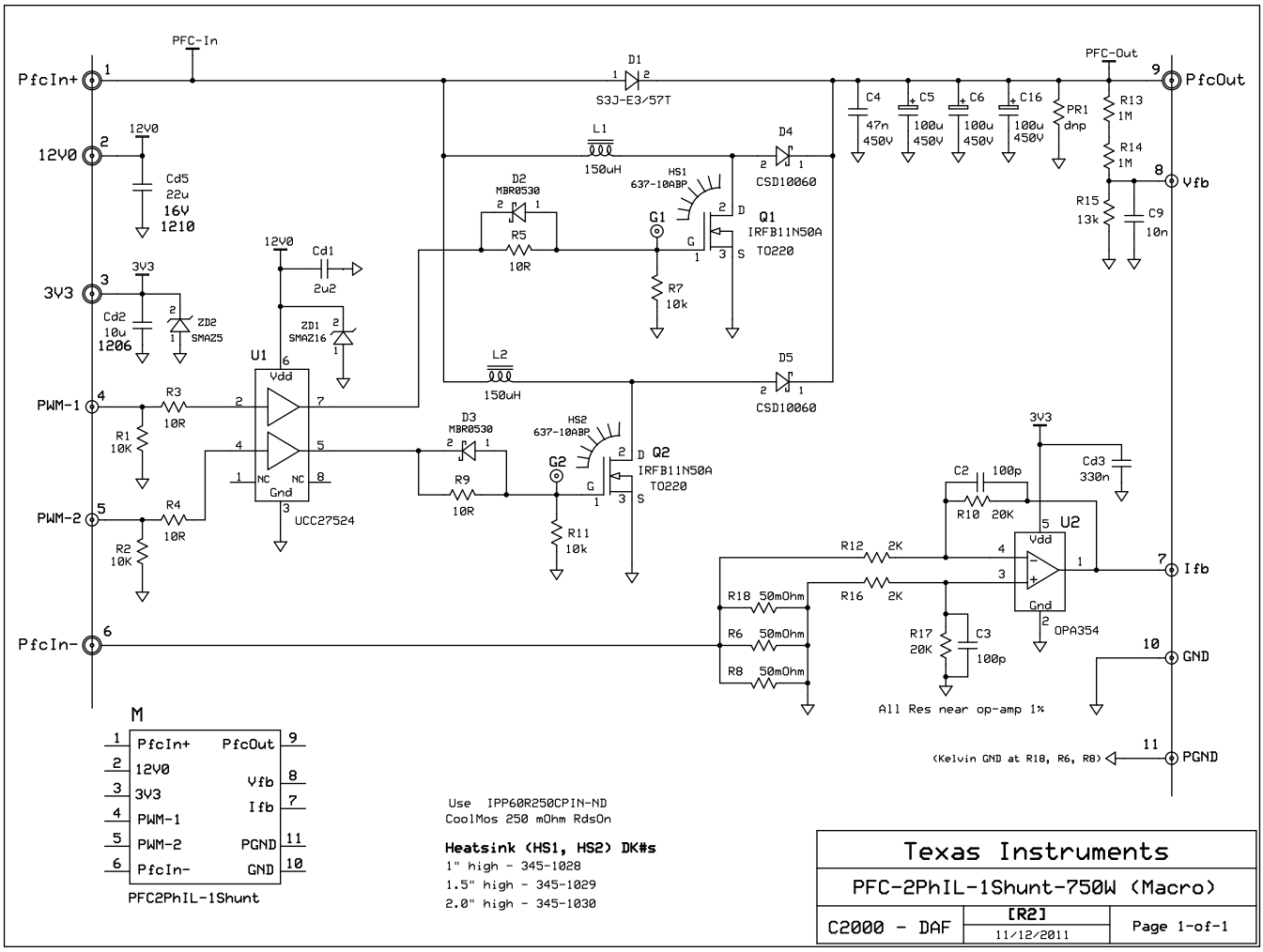
Vfb-U
Vfb-V
Vfb-W
Ifb-Sum
Ifb-U
Ifb-V
Ifb-W


PFC-In
PFC-Out
PfcIn+
PfcIn-
PfcOut
12V0
3V3
Vfb
Ifb
GND
PGND
PWM-1
PWM-2
D1
S3J-E3/57T
L1
150uH
L2
150uH
D2
MBR0530
D3
MBR0530
D4
CSD10060
D5
CSD10060
HS1
637-10ABP
HS2
637-10ABP
Q1
IRFB11N50A
TO220
Q2
IRFB11N50A
TO220
G1
G2
R5
10R
R7
10k
R9
10R
R11
10k
R1
10K
R2
10K
R3
10R
R4
10R
C4
47n
450V
C5
100u
450V
C6
100u
450V
C16
100u
450V
PR1
dnp
R13
1M
R14
1M
R15
13k
C9
10n
Cd5
22u
16V
1210
Cd2
10u
1206
Cd1
2u2
ZD1
SMAZ16
ZD2
SMA25
U1
Vdd
Gnd
NC
NC
UCC27524
C2
100p
R10
20K
Cd3
330n
U2
OPA354
R12
2K
R16
2K
R17
20K
C3
100p
R18
50mOhm
R6
50mOhm
R8
50mOhm
All Res near op-amp 1%
(Kelvin GND at R18, R6, R8)
M
PFC2PhIL-1Shunt
Use IPP60R250CPIN-ND
CoolMos 250 mOhm RdsOn
Heatsink (HS1, HS2) DK#s
1" high - 345-1028
1.5" high - 345-1029
2.0" high - 345-1030
Texas Instruments
PFC-2PhIL-1Shunt-750W (Macro)
C2000 - DAF
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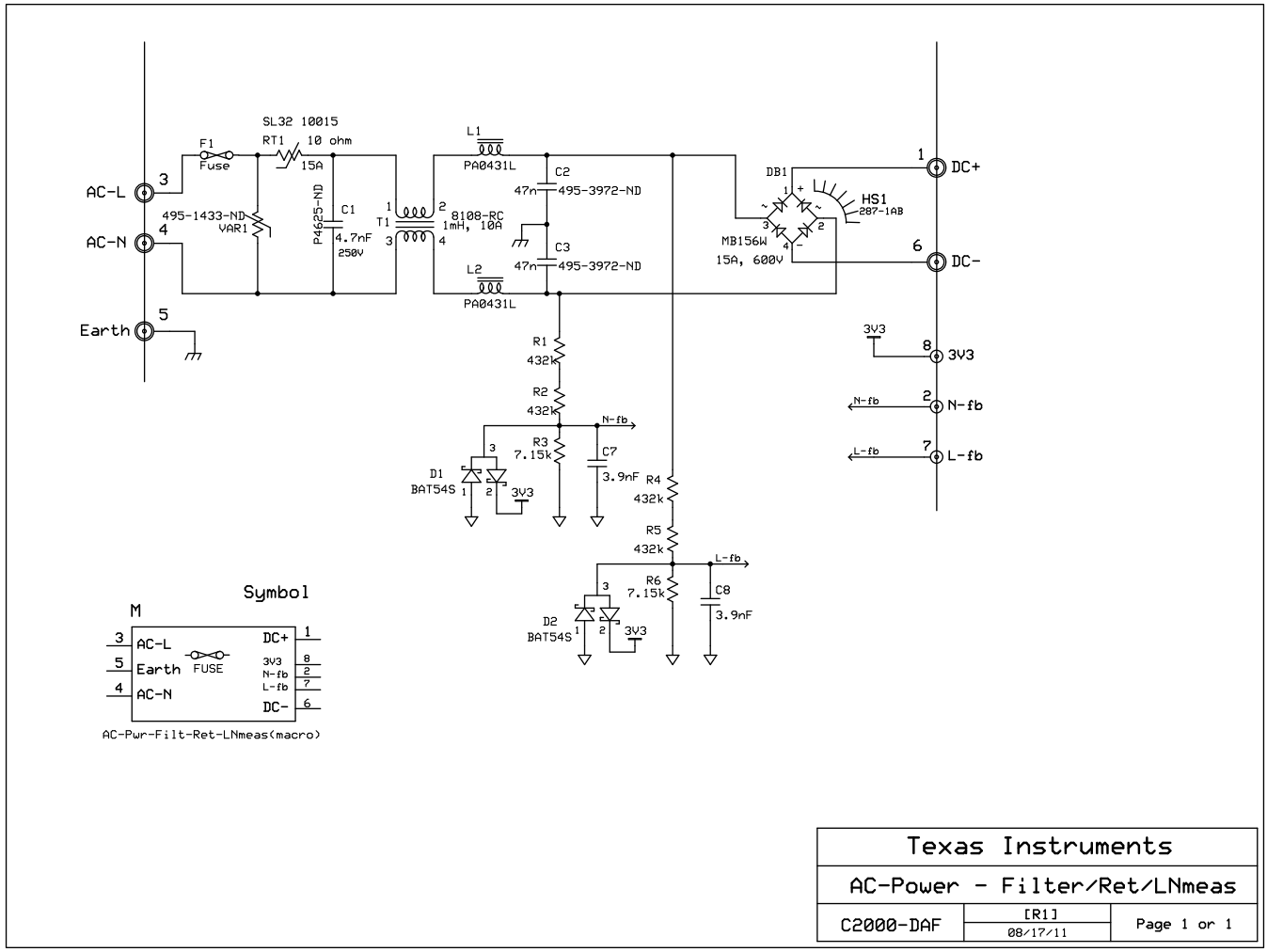
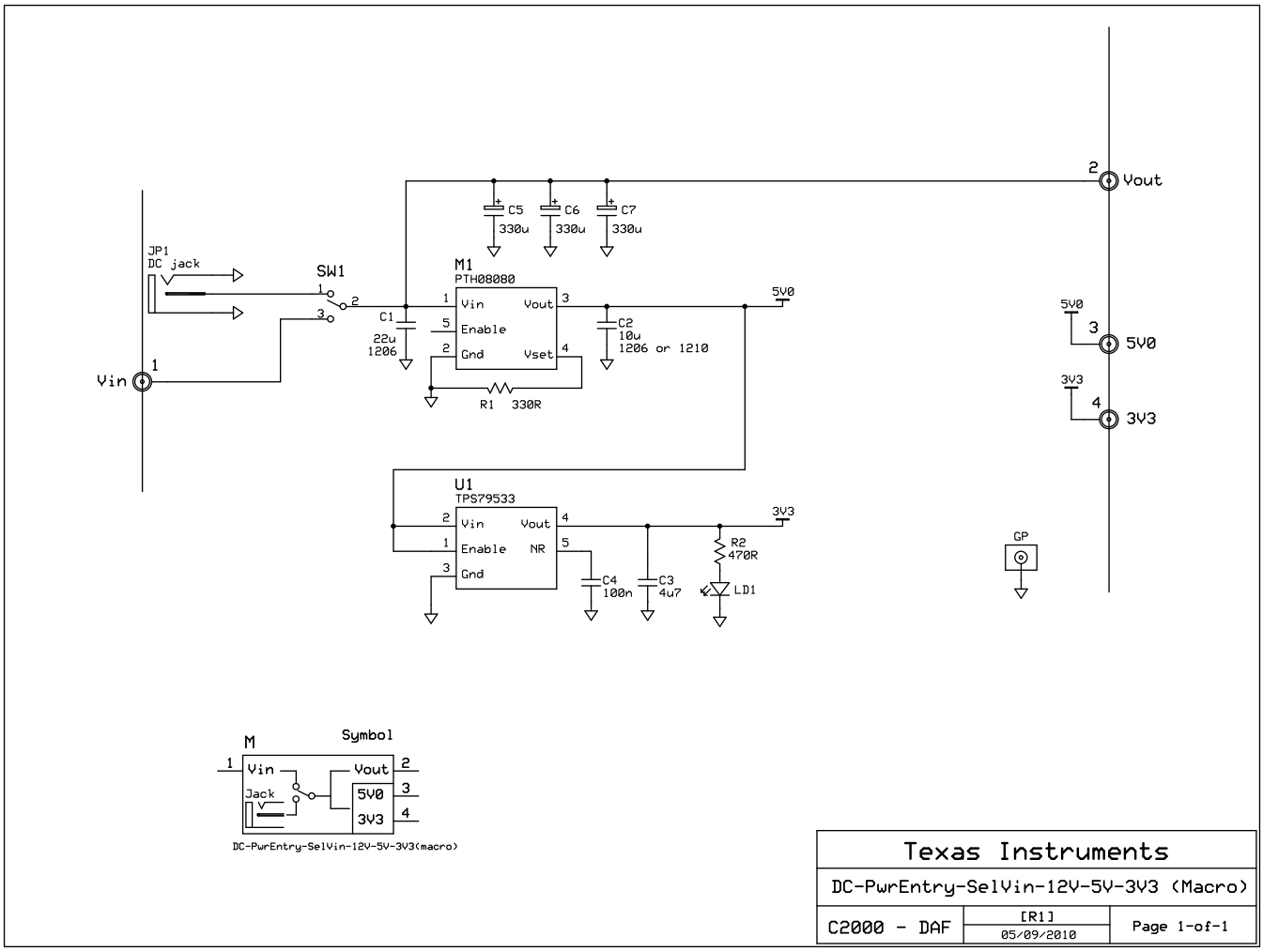


Texas Instruments		
AC-Power - Filter/Ret/LNmeas		
C2000-DAF	[R1] 08/17/11	Page 1 or 1


JP1
DC jack
SW1
Vin
C1
22u
1206
M1
PTH08080
Vin
Enable
Gnd
Vout
Vset
C5
330u
C6
330u
C7
330u
C2
10u
1206 or 1210
R1 330R
5V0
U1
TPS79533
Vin
Enable
Gnd
Vout
NR
3V3
C4
100n
C3
4u7
R2
470R
LD1
GP
2
Vout
5V0
3
5V0
3V3
4
3V3
M
Symbol
Vin
Jack
Vout
5V0
3V3
DC-PwrEntry-SelVin-12V-5V-3V3(macro)
Texas Instruments
DC-PwrEntry-SelVin-12V-5V-3V3 (Macro)
C2000 - DAF
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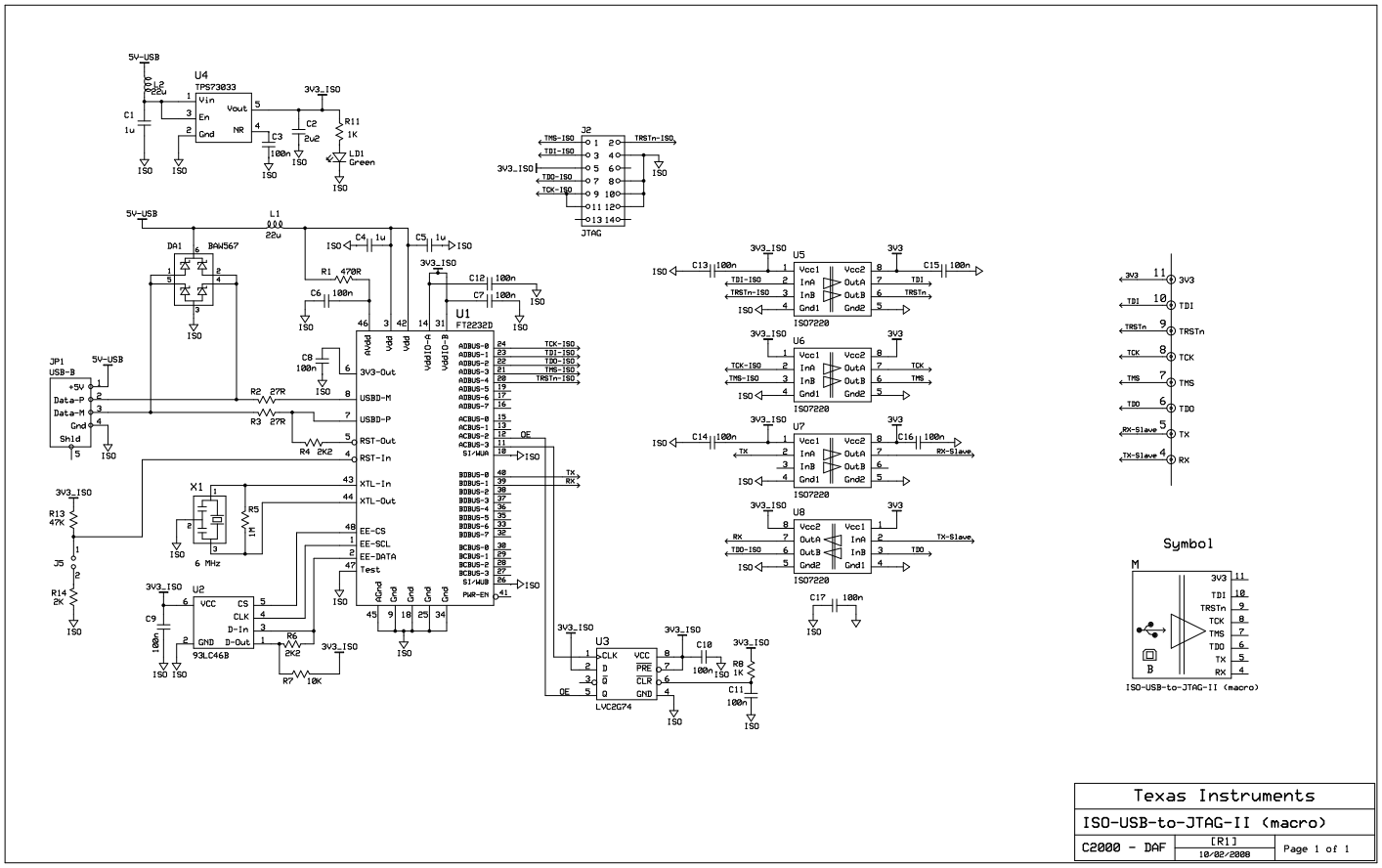
5V-USB
U4
TPS73033
Vin
En
Gnd
Vout
NR
3V3_ISO
C1
1u
C2
2u2
C3
100n
R11
1K
LD1
Green
ISO
J2
JTAG
TMS-ISO
TDI-ISO
TDO-ISO
TCK-ISO
TRSTn-ISO
3V3_ISO
L1
22u
DA1
BAW567
C4
1u
C5
1u
C6
100n
R1
470R
C12
100n
C7
100n
U1
FT2232D
3V3-Out
USBD-M
USBD-P
RST-Out
RST-In
XTL-In
XTL-Out
EE-CS
EE-SCL
EE-DATA
Test
PWR-EN
ADBUS-0
ADBUS-1
ADBUS-2
ADBUS-3
ADBUS-4
ADBUS-5
ADBUS-6
ADBUS-7
ACBUS-0
ACBUS-1
ACBUS-2
ACBUS-3
BDBUS-0
BDBUS-1
BDBUS-2
BDBUS-3
BDBUS-4
BDBUS-5
BDBUS-6
BDBUS-7
BCBUS-0
BCBUS-1
BCBUS-2
BCBUS-3
JP1
USB-B
+5V
Data-P
Data-M
Gnd
Shld
R2 27R
R3 27R
R4 2K2
C8
100n
X1
6 MHz
R5
1M
J5
R13
47K
R14
2K
U2
93LC46B
VCC
CS
CLK
D-In
D-Out
GND
C9
100n
R6
2K2
R7
10K
U3
LVC2G74
CLK
D
Q
VCC
PRE
CLR
GND
C10
100n
R8
1K
C11
100n
U5
U6
U7
U8
ISO7220
Vcc1
Vcc2
InA
InB
Gnd1
Gnd2
OutA
OutB
C13
100n
C14
100n
C15
100n
C16
100n
C17
100n
TDI
TRSTn
TCK
TMS
TDO
TX
RX
TX-Slave
RX-Slave
Symbol
ISO-USB-to-JTAG-II (macro)
Texas Instruments
C2000 - DAF
[R1]
10/02/2008
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Appendix B

Texas Instrument kit programming with Simulink

B.1 Package installation

First the C2000 blockset has to be installed, the procedure is not explained here because it is well described on MathWorks© website.

B.2 No control - fixed duty cycle

The first step to implement the control on the kit is to understand how to use the ePWM blocks of Simulink. To do so we start with a simpler situation were there is no control at all and a fixed duty cycle is applied, as represented on Figure B.1.

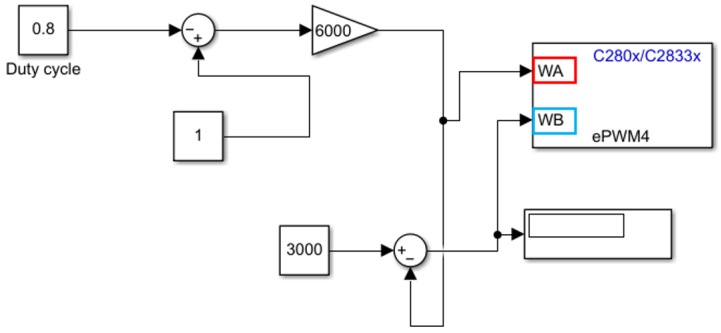

Figure B.1: Simulink blocks for fixed duty cycle

Let us explain the values used on this schematic. The CPU clock is 150Mhz, we want a PWM frequency of 25kHz so we 6000 CPU period to achieve one PWM period, this is why we multiply by 6000.

$$\text{number of cpu cylces} = \frac{f_{CPU}}{f_{PWM}} \tag{B.1}$$

We need to take $1 - D$ because the input value WA is the number of cycle before rising (CAU on Figure B.2). For the input value WA it is a bit more complicate and counting is in the opposite direction (CBD on Figure B.2). As we can see on the figure CBD is actually the complementary of CAU on a half switching period. This is the key element to achieve 180°phase between the two PWM signals and this simple relation has been really tricky to find because of the way number CBD cycles are counted.

$$CBD = 3000 - CAU \tag{B.2}$$

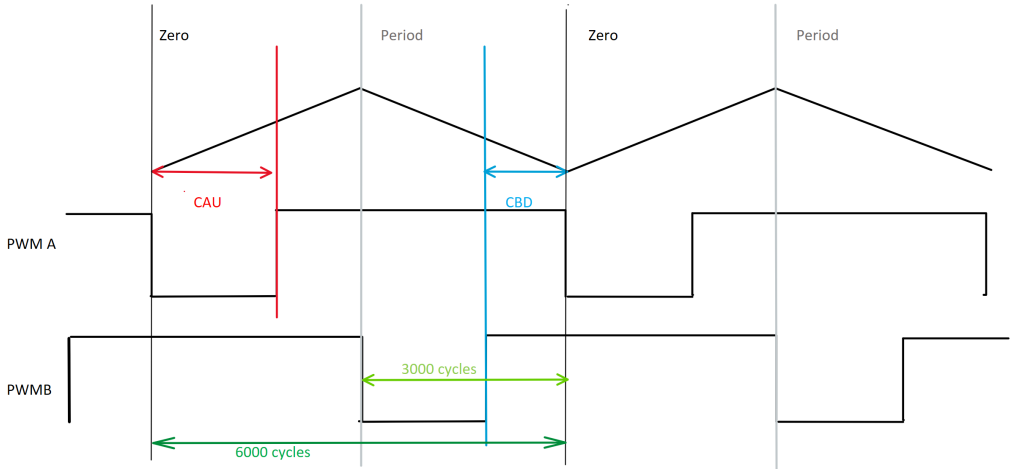

Figure B.2: Blocks parameter representation on waveforms

The parameter used are given on Firgure B.3

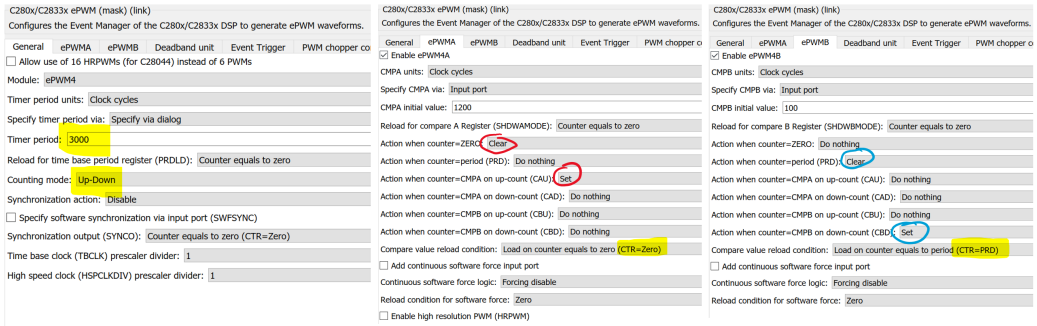

Figure B.3: ePWM Block parameters to achieve 180°phase shift of PWM signals

B.3 With control

This step is really straightforward. The fixed duty cycle of figure B.1 has just to be replaced with the control paying attention to the fact that the output of the control loop is the duty cycle between 0.5 and 1.

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