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Study and energetic optimization of the electrical supply of a nanosatellite

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Abstract

In recent years, CubeSats gain in popularity among researchers due to their cheapness and lightweight allowing them to conduct space researches and missions for competitive prices. These satellites are mostly launched in low earth orbit where regular eclipses, experienced by the spacecraft, challenges the satellite developers in the design of efficient and reliable power supplies.

This thesis aims to study and optimize the power supply of a CubeSat. Therefore, an overview of the CubeSat technology, power generation and energy storage is provided so that the main challenges of space missions are identified. Afterwards, a study and energetic optimization is conducted to determine and select the optimal system configuration. At last, a system implementation is performed along with a failure analysis.

Optimization results have shown that many configurations can be selected but robustness should also be taken into account. Therefore, in spite of all considerations, a robust and moderately efficient configuration is preferred rather than a system with maximum efficiency. In addition, the failure analysis has shown that the basic implementation is rather susceptible to failure, but many methods of compensation are available. Therefore, the final implementation is based on the trade-off between complexity and robustness.

This thesis sets the ground for optimizing and implementing mission-specific power supplies that could lead to cost saving and time cutting in CubeSat design. But many different design choices, configurations, implementations, tests have been left for future work. For instance, an electrical implementation of the final system, PCB realization, software implementation and measurements can be done to compare the results obtained in this work with the actual system performances.

Keywords— Nanosatellite, CubeSat, Power supply, EPS, Energetic study, Energetic optimization, System implementation, Failure analysis

Contents

List of Abbreviations

C_6	Graphite
CO_2	Dicarbon monoxide
CoO_2	Cobalt (II) Peroxide
CoO	Cobalt (II) oxide
H_2O	Water
Li^+	Lithium ion
Li_2O	Lithium oxide
LiC_6	Lithium-intercalated graphite compound
$LiCoO_2$	Lithium Cobalt oxide
LiPo	Lithium Phosphate
O_2	Dioxygen
O_3	Ozone
e^-	Electron
ACU	Array Conditioning Unit
AM0	Air Mass Zero Spectrum
AOCS	Attitude and Orbit Control System
ARM	Advanced RISC Machine
BOL	Beginning Of Life
BPA	Battery Pack Array
CAN	Controller Area Network
CC	Constant-Current
CMOS	Complementary Metal Oxide Semiconductor
COM	Communication System
COTS	Commercial Off-The-Shelf
CPU	Central Processing Unit
CRC	Cyclic Redundancy Checker
CV	Constant-Voltage

DC/DC	Direct Current to Direct Current
DD	Displacement Damage
DET	Direct Energy Transfer
DET	Detection Rank Number
DOD	Depth Of Discharge
DSP	Digital Signal Processing
ECC	Error-Correcting Code
EPS	Electric Power System
ESA	European Space Agency
ESM	Error Signaling Module
ESR	Equivalent Series Resistance
FMECA	Failure Modes, Effects and Criticality Analysis
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GPIO	General Purpose Input/Output
GPS	Global Positioning System
I-V	Current-Voltage
I^2C	Inter-Integrated Circuit
I/O	Input and Output
ISL	Inter-Satellite Link
ISS	International Space Station
LDO	Linear Drop-Out
LEO	Low Earth Orbit
MCU	Micro-Controller Unit
MIPS	Million Instructions Per Second
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
MPU	Memory Protection Unit
MTBF	Mean Time Between Failure
NASA	National Aeronautics and Space Administration

OBC	On-Board Computer
OCC	Occurrence Rank Number
OP	Operating Point
OS	Operating System
P&O	Perturb and Observe
PCB	Printed Circuit Board
P-V	Power-Voltage
PCDU	Power Control and Distribution Unit
PDU	Power Distribution Unit
PPT	Power Point Tracking
PV	Photovoltaic Panel
PWM	Pulse Width Modulation
RAM	Random Access Memory
RC	Resistor-Capacitor
RHA	Radiation Hardened Assurance
RISC	Reduced Instruction Set Computer
RPN	Risk Priority Number
SEB	Single-Event Burnout
SEE	Single-Event Effect
SEFI	Single-Event Functionality Interrupt
SEGR	Single-Event Gate Rupture
SEI	Solid Electrolyte Interphase
SEL	Single-Event Latchup
SET	Single-Event Transient
SEU	Single-Event Upset
SEV	Severity Rank Number
SOC	State Of Charge
SPI	Serial Peripheral Interface
SSO	Sun Synchronous Orbit
THERM	Thermal Management System
TID	Total Ionizing Dose
UHF	Ultra High Frequency
USB	Universal Serial Bus
VHF	Very High Frequency

List of Symbols

η	Power conversion efficiency of solar cell	[%]
η_{conv}	DC/DC converter efficiency	[%]
η_{panel}	Conversion efficiency of solar cell	[%]
$\hat{N}$	Solar Panel normal unit vector	[−]
$\hat{S}$	Spacecraft-Sun unit vector	[−]
λ	Wavelength of electromagnetic wave	$[m]$
ρ	Angular response	[−]
θ	Angle between $\hat{N}$ and $\hat{S}$	$[rad]$
A	Area of solar panel	$[m^2]$
A_S	Reference dark current	$[A \cdot K^{-\frac{3}{2}}]$
$A_{eff,avg}$	Average effective area of solar panel	$[m^2]$
B_λ	Solar irradiance	$[W \cdot m^{-3}]$
c	Speed of light	$3 \times 10^8 \quad [m \cdot s^{-1}]$
C	Capacitance value	$[F]$
C_{nom}	Nominal battery pack capacity	$[A \cdot h]$
D	Duty cycle	[%]
DT	Dead Time Ratio	[−]
E	Photon energy	$[J]$
E_g	Material band gap	$[eV]$
$E_{b,discharge}$	Discharge battery energy	$[J]$
$E_{b,max}$	Maximum battery energy	$[J]$
E_L	Load energy	$[J]$
E_{max}	Maximum energy	$[J]$
ESR_C	ESR of capacitor	[Ω]
ESR_L	ESR of inductor	[Ω]

f_{sw}	MOSFET switching frequency	$[Hz]$
FF	Fill factor	$[-]$
G	Solar constant outside atmosphere	1353 $[W \cdot m^{-2}]$
h	Planck Constant	6.626×10^{-34} $[m^2 \cdot kg \cdot s^{-1}]$
I	Electrical current	$[A]$
I_0	Dark current	$[A]$
I_D	Current flowing in the semiconductor	$[A]$
I_b	Current flowing in battery pack	$[A]$
$I_{cap,RMS}$	RMS current flowing across capacitor	$[A]$
$I_{L,max}$	Maximum load current	$[A]$
I_L	Load current	$[A]$
$I_{mp,nom,sa}$	Solar array current at MPP	$[A]$
I_{mp}	Maximum Power current	$[A]$
I_{OC}	Open-circuit current	$[A]$
$I_{par,sa}$	Current flowing in one solar network	$[A]$
I_{SC}	Short-circuit current	$[A]$
I_{SH}	Shunt current	$[A]$
J_{mp}	Maximum Power current density	$[mA \cdot cm^{-2}]$
J_{ph}	Photon flux	$[A \cdot m^{-3}]$
k_B	Boltzmann Constant	1.38×10^{-23} $[m^2 \cdot kg \cdot s^{-2} \cdot K^{-1}]$
L	Inductance value	$[H]$
M_{gen}	Safety margin on power generation	$[-]$
n	Ideality factor of solar cell	$[-]$
$n_{cell,b}$	Total number of battery cell	$[-]$
$n_{par,b}$	Number of battery cell in parallel	$[-]$
$n_{par,sa}$	Number of solar cell in parallel	$[-]$
$n_{ser,sa}$	Number of solar cell in series	$[-]$
P	Electrical power	$[W]$
P_b	Power to battery pack	$[W]$
P_C	Power losses in capacitor	$[W]$

P_D	Power losses in diode	$[W]$
P_{in}	Input solar power	$[W]$
P_I	Power losses in inductor	$[W]$
$P_{loss,b}$	Power losses in battery pack	$[W]$
$P_{loss,sa}$	Power losses in solar array	$[W]$
P_l	Power to load converters	$[W]$
P_L	Load power	$[W]$
P_{max}	Maximum power	$[W]$
P_{MOS}	Power losses in MOSFET	$[W]$
P_{sa}	Power generated by solar array	$[W]$
P_s	Power from solar converters	$[W]$
q	Electron charge	1.6×10^{-19} $[C]$
Q_g	MOSFET gate capacitance	$[F]$
R_S	Series resistance	$[\Omega]$
$R_{ds,on}$	On-state conduction resistance of MOSFET	$[\Omega]$
R_{int}	Internal impedance of battery cell	$[\Omega]$
R_L	Load resistance	$[\Omega]$
R_{SH}	Shunt resistance	$[\Omega]$
T	Temperature	$[K]$
t_{rr}	MOSFET transition time	$[s]$
T_{sw}	MOSFET switching period	$[s]$
V	Voltage	$[V]$
V_D	Voltage across the semiconductor	$[V]$
V_T	Threshold voltage	$[V]$
$V_{b,nom}$	Nominal battery pack voltage	$[V]$
$V_{cell,b}$	Battery cell voltage	$[V]$
$V_{cell,sa}$	Solar cell voltage	$[V]$
V_F	Forward voltage of diode	$[V]$
V_{gs}	MOSFET Gate-to-Source voltage	$[V]$
V_{in}	Input voltage	$[V]$
V_L	Load voltage	$[V]$
$V_{mp,nom,sa}$	Solar array voltage at MPP	$[V]$
V_{mp}	Maximum Power voltage	$[V]$
V_{OC}	Open-circuit voltage	$[V]$
V_{out}	Output voltage	$[V]$
$V_{sw,max}$	Maximum voltage at switching node	$[V]$

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Chapter 1

Introduction

In recent years, CubeSats gain in popularity among researchers due to their cheapness and lightweight allowing them to conduct space researches and missions for competitive prices. These satellites are mostly launched in low earth orbit where regular eclipses, experienced by the spacecraft, challenges the satellite developers in the design of efficient and reliable power supplies.

Satellite designers are usually committed to purchasing commercial off-the-shelf (COTS) power supplies as it represents a time-saving choice. Although space electronic companies provide generic products with a wide range of features despite moderate efficiency, the goal being to supply a larger customer market. Mission-specific power supplies represent an alternative but are time consuming and more complex than purchasing ready-to-use products. However, the results are significant with this method that improves the satellite efficiency and at last reduces production cost. Therefore, a procedure for designing mission-specific power supplies is crucial to cut the development time. The design of such supplies is the topic of this work.

This master thesis has been realized in collaboration with Aerospacelab. The Walloon start-up was founded in 2017 by Benoît Deper. The company is located in Mont-Saint-Guibert, Belgium and is relentlessly aiming at revolutionize space surveillance by launching 5 satellites prior to 2021.

First, theoretical information about satellite operation basics will be provided along with explanations on solar panels and electrochemical batteries. Next, the main focus of this work is the study and optimization of the power supply of a CubeSat. Particular attention is given to the sizing of power generation and storage cells, study of power losses and optimization of the system. Finally, we propose a system implementation with a special attention to the analysis of potential failures.

Chapter 2

CubeSat Technology

2.1 Definition of CubeSat

The CubeSat is the most common type of nanosatellite currently used in space applications. The nanosatellite is a category of satellite whose weight is comprised between 1 and 10kg. Other types of nanosatellite do exist which are topics of scientific researches, therefore they are still in their development phase and not yet suitable for space missions. Among these emerging types of nanosatellite, we can mention the PocketQube, TubeSat or even SunCube.

Figure 2.1: Illustration of a CubeSat orbiting in space [3]

CubeSats are in fact composed of square-shaped units which are attached together to form a complete nanosatellite. The CubeSat unit is then a cube whose dimensions are $10cm \times 10cm \times 10cm$ and whose weight per unit does not exceed 1.33kg. Typical arrangement of CubeSats ranges between 1U to 6U or even more for considerable missions. The number of unit is selected based on a multitude of parameters such as the cost limit, maximum weight, payload size and more.

Typically, engineers use COTS electronic devices and even structures elements in order to simplify the design procedure and reduce drastically the development time. These COTS components are frequently fabricated in large production volumes, their costs are then highly reduced.

For larger satellites, launch costs represent a large proportion of the total mission cost. But CubeSats overcome this drawback due to their light-weight and low volume characteristic. As a result, CubeSats are preferred by universities, states and private companies. CubeSats are deployed on their orbit by either being dispatched from the International Space Station (ISS) by conveyors or being launched as secondary payloads in rockets which have extra room for secondary payloads.

Figure 2.2: CubeSat launched from the International Space Station [4]

CubeSats became popular thanks to advances in miniaturization of electronic devices and their capabilities to perform commercial missions that were previously done by more expensive microsatellites. CubeSats can be launched individually or they can become part of a satellite swarm achieving a more complex task. CubeSats can achieve a wide range of missions which can be subdivided into different classes:

- Technology demonstration: The space environment is the ultimately harsh environment in order to test the reliability and good operation of a technology. CubeSats can be used to test instruments, materials and actuators.
- Science: CubeSats are preferred for scientific experiments and measurements on various topics such as biology, physics, electronics, etc.
- Educational projects: In several universities, graduate students can design, develop, test and operate CubeSats in orbit. Such projects are important to educate and train the upcoming satellite designers.

- Commercial applications: CubeSat is a cheap and reliable way to implement and deploy a commercial technology such as telecommunication or Earth observation.

Another advantage of CubeSats is that they do not result in space debris upon mission completion. CubeSats will be burnt up in the atmosphere upon re-entry as they are low weight facilitating the disintegration of its structure at the end of its life. On the other hand, CubeSats have two main drawbacks which are the restricted scope of missions due to their low volume and the limited mission duration. In fact, CubeSats are usually intended to have a maximum lifetime of around 3 to 12 months as they usually do not incorporate a propulsion system.

An important aspect of CubeSat space operation is the type of orbits. The altitude of the orbit will impact the measurement precision and also the failure occurrence rate as the electromagnetic shield of the Earth has a reduced impact at higher altitude. The speed at which the satellite is moving in the orbit, the trajectory angle of the satellite over the Earth, the area that the satellite can observe and the frequency at which the satellite can observe certain area are also important factors when selecting an orbit.

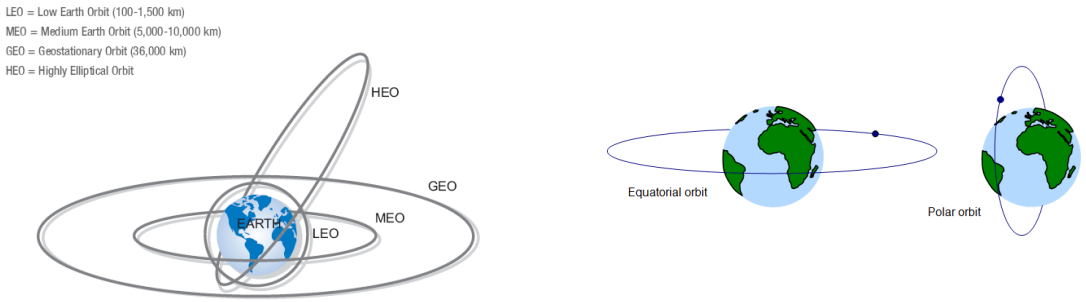

Figure 2.3: Type of Earth orbits [5]

The Earth orbits can be divided in multiple types depending on altitude and inclination as it is represented in figure 2.3. CubeSats are typically launched in Low Earth Orbit (LEO) as telecommunications and Earth observation is more efficient at lower altitude. LEO can also be subdivided into several types depending on orbit inclination. Equatorial orbits are used for telecommunications, weather monitoring and surveillance while polar orbits for Earth observation and mapping. We can note that special orbit exists such as the Sun synchronous orbit (SSO) which is a special case of polar orbit where the satellite passes over the same region at the same time every day making it optimal for certain region observation.

2.2 Main modules of CubeSats

In this section, we will explore the different modules necessary for the operation of CubeSats in space and the basic inner working of these modules inside the satellite. Finally, we will investigate the different state-of-art power systems available on the market.

CubeSats are composed of multiple modules each of which have unique functions crucial for the good progress of the assigned mission. The main functions are:

- Manage satellite state (OBC)
- Maintain trajectory (AOCS)
- Generate electrical power (EPS)
- Maintain an operating temperature (THERM)
- Transmit data to and from Earth (COM)
- Accomplish the intended mission (PAYLOAD)

Each function and the corresponding module are explored beneath except from the payload that accomplish the intended mission. The payload is mission-specific and can be devoted for telecommunication, scientific research, surveillance or navigation. A global satellite schematic with the main modules is represented in figure 2.4.

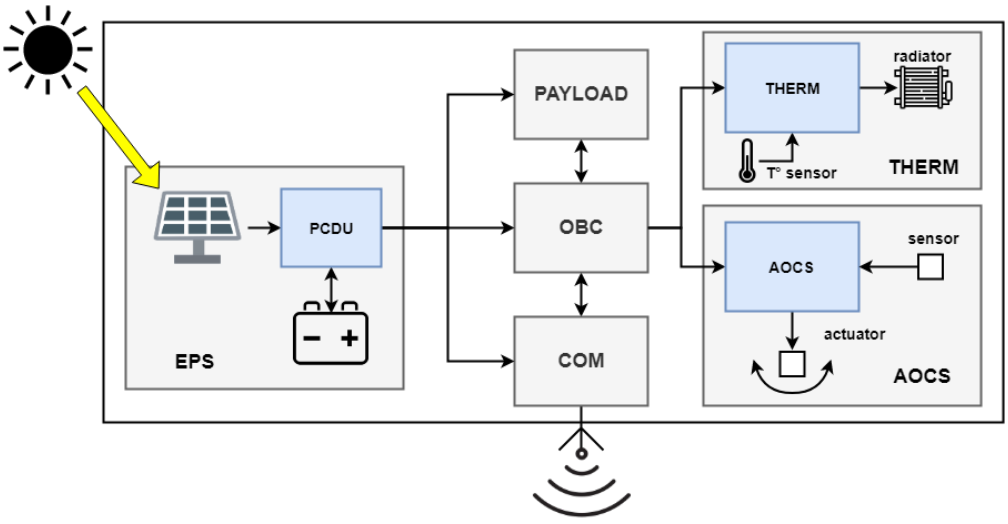

Figure 2.4: Satellite modules block diagram

2.2.1 On-Board Computer

The most important module in a CubeSat is the On-board Computer (OBC) which is responsible for data and command handling. The OBC is typically composed of one primary computer and multiple secondary computers. The primary computer is used for the delegation of tasks to secondary computers, controlling the Attitude and Orbit Control System (AOCS), scheduling task and operation, and activation of Thermal Management System (THERM). While the secondary computers are used for controlling the other modules of the CubeSats such as the Electric Power System (EPS), the Communication System (COM) and eventually the payload.

The computers in the OBC can be implemented by either a Micro-Controller Unit (MCU) or Field Programmable Gate Array (FPGA) as these systems can embed a large variety of processor cores. Typically processors cores are implemented using the Advanced RISC Machine (ARM) family architecture which is characterized by a high power efficiency. These computing systems should be highly power and mass efficient as the CubeSats are volume and mass restricted.

The computers should also have a large variety of Input and Output (I/O) to easily interface with the other subsystems. Typical I/O's are Universal Serial Bus (USB), Controller Area Network (CAN), as well as Inter-Integrated Circuit (I^2C) interfaces and Serial Peripheral Interface (SPI).

Rockets payloads undergo harsh conditions during the climbing phase, they are subject to vibrations and shocks. Therefore, the OBC should be shock- and vibration-resistant so that the satellite is fully functional after the take-off phase. The OBC should also be functional under the vacuum conditions of space.

During orbital phase, satellites are no more protected by the electromagnetic field of the Earth, then they are subject to electromagnetic radiations coming from the Sun that can produce glitches and bugs in electronic systems. They are several ways to deal with these radiations: make the OBC radiation-resistant or use triple redundancy to detect and resolve radiation induced glitches.

Satellites that are orbiting around the Earth will undergo cycles with sunlight and eclipse which are characterized by extremely different temperature even with a thermal management system. In eclipse, the temperature can drop to -40$°C$ while in sunlight, the temperature can rise up to +80$°C$. The OBC should be fully functional over this range of temperature without large drop of performance.

2.2.2 Attitude and Orbit Control System

Another important subsystem is the attitude and orbit control system which is responsible for controlling the orientation of the CubeSat and its orbital trajectory. It is really important to control the attitude so that we can orient the solar array for optimal power generation, orient the antennae towards the Earth for data transmission to and from the Earth and finally for operating the instruments of the payload. A typical AOCS diagram is represented in figure 2.5.

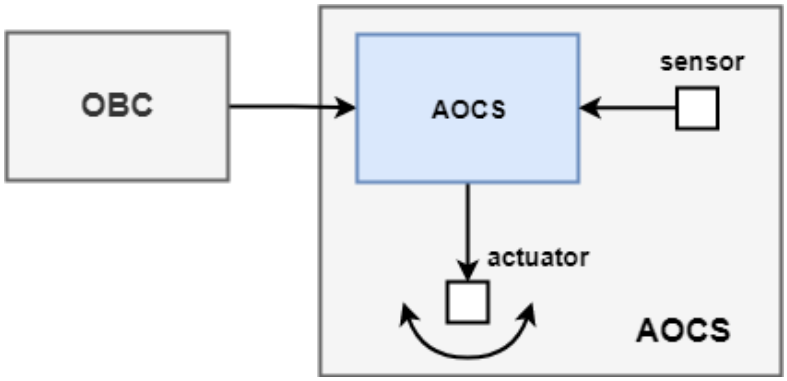

Figure 2.5: Typical diagram of the Attitude and Orbit Control System

The first step in controlling the attitude and is to determine the actual attitude through the use of sensors. Multiple sensors exists commercially such as the Earth sensor which is a thermopile sensor that determines the attitude based on the position of the Earth, the Sun sensor is based on the same principle but it will determine the attitude with respect to the Sun. We have also the angular rate sensor which determines the attitude based on angular rate measurements. The Star tracker is an attitude sensor which is based on the recognition of stars.

The second step in attitude control is the actuation to change the attitude of the satellite to the desired value. These actuators are either characterized by accuracy or efficiency, then CubeSats are typically designed with a combination of actuators to obtain the best of each actuator type. Reaction wheels and thrusters are characterized by a high efficiency but they have a lack in accuracy. We typically coupled them with magnetorquers which will align itself with respect to the magnetic field of the Earth enabling an accurate attitude control. Reaction wheel is a spinning flywheel that will change the attitude while thrusters are propulsive devices that expels propellant through a nozzle to produce momentum.

As CubeSats are volume restricted, they typically do not incorporate a propulsion device for orbit control but we can list the different alternatives for propulsion implementation. Propulsion systems are subdivided into two main classes which are chemical propulsion systems using propellant to produce thrust and electrical propulsion systems which used electric power to produce momentum. We can also note new emerging propulsion systems such as the solar sail that uses the solar wind to produce momentum.

2.2.3 Thermal Management System

Next important module in CubeSat is the thermal management system which is essential for the survival of the electronic devices. During an orbital cycle, the electronic devices are subject to large variations of temperature so we need to accurately control the temperature of components such as the OBC and the EPS that are critical for good operation of the mission. Thermal management systems are either passive or active and they are typically used in combination. A typical thermal management system diagram is represented in figure 2.6.

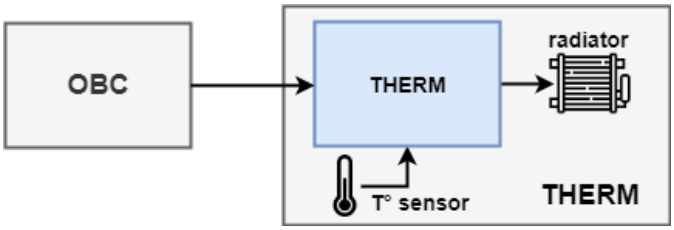

Figure 2.6: Typical diagram of Thermal Management System

Passive thermal systems do not require input power to be functional, they are also low cost, volume, weight and safety-proof. Thermal insulation and coating is implemented by applying a material on the CubeSat in order to modify its thermal characteristics. We can mention sunshields used to reduce heat absorbed from the sun while deployable radiators are used to dissipate thermal heat. We can also mention thermal straps and heat pipes as alternatives

While the active thermal systems do indeed use input power to operate, they are more precise and more efficient than their passive counterparts. Typically, active thermal systems are used for temperature critical devices such as the batteries, cameras and electronics. We can name electric heaters which consists in electrical resistors that produce heat upon current flow through it. Microcryocoolers are active devices used to precisely reduce the temperature of CubeSats. Active thermal straps do also exist, they are similar to the passive ones except that they require input power to regulate the temperature.

2.2.4 Communication System

The main mission of nanosatellites consists in making measurements in space and send the results back to Earth, therefore the Communication system is an important module of the CubeSat. The COM system is responsible for transmitting data and telemetry to Earth, receiving commands from Earth and eventually relay data to another spacecraft through Inter-Satellite Link (ISL).

The COM system is composed of two main modules which are the communication computer for Digital Signal Processing (DSP) operation and the antennae for data transmission. The main parameter of the communication system is the transmission band. This band is a trade-off between data rate and power. For instance, higher frequency bands are characterized by larger data bandwidth but it consumes more power and requires more complex geometry for antennae to be effective leading to higher cost.

The most reliable and mature bands are the UHF and VHF band characterized by relatively low frequencies, low transmission power and a low data rate. L-band and S-band are also a commercially mature technology but they do not have a lot of flight heritage. They are characterized by intermediate data rate and low power consumption. We can also mention Ku-band, K-band and Ka-band which are new emerging communication technologies characterized by a high data rate but higher transmission power and more complex antennae geometry. All these bands are represented here below in figure 2.7 with their corresponding frequency range.

Figure 2.7: Radio spectrum for satellite communication [6]

The antennae have a large variety of geometry such as patch antennae or whip antennae which are cheap antennae but only suitable for low data rate. While other more complex geometries do exist such as the high gain antennae essential for data transmission in Ku-band and higher. We can also mention new trends in nanosatellites that are based on multi-band communications which is made possible through the use of FPGA for the complex signal modulation and demodulation. This trend allows to have a higher data rate with low frequency bands.

2.2.5 Electric Power System

The EPS is the main module of the satellite as its function is the supply of reliable and continuous power to all the other modules of the CubeSat. Then, it is responsible for the power generation, storage and distribution of the electric power. Power generation is typically managed by solar panels, power storage by rechargeable batteries and the distribution of power is managed by the Power Control and Distribution Unit (PCDU). The block diagram of typical EPS architecture is represented on figure 2.8 along with the main modules constituting the system.

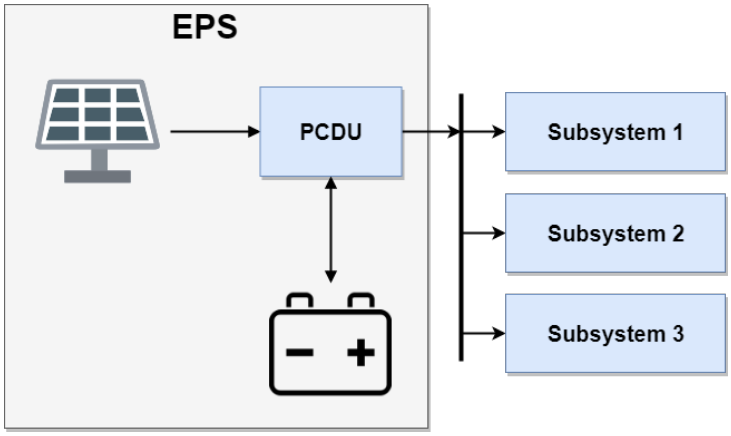

Figure 2.8: EPS standard block diagram

In nanosatellites, power generation is performed by solar cells arranged in a solar array. This way of doing is a reliable and secure means to generate power compared to nuclear power generation as it presents huge risks during the take-off and orbital phases. The main limitation of solar arrays is that there is no power generated when the satellite is in eclipse. Therefore we need a power storage system to supply the other modules of the CubeSat when no direct power is generated. We can also mention that solar arrays are high volume and high weight increasing the launch cost and also reducing the effectiveness of the AOCS.

It is well known that the Earth generates a magnetic field affecting the solar spectrum intercepted at sea-level while the solar spectrum in space is left unperturbed due to a lack of magnetic shield outside the atmosphere. Therefore, the solar spectrum in space can be assimilated to the spectrum of a black body allowing a larger portion of solar power to be extracted. Consequently solar cells used in space applications are different from the one used in typical solar arrays on Earth.

Multi-junction cells are preferred in space applications because of their higher efficiency-to-cost ratio extracting power over a larger range of wavelength. These cells are more expensive than single-junction cells but are generally preferred in space applications where reducing the volume and the mass of the satellite is crucial. Four-junction solar cells already exists but the technology is not yet mature for space applications and they are way too expensive for low cost missions. The differences between single-junction and multi-junction solar cells are explained in depth in section 3.3.

Researchers are continuously working on improving the efficiency of solar panels with state-of-the-art manufacturing technologies. Triple-junction cells are typically preferred in space applications and are widely used among satellite designers due to the good trade-off that they exhibit.

Figure 2.9: Technicians stow for launch a solar array on NASA's Juno spacecraft [7]

The role of power storage is to provide power to the subsystems during the eclipse when no power is generated from the solar array. Electrochemical batteries are the most common power storage technology because they encompass a high power density and high energy density compared to other technologies such as fuel cells, super-capacitors and others. Non-rechargeable batteries can be used for short duration missions, but in most missions, rechargeable batteries are usually used.

For space applications, Lithium-ion batteries are preferred due to their low cost, high capacity, higher energy density in volume and in weight. Lithium-phosphate and Lithium-polymer batteries are emerging technologies but they present drawbacks such as higher cost, no flight heritage and not yet mature for space applications. The Li-ion batteries comes in a wide variety of shape and capacity as represented in figure 2.10.

Figure 2.10: Lithium-Ion (Li-ion) battery with capacities ranging from 200 to 2800mAh [8]

Finally, the last EPS module is the PCDU which is responsible for controlling and distributing the power to the loads. They are two main regulation topologies which are Direct Energy Transfer (DET) and Power Point Tracking (PPT).

In DET topology as seen in figure 2.11, the power from the solar panel is directly transferred to the battery bus. To regulate the bus power to the desired value, a shunt regulator dissipates any excessive power as heat, introducing thermal design challenges. A blocking diode is necessary on the battery bus to prevent the battery from discharging during the eclipse. The battery regulator aims to charge the batteries with a constant current during sunlight and to control the discharge current of the batteries during the eclipse. The Power Distribution Unit is used to supply the loads with the corresponding electrical ratings.

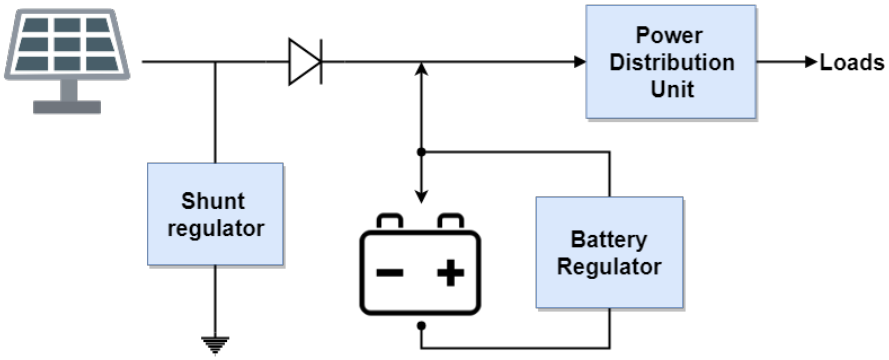

Figure 2.11: Typical DET block diagram

While a PPT system aims to extract the maximum power from the solar array and hence dissipate very little power internally, the architecture of such topology is show in figure 2.12. The PPT regulator sets the operating point of the solar array in such a way that it maximizes the generated power following a Maximum Power Point Tracking (MPPT) algorithm. This topology increases the system efficiency and side-steps the potential thermal dissipation problems occurring in DET regulation system.

When the batteries are fully charged, the regulator sets the operating point away from the Maximum Power Point (MPP), towards the open circuit condition. It leaves the energy from the sun as heat in the solar array itself preventing thermal problems in the electronic devices. Another advantage of PPT approach is that the batteries are directly connected to the loads maximizing the system efficiency during the eclipse.

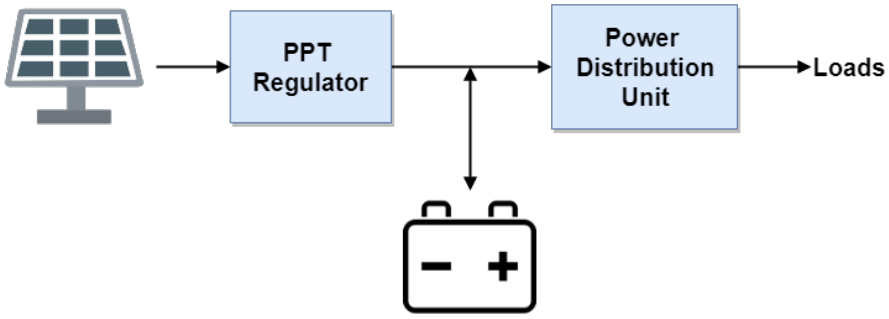

Figure 2.12: Typical PPT block diagram

2.3 Electric Power System State-of-the-Art

Now, we will explore the state-of-the-art power systems available in the market. Important features in such systems are the number of input channels for the solar panels with corresponding voltage and current ratings, the number of output buses with availabilities in voltage and current ratings, and also the regulation topology for controlling the operating point of solar array.

Here below, we listed several products from companies such as GomSpace, Clyde Space, EnduroSat and Crystal Space. We constructed a comparative table of these products in order to have an overview of key features of state-of-the-art EPS and we provided illustrations of some of these products.

Product	**GomSpace NanoPower P31u [9]**	**GomSpace NanoPower P60 [10]**	**Crystal Space P1u Vasik [11]**	**EnduroSat CubeSat Power Module II [28]**	**Clyde Space FlexU EPS [12]**
# PV input channels	3	6	1	6	9
Max. power	30W	64W	10W	300W	100W
Regulated outputs	3.3V, 5V	3.3V, 5V, 12V and others	3.3V, 5V, 12V	3.3V, 5V, 12V	3.3V, 5V, 12V
# output switches	6	9	6	3	10
MPPT	✓	✓	✓	✓	✓
Battery included	✓	×	✓	✓	×
Features	Battery protection	3 buck converters	Critical components doubled	Custom 6-12V bus	Battery protection

Table 2.1: Comparative table of state-of-the-art EPS

GomSpace NanoPower P31u (see figure 2.13): Conceived for critical space applications with limited resources[9].

Figure 2.13: GomSpace NanoPower P31u [9]

GomSpace NanoPower P60 (see figure 2.14): Consists of motherboard, ACU and PDU [10].

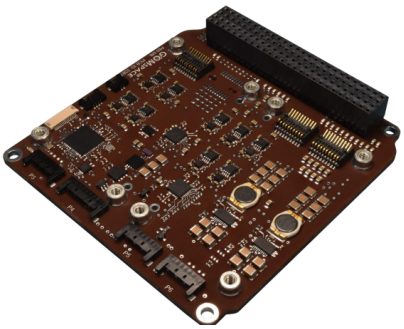

Figure 2.14: GomSpace NanoPower P60 [10]

Crystal Space P1u Vasik (see figure 2.15): conceived for densely packed 1U and 2U CubeSats [11].

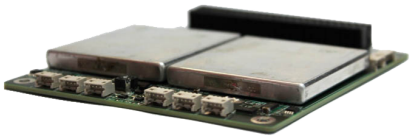

Figure 2.15: Crystal Space P1u Vasik [11]

Clyde Space 3rd Generation FlexU EPS (see figure 2.16): offers experience and flight heritage over numerous missions [12].

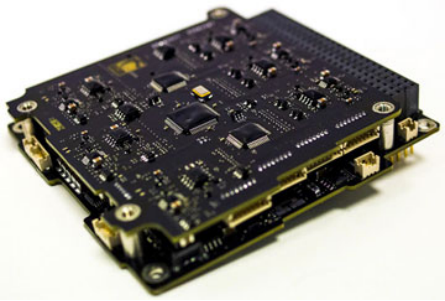

Figure 2.16: Clyde Space 3rd Generation FlexU EPS [12]

Chapter 3

Power Generation

As explained in the previous chapter about the EPS module, we concluded that the most reliable way to harvest electrical power is through the use of solar panels. In this section, we will explore the origins of solar power, the conversion from solar to electrical energy, some semiconductors basics to develop an electrical model, an analysis of the behavior of the solar panels and the angular response of these panels. Finally, the last section describes typical algorithms for controlling the solar panels and extracting electrical power.

3.1 Solar energy

It had been demonstrated that the Sun can be classified as a black body meaning that it will emit electromagnetic radiation called black-body radiation. In order to determine the solar spectrum, scientists developed an analytical model for describing the emission of black-body radiation. This analytical model is called the Planck's law and it describes the spectral density of electromagnetic radiation emitted by a black body at a given temperature. The solar irradiance B_λ of a body with respect to the wavelength λ is given by:

$$B_\lambda(\lambda, T) = \frac{2hc^2}{\lambda^5} \cdot \frac{1}{e^{\frac{hc}{\lambda k_B T}} - 1} \qquad [W \cdot m^{-3}] \tag{3.1}$$

where

- h is the Planck constant
- k_B is the Boltzmann constant
- c is the light speed
- T is the temperature of the black body
- λ is the wavelength of electromagnetic wave

The spectrum of the Sun outside the atmosphere is known as the Air Mass Zero Spectrum (AM0). Due to the lack of electromagnetic attenuation in vacuum, the solar spectrum in space closely matches the spectrum of a black body radiator at the temperature of 5778K. The figure 3.1 compares the spectrum of a black body at the temperature of 5778K with the one measured outside the atmosphere and at sea level.

We can observe in figure 3.1 that the solar spectrum at sea level is attenuated compared to the one measured outside the atmosphere. The difference in spectrum can be explained by the fact that some wavelengths will be attenuated when entering the Earth's atmosphere. For instance, we can observe multiple drops in the solar spectrum called the atmospheric absorption bands that represent the absorption of certain wavelengths by molecules present in the atmosphere. For example, low wavelength radiations (<250nm) will be absorbed and therefore attenuated by molecules of ozone (O_3). We can also mention other molecules such as O_2, H_2O, CO_2 that will also absorb radiation but in other wavelength ranges.

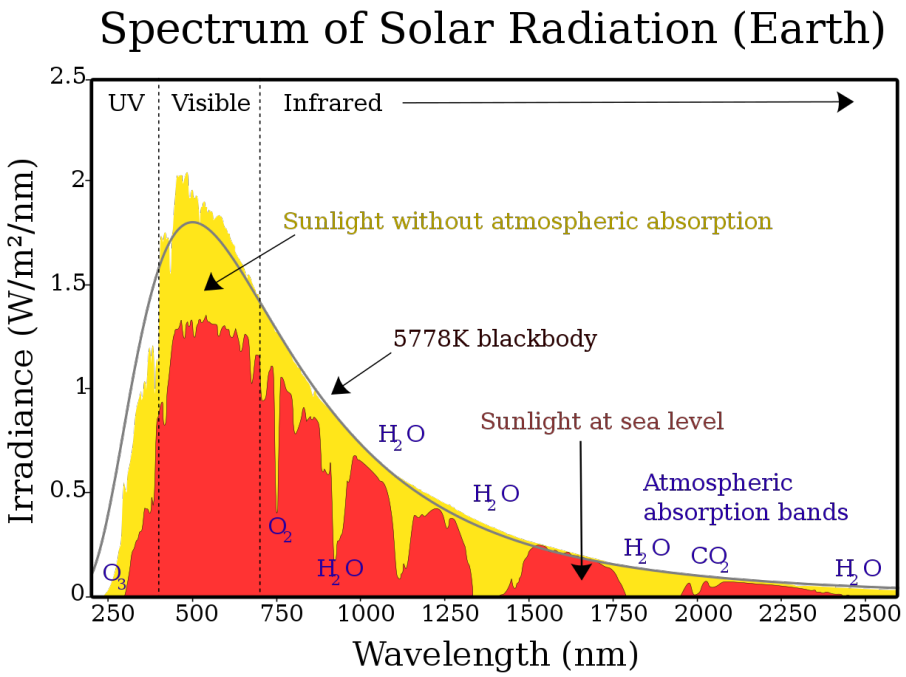

Figure 3.1: Spectrum of solar irradiance outside the atmosphere and at sea level [13]

We can integrate the solar spectrum in order to obtain the solar constant which is the amount of incoming electromagnetic radiation per unit of area that would be incident on a plane perpendicular to the sun rays. The solar irradiance has been measured to be roughly $1353W/m^2$ in space compared to $1000W/m^2$ at sea level. Therefore, the solar panels can absorb more energy outside the atmosphere than at sea level resulting in different technologies.

To further understand the behavior of the Sun's radiation, we will investigate the energy of these radiation and hence we introduce the notion of photon. The photon is a type of elementary particle which is the quantum of the electromagnetic field including the electromagnetic radiation. Therefore the energy of electromagnetic wave can be determined by the energy of the photon.

The photon energy E is given by:

$$E = \frac{hc}{\lambda} \qquad [J] \tag{3.2}$$

Furthermore, we can express the photon energy in eV for clarity purposes and draw the figure 3.2. We can observe that the low wavelength photons carry more energy than higher wavelengths photon. This result implies that low wavelength photons are the most important photons when it comes to solar power generation.

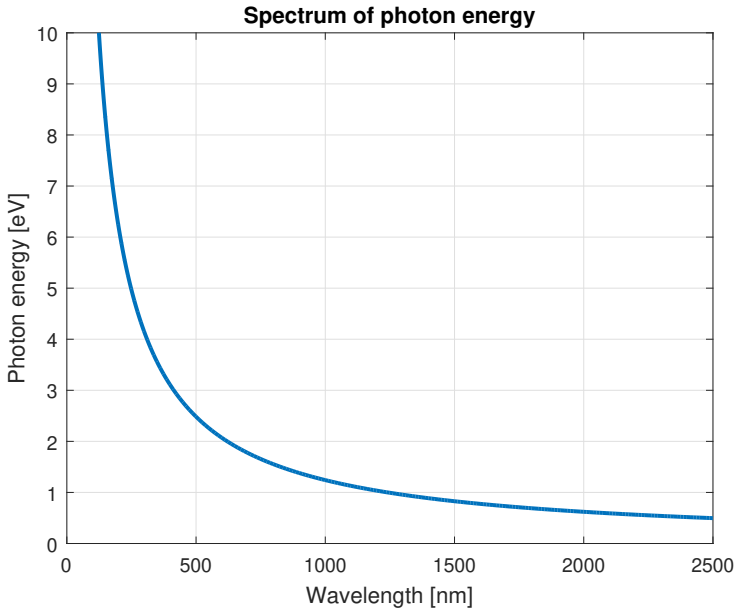

Figure 3.2: Spectrum of photon energy

Finally, we can investigate the photon flux which is in fact the number of photons that an incident surface normal to the Sun will intercept. By inspecting the profile of the solar irradiance and the one of the photon energy, we can predict that the photon flux will not be constant over the photon wavelength. As we can observe on figure 3.3, there is almost no photons that carry an energy greater than $E_{max} \approx 4eV$ which corresponds to a wavelength of approximately 300nm.

The photon flux J_{ph} is given by:

$$J_{ph} = q \cdot \frac{B_\lambda}{E} \qquad [A \cdot m^{-3}] \tag{3.3}$$

where

- q is the electrical charge

It is more convenient to quantify the photon flux in the equivalent units of electric current density because this photon flux will be equal to the electric current that a cell can deliver if it converts every photon into a free electron–hole pair.

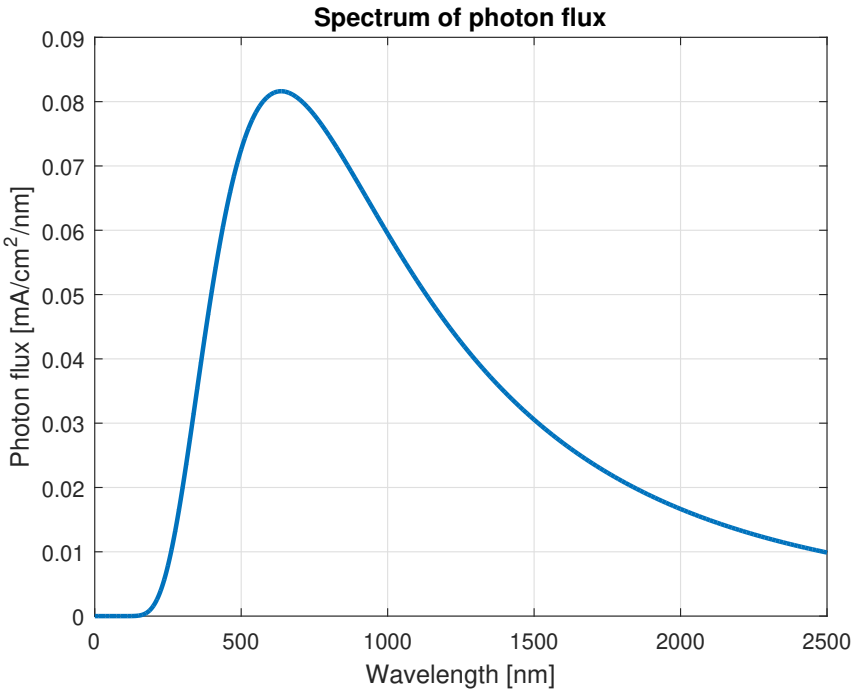

Figure 3.3: Spectrum of photon flux emitted by a black-body

3.2 From solar to electrical energy

In order to convert the electromagnetic waves into electrical energy, we will use the photovoltaic effect. The photovoltaic effect is the generation of a voltage and electric current upon exposition of a material to light. This generation of electric power occurs only when the light is absorbed by the material. Materials that exhibits a strong photovoltaic effect are semiconductors such as Silicon and Germanium.

The state-of-the-art solar cells are typically multi-junction solar cells which allows to increase the efficiency of conversion compared to single-junction solar cells. Multi-junction solar cells are in fact constructed by stacking multiple layers of different semiconductors on top of each other. For instance, the Spectrolab's XTJ Prime solar cells can achieve an efficiency of approximately 30.7%. The figure 3.4 shows the two types of configurations for constituting a solar array. The solar cells can be connected either in series or in parallel. The series connection has the property to sum up the voltage while the parallel connection leads to the summing of the currents.

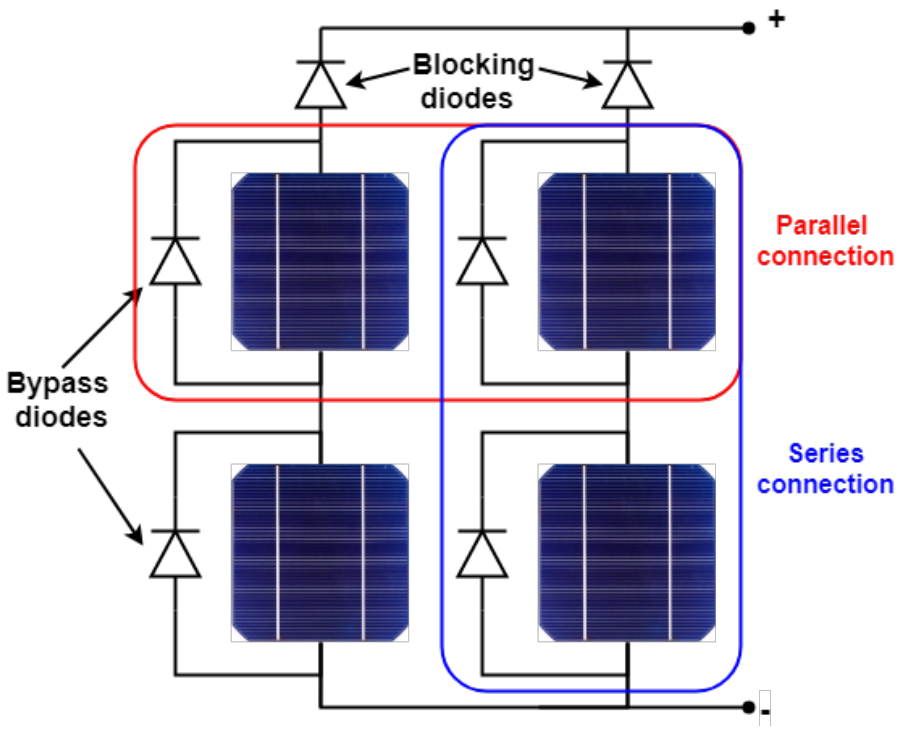

Figure 3.4: Typical configuration of solar cells constituting a solar array

In order to properly connect solar cells together, solar cells are mounted with bypass diodes that sit in parallel to the solar cells and blocking diodes that sit in series with the solar cells as represented in figure 3.4. The blocking diodes are used to prevent the current generated by other solar cells flowing back through a weaker, shadowed or damaged network and also to prevent the fully charged battery from discharging. While the bypass diodes are used in case of failure of solar cells. These diodes will allow to continue supplying power at reduced voltage rather than no power at all.

When sunlight hits solar cells, one of the 3 following event happens:

- The photon is reflected off the surface
- The photon passes straight through the material
- The photon is absorbed in the semiconductor material

The reflection is related to unfavorable incident angles and surface coating of the cells while the other phenomena are related to quantum mechanics. These quantum mechanics phenomena will be discussed deeper in the section 3.3 about the semiconductors basics while the reflection mechanisms will be discussed in section 3.5 about the angular response of a solar cell.

3.3 Semiconductors Basics

In order to understand the comportment of the photons when it is non-reflected by the surface, we make a detour to semiconductor basics. The electrons in a semiconductor are either in the valence band where the electrons are not free and are orbiting around the nucleus of an atom or in the conduction band where the electrons can circulate freely in the material. In between these 2 bands, there is a gap whose depth is determined by the material band gap (E_g). The energy band gap is a measure of the amount of energy required to free an outer shell electron from its orbit around the nucleus to a free conducting state. A semiconductor is defined as a material with $0 \leq E_g \leq 3eV$ at T = 300K. We can define then the voltage across a semiconductor:

$$V_D \approx \frac{E_g}{q} - 0.4V \tag{3.4}$$

where

- V_D is the voltage across the semiconductor
- E_g is the energy band gap

Multi-junction solar cells are constructed by stacking multiple different semiconductors materials on top of each others as we can see on figure 3.5. If a photon has insufficient energy to knock loose an electron in a layer, it will simply pass through the next layer. By placing the semiconductors in a descending order with respect to their energy band gap, the multi-junction solar cell achieves higher conversion efficiency due to the stack's collective ability to match the solar spectrum. In fact, the stacking of multiple semiconductors allows to intercept a larger range of wavelength at a higher efficiency as we can observe in figure 3.5.

Tunnel diodes (represented in light blue on the right schematic) are widely used for inter-connecting the n-p junctions otherwise parasitic p-n junctions will block the current flow across the solar cells. Tunnel junctions are highly doped p-n junctions which allow for quantum tunneling of the electrons. We can note that these tunnel diodes have a minor effect on the electrical behavior of the solar cell and therefore they will be neglected in the presented electrical behavior.

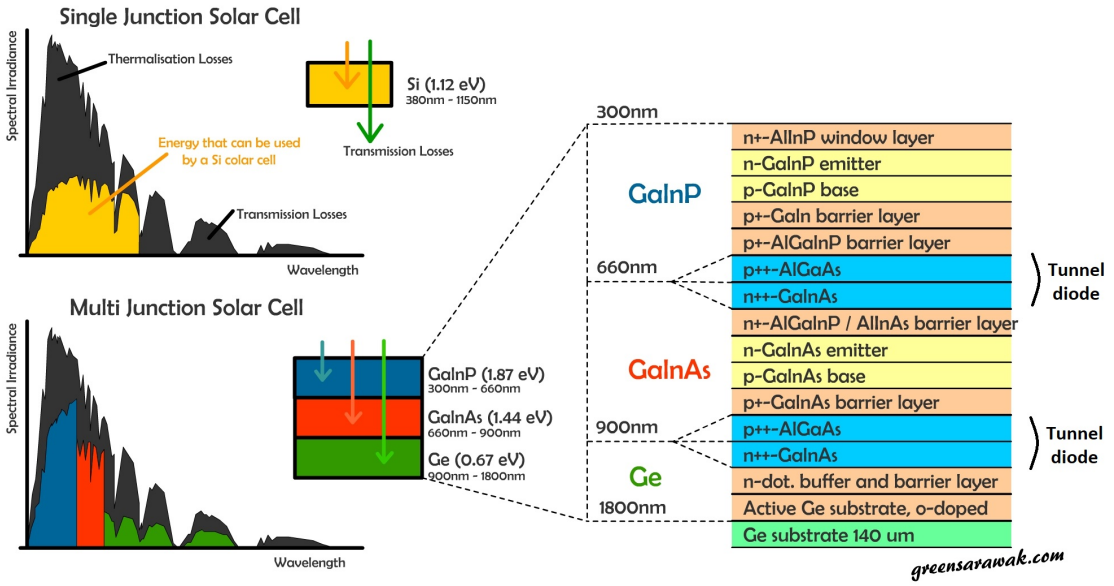

Figure 3.5: Comparison between single-junction and triple-junction solar cells [14]

3.4 Electronic behavior of a triple-junction solar cell

The model used ignored the effects such as the parallel non-ohmic current paths caused by recombination and other quantum mechanisms in order to remain simple in the system equations. As mentioned earlier, the effect of tunnel diodes are also neglected. The figure 3.6 represents the equivalent circuit of the electrical model of a triple-junction solar cell.

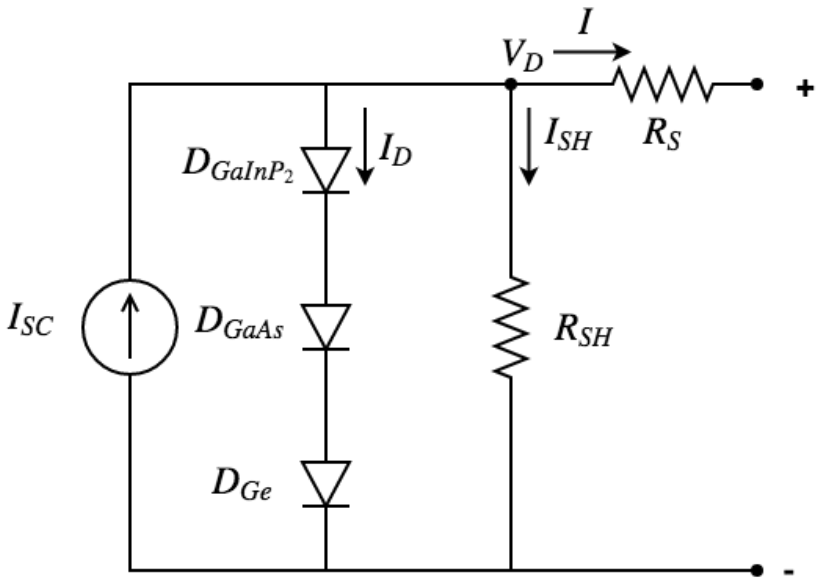

Figure 3.6: Equivalent circuit of the triple-junction solar cell

The solar cell acts as a constant current source shunted by diodes. The number of shunt diode is equal to the number of junctions in the solar cell while the current source is proportional to the photon flux intercepted by the solar cell. The internal resistance to the current flow R_S, is caused by the resistivity of the semiconductor material but also from the metal grid and contacts of the cell. The shunt resistor R_{SH} represents the leakage current across the junction. A high quality cell is therefore achieved if $R_{SH} \gg R_S$.

3.4.1 Short-circuit current

From the electrical model, we can compute and analyze the behavior of the solar cell. The system equations are obtained with Kirchhoff's current law:

$$\begin{cases} I & = I_{SC} - (I_D + I_{SH}) \\ I_{SH} & = \frac{V_D + R_S \cdot I}{R_{SH}} \end{cases} \tag{3.5}$$

Shockley diode equation:

$$I_D = I_0 \cdot \left[\exp\left(\frac{q(V_D + R_S \cdot I)}{n k_B T} \right) - 1 \right] \tag{3.6}$$

where

- n is the ideality factor
- $I_0 = A_S \cdot T^{\frac{3}{2}} \cdot \exp\left(\frac{-E_g}{2k_B T}\right)$

We can finally obtain the equation for the output current of the solar cell (figure 3.7):

$$I = I_{SC} - I_0 \cdot \left[\exp\left(\frac{q(V_D + R_S \cdot I)}{n k_B T} \right) - 1 \right] - \frac{(V_D + R_S \cdot I)}{R_{SH}} \tag{3.7}$$

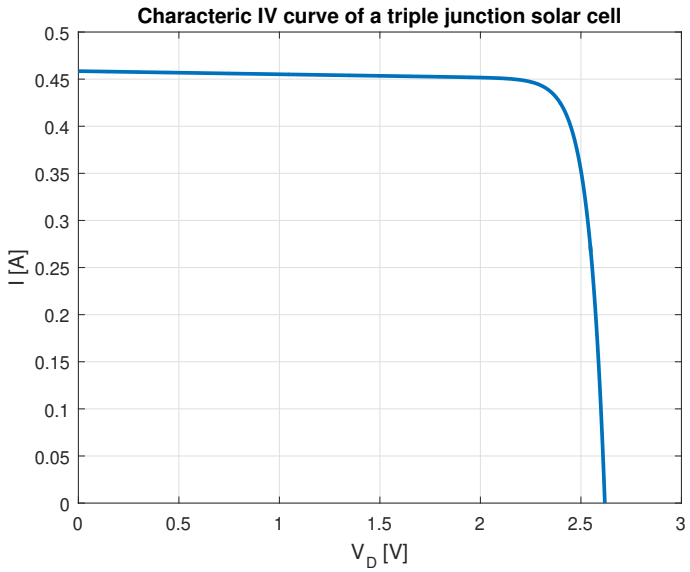

Figure 3.7: Characteristic I-V curve of a triple-junction solar cell

3.4.2 Open-circuit voltage

$$V_D = V_{OC} + I \cdot R_S \tag{3.8}$$

$$I = I_{OC} = 0 \tag{3.9}$$

$$\Rightarrow I_{OC} = I_{SC} - I_0 \cdot \left[\exp\left(\frac{qV_{OC}}{nk_BT}\right) - 1\right] - \frac{V_{OC}}{R_{SH}} = 0 \tag{3.10}$$

$$\Leftrightarrow V_{OC} = V_T \cdot \ln\left(1 + \frac{I_{SC}}{I_0}\right) \approx V_T \cdot \ln\left(\frac{I_{SC}}{I_0}\right) \tag{3.11}$$

$$\Leftrightarrow V_{OC} \approx \frac{k_BT}{q} \cdot \left(\ln I_{SC} - \frac{E_g}{k_BT}\right) \propto -T \tag{3.12}$$

From the equation of the open-circuit voltage, we can conclude that V_{OC} increases linearly with decreasing temperature, depends logarithmically on $\frac{I_{SC}}{I_0}$ ratio which depends on irradiance and is independent of the cell area as seen on figures 3.8 and 3.9.

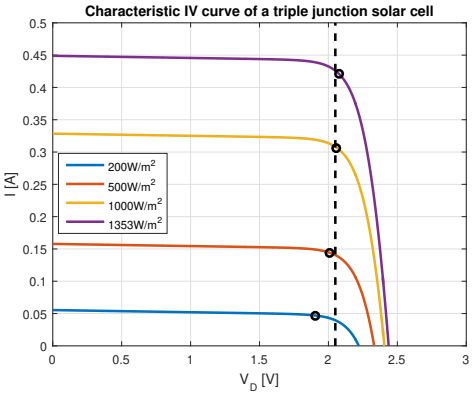

Figure 3.8: Characteristic I-V curve with different solar irradiances with constant junction temperature of $+28°C$

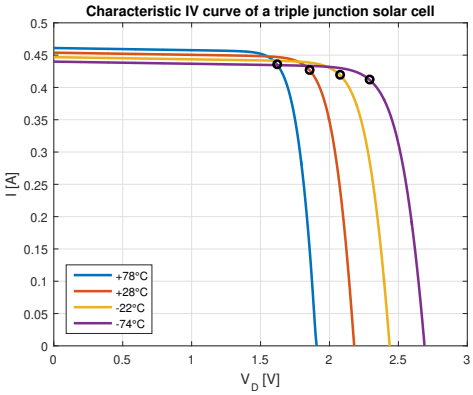

Figure 3.9: Characteristic I-V curve with different junction temperatures with constant irradiance of $1353W/m^2$

From the figures above, we can conclude that the current generated by the junction is proportional to the intercepted irradiance, then the power generated will increase as the irradiance increases. But we can observe that the MPP is nearly independent of the irradiance as the MPP voltage remains unchanged for typical solar irradiances ($> 500W/m^2$) as represented in figure 3.8 with the black circles being the MPP. While on figure 3.9, the MPP voltage is dependent of the junction temperature and therefore the lower the junction temperature, the higher the generated power.

3.4.3 Maximum Power Point

The MPP of a solar cell is the operating point on the I-V curve where the product of I_L (load current) and V is at its maximum:

$$P_{max} = V_{mp} I_{mp} \tag{3.13}$$

$$I_{mp} = I_L - I_0 \cdot \left[\exp\left(\frac{V_{mp}}{V_T}\right) - 1\right] \tag{3.14}$$

$$\frac{dP}{dV} = 0 \tag{3.15}$$

$$\frac{dP}{dV} = I_L - I_0 \cdot \left[\exp\left(\frac{V_{mp}}{V_T}\right) - 1\right] - \frac{V_{mp}}{V_T} \cdot I_0 \cdot \exp\left(\frac{V_{mp}}{V_T}\right) \tag{3.16}$$

$$= I_{mp} - \frac{V_{mp}}{V_T} \cdot I_0 \cdot \exp\left(\frac{V_{mp}}{V_T}\right) \tag{3.17}$$

$$\Rightarrow V_{mp} = \frac{I_{mp} V_T}{I_0} \cdot \exp\left(\frac{V_{mp}}{V_T}\right) \tag{3.18}$$

$$= V_T \cdot \exp\left(-\frac{V_{mp}}{V_T}\right) \cdot \left(\frac{I_L}{I_0} + 1\right) - V_T \tag{3.19}$$

The equation for finding the maximum power is an implicit equation, the solution can be found by graphical or numerical methods, or simply by using the alternative solution $V_{mp} \approx V_{OC} - 3 \cdot V_T$

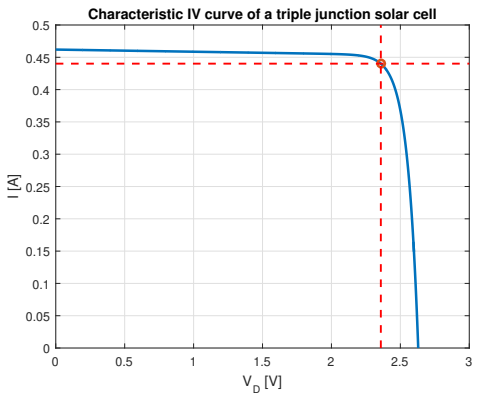

Figure 3.10: Characteristic I-V curve of the triple-junction solar cell and the corresponding MPP

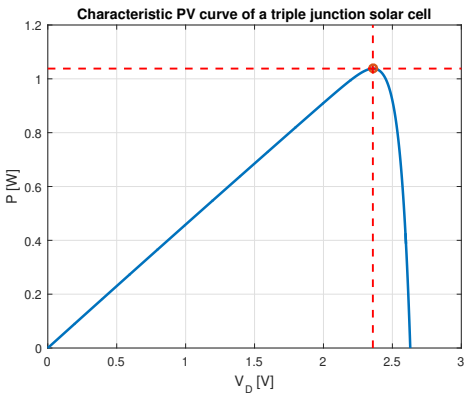

Figure 3.11: Characteristic P-V curve of the triple-junction solar cell and the corresponding MPP

3.4.4 Power conversion efficiency

The power conversion efficiency is the measure of the cell ability to convert solar energy into electrical energy:

$$\eta = \frac{P_{max}}{P_{in}} = \frac{V_{mp} \cdot I_{mp}}{A \cdot G} = FF \cdot \frac{V_{OC} \cdot I_{SC}}{A \cdot G} \tag{3.20}$$

where

- A is the area of a triple-junction cell
- G is the solar constant
- $FF = \frac{V_{mp} I_{mp}}{V_{OC} I_{SC}}$ is the fill factor.

3.4.5 Loading the solar cell

When the load is directly connected to a non-linear source, the system operating point is at the intersection of the I-V curve and the load line. For a single linear load with constant resistance, the load line would not intersect the I-V curve at MPP. The switching regulator is a constant power load which aims to regulate its output at a steady voltage regardless of variations in input voltage or load current draw.

If P = VI and the operating point moves away from its point :

$$P + \Delta P = (V + \Delta V) \cdot (I + \Delta I) \tag{3.21}$$

$$= VI + V\Delta I + \Delta V I + \Delta V \Delta I \tag{3.22}$$

$$\Rightarrow \Delta P = V\Delta I + \Delta V I + \Delta V \Delta I \approx V\Delta I + \Delta V I \tag{3.23}$$

At MPP, ΔP should necessarily be zero and lie on a locally flat neighborhood, and we obtain the following relationship between the dynamic and static impedance at MPP:

$$\frac{\Delta V}{\Delta I} = -\frac{V}{I} \tag{3.24}$$

Electrically stable operation of the solar array is characterized by:

$$\left[\frac{dP}{dV}\right]_{load} > \left[\frac{dP}{dV}\right]_{source} \tag{3.25}$$

3.5 Angular response of a solar cell

The fundamental parameter to determine the rate of photon reflection is the angle θ between the solar panel normal vector $\hat{N}$ and the spacecraft-Sun vector $\hat{S}$ which is given by the formula:

$$\hat{N} \cdot \hat{S} = \overrightarrow{N_x} \cdot \overrightarrow{S_x} + \overrightarrow{N_y} \cdot \overrightarrow{S_y} + \overrightarrow{N_z} \cdot \overrightarrow{S_z} = \cos\theta \tag{3.26}$$

The amount of solar energy generated by the current frame cell is proportional to $\cos\theta$. Beyond 50°, the reflection of the photons is increased and it causes the angular response to deviate from the cosine law, the actual response is more accurately expressed by the Kelly cosine:

$$\rho = -0.369\cos^3\theta + 0.637\cos^2\theta + 0.750\cos\theta - 0.015 \tag{3.27}$$

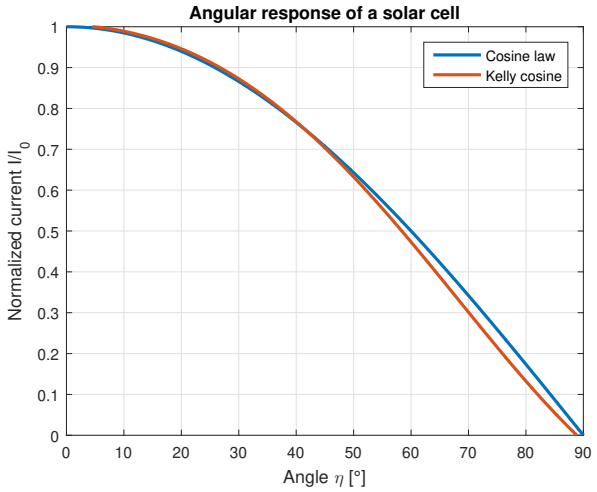

Figure 3.12: Comparison of normalized current between cosine law and Kelly cosine

The actual electrical output drops off slightly steeper with the Kelly cosine. There is no current produced at angles greater than 85°. The deviation is not large enough to outweigh the benefits of simpler calculations. With these reflection considerations, we can compute the electrical power generated by the solar cells:

$$P = A \cdot \cos\theta \cdot G \cdot \eta_{panel} \tag{3.28}$$

where

- $A \cdot \cos\eta$ is the effective area
- η_{panel} is the conversion efficiency

3.6 Maximum Power Point Tracking algorithm

They are several MPPT algorithms used in nanosatellites such as Fractional Open-Circuit Voltage, Fractional Short-Circuit Current, Perturb and Observe, and also Incremental Conductance. In most CubeSats, the Perturb and Observe or Incremental Conductance algorithm are implemented. These are based on the same principle which are the periodic perturbation of the solar array voltage and observation of power change in order to reach the MPP. We can note that temperature based MPPT algorithms do exist and are typically more efficient than aforementioned algorithms while being more complex.

The Fractional voltage algorithm is based on the fact that the maximum power point voltage is a fraction of the open-circuit voltage. At regular intervals, the open-circuit voltage is measured stopping the power flow from the solar panels. A fine characterization of the solar panels should be performed beforehand for optimal efficiency of the algorithm. This algorithm does not support continuous power flow but it has a low refresh time and low complexity.

The Fractional current algorithm is based on the fact that the maximum power point current is a fraction of the short-circuit current. This algorithm has the same advantages and drawbacks as the fractional voltage algorithm with exception that the current is measured instead of the voltage. The operation of these algorithms is represented in figure 3.13 and 3.14. We can note that the efficiency of these two algorithms can be increased by performing a temperature measurement.

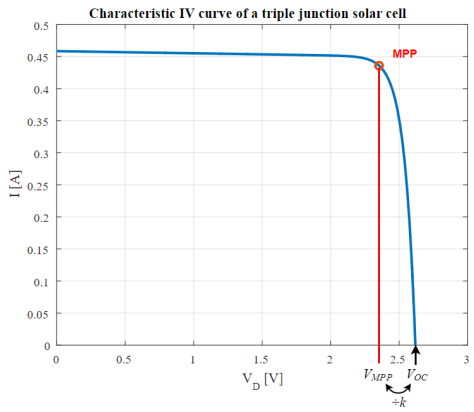

Figure 3.13: Fractional voltage algorithm

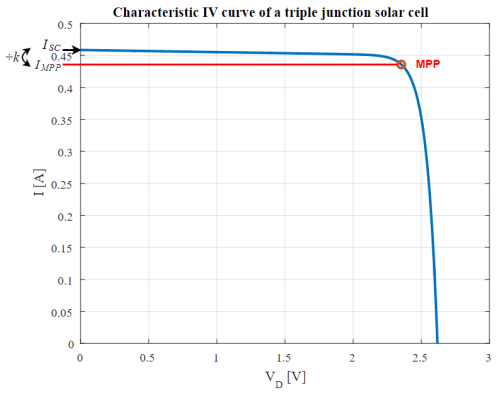

Figure 3.14: Fractional current algorithm

The Perturb and Observe (P&O) method is based on the perturbation of the solar panel voltage and observation of the power change. This algorithm is simple and precise but the drawback is that the MPP is never reached and the operating point of the solar array will oscillate around the MPP as we can observe on figure 3.15. The oscillation magnitude is fixed by the resolution of the Pulse Width Modulation (PWM) generator. Another drawback is that the P&O algorithm can not differentiate a power reduction due to reduced irradiance from a power reduction due to increased distance from MPP.

The Incremental Conductance is based on the same principle as the Perturb and Observe method with the difference that the voltage perturbation is determined with the relationship between $\Delta I/\Delta V$ and -I/V. With this relationship, we can detect that the algorithm has reached the MPP and the voltage perturbation is interrupted. This way of fixing the new Operating Point (OP) overcomes the oscillation problem and increases the efficiency but at the cost of increased complexity as represented on figure 3.16.

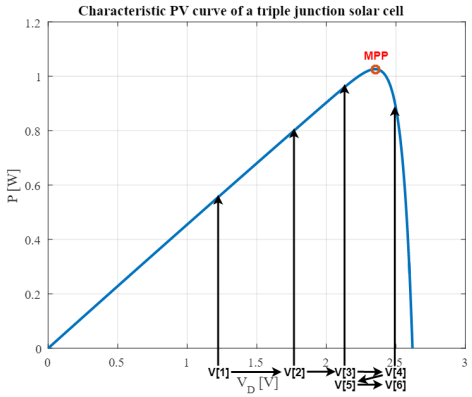

Figure 3.15: Perturb and Observe algorithm

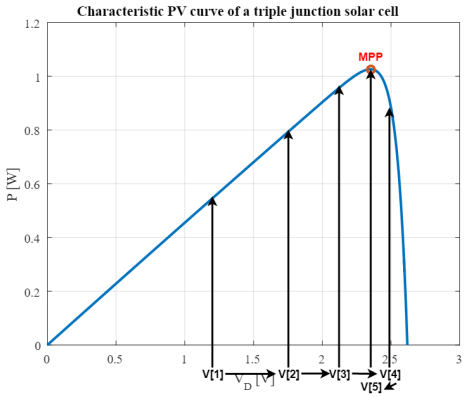

Figure 3.16: Incremental Conductance algorithm

Finally, temperature based MPPT algorithm do exist and provides an alternative to current sensing by replacing it by temperature measurements. This algorithm is based on the dependence of the MPPT with respect to the solar cell temperature. The drawback of such algorithm is the additional information required such as the temperature coefficients, the reference temperature. Also temperature measurements can be used in addition to incremental conductance to obtain a faster transient response and increased efficiency.

Chapter 4

Energy Storage

For typical space missions, an energy storage device is needed to supply the subsystems with energy when no power is generated by the solar array. In this section, we will investigate the different state-of-the-art energy storage technologies and we will select the most suitable technology based on the Ragone plot and mission requirements. Next, we will explore the operation principle and the electrochemistry of the selected technology based on its chemical reactions. Then, we will study the electronic behavior and the method for charging and discharging the storage device. Finally, we will examine the metrics and origins of the performance degradation of this technology.

4.1 Energy storage technologies

An energy storage device is a device that converts energy from any forms to a more conveniently storable forms (for instance chemical, gravitational potential, electricity, kinetic or others). Any energy storage system can be modeled as an ideal source of voltage with a series resistance representing the conduction losses and a parallel resistance representing the power leakage that is slowly discharging even when the storage device is inactive.

The electrical model of any storage system is represented in figure 4.1. From this model, we can compute the energy and power that can be supplied to a load based on its internal parameters and therefore draw the Ragone plot represented in figure 4.2. The set of equations describing the storage system are given by:

$$I_{SH} = \frac{V_{OC}}{R_{SH}} \tag{4.1}$$

$$I_L = \frac{V_{OC}}{R_S + R_L} \tag{4.2}$$

$$V_L = \frac{R_L}{R_L + R_S} \cdot V_{OC} \tag{4.3}$$

$$P_L = \frac{R_L}{(R_L + R_S)^2} \cdot V_{OC}^2 \tag{4.4}$$

$$\frac{E_L}{E_{max}} = \frac{R_L \cdot I_L^2}{R_L \cdot I_L^2 + R_S \cdot I_L^2 + R_{SH} \cdot I_{SH}^2} \tag{4.5}$$

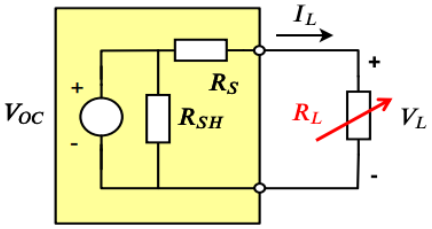

Figure 4.1: Electrical model of a power storage system

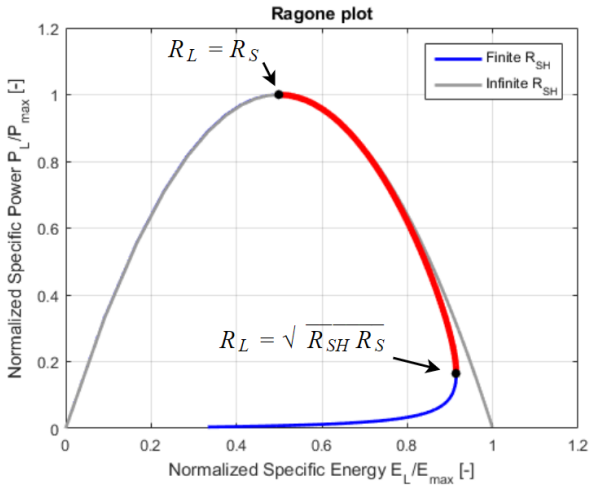

Figure 4.2: Ragone plot of a power storage system

In the Ragone diagram, there are two points of interest represented in black in figure 4.2. The first interesting point is the maximum specific power point reached when $R_L = R_S$, the storage device can provide the load with reduced energy but at maximum power. The second point of concern is the maximum specific energy point achieved when $R_L = \sqrt{R_{SH} \cdot R_S}$, the device can provide a maximum of energy but at reduced power. At last, the red line represents the usable domain in which the storage device is operating at optimal conditions. Therefore, typical Ragone diagrams exhibit trends like the red curve in figure 4.2.

There exists a broad range of energy storage technology. The main parameters in any energy storage device are the specific energy density (in W/kg), the specific power density (Wh/kg) and the discharge time (in h). The figure 4.3 shows different energy storage with the corresponding range of characteristic parameters.

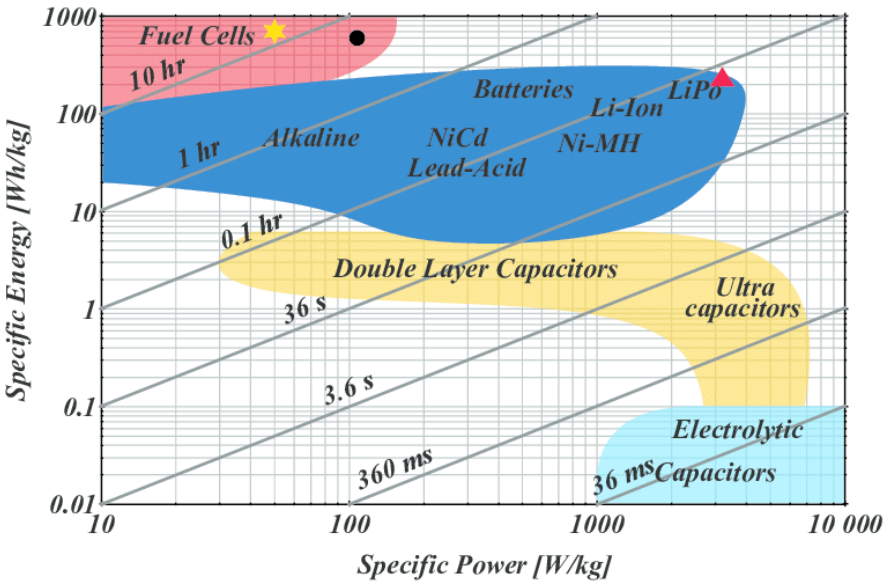

Figure 4.3: Ragone plot for different energy storage technologies [15]

The Ragone diagram in figure 4.3 represents storage technologies that output electrical energy as only this type of technology is considered in space missions. Note that in the Ragone diagram, both rechargeable and non-rechargeable technologies are represented, but in the selection process, we will consider only rechargeable technologies.

Fuel cells are electrochemical cells that convert the chemical energy of a fuel (eg. hydrogen) and an oxidizing agent (eg. oxygen) into electrical energy through a pair of redox reactions. The electrolytic capacitors are polarized capacitors whose anode is made of metal that forms an insulating oxide layer acting as the dielectric of the capacitor. The batteries are supplying electrical energy by converting high energy reactants to low energy products, the difference being supplied to the load through redox reactions. The double layer capacitors are high capacity capacitors which are composed of two electrodes separated by a separation membrane and an electrolyte. Double layer capacitors or also super-capacitors close the gap between batteries and electrolytic capacitors as they exhibit high power density and moderate energy density.

In nanosatellite, we have to select a storage device that exhibits a high energy density in order to reduce the launch cost and also a high power density as the consumption profile shows peak power consumption when typically a high power system is activated such as the AOCS or COM system. Thus, we can conclude that rechargeable battery is the most suitable storage technology which displays both high energy and high power density.

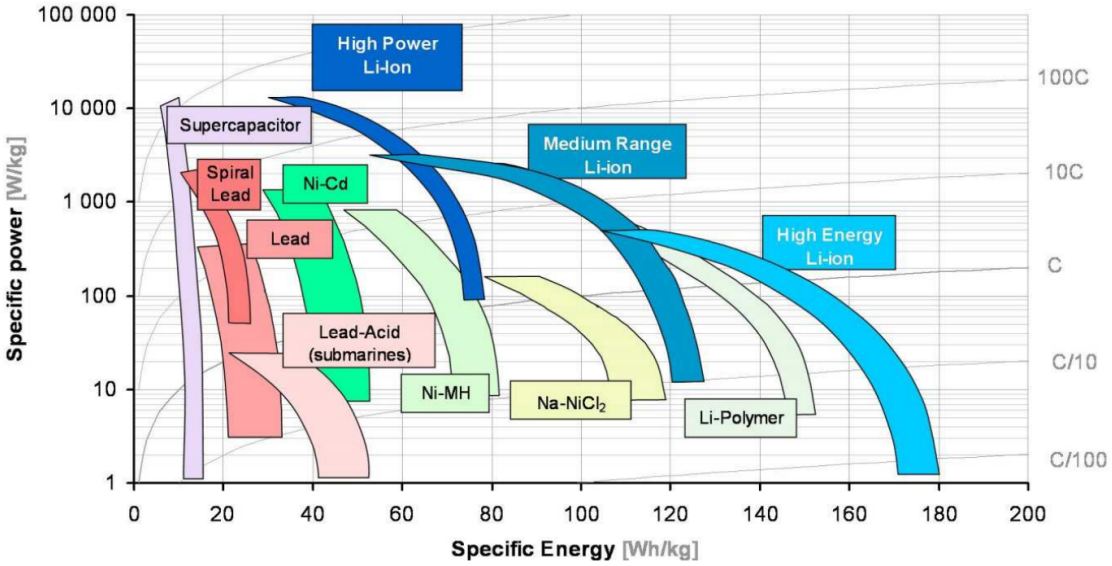

Figure 4.4: Ragone plot for different rechargeable battery technologies [16]

We can go deeper in the selection of storage device by comparing the different type of rechargeable batteries. The Ragone diagram for different rechargeable battery technologies have been presented in figure 4.4. We can observed that Li-ion batteries covers all ranges of energy and power density and they are therefore the primary selected technology. There are multiple types of Li-ion battery: high power, medium range and high energy version. In space applications, we need to reduce as much as possible the weight of the satellite while the power consumption does not exceed typically several hundreds Watts of power, therefore the high energy version of Li-ion battery is the selected technology.

We can note that other state-of-the-art batteries exist such as LiPo and Li-polymer which exhibit higher power and high energy density but theses technologies are in development and are not yet ready for space applications at the moment.

Another advantage of Li-ion batteries is that they do not exhibit memory effect. The memory effect is observed in nickel-cadmium (NiCd) and nickel-metal hybrid (NiMH) rechargeable batteries which has the effect of retaining less energy. This effect describes the loss of capacity when nickel-cadmium or nickel-metal batteries are being charged after being partially discharged [29].

Li-ion batteries also exhibit low self-discharge compared to other technologies. Self-discharge is a phenomenon observed in rechargeable batteries where the stored energy slowly decreases over time, without the battery being connected to a load. This is mainly due to internal chemical reactions occurring naturally in the batteries. This phenomenon decreases also the battery life cycle and causes them to store less charge than a full charge when in use. The self-discharge is modeled by the parallel leakage resistance, thus we can consider from now that the leakage resistance is infinite for Li-ion batteries [30].

But Li-ion batteries present safety risks when being damaged because they contain an inflammable electrolyte that can take fire or explode. Also short-circuits can appear when the batteries are being charged at excessive rates resulting in fires or explosion, therefore a protection circuitry should be incorporated in the system. Another drawback of Li-ion batteries is that they suffer from ageing which will be explained in details in section 4.4.

4.2 Electrochemistry of Lithium-Ion Battery

Lithium-ion batteries are composed of a negative electrode (anode) and a positive electrode (cathode), and an electrolyte providing a conductive medium for lithium ions to move between the electrodes. There is also a separator membrane usually made out of polymer used to electrically separate the anode and cathode because the reactivity of the lithium is so high. The internal composition of a Li-ion battery is represented in figure 4.5.

Li-ion batteries undergoes chemical reactions in which lithium ions move from the anode to the cathode when discharging (inversely when charging). The lithium ions enter and exit the electrodes structure with insertion and extraction process, respectively. During discharge, the lithium ions move to lower energy state enabling the electrons to flow from the anode to the cathode and supply energy to the load. When the cell is charging, the reverse process occurs with the lithium ions being transformed into higher energy products. These processes are given by the following set of chemical equations [29] [31].

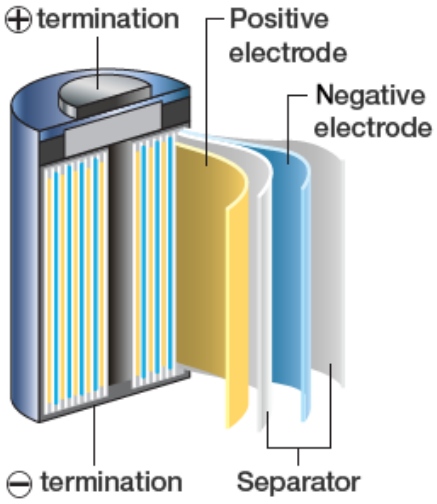

Figure 4.5: Internal composition of a Lithium-ion battery [17]

The cathode half-reaction is:

$$CoO_2 + Li^+ + e^- \rightleftharpoons LiCoO_2 \tag{4.6}$$

The anode half-reaction is:

$$LiC_6 \rightleftharpoons C_6 + Li^+ + e^- \tag{4.7}$$

The full chemical reaction occurring in the battery is:

$$LiC_6 + CoO_2 \underset{charging}{\overset{discharging}{\rightleftharpoons}} C_6 + LiCoO_2 \tag{4.8}$$

The chemical reactions described above only occurs in typical operating conditions of the battery. Other chemical reactions can occur when the battery is over-charged or over-discharged leading to performance degradation of the battery such as loss of capacity and permanent damages. Such atypical conditions should therefore be avoided in order to preserve the good operation of the battery. Over-discharging the battery could lead to the production of lithium oxide and possibly results in the following irreversible reaction [32]:

$$Li^+ + e^- + LiCoO_2 \rightarrow Li_2O + CoO \tag{4.9}$$

Overcharging up to 5.2V leads to the production of cobalt oxide described by the following reaction [33]:

$$LiCoO_2 \rightarrow Li^+ + CoO_2 + e^- \tag{4.10}$$

4.3 Electronic Behavior of a Li-Ion Battery

4.3.1 Electronic behavior upon charging and discharging

An ideal battery can be modeled as a constant voltage source but a more realistic battery model should be a variable voltage source whose voltage is depending on many parameters which are the capacity, discharge rate and battery temperature being the most important.

We also need to consider the different sources of losses present in Li-ion battery in order to have a complete model of the battery. As mentioned in chapter 4.1, the Li-ion battery exhibits a low self-discharge which is evaluated at approximately 0.5% to 2% per month [30]. Therefore, we can consider that the leakage resistance is infinite. The other source of losses is the conduction resistance coming from the electrical resistivity of electrode contacts and can be as high as 20% [34]. In typical Li-ion batteries, the internal conduction resistance is always below $100m\Omega$ [35] [2] [36] [37].

Therefore, we can construct an electrical model of a Li-ion battery as represented in figure 4.6. This model neglects the dynamic response of the battery upon connection to a load.

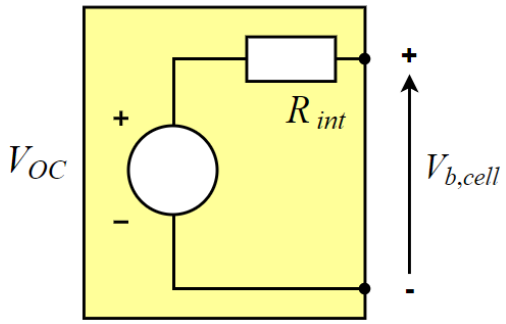

Figure 4.6: Electronic model of a battery

The battery can operate on a broad range of voltage approximately from 2.5V to 4.2V and the cell voltage is proportional to its State of Charge (SOC). The available battery capacity decreases as the discharge rate is increased as we can observe on figure 4.7 due to the internal conduction resistance. Therefore, when a high-power system is activated drawing a high current, we should limit the discharge rate in order to optimize the available capacity and reduce the losses. The discharge rate capacities are expressed in terms of capacity (C), then a rate of 1C is equal to the current that the cell can supply during 1 hour.

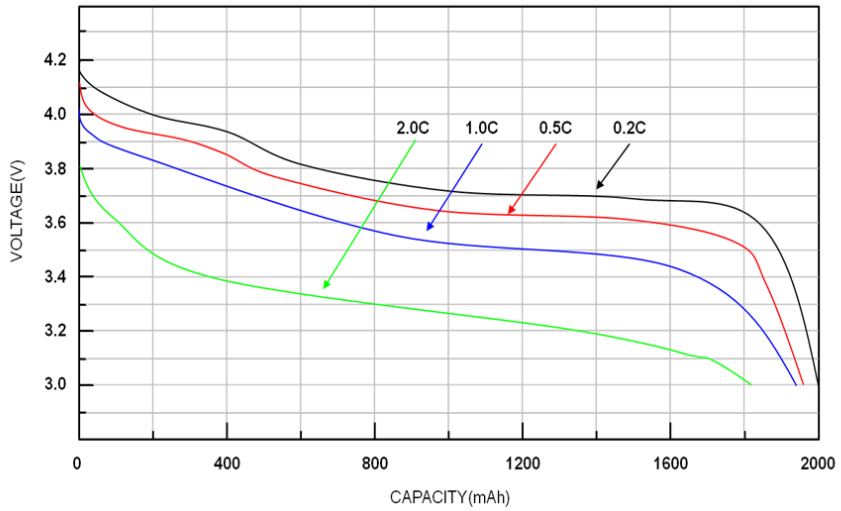

Figure 4.7: Discharge rate capacity at +25° of a Li-ion battery cell [18]

The discharge rate capabilities also vary with the battery cell temperature as shown in figure 4.8. The capabilities are enhanced when the temperature is increased as the temperature rise will boost the rate at which the chemical reactions can operate resulting in larger discharge rate capabilities. The temperature rise should be limited otherwise it can lead to irreversible damages that can ultimately result in fires or explosion.

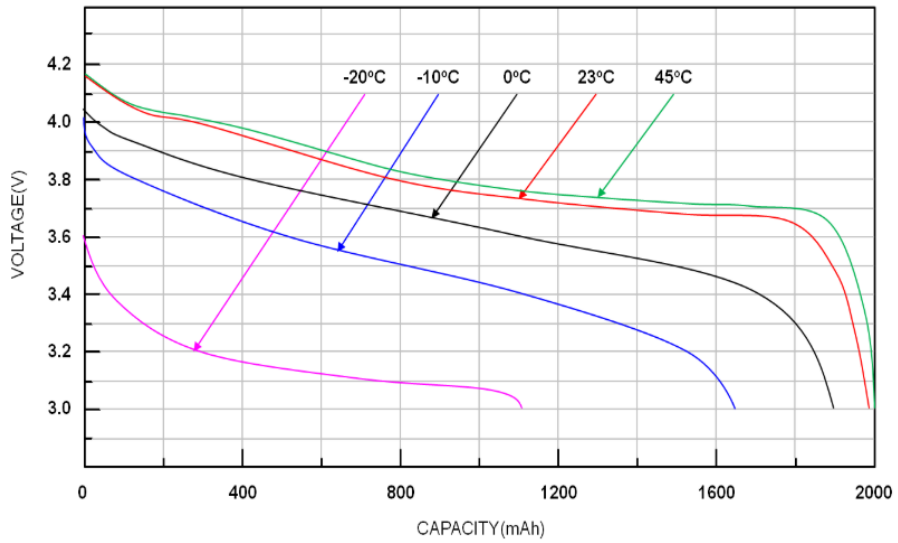

Figure 4.8: Discharge rate capacity at -1C rate of a Li-ion battery cell [19]

4.3.2 Charging and discharging a Li-ion battery pack

A battery pack is formed by connecting in series or in parallel multiple cells such that the total energy capacity of the storage device is increased. The charging of a Li-ion battery pack is performed following three stages:

- Constant-Current (CC)
- Balance
- Constant-Voltage (CV)

The Constant-Current and Constant-Voltage phases of a Li-ion battery cell are represented on figure 4.9. The first stage is the Constant-Current phase where the battery is supplied with a constant current while the voltage is increasing. This stage is done when the cell voltage reaches the charging voltage (typically 4.2V).

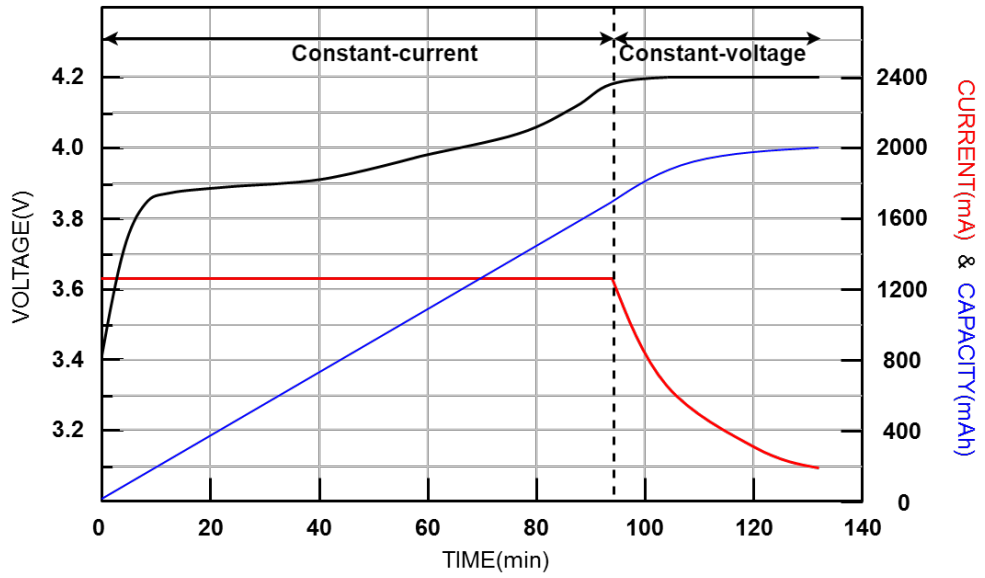

Figure 4.9: The Constant-Current and Constant-Voltage charging profiles of a Li-ion battery [20]

The next stage is the balance phase in which the individual cells are being charged to the same state of charge. The stage is performed by a balancing circuit supplying reduced current to individual cell. This stage is terminated when all cells are balanced. Some chargers skip this stage while others balance the battery pack by charging each cell separately.

The last stage is the Constant-Voltage phase where the charger applies the maximum cell voltage (typically 4.2V) multiplied by the number of cells connected in series. During this phase, the current slowly decreases towards 0 and this phase is completed when the current is reduced below 3% of initial constant charge current [20]. The charging and discharging is a critical operation as a failure to follow current and voltage limitations can result in an explosion.

4.4 Battery Performance Degradation

Battery cycle life is expressed in terms of the number of full charge/discharge cycles before significant capacity loss (typically 20%). A typical cycle life profile of Li-ion battery with respect to the depth of discharge is represented in figure 4.10.

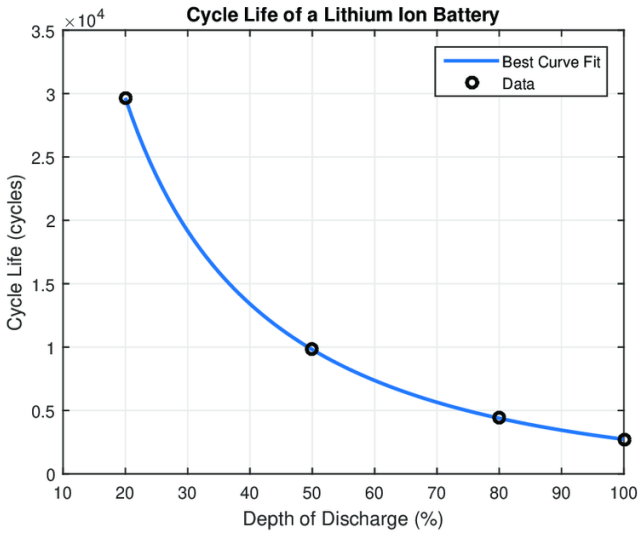

Figure 4.10: Cycle life of a Li-ion battery versus the depth of discharge [20]

When the battery reaches its cut-off voltage (can vary from 2.4 to 2.9V depending on chemistry), it stops discharging until the battery is finally being recharged. When discharging, undesired discharge paths are created due to the fact that the cell metallic contents hang on its internal structure.

The cycle life of a battery is typically measured by applying full charge/discharge cycles but this way of doing may be biased as the depth of discharge is the main parameters that will impact the performance degradation. In order to have a more realistic estimation of the cycle life, we should have several cycle life measurements with various depth of discharge, maximum state of charge, discharge rate and storage temperature.

Now, we will investigate the origins of performance degradation in Li-ion batteries. Over time, we can observe performance degradation in batteries with reduced capacity, cycle life and safety due to chemical changes in electrodes. Typically in datasheets, the capacity loss is given in terms of number of cycles after a percentage of the initial capacity is lost. This capacity loss can be divided into two types of losses that are the calendar loss and cycling loss. The calendar loss is a result of the ageing process of the battery and is expressed as the deviation from the maximum state of the charge. While on the other hand, the cycling loss is linked to the extensive operation of the battery and therefore is dependent on the operation habits that is the maximum state of charge (SOC) and the depth of discharge (DOD). The DOD has the main impact on the cycle life of a battery and should be designed with extreme precaution.

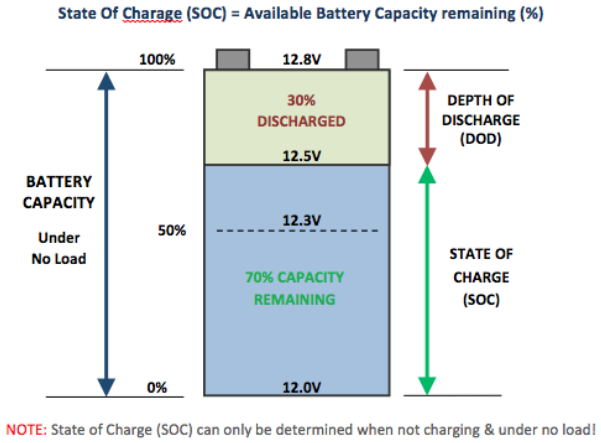

Figure 4.11: State of charge and depth of discharge of a battery [21]

Storage temperature is also a parameter in performance degradation where we can identify that the lowest degradation temperature is around $+25°C$ and increased degradation is observed when the temperature is above or below this optimal value. The capacity loss soars with high discharge rates and temperatures. In fact, heat is generated in the carbon anode upon battery charging or discharging but we could refrigerate to reduce performance degradation.

Upon first charge and discharge of the battery, a Solid Electrolyte Interphase (SEI) layer is formed on the anode and cathode, and is the result of the consumption of lithium ions. The consumption of lithium ions degrades the performance of the electrode as it reduces the charge and discharge efficiency. The battery is also more susceptible to temperature-related degradation due to the SEI layer formation. This layer should typically reach a fixed thickness but under critical conditions, the layer thickness could increase resulting in performance degradation.

Chapter 5

Energetic Study and Optimization

In the previous section, we have explored the principles of power generation with solar panels and the basics of power storage with the Li-ion technology. Now, we would like to study the power fluxes inside the EPS and to optimize the system configuration in order to reduce the mean power losses and therefore increase the system efficiency. This chapter constitutes the main contribution of this work, therefore this chapter must be closely examined. At first, we will enumerate the mission specifications to have an overview of the requirements and constraints of the system. Next, we will select the solar panels and battery cells among state-of-the-art products. Then, we will size the solar array and battery pack through the energetic study and finally we will optimize the system by selecting the solar array and battery pack voltages resulting in the least power losses.

5.1 Mission specifications

The first part of the study is the mission specifications as they state the mission frame and set the system constraints. The specifications can be divided in multiple categories and can either be related to the satellite, orbit, consumption profiles or PCDU outputs. Here below, we can find the exhaustive list of the mission specifications which were provided by Aerospacelab.

- Satellite:
  - Size: $40 \times 40 \times 60 cm^3$.
  - Mission duration: 2 years.
  - Orientation: CubeSat always in nadir pointing meaning that ABCD normal vector is always pointing to the center of the Earth (cfr. figure 5.1). Therefore, the irradiance intercepted by the solar panels will have a sinus profile.

- Solar panels: They are not adjustable independently of the satellite. There are many possibilities for the arrangement of solar panels:
  * Panels fixed on the satellite faces.
  * Deployable panels fixed on the edges EH, FG, FE or GH.
  * Double deployable panels (panels of $2 \times 40cm \times 60cm$ fixed on edges EH/FG) as depicted in figure 5.2.
  * Another option to generate more power: orient the satellite towards the Sun during daytime and neither in imaging nor transmitting mode.
  * Temperature of the solar panels vary from $-50°C$ + $+100°C$ over a period with negative exponential profile.

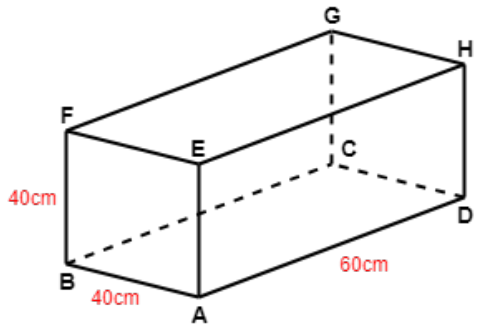

Figure 5.1: CubeSat structure drawing

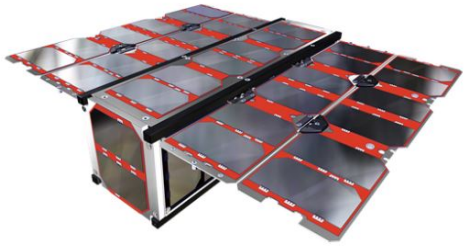

Figure 5.2: CubeSat with double deployable panels [22]

- Orbit:
  - Orbit is a Sun Synchronous Orbit (SSO) as represented in figure 5.3.
  - The satellite is orbiting at an altitude of 530km.
  - The orbit tilt is 97.5 degree. The orbit is therefore a near polar orbit.
  - The orbit period lasts approximately 1h35. Such type of orbit offers 50% of sunlight (47.5min) and 50% of eclipse (47.5min).
- Consumption profile:
  - Imaging mode: Payload consumes 30W during 75% of daytime. It is centered on the equator and supplied on 12V bus.
  - Transmitting mode: Communication consumes 70W during 5 minutes after imaging mode or during nighttime above Scandinavia. It is also supplied on 12V bus.

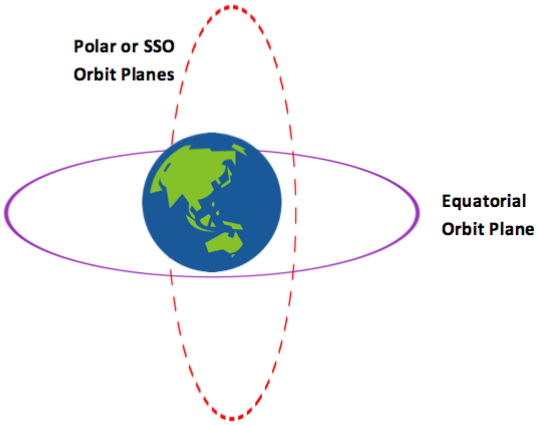

Figure 5.3: Satellite in near polar orbit (SSO) [23]

  - Other systems of the CubeSat consumes 20W permanently. The consumption of other systems is distributed as follows: 15W on 5V bus and 5W on 3.3V bus.

- PCDU Outputs: Maximum voltage and current ratings per bus are mentioned in the table 5.1. We should note that these ratings will not occur at the same time:

Subsystem	Bus voltage [V]	Current rating [A]	Power rating [W]
GPS	3.3	1	3.3
Star tracker	3.3	1	3.3
OBC 1	3.3	1	3.3
PCDU + BPA	3.3	1	3.3
Subtotal	3.3	4	13.2
Reaction wheel 1	5	4	20
Reaction wheel 2	5	4	20
OBC 2	5	3	15
Subtotal	5	11	55
Propulsion	12	8	96
Payload 1	12	1	12
Payload 2	12	2	24
Subtotal	12	11	132

Table 5.1: Summary table of PCDU output ratings

5.2 Cells selection

Before starting the energetic study of the EPS, we need to select the basic building blocks constituting the power system which are the solar panels and battery cells. This step is important as it will have a strong impact on the EPS sizing and on energetic optimization. In order to properly select the most suited cell for the mission, we will build a comparative chart for state-of-the-art solar panels and another for state-of-the-art battery cells.

The main parameters to look forward in the selection of solar cells are the maximum generated power and average conversion efficiency. We also need to pay attention to the available dimensions and corresponding cell area because there is more room for optimization when considering small dimensions. The last important parameter is the cell weight as it will impact the launch cost as well as the effectiveness of the AOCS, thus we prefer to consider low weight cells.

Now considering the selection of battery cell, the main parameter of interest is the energy density and weight as it represents a good metric for the battery efficiency. Other important parameters are the maximum current rate and operating temperature range as space missions offer a wide range of operating conditions. The internal impedance should be as low as possible in order to reduce the power losses. Finally, the most important feature of battery cell is the cycle life because the DOD, maximum capacity and at last satellite weight are designed based on the cycle life.

Note that the cost of the cells is also an important selection parameter but as this information is not mentioned in the datasheets, we will consider that all the cells are sold at the same price. This way of doing is the most straightforward, furthermore the budget allowable for the mission is not mentioned in the specifications provided by Aerospacelab.

5.2.1 Selection of solar cell

Product	**AZURSPACE 3G30C Triple Junction Solar Cell [38]**	**Spectrolab XTJ Prime Triple Junction Solar Cell [1]**	**SolAero ZTJ-Ω Space Solar Cell [39]**	**Emcore ZTJ Photovoltaic Cell [40]**
Dimensions $[cm \times cm]$	1. 4×8 2. 8×8 3. 12×6	1. 3.97×6.91 2. 6.76×13.81 3. 7.05×13.89	Custom sizes available	3.97×6.91
Cell area $[cm^2]$	1. 30.18 2. 60.36 3. 68.76	26 to 84	1. $2 \times 27 - 30$ 2. $1 \times 60 - 65$ 3. $2 \times 70 - 80$	26.6
Average weight $[mg/cm^2]$	86 to 130	50 to 84	Not given	84
Voltage at max power V_{mp} **[V]**	2.411	2.406	2.43	2.41
Current at max power J_{mp} $[mA/cm^2]$	16.7	17.5	16.8	16.5
BOL Average efficiency η **[%]**	29.7	30.7	30.2	29.5

Table 5.2: Comparative table of triple-junctions solar cells with corresponding parameters

Based on table 5.2, we can observe that one cell stands above the others that is the Spectrolab XTJ Prime Triple Junction Solar Cell. This panel exhibits the higher efficiency and lowest weight making it the optimal solution. Furthermore, this cell is available in many different dimensions making it very versatile as we can see on page 2 of Appendix A. We choose the $3.97cm \times 6.91cm$ rectangular version of this cell because it offers a large room for optimization and the rectangular geometry is the most area efficient with respect to the others standard sizes. This cell is space qualified as it displays a proven flight heritage. Useful technical information are present in the Spectrolab XTJ Prime datasheet [1] (Appendix A).

5.2.2 Selection of battery cell

Product	GomSpace NanoPower Battery Cell [35]	SAFT MP 174565 xtd Cell [2]	LG ICR18650 B4 Battery Cell [36]	Panasonic NCR18650PF Cell [37]
Nominal Voltage[V]	3.7	3.65	3.6	3.6
Nominal Capacity[Ah]	2.6	4	2.6	2.9
Energy density [Wh/kg]	200.4	150	195	207
Weight [g]	48	97	48	48
Maximum current rate [A]	• Charge: 2.5 • Discharge: 3.75	• Charge: 4 • Discharge: 8	• Charge: 2.5 • Discharge: 5	Discharge: 10
Operating Temperature [$°C$]	• Charge: 0 to +45 • Discharge: -20 to +60	• Charge: -30 to +85 • Discharge: -40 to +85	• Charge: 0 to +45 • Discharge: -20 to +60	• Charge: 0 to +45 • Discharge: -20 to +60
Internal Impedance [$m\Omega$]	70	25	70	≤ 100
Cycle Life (20% capacity loss) [cycles]	350 (100% DOD, Temp +25$°C$, +1C/-1C)	1500 (100% DOD, Temp +25$°C$, +1C/-0.5C)	300 (100% DOD, Temp +25$°C$, +0.5C/-0.5C)	500 (100 % DOD, Temp +25$°C$, +0.5C/-1C)

Table 5.3: Comparative table of Lithium-ion battery cells with corresponding parameters

Based on table 5.3, we can observe that one battery cell stands above the others that is the SAFT MP 174565 xtd cell. Even though this cell does not exhibit the higher energy density, other important parameters are well above the other solutions making it the best option. This cell has a large operating temperature range and high current rate, making it suitable for the versatility of space missions. This cell has the lowest internal impedance resulting in the least internal power losses and also the cycle life is far larger than the other relaxing the battery requirements for the 2 years of mission duration. Useful technical information are present in the SAFT MP 174565 xtd cell datasheet [35] (Appendix A).

5.3 Energetic study

5.3.1 Architecture

With the mission specifications, we can begin the energetic study of the EPS. In the first place, we need to select a regulation topology before designing the system architecture. The regulation topologies have been discussed in section 2.2.5. We selected the PPT approach because it offers advantages that are really important in CubeSat design. The CubeSats are mass and volume limited, therefore we need an efficient regulation topology that extracts the maximum power from the solar array. CubeSats are also very dense which makes the thermal dissipation a real challenge but the PPT approach side-steps the potential thermal dissipation problems.

One of the main features of PPT approach is the MPPT algorithm, we will consider that the algorithm is of the incremental conductance type with temperature measurement for high precision and enhanced dynamic response. The PPT topology consists of a PPT regulator that can be implemented by a DC/DC converter, controlled by a MCU. This converter will be used for fixing the OP of the solar array. For clarity concerns, this converter will be referred to as solar converter.

The satellite subsystems are supplied with 3 different voltages which are 3.3V, 5V and 12V. To provide three different regulated outputs, we need one converter for each bus voltage which are designed to satisfy the constraints on PCDU outputs. For clarity concerns, these converters will referred to as load converters. The EPS architecture is represented in figure 5.4.

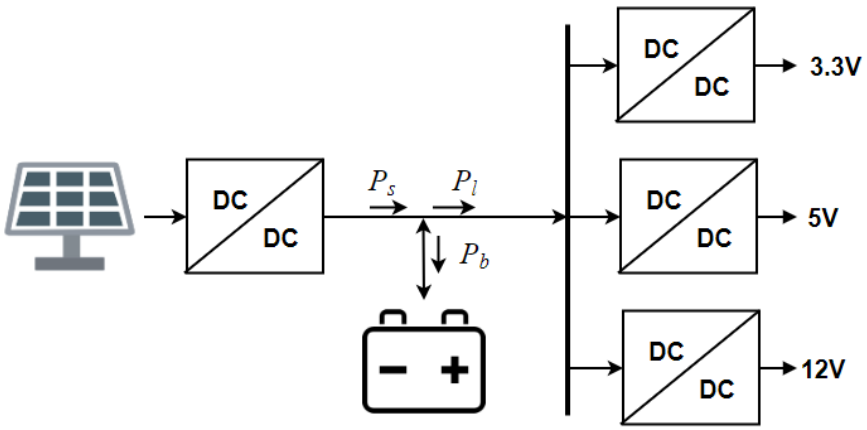

Figure 5.4: EPS design architecture

5.3.2 Solar array sizing

The first step in the energetic study is the analysis of consumption profiles. As stated in the specifications, the data transmission can be performed at 2 moment as represented in figure 5.5. This will not have any impact on the generation profile as the satellite attitude remains unchanged during imaging and transmitting mode. All the power fluxes will be represented with a safety margin of 20% (M_{gen}) as done for the design of the ESTCUBE-1 satellite [41] and as recommended by the European Space Agency (ESA).

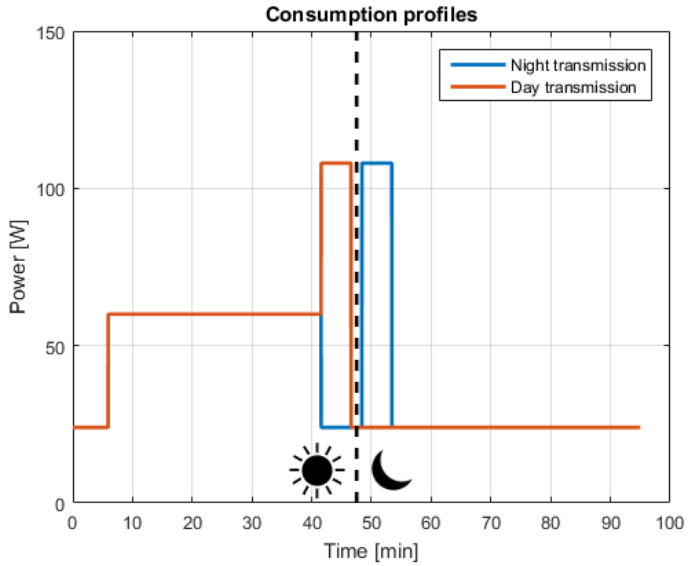

Figure 5.5: Consumption profiles with safety margin for both transmission cases

The first thing to consider is the temperature variation of solar panels over the period duration. The solar panel voltage and current is linearly dependent on the temperature junction. The temperature profile will follow a negative exponential profile and will vary from $-50°C$ to $+100°C$. The temperature profile is represented in figure 5.6 and the solar cell voltage and current dependency with respect to the temperature in figure 5.7. We can conclude that the generated power will decrease as the temperature increases because the voltage drops faster than the current increases. The solar panel performances degrade at high temperatures.

In the sizing process, we will also consider that the satellite is kept in nadir pointing otherwise the AOCS will consume more power, rising the consumption profiles and therefore increasing the number of solar cells needed. As mentioned in the specifications, the SSO orbit provides the satellite with sunlight only 50% of the period, further reducing the energy that we can generate over one period.

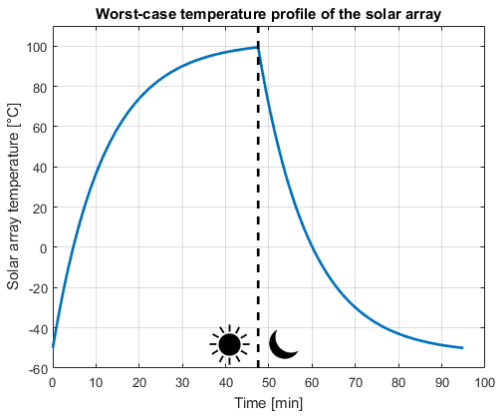

Figure 5.6: Solar panel temperature profile over one period

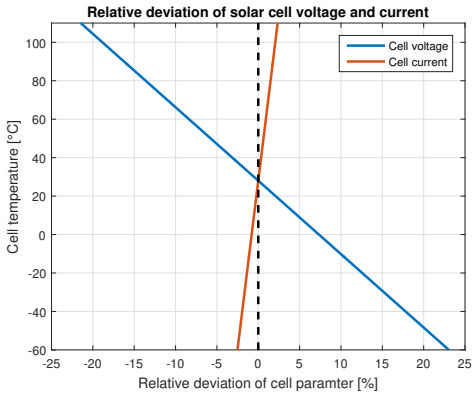

Figure 5.7: Solar panel voltage and current dependence with respect to cell temperature

The power generation normalized profile is the generated power with the temperature effect and angular response which is normalized with the nominal generated power considered at the temperature of $+28°C$ and an incident angle of 90°. This normalized profile is then represented in figure 5.8. We can note that the temperature has a constraining effect on the total generated energy.

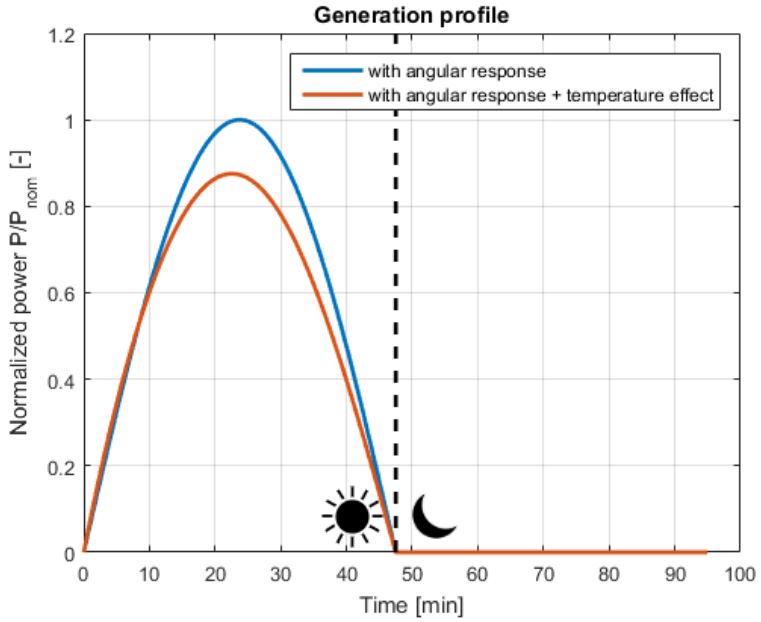

Figure 5.8: Normalized generation profile with respect to the nominal generated power

From this profile, we can compute the average effective area of the solar panel which is the equivalent cell area taking into account the temperature effect and angular response by integrating the generation profile. As mentioned in section 3.5, we will consider the simple cosine law for the angular response due to the simple computations and relatively good accuracy.

$$A_{eff,avg} \approx 0.28 \cdot A \tag{5.1}$$

Now, we can start the energetic study by sizing the solar array. We will first compute the energy supplied to the loads over one period while considering the power losses in the solar array, battery pack and DC/DC converters. The energy can be computed by multiplying the average power flux by the period duration.

For the sizing, we will consider that the power losses are estimated to approximately 10% of the power flux going through the DC/DC converters. This value of 10% is comforted by the information provided in the datasheet of the GomSpace P31u EPS about the converter efficiency of photovoltaic converter [9]. The power losses will then be integrated in the efficiency of the converter ($\eta_{conv} = 0.9$). Starting from figure 5.4, we can state the power equations of the system:

$$P_s = P_b + P_l \tag{5.2}$$

$$\Rightarrow \quad < P_s > = < P_l > \qquad \text{on average} \tag{5.3}$$

We can note that the energy supplied to the battery over one period is zero because the battery should always remain at the same SOC at the end of a period. From equations (3.28) and (5.3), we can compute the power that needs to be generated by the solar array in order to have the energetic balance of the satellite:

$$< P_l > \approx 46.6W \tag{5.4}$$

$$< P_s > = \frac{A_{eff,avg} \cdot G \cdot \eta_{panel} \cdot \eta_{conv}}{1 + M_{gen}} \tag{5.5}$$

$$\Rightarrow A = \frac{A_{eff}}{0.28} = \frac{< P_l > \cdot (1 + M_{gen})}{0.28 \cdot G \cdot \eta_{panel} \cdot \eta_{conv}} \approx 0.52m^2 \tag{5.6}$$

The mechanical dimensions of the selected cells and interconnect spaces are represented in figure 5.9. From the datasheet in Appendix A, we know that the dimensions are $6.91cm \times 3.97cm$ and the cell area is $27.4cm^2$. With such dimensions, we need 190 cells in order to produce enough power to supply all electrical systems. Interconnect spaces should be considered for connecting the inter-connect circuitry such as wires and cell connectors.

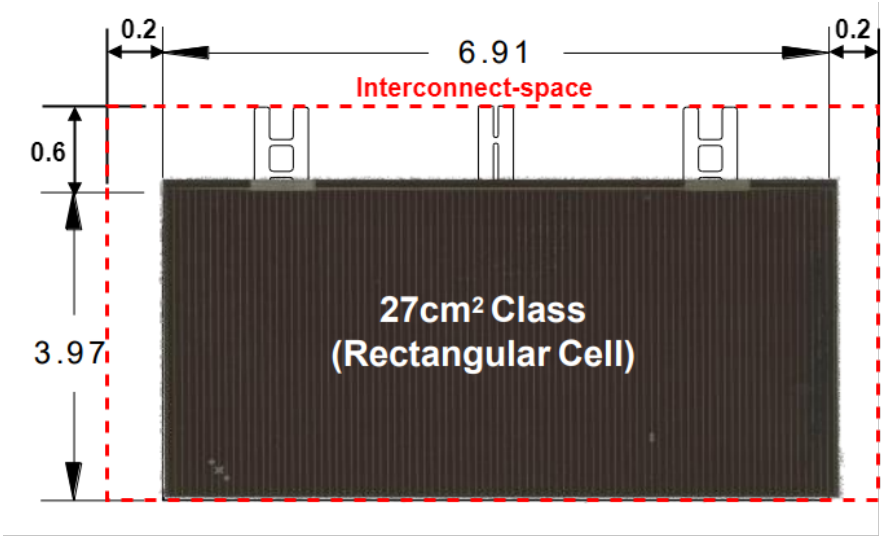

Figure 5.9: Mechanical drawing of the XTJ solar cell [1]

Hence, we can determine the optimal arrangement of panels on the satellite faces using their mechanical dimensions. The pattern represented in figure 5.10 is optimal for placing a maximum of such panels where the black rectangles represent the solar cells. With this pattern, we can place 72 solar panels on a $60cm \times 40cm$ face. Therefore, we only need 3 such faces in order to place all the cells. We will use the face EFGH and also deployable panels on edges EH and FG (cf. figure 5.1).

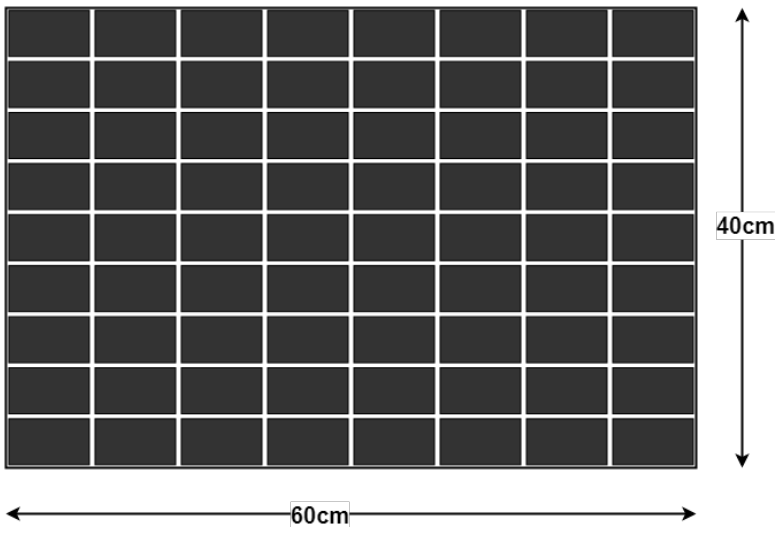

Figure 5.10: Optimal arrangement of solar cells on $60cm \times 40cm$ face

One thing to consider is that these faces will not have the exact same incidence with respect to the Sun, then the junction temperature will be different for each panel. In order to increase the power extracted from the array, we will use one converter for each faces, so that the generated power is further optimized. Another advantage of this design choice is the redundancy of solar converters such that in case of failure in one of the converters, the satellite is still supplied with electrical energy. However, the control logic for the converters is tripled increasing the average power losses in the system. The modified EPS architecture is drawn in figure 5.11.

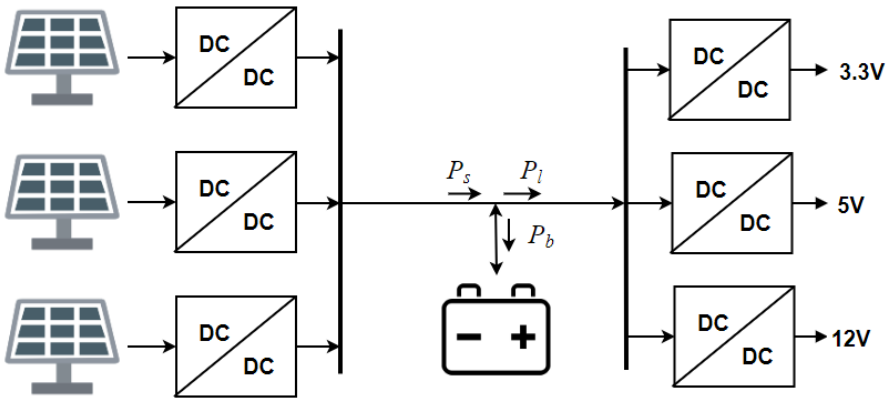

Figure 5.11: Modified EPS architecture

5.3.3 Battery pack sizing

As the solar array sizing is done, we can size the battery pack using the previous results. The transmission moment has a significant impact on the battery sizing. Therefore, we need to determine the worst transmission case before sizing the battery pack. We can determine this by comparing the battery power flux for both cases. We can conclude from figure 5.12 that the night transmission will be the most critical for the battery as it introduces a larger battery discharge.

Considering the most critical scenario, we can compute the generation and consumption profiles and draw the figure 5.13. Using equation (5.2), we can compute the power flux flowing in the battery pack which is represented in figure 5.14. The energetic balance of the battery is important for its cycle life. The charging energy (green area) should be equal to the discharging energy (red area) at each orbit to maintain the battery SOC constant. If the charging energy is higher than intended, the solar array OP should be moved away from MPP to reduce the generated power resulting in a plateau in the battery power flux. If the charging energy is lower, the loads consumption should then be reduced.

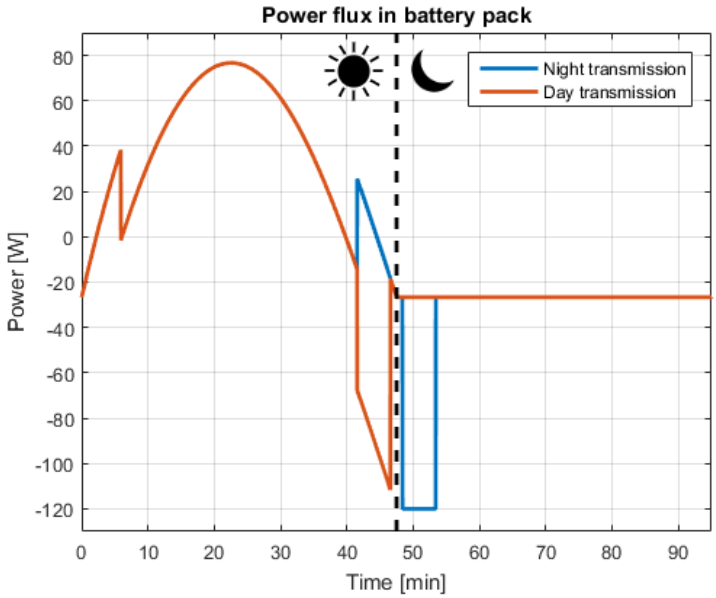

Figure 5.12: Battery power flux for both transmission cases

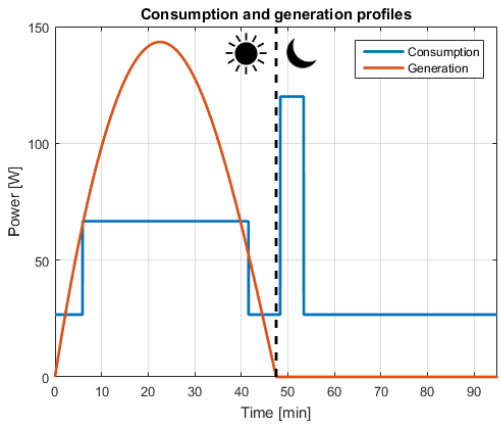

Figure 5.13: Consumption and generation profiles

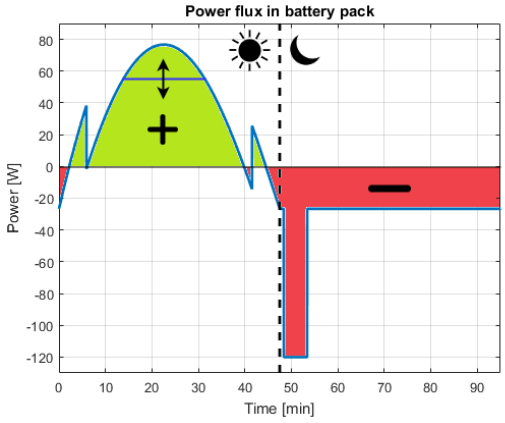

Figure 5.14: Battery power flux profile

The next step in the battery sizing is to compute the depth of discharge in Wh. From the power flux acting on the battery, we can compute the evolution of the battery capacity over one orbit which is represented in figure 5.15. From figure 5.15, we can extract the battery discharge over one period and compute the total battery capacity in order to obtain the intended DOD. The battery DOD is the main parameter as it largely affects the battery cycle life. The mission is intended to last at least 2 years which is equivalent to 11.680 charge/discharge cycles.

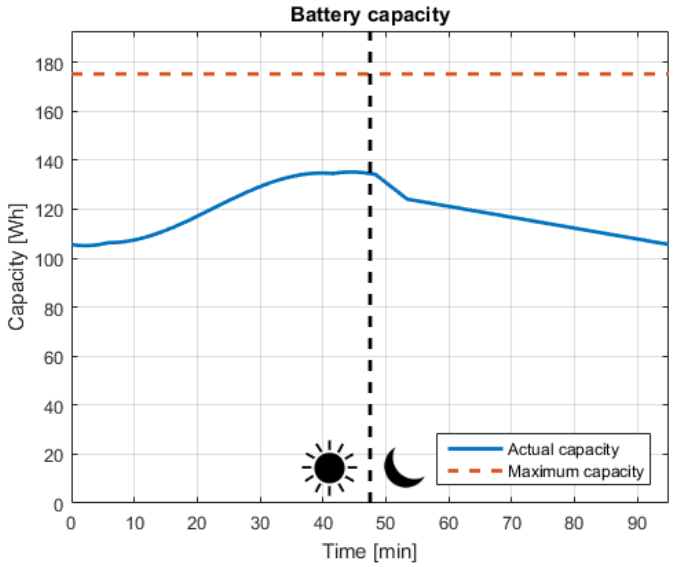

Figure 5.15: Battery capacity over 4 cycles with night transmission

From the battery cell datasheet in Appendix A, we know that the cycle life is 1.500 cycles for the following conditions: 100% DOD, Temperature $+25°C$ and +1C/-0.5C. But as stated in a report about the battery capacity loss in automotive [42], the results show that the number of cycle for the same capacity loss (20%) is multiplied by 10 when reducing the DOD from 100% to 20%. Therefore, we can state that the cycle life will be equal to 15.000 cycles for the following conditions: 20% DOD, Temperature $+25°C$ and +1C/-0.5C. The required battery capacity can be computed:

$$E_{b,discharge} \approx 30.1Wh \tag{5.7}$$

$$E_{b,max} = \frac{E_{b,discharge}}{DOD} \approx 150.7Wh \tag{5.8}$$

The nominal capacity of a battery cell is 14.6Wh, thus we need at least 11 battery cells in order to have a maximum capacity above 150.7Wh. For the rest of the chapter, we will consider 12 cells so that it offers more possible configurations and therefore more room for optimization. Increasing the number of cells to 12 will further increase the cycle life as the DOD is reduced below 20% and the SOC is reduced below 80%.

Another thing that we need to consider for the energetic optimization is the battery cell voltage variation with respect to the SOC. As mentioned in section

4.4, the battery cell voltage is linearly dependent on the SOC. The SOC and corresponding battery cell electromotive force are represented in figure 5.16. Therefore, the battery cell voltage will oscillate around the nominal cell voltage (3.65V) with a oscillation magnitude which is equal to approximately 300mV.

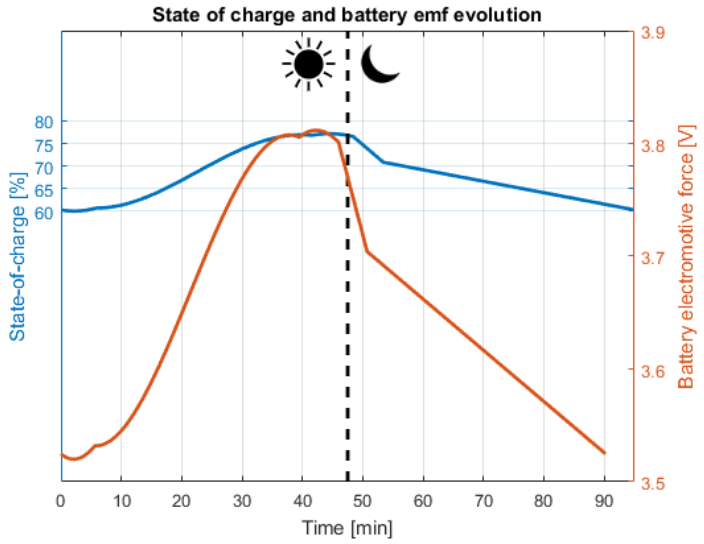

Figure 5.16: State of charge of batteries over 4 cycles with night transmission

5.4 Energetic optimization

This section is related to the energetic optimization of the system by selecting the optimal configuration for the solar array and battery pack. Firstly, we will explore the possible system configurations with corresponding electrical parameters. Then, we will investigate the power losses in the different modules of the EPS which are the solar array, battery pack and DC/DC converters. Finally, we will compute and select the optimal configuration, and investigate the effects on the power system.

5.4.1 System configurations

We have computed the number of cells needed, now we should select the connection type of the cells. There are only two types of connection possible that are the parallel connection or series connection. The parallel connection has the effect of summing the supplied currents while the series connection has the effect of summing the voltages. We have listed all the possible configurations for the battery pack in table 5.4 and for the solar array in table 5.5.

Configuration	**Battery voltage $V_{b,nom}$ [V]**	**Battery capacity C_{nom} [Ah]**
1p 12s	43.8	4
2p 6s	21.9	8
3p 4s	14.6	12
4p 3s	10.95	16
6p 2s	7.3	24
12p 1s	3.65	48

Table 5.4: Battery configurations with corresponding nominal voltage and current

Configuration	**Voltage $V_{mp,nom,sa}$ [V]**	**Max. current $I_{mp,nom,sa}$ [A]**
3p 65s	156.39	1.44
4p 48s	115.49	1.92
5p 38s	91.43	2.4
6p 32s	76.99	2.88
7p 28s	67.37	3.36
8p 24s	57.74	3.84
9p 22s	52.93	4.32
10p 19s	45.71	4.8
11p 18s	43.31	5.28
12p 16s	38.50	5.76
13p 15s	36.09	6.24
14p 14s	33.68	6.72
15p 13s	31.28	7.2
16p 12s	28.87	7.68
18p 11s	26.47	8.64
19p 10s	24.06	9.12
22p 9s	21.65	10.56
24p 8s	19.25	11.52
28p 7s	16.84	13.44
32p 6s	14.44	15.36
38p 5s	12.03	18.24
48p 4s	9.62	23.04
65p 3s	7.22	31.2
95p 2s	4.81	45.6
190p 1s	2.41	91.2

Table 5.5: Array configurations with corresponding nominal voltage and current

5.4.2 Power losses in solar array

The only source of power dissipation in the solar array is the blocking diode which is connected in series with each string of solar cells as represented in figure 5.17. As a reminder, the blocking diodes are used to prevent the current generated by a solar cell flowing back through a weaker or shadowed network. Then these diodes exhibit power dissipation proportional to the current flowing through the diode and to the forward voltage of the diode. Then, we can compute the total power losses in the solar array using the following equation:

$$P_{loss,sa} = n_{par,sa} \cdot V_F \cdot I_{par,sa} = \frac{P_{sa} \cdot V_F}{V_{cell,sa} \cdot n_{ser,sa}} \tag{5.9}$$

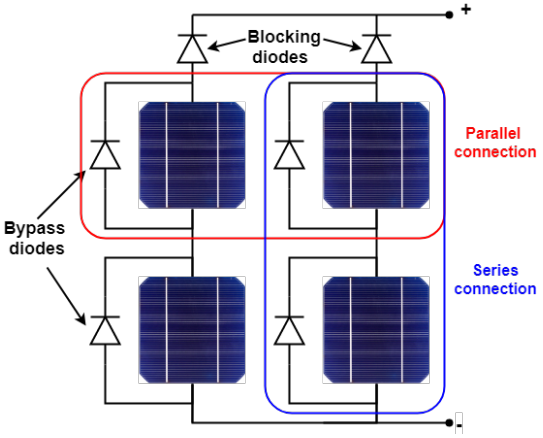

Figure 5.17: 2p 2s configuration of the solar array

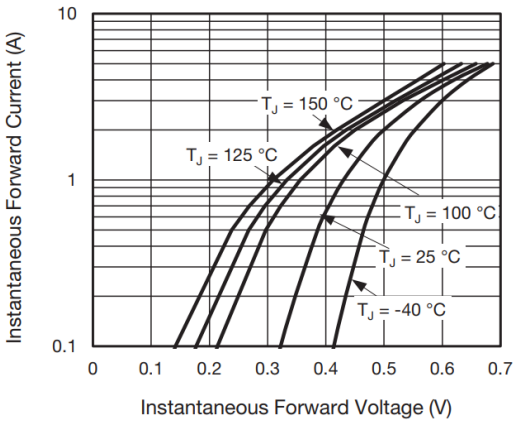

Figure 5.18: Instantaneous forward characteristic of SS1FL4 diode from Vishay [24]

The forward voltage is an intrinsic parameter of the diode. Then, we have to select for each configuration a diode that exhibits the lowest forward voltage while satisfying the electrical constraints that are the maximum reverse voltage, maximum average forward current and peak forward current. Therefore, we constructed a database which makes a list of all the Schottky diodes that are manufactured by Vishay, an important electronic device manufacturer. In the Vishay site, the listed diodes can be found in the tab Products → Diodes and Rectifiers → Schottky [43]. From this database, we computed the losses for each diodes and selected the diode which resulted in the least power losses.

From the equation (5.9), we can note that series configurations are favored as the number of blocking diodes in these configurations is lower, as we can observe in figure 5.19. But one factor has been neglected which is that the forward voltage is dependent on the forward current as we can observe in figure 5.18. Therefore, the power losses in configurations with numerous series connection should be higher than represented.

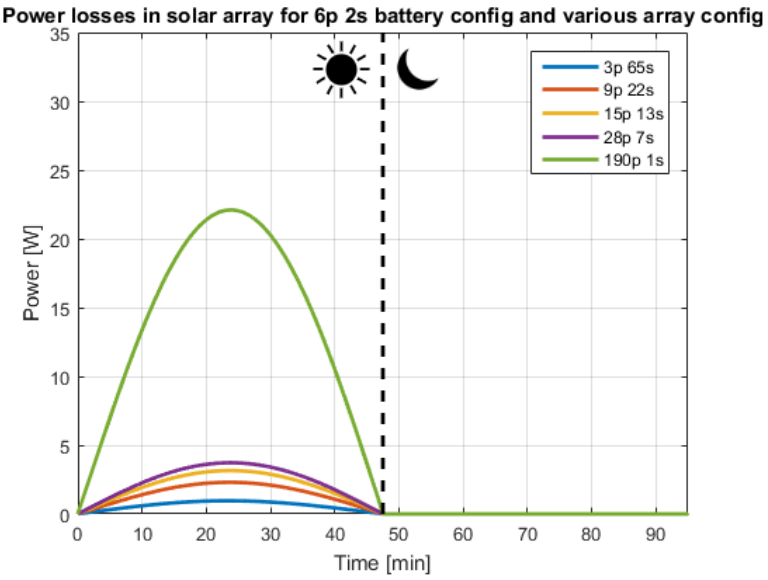

Figure 5.19: Internal power losses in solar array for 6p 2s battery configuration

5.4.3 Power losses in battery pack

The Li-ion battery is a non-ideal source of energy as it exhibits internal power losses. A storage technology is characterized by conduction losses and leakage losses. As explained in section 4.1, Li-ion batteries are only characterized by conduction losses which is modeled by an internal series resistance dissipating a part of the power flowing through it. Battery cells are connected in series and/or in parallels to form a battery pack. A battery pack configuration is represented in figure 5.20.

The value of the internal resistance ($25m\Omega$) can be found in the datasheet of the selected battery cell (cfr. Appendix A). Therefore, we can compute the power dissipation inside the battery pack:

$$P_{loss,b} = R_{int} \cdot n_{cell,b} \cdot (\frac{I_b}{n_{par,b}})^2 = \frac{R_{int}}{n_{cell,b}} \cdot (\frac{P_b}{V_{cell,b}})^2 \tag{5.10}$$

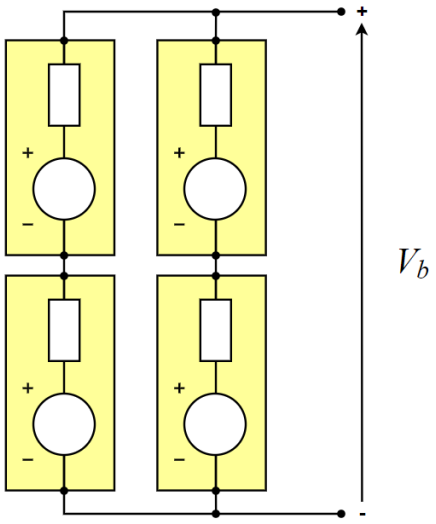

Figure 5.20: 2p 2s configuration of the battery pack

From the equation (5.10), we can conclude that the power dissipation are independent of the battery configuration. we can verify this hypothesis with figure 5.21 which represents the battery power dissipation over time for every configurations. Therefore no configuration is favored when considering the internal battery losses but the battery configuration has a significant effect on the power losses in DC/DC converters.

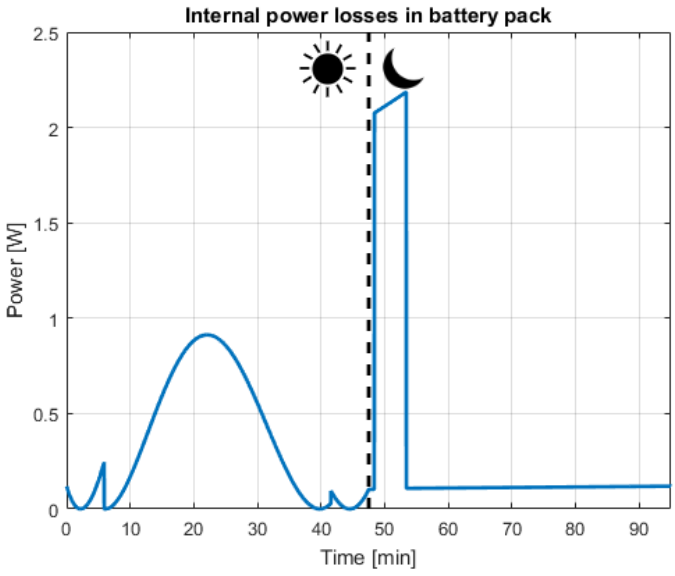

Figure 5.21: Internal power losses in battery pack

5.4.4 Power losses in DC/DC converter

The last modules constituting the EPS are the DC/DC converters which are divided into three topologies. The buck topology is used to step down the voltage level, the boost topology is used to step up the voltage level and the buck-boost converter can either step up or down the voltage level. The three topologies are represented in figure 5.22 and we can observe that they are implemented with the same components, thus the power dissipation is expressed in the same way. Note that the buck-boost have two times the number of transistors and diodes.

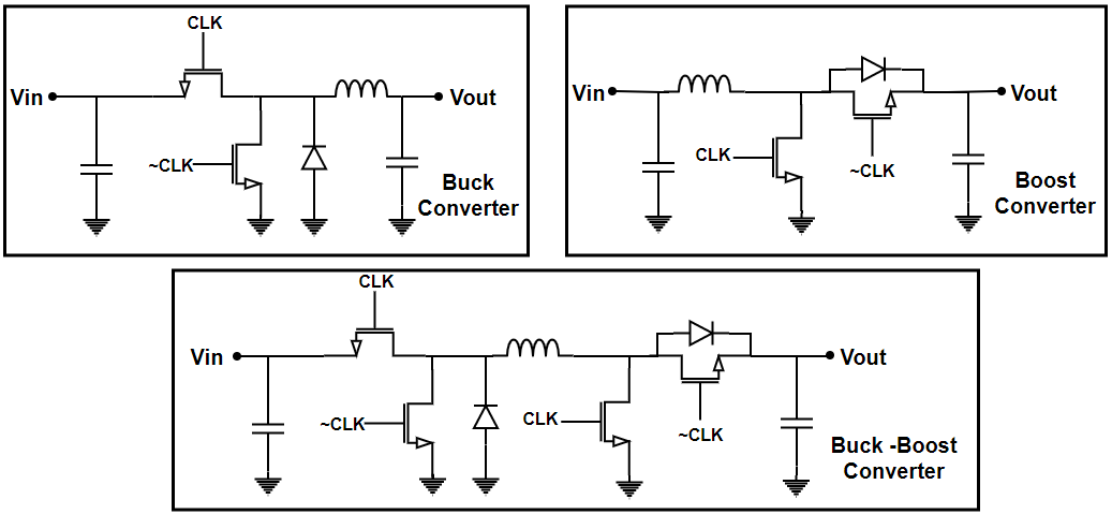

Figure 5.22: Buck topology on top left, boost topology on top right and buck-boost topology on bottom

These electrical components exhibit non-idealities resulting in power dissipation. For instance, the inductor exhibits a resistive behavior due to the intrinsic resistance of copper wire and the metallic contacts (ESR_L). Evenly, the capacitor has a resistive behavior due to the metallic contacts (ESR_C). The diode also produces conduction losses due to its forward voltage (V_F). Finally, MOS transistors produce conduction loss due to the drain-to-source resistance in active mode ($R_{ds,on}$), switching loss due to finite switching time (t_{rr}) and gate loss due to parasitic gate capacitance (Q_g). Here below is the loss equation for all components:

- 2 MOSFETs losses: $P_{MOS} = \underbrace{I_L^2 \cdot R_{ds,on} \cdot (1 - DT)}_{\text{conduction loss}} + \underbrace{V_{sw,max} \cdot I_L \cdot t_{rr} \cdot f_{sw}}_{\text{switching loss}} + \underbrace{2 \cdot V_{gs} \cdot Q_g \cdot f_{sw}}_{\text{gate loss}}$
- Diode conduction loss: $P_D = V_F \cdot I_L \cdot DT$
- Inductor conduction loss: $P_I = I_L^2 \cdot ESR_L$
- Capacitor conduction loss: $P_C = I_{cap,RMS}^2 \cdot ESR_C$

Now, we can design each converter based on specifications and flux profiles, and at last we can compute the losses in the converters for each configurations. The specifications and design equations are expressed below. The design of the buck-boost consists of a combination of design equations of buck and boost converter.

- Specifications:

$$f_{sw} = 300\text{kHz}$$
$$\Delta V_{out} = 20\text{mV}$$
$$\Delta I_L/I_L = 20\ \%$$
$$DT = 100\text{ns}$$

- Design of buck converter:

$$D = \frac{V_{out}}{V_{in}}$$
$$L = \frac{(V_{in}-V_{out})\cdot D\cdot T_{sw}}{\Delta I_L}$$
$$C = \frac{\Delta I_L\cdot T_{sw}}{8\cdot\Delta V_{out}}$$

- Design of boost converter:

$$D = 1 - \frac{V_{in}}{V_{out}}$$
$$L = \frac{V_{in}\cdot D\cdot T_{sw}}{\Delta I_L}$$
$$C = \frac{I_{L,max}\cdot D\cdot T_{sw}}{\Delta V_{out}}$$

Now from the Spice library, we can select the capacitor and inductor based on their computed value while satisfying the voltage and current ratings and exhibiting the minimal ESR value. The selection of the diode is based on the same process as explained in section 5.4.2. The MOSFETs have been selected from the Vishay database (in tab Product → MOSFETs → Automotive [44]). The MOSFETs are selected by satisfying the voltage and current ratings and minimizing the total power losses. For instance, there is a trade-off between the drain-source resistance ($R_{ds,on}$) and total gate charge (Q_g) as these two parameters are tightly linked. This can be observed in figure 5.23 where each point represents a different MOSFET. The gate losses are dominant when the resistance value is low while the conduction losses are dominant for large resistance value, therefore there is a resistance value that minimizes the total power dissipation.

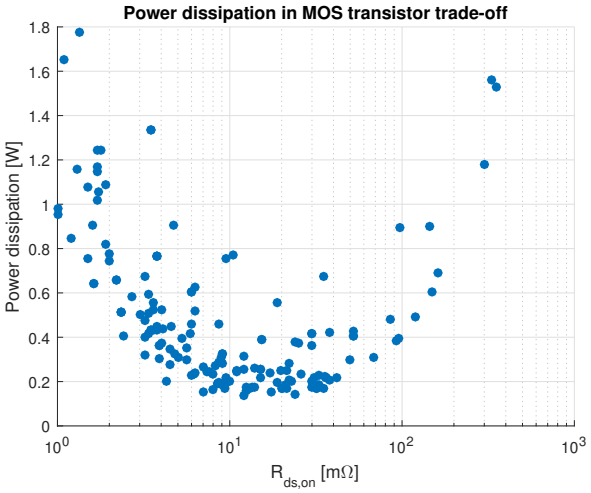

Figure 5.23: Power dissipation in different MOS transistors at $f_{sw} = 300kHz$, $I_{load} = 2A$ and $DT = 100ns/Tsw$

At last, we can compute the power dissipation in the converters for each configuration. We can conclude that if the input and output voltage levels are close, the power losses are small but if these voltages intersect, a buck-boost topology should be considered leading to higher dissipation. We can observe in figure 5.25 where configurations with few series connection are favored as they are closer to the 3 regulated output voltages. Note that the power dissipation in solar converters (5.24) is only shown for one battery configuration but generally, configurations with few series connections are favored in terms of power dissipation.

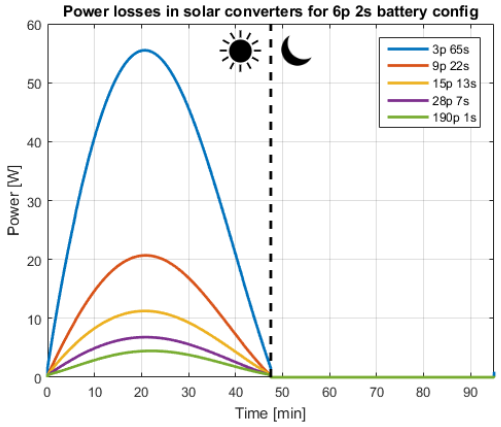

Figure 5.24: Power losses in solar converters for different solar array configurations

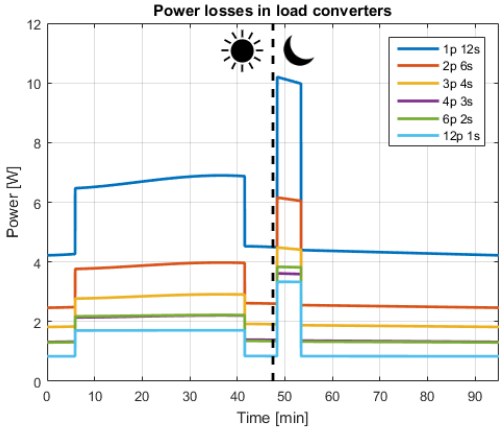

Figure 5.25: Power losses in load converters for different battery configurations

5.4.5 Energetic optimization

The main challenge in the energetic optimization is the selection of the DC/DC converter topology. Hence, there are three different topologies explored in this chapter. The buck converter and boost converter are preferred as they use less components, and therefore induce less power dissipation. Although, these topologies cannot be used in every configurations due to their constraints.

The buck can only be used to step down the voltage level while the boost converter can only be used to step up the voltage level. The figure 5.26 shows the total power losses when considering only the buck topology for solar converters. We can observe that low voltage solar arrays ($< 5V$) are not achievable but the losses become smaller when considering low voltage configurations. We can also observe that the solar array configurations with voltage around 20V are the most efficient.

Similarly, the figure 5.27 shows the total power losses when considering only the boost topology for solar converters. We can observe that high voltage solar arrays ($> 35V$) are not achievable but the losses become smaller when considering configurations with voltage around 15V. We can note that there are few configurations with only boost topology as the number of battery configurations is limited.

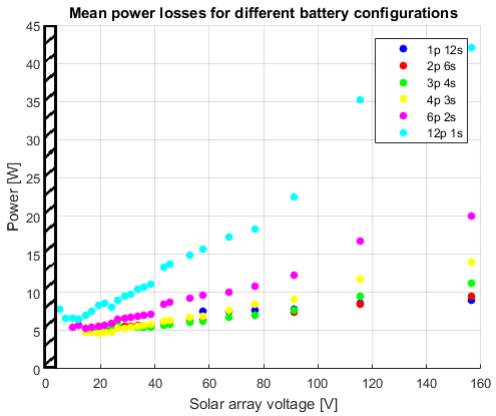

Figure 5.26: Optimization with only buck converters as solar converters

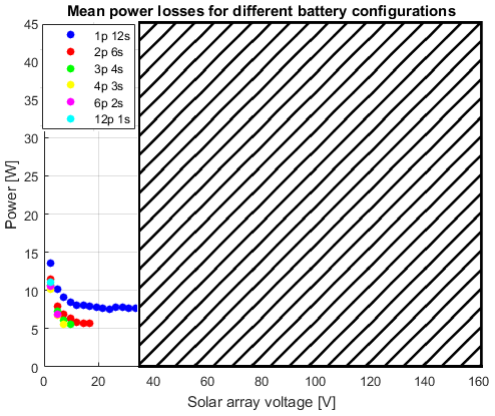

Figure 5.27: Optimization with only boost converters as solar converters

One way to conciliate high and low voltage solar arrays is to consider the buck-boost topology as this topology can either step up or down the voltage level. Therefore, any configuration is achievable with buck-boost converters but at the cost of increased power losses. The figure 5.28 represents the total power losses for every configurations when considering only buck-boost converters. We can observe that the power dissipation for buck-boosts ($\approx 7W$ for best configurations) is higher than the power dissipation for bucks or boosts ($\approx 5W$ for best configurations).

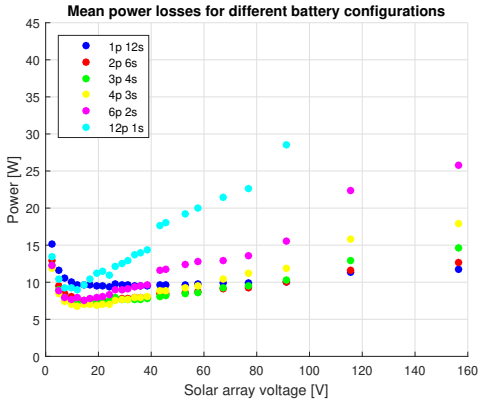

Figure 5.28: Optimization with only buck-boost converters

In order to optimize at best, we should take a combination of buck and boost converters and preferably avoid the buck-boost topology. The optimization is therefore the determination of the Pareto front and is determined by considering the best solutions from figures 5.26, 5.27 and 5.28. Once the Pareto front is determined, we can at last select a configuration resulting in the least average power dissipation. The Pareto front has been drawn in figure 5.29 for all configurations.

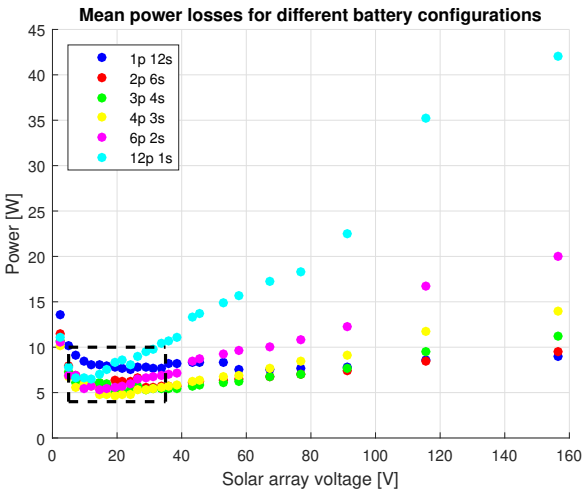

Figure 5.29: Total mean power losses with respect to the solar array voltage for different battery configurations

From this figure, we can observe the most efficient configurations are located around 20V of solar array voltage. The optimum is located in this range as the number of blocking diodes and the gap between the input and output voltage are kept low. Lower voltage configurations are less efficient as the number of blocking diodes is soaring while high voltage configurations are less efficient due to the large gap between input and output voltage of the converters.

The figure 5.30 gives a better look at the interesting configurations. From this figure, we can conclude that the optimal configuration in terms of power dissipation is 10.95V battery voltage (4p 3s) and 19.25V solar array voltage (24p 8s) resulting in 4.69W of power dissipation (Configuration (1)). But one point to consider is the possibility of failure in the battery pack resulting in reduced battery capacity. If such problem occurs, we should reduce the payload operation so that the DOD is maintained to its design value of 20% for preserving the battery cycle life. In the optimal configuration, the payload should be reduced by 58.4% in case of failure (cfr. table 5.6). A design trade-off could be to select another configuration that results in less payload reduction at the cost of increased average power dissipation.

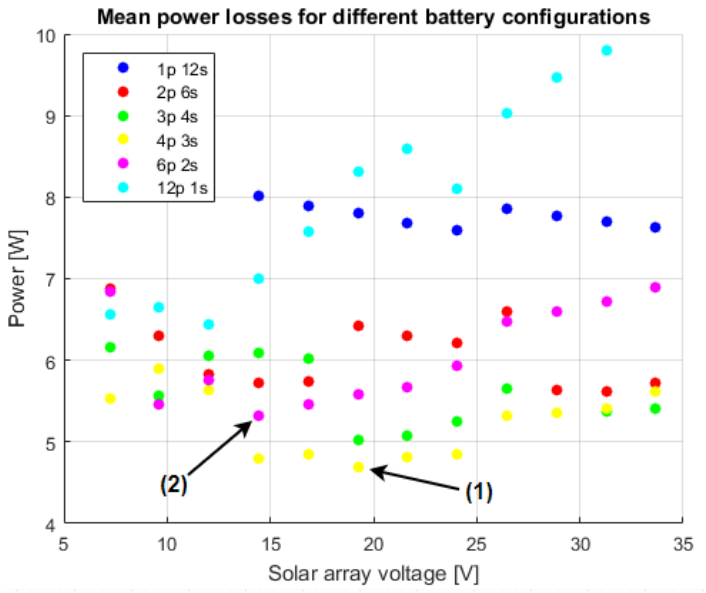

Figure 5.30: Zoom on the interesting solar array and battery pack configurations

Based on this trade-off idea, we finally selected another configuration that is 7.3V battery voltage (6p 2s) and 14.4V solar array voltage (32p 6s) resulting in 5.31W of power dissipation (Configuration (2)). This choice allows to reduce the payload reduction in case of failure to 38.9% (decrease of $\approx$ 20%) at the cost of 630mW (increase of $\approx$ 14%).

Configuration	Payload reduction [%]
1p 12s	233.7
2p 6s	116.9
3p 4s	77.9
4p 3s	58.4
6p 2s	38.9
12p 1s	19.5

Table 5.6: Payload reduction for each battery configuration in case of failure

We can draw the figure 5.31 which represents the generation profile and the power dissipation profile for the selected configuration. We can compute the average efficiency of the power system from these profiles. The average efficiency is evaluated at 89.0% which is relatively large compared to other state-of-the-art power systems. We can note that the red plateau at 50 min into the orbit corresponds to the transmitting mode consuming 70W on the 12V bus. We can also observe that the day mean losses (8.77W) are much larger than the night mean losses (1.89W).

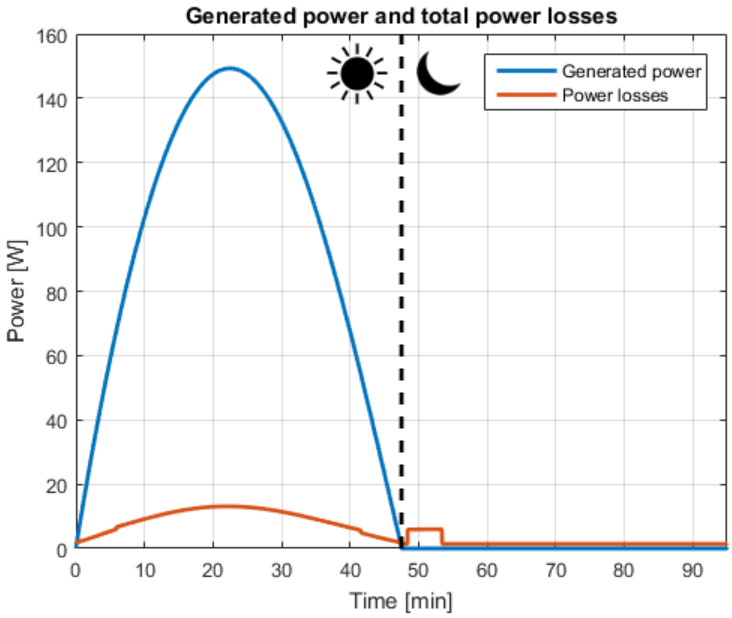

Figure 5.31: Generated power and total power losses for the selected configuration (7.3V battery voltage and 14.4V solar array voltage)

The configuration has been selected at last, therefore we can design the arrangement of the solar cells on the satellite faces. The solar array configuration is 32p 6s, then we will set 2× 11p 6s on the two deployable panels attached to edges FG and EH, and 10p 6s on the face EFGH (cfr. figure 5.1). We remove the cells located on the corners of the faces in order to make room for the clips that will hold the deployable panels and we also made sure that the arrangement is symmetric along the vertical axis. The designed arrangement is then represented in figure 5.32 where the black rectangles are the solar panels and the blue rectangles are the panel clips.

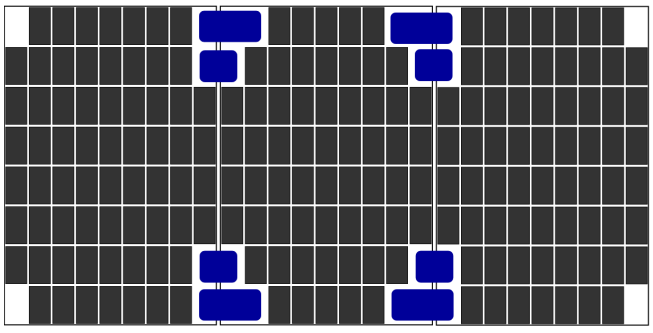

Figure 5.32: Solar array arrangement for optimal configuration

Now, we can analyze the losses distribution of the selected configuration with figure 5.33. We can observe that the main contributors are the MPPT regulators, load converters and the solar array. We can note that the main contributors have the same loss level meaning that the optimization goal is to equalize them to obtain the optimal configuration. The losses in the 5V converter are larger than in the other load converters because this bus exhibits the largest average load current. The battery pack losses are low and independent of the configuration.

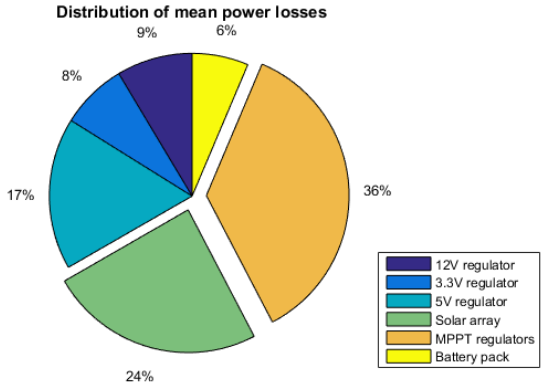

Figure 5.33: Distribution of the mean power losses

Then, we can analyze the differences between day and night power losses with figure 5.34. The losses in 3.3V bus, 5V bus and battery pack stay at the same level between day and night in absolute value (but increase relatively) while the 12V bus consumes less power during nighttime but nevertheless increases relatively. Finally, the MPPT regulators and solar array are the main contributors during daytime while they are almost zero during nighttime. This comes from the fact that in nighttime, they are disabled and only power leakage is present.

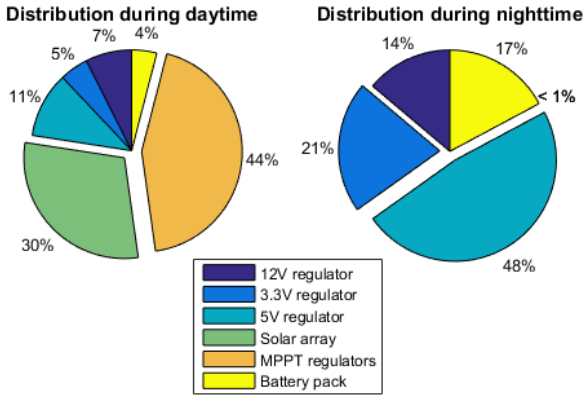

Figure 5.34: Comparison of distribution between daytime and nighttime

Following the configuration selection, we can compute the solar array and battery pack voltage ranges. These ranges are represented in figure 5.35. The solar bus voltage is evaluated between 11.7V and 17.4V while the battery bus voltage between 7V and 7.6V. These ranges do not intersect fortunately otherwise buck-boost converters should be used which have more components than basic buck or boost topology resulting in higher power dissipation.

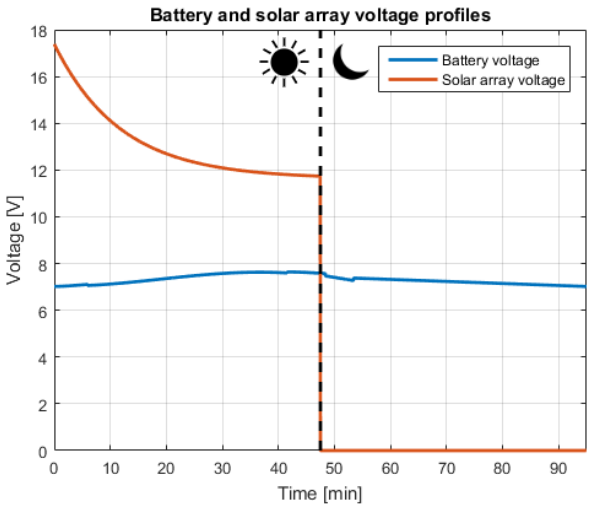

Figure 5.35: Battery pack and solar array voltage profiles for the selected configuration

Finally, we can assign the topology and average efficiency of each converters present in the EPS. Then, we can also complete the EPS architecture with bus voltage ranges, all the information are represented in figure 5.36.

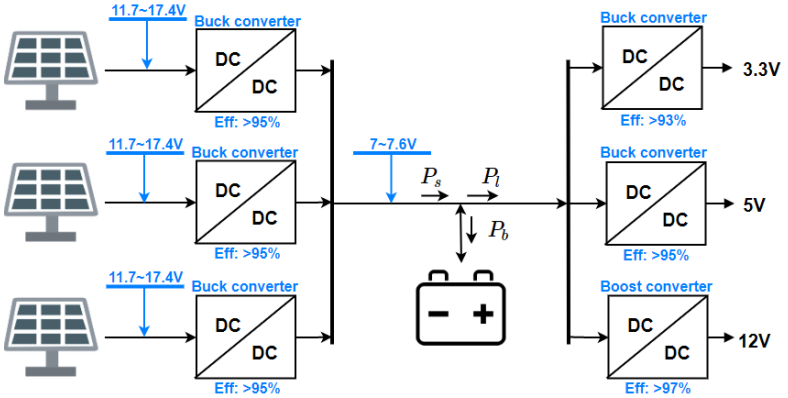

Figure 5.36: Selected EPS architecture with bus voltage ranges and converters topology

Chapter 6

System Implementation and Failure Analysis

In the previous chapter, we have studied and optimized the system configuration by reducing the power losses in each module. From this study, the solar array and battery pack have been sized and configured based on efficiency and system degradation upon failures. This chapter is focused on the implementation of the EPS which is performed in two design iterations. The first iteration consists in a basic system design focused on functionality while the second iteration is focused on system reliability and robustness.

In the first section, the control logic and sensors are selected and implemented with connection diagrams. Afterwards, an overview of the potential failure causes is provided with a special attention to radiation induced effects. Next section will be dedicated to the Failure Mode, Effects and Criticality Analysis which is introduced and then performed on the EPS. In the final section, extra compensation actions will be implemented for reducing the risk level of the most critical failures.

6.1 Components selection

This section is dedicated to the component selection for implementing the critical functions of the EPS. The components have been selected from the Texas Instruments product library. Texas Instruments is preferred to other manufacturers as they provide a wide choice of analog and digital solutions with handful documentation. Automotive rated devices are preferred as they exhibit a guarantee of quality while being cheap as they are manufactured in large quantities. But in the case where automotive devices do not satisfy the system requirements, space rated products can be considered despite their higher cost.

The global schematic of the EPS is represented in figure 6.1. A special care is taken to implement the satellite telemetry which is the monitoring of voltage and current in each bus of the EPS. The telemetry is an useful tool for the satellite developers to improve the system for further space missions while being useful of the micro-controller to detect potential failures and activate compensation methods. The telemetry is implemented by using a power monitor on each important bus.

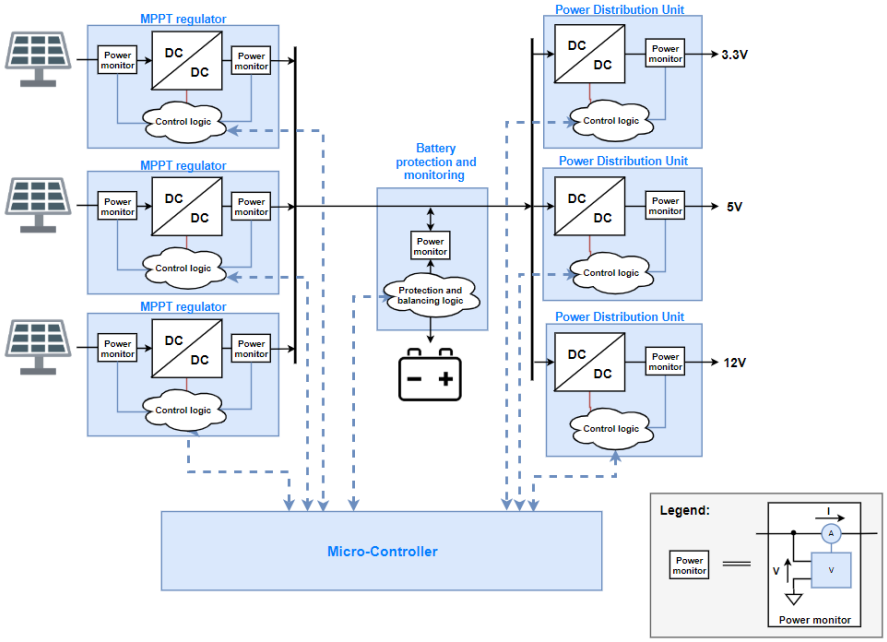

Figure 6.1: Implementation of the satellite telemetry

6.1.1 MPPT Regulator

The first main module of the EPS is the MPPT regulator which is responsible for conditioning the solar panel power, sampling the solar panels parameters, and controlling the array OP based on a temperature based MPPT algorithm. This module is therefore composed of blocking diodes, temperature sensors, power monitors, DC/DC converters and gate drivers. The implementation diagram of one channel is represented in figure 6.2.

The blocking diodes are used to prevent a solar network from supplying power to a shadowed or damaged solar network and therefore improve system efficiency. This type of event is most likely to occur during a 2-year term mission. The MPPT algorithm requires temperature, voltage and current measurements of the solar panel to optimally operate.

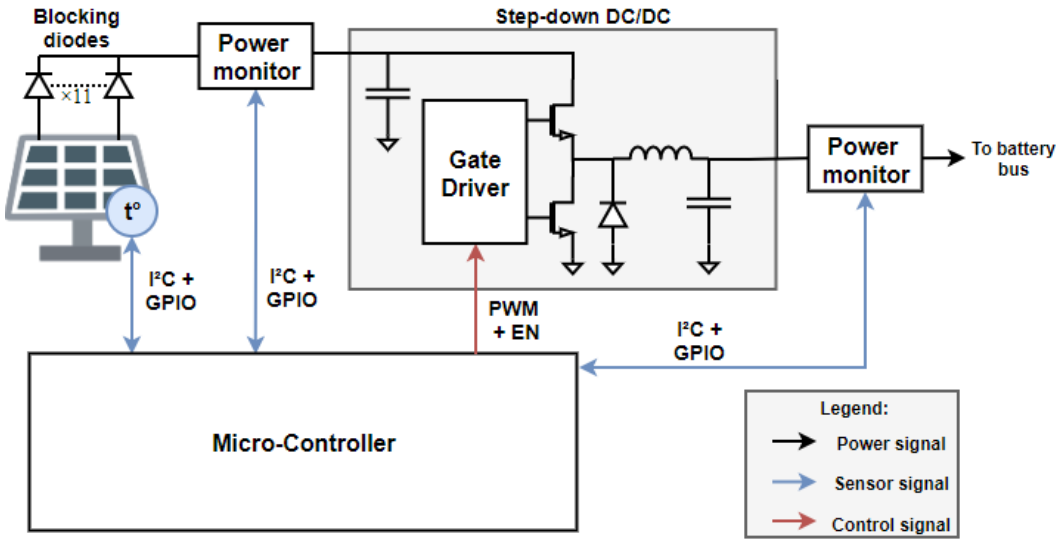

Figure 6.2: Implementation of the MPPT regulator

The step-down DC/DC converter is used to set the operating point of the solar panel and to transfer the generated power to the battery bus. The gate driver is used to increase the drive strength of the PWM control signal as the PWM generated by the micro-controller has a weak driving strength. The sensor and control signals are controlled by the micro-controller and its selection will be done in section 6.1.4.

The selection and implementation of the blocking diodes and the DC/DC converters has already been performed in the energetic optimization chapter (Chapter 5). However we can note that the electrical ratings of these components have been selected with a safety factor of 2 as large transients are most likely to occur.

Temperature Monitoring

Temperature monitoring is necessary to implement an optimal MPPT algorithm. Therefore a temperature monitor is necessary to measure the temperature of the solar panel and transfer the information to the micro-controller. We selected digital sensors that withstand temperatures ranging from $-60°C$ to $+150°C$, and digital sensor as it is easier to interface them with the micro-controller. We also decided to use the I^2C bus for interfacing the sensor because this protocol is compact as it only needs two wires, robust as it ensures that the data sent are received, supports multiple masters and slaves on the same bus, and is less susceptible to noise.

The solar panel temperature monitoring will be performed by the space rated TMP461-SP sensor. The TMP461-SP is a 3.3-V Digital Temperature Sensor with Two-Wire Interface and Alert. The sensor electrical implementation is represented in figure 6.3. The sensor is set to the continuous conversion mode under nominal temperature conditions. The I^2C bus in fast mode allows the sensor and the micro-controller to interface together at high rates.

The sensor is powered by connecting VS to the 3.3V bus and GND to ground while the SDA and SCL are the data and clock lines of the I^2C bus respectively. We can connect up to 9 devices on the same I^2C bus with configurable addresses using pins A0 and A1 and we selected the addresses 0x4E, 0x4F and 0x50. The $\overline{ALERT}$ and $\overline{THERM}$ pins toggle when the sensor is operating outside the configurable temperature limits and is connected to GPIOs of the micro-controller. If the solar panels comes to operate outside the operating range, the $\overline{ALERT}$ pin will be used to protect the sensors by setting the shutdown mode. The D+ and D- pins can be used to connect a remote analog temperature sensor but are grounded as this feature is not used.

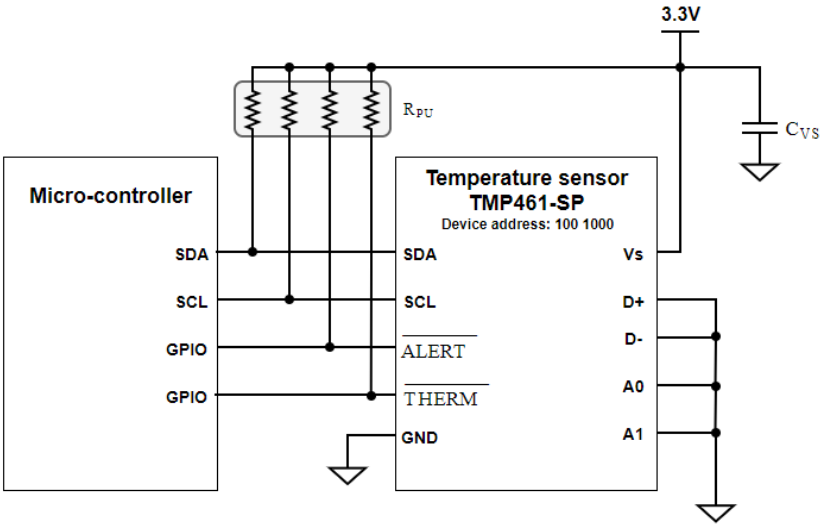

Figure 6.3: Temperature Monitoring using the TMP75C-Q1 device

Component	Value	Purpose
R_{PU}	$10k\Omega$	Pull-up resistor for I^2C communication
C_{VS}	$0.01\mu F$	Bypass capacitor for supply stability

Table 6.1: External components selection for Temperature Monitoring

Power monitors

The next component of the MPPT regulator is the power monitor used to measure the voltage and current on the channel and transfer to the data the micro-controller. The system requires that the monitor should sense voltages up to 17.4V and currents up to 5.2A. Therefore, we selected the INA226-Q1 due to the high-side capability, low quiescent current and high accuracy. We decided to use the I^2C bus to interface with the micro-controller because the I^2C protocol is less sensitive to noise and efficient even with long cables knowing that the power monitor will most likely be located on a different PCB. The I^2C address can be programmed with up to 16 addresses, which is sufficient to connect all the power monitors on a single I^2C bus, then we selected addresses ranging from 0x41 to 0x4C. The measurements are monitored at low rates, therefore the device is set to averaging mode resulting in higher precision results.

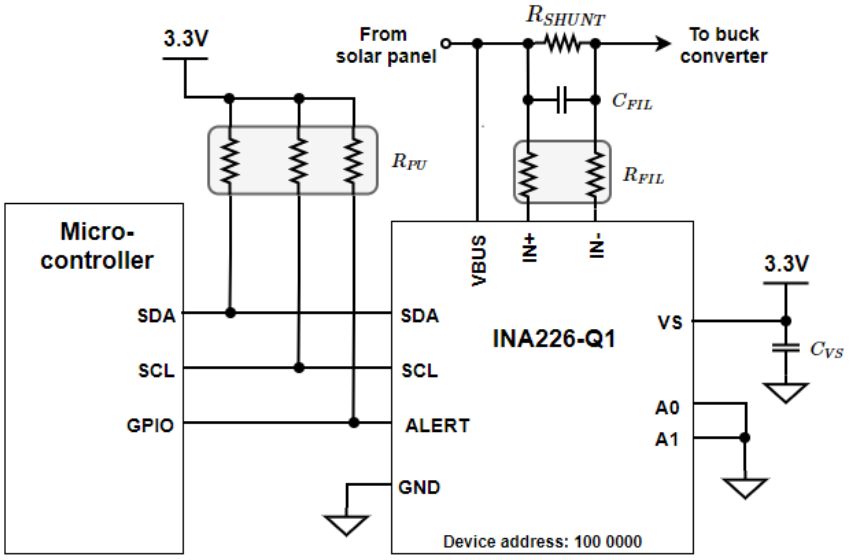

Figure 6.4: Power Monitoring using the INA226-Q1 device

Component	Value	Purpose
R_{PU}	$10k\Omega$	Pull-up resistor for I^2C communication
C_{VS}	$0.01\mu F$	Bypass capacitor for supply stability
R_{SHUNT}	2Ω	Shunt resistor for current sensing
R_{FIL}	10Ω	Filter resistor for noise filtering
C_{FIL}	$0.1\mu F$	Filter capacitor for noise filtering

Table 6.2: External components selection for Power Monitoring

The sensor is powered by connecting VS to the 3.3V bus and GND to ground while the SDA and SCL are the data and clock lines of the I^2C bus respectively. The A0 and A1 pins are used to configure the device I^2C address. The power monitor comes also with the possibility to implement a filter for the current sensing as the current signal is susceptible to noise. The filter is implemented with RC filters connected to the IN+ and IN- pins. The cut-off frequency of the filter should be lower than the internal sampling frequency for optimal filtering. The shunt resistor experiences a small voltage drop that can be monitored to obtain channel current measurements. The shunt resistor should be carefully designed so that the power dissipation is low while the sensor range is wide. The VBUS pin is used to measure the bus voltage and is connected directly to the bus.

The INA226-Q1 comes with one alert signal that will be connected to a GPIO of the micro-controller. The ALERT signal can monitor up to five alert functions such as under-voltage, over-voltage, under-current, over-current and over-power. Therefore, the ALERT signal can be used to detect short-circuit in the DC/DC converter or detect a failure in the solar panel.

Gate drivers

The last component which is required to implement the MPPT regulator is the Gate Driver. As the driving strength of the PWM from the micro-controller is limited, we selected a gate driver whose function is to output 2 complementary PWM signal with a configurable dead time that will drive the high-side and low-side MOSFETs of the DC/DC converter. Therefore, the role of the gate driver is to output, from one PWM signal, 2 stronger complementary PWM signals which are able to correctly drive the MOSFET gates.

We selected the UCC20225-Q1 Isolated Dual-Channel Gate Driver as it exhibits useful features such as Disable pin, Configurable Dead Time, Dual Complementary Channel and PWM input. The driven MOSFETs are the 40V-SQJA88EP Automotive MOSFETs that will be driven with 12V at 300kHz. Therefore the VDDA and VDDB pins will be connected to the 12V bus voltage and the device logic is supplied with 5V. Note that the output A requires a bootstrap circuit as it drives a high-side MOSFET. The bootstrap circuit is necessary to bias the gate voltage of the high-side MOSFET referenced to the switching node. The most popular and cost effective way to implement the bootstrap circuit is to use a diode, a resistor, a capacitor and a bypass capacitor. The component values have been selected to limit the inrush bootstrap current to 4A.

The PWM pin is connected to the ePWM output of the micro-controller through a filter in order to obtain a stable PWM signal. The filter corner frequency should be higher than the switching frequency of the transistor (300kHz) so that the PWM distortion is limited. The transistor features a rise and fall time of 10ns, therefore we selected a dead time of 50ns which is sufficient to avoid the simultaneous activation of both MOSFETs. The DIS pin will shutdown the outputs reducing power consumption during nighttime.

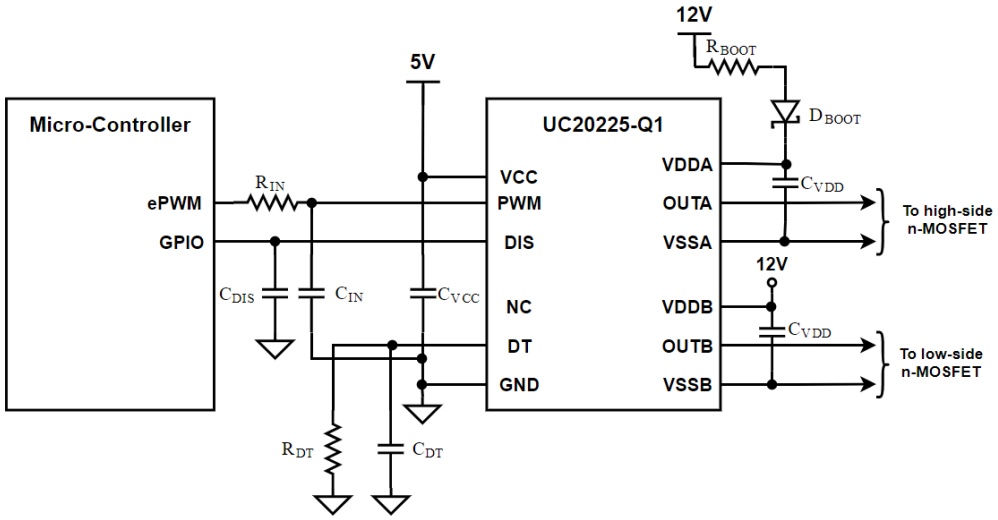

Figure 6.5: Gate driver implementation using the UC20225-Q1 device

Component	Value	Purpose
R_{IN}	51Ω	PWM filter resistor for noise filtering
C_{IN}	$33pF$	PWM filter capacitor for noise filtering
C_{VCC}	$0.1\mu F$	Decoupling capacitor for supply stability
C_{DIS}	$1nF$	DIS filter capacitor for noise filtering
R_{DT}	$5k\Omega$	Dead time setting resistor
C_{DT}	$2.2nF$	Capacitor for better noise immunity and DT matching
C_{VDD}	$2\mu F$	Decoupling capacitor for gate voltage stability
R_{BOOT}	3Ω	Resistor for limit inrush bootstrap current
D_{BOOT}	SS1FL4	Diode for limit inrush bootstrap current

Table 6.3: External components selection for Gate Driver

6.1.2 Battery protection and monitoring

The battery pack is a critical component of the EPS as the satellite cannot operate without a battery pack. The batteries are fragile and susceptible to over-voltage, over-current and over-temperature failures. Therefore, we should protect the battery pack and monitor its parameters in order to make the system robust and failure-free. The battery monitoring should also include a cell balancing circuit which is used to equalize the cell voltage in order to increase the battery cycle life and protect the batteries from over-voltage condition.

The battery protection is implemented with smart-power switches that will monitor the voltage, current and temperature of the battery as well as set the current limit protection. The battery cells will be connected in packs of 2-parallel 2-series cells so that the logic area and power consumption are limited while reducing the system losses in case of cell failure. On each pack, a power monitor is connected to obtain the telemetry of the battery bus using the INA226-Q1 module (same device as used in the MPPT regulator). The implementation diagram of the battery protection and monitoring for one 2p-2s battery pack is represented in figure 6.6.

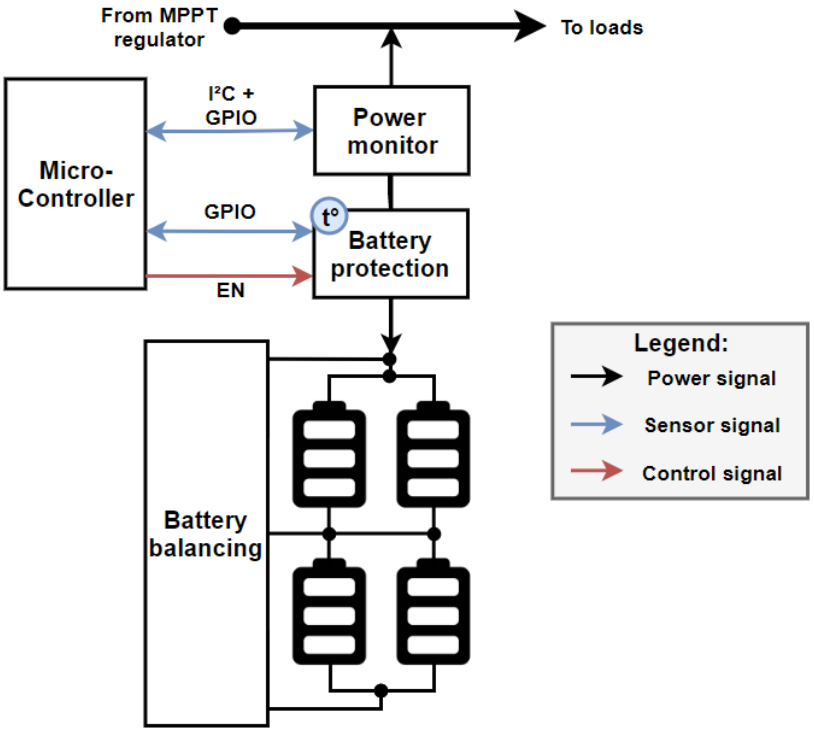

Figure 6.6: Battery monitoring schematic

Cell balancing

The cell balancing module will sense and compare the cell voltage, and then apply an additional current to the weaker cell in order to equalize the cell voltage. The selected cell balancing device is the Automotive rated BQ29209-Q1 Voltage Protection with Automatic Cell Balance feature.

The supply voltage is connected to the positive terminal of battery pack through a RC filter to obtain a stable power supply. The pin VC2 and VC1 are the balancing connections to the battery cells connected through a RC filter at 1.6kHz and the balancing current is set to 15mA. The Control Delay (CD) pin is used to set the desired delay (designed at 1s) for triggering the OUT pin which is toggling when the battery reaches the over-voltage limit. The $\overline{CB\_EN}$ pin is grounded so that the cell balance feature is always enabled.

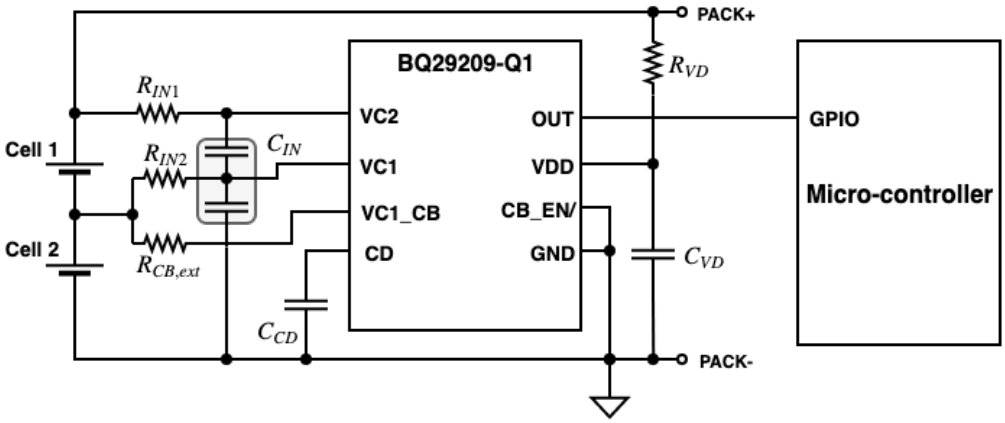

Figure 6.7: Battery Balancing using the BQ29209-Q1 device

Component	Value	Purpose
R_{IN1}	$1k\Omega$	Voltage monitor filter resistance of Cell 1
R_{IN2}	$1k\Omega$	Voltage monitor filter resistance of Cell 2
C_{IN}	$0.1\mu F$	Voltage monitor filter capacitance
$R_{CB,ext}$	120Ω	Cell balance setting resistor
C_{CD}	$0.1\mu F$	Delay time setting capacitor
R_{VD}	100Ω	Supply voltage filter resistor
C_{VD}	$0.1\mu F$	Supply voltage filter capacitor

Table 6.4: External components selection for Battery Balancing

Battery Protection

The Battery Protection module is implemented with the TPS1H100-Q1 Single-Channel Smart High-Side Power Switch. The smart switch exhibits important features such as adjustable current limit up to 10A, over-current protection, thermal shutdown and current/thermal diagnosis. The bus voltage and current measurement is performed by the channel power monitor.

The VBB and OUT pins are used to connect the bus to the battery pack through the switch while the IN pin is a digital pin that controls the switch state. The other pins will be connected to GPIOs of the micro-controller. DIA_EN is used to run a battery diagnosis with thermal and current faults. An interrupt signal on $\overline{ST}$ is toggling when operating in extreme conditions such as over-current or over-temperature. The CL pin is used to set the current limit to 6A which should be below the battery current rating. The module is protected from reverse voltage with a resistor and diode which are connected to the GND pin.

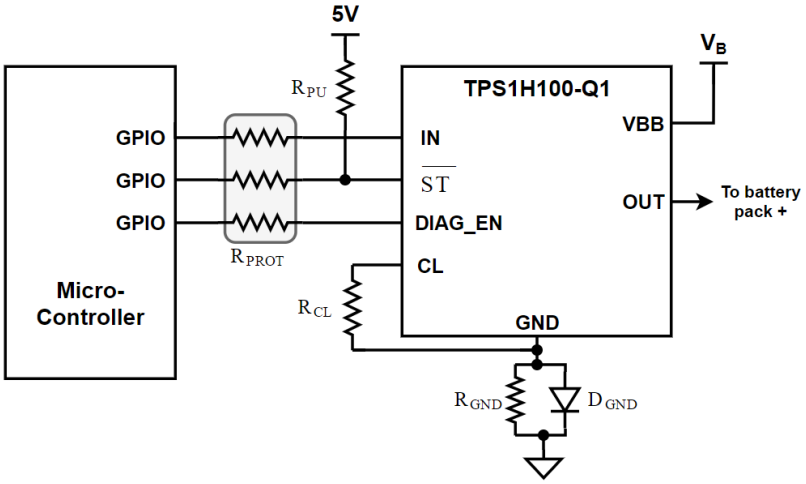

Figure 6.8: Battery monitoring and protection using TPS1H100-Q1

Component	Value	Purpose
R_{PU}	$15k\Omega$	Pull-up resistor for I^2C communication
R_{PROT}	$10k\Omega$	Micro-controller protection resistor
R_{CL}	400Ω	Current limit setting resistor
R_{GND}	$1k\Omega$	Reverse protection resistor for GND network
C_{GND}	V1P22	Reverse protection diode for GND network

Table 6.5: External components selection for Battery Protection

6.1.3 Power Distribution Unit

The Power Distribution Unit is responsible for supplying the loads with 3 regulated voltages of 3.3, 5 and 12V. The buses are regulated with DC/DC converters which are individually controlled by a PWM controller. The electrical power is supplied to the loads through switches which have the purpose of activate/deactivate the load and limit the load current.

The switches are the TPS1H100-Q1, also used in the Battery Protection module. The PWM controllers should be able to drive synchronous buck converter for the 3.3V and 5V buses and synchronous boost converter for the 12V bus. Power monitors are also implemented on each bus for satellite telemetry and failure detection using the INA226-Q1 module (same device as used in the MPPT regulator). The Power Distribution Unit of the 3.3V bus is represented in figure 6.9.

The selection and implementation of the DC/DC converters has already been performed in the energetic optimization chapter (chapter 5). However we can note that the electrical ratings of these components have been selected with a safety factor of 2 as large transients are most likely to occur.

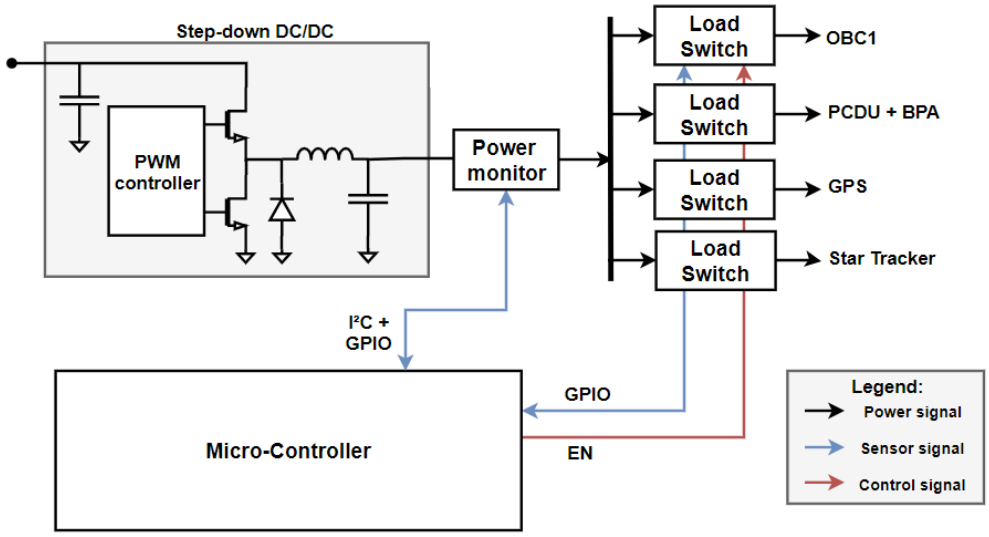

Figure 6.9: Power Distribution Unit of 3.3V bus schematic

PWM buck controller

The PWM controller operation is the measure of the actual output voltage and then the adaptation of the PWM signals which are driving the MOSFET gates such that the output voltage is controlled to the desired value. The PWM controller for the 2 buck converters is implemented with the LM25117 Wide Input Range Synchronous Buck Controller With Analog Current Monitor. This controller has been selected due to its wide input range, adaptive dead time, programmable current limit, over current protection and programmable Soft-start. The Analog Current Monitor feature is left unused as a power monitor with extended features is already implemented on the channel.

The PWM controller input VIN is connected to the battery bus while the VCC pin is connected to the 12V bus voltage so that the MOSFET gates are driven with 12V. The UVLO pin is used to protect the DC/DC converter against under-voltage condition. The RAMP pin is used to set the emulated current ramp. The use of emulated current ramp reduces the noise sensitivity of the PWM signal. The FB pin is used to set the output voltage while the COMP pin is used to obtain a more stable output voltage. The RT, RES and SS pins are used to set the switching frequency, restart time between hard failures and soft-start time respectively. The CS and CSG pins are used for the current monitoring of the DC/DC converter.

Component	Value	Purpose
R_{UV1}	$50k\Omega$	Start-up voltage setting resistor
R_{UV2}	$16.7k\Omega$	UVLO hysteresis setting resistor
R_T	$16.38k\Omega$	Oscillator frequency setting resistor
R_S	$8m\Omega$	Current sense resistor
C_{RAMP}	$820pF$	Ramp capacitor for noise sensitivity reduction
R_{RAMP}	$274.4k\Omega$	Ramp capacitor for noise sensitivity reduction
C_{BOOT}	$820pF$	Capacitor for limit inrush bootstrap current
D_{BOOT}	SS1FL4	Diode for limit inrush bootstrap current
C_{SS}	$47nF$	Soft start time setting capacitor
C_{RES}	$0.47nF$	Restart time setting capacitor
R_{FB1}	$3.24k\Omega$	Feedback resistor for output voltage setting
R_{FB2}	$1.05k\Omega$	Feedback resistor for output voltage setting
R_{COMP}	$2k\Omega$	Compensation resistor for stable voltage loop
C_{COMP}	$7nF$	Compensation capacitor for stable voltage loop
C_{HF}	$100pF$	Compensation capacitor for stable voltage loop

Table 6.6: External components selection for the 3.3V bus PWM controller

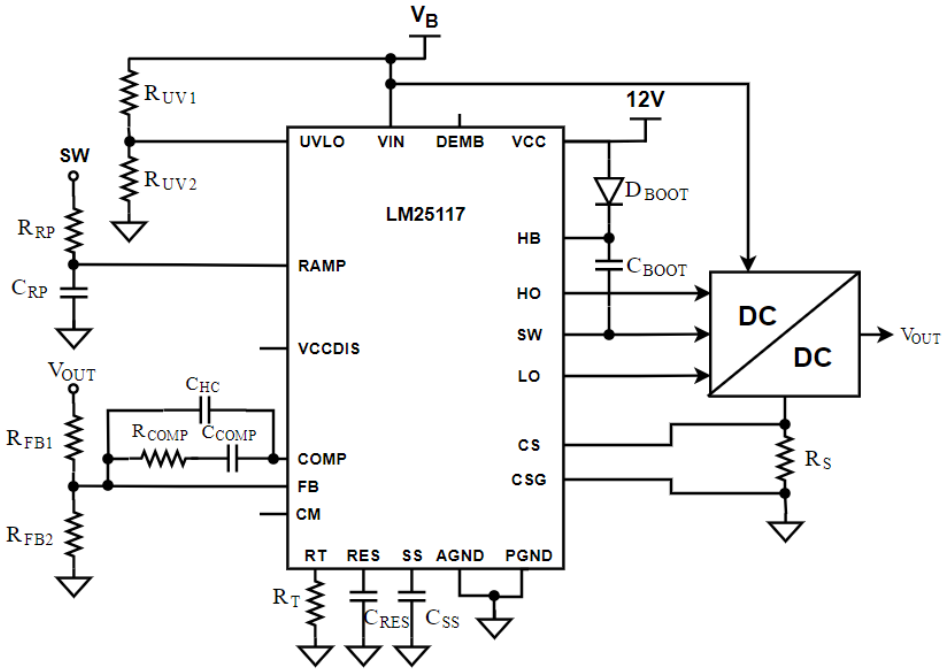

Figure 6.10: PWM controller implementation for buck converter using LM25117

PWM boost controller

The PWM boost controller has the same operation principle as the PWM buck controller except from the fact that it drives a boost converter instead of a buck. The PWM controller for the boost converter is implemented with the LM5122-Q1 Wide-Input Synchronous Boost Controller With Multiple Phase Capability. This controller has been selected due to its wide input range, adaptive dead time, programmable current limit, over-current protection and programmable Soft-Start.

The PWM controller input VIN is connected to the battery bus while the VCC pin is connected to the 12V bus voltage so that the MOSFET gates are driven with 12V. The UVLO pin is used to protect the DC/DC converter against under-voltage condition. The SLOPE pin is used to set the current of an artificial ramp for eliminating the sub-harmonic oscillations. The FB pin is used to set the output voltage while the COMP pin is used to obtain a more stable output voltage. The SYNCIN/RT, RES and SS pins are used to set the switching frequency, restart time between hard failures and soft-start time respectively. The CSP and CSN pins are used for the current monitoring of the DC/DC converter. Finally, the SYNCOUT pin provides 180° shifted clock output for an interleaved operation but is left floating as this feature is not used.

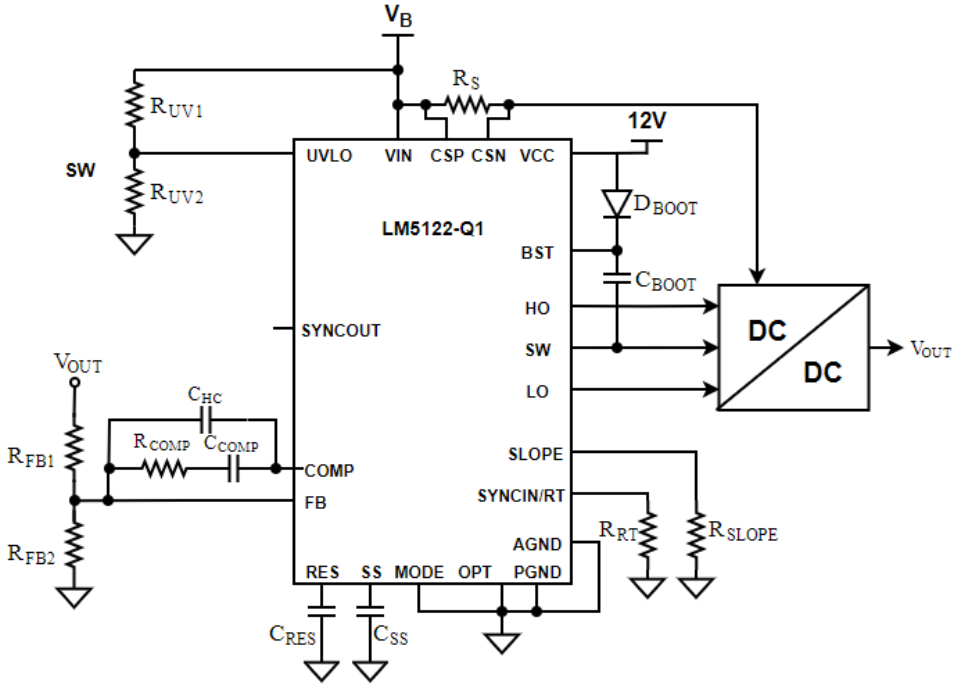

Figure 6.11: PWM controller implementation for boost converter using LM5122-Q1

Component	Value	Purpose
R_{UV1}	$50k\Omega$	Start-up voltage setting resistor
R_{UV2}	$16.7k\Omega$	UVLO hysteresis setting resistor
R_T	$30k\Omega$	Oscillator frequency setting resistor
R_{SLOPE}	$105k\Omega$	RAMP setting resistor for sub-harmonic oscillation
R_S	$8m\Omega$	Current sense resistor
C_{BOOT}	$820pF$	Ramp capacitor
D_{BOOT}	SS1FL4	Diode for limit inrush bootstrap current
C_{SS}	$47nF$	Soft start time setting capacitor
C_{RES}	$0.47nF$	Restart time setting capacitor
R_{FB1}	$3.24k\Omega$	Feedback resistor for output voltage setting
R_{FB2}	$1.05k\Omega$	Feedback resistor for output voltage setting
R_{COMP}	$2k\Omega$	Compensation resistor for stable voltage loop
C_{COMP}	$7nF$	Compensation capacitor for stable voltage loop
C_{HF}	$100pF$	Compensation capacitor for stable voltage loop

Table 6.7: External components selection for the 12V bus PWM controller

Load switches

The load switches are implemented with the TPS1H100-Q1 Single-Channel Smart High-Side Power Switch which are the same switches as used in the Battery Protection module. The smart switch exhibits important features such as adjustable current limit up to 10A, over-current protection, thermal shutdown and current/thermal diagnosis.

The implementation diagram and the definitions of the pins are already explained in the Battery Protection section. The external components selection for the load switches is therefore resumed in table 6.5 except for the current limiting resistor which value is depending on the load ratings. Therefore, the value of R_{CL} should be adapted to match the current rating of each load.

6.1.4 Micro-controller

The micro-controller is the most important module constituting the EPS. The micro-controller should be high-performance, automotive rated, highly reliable and robust against potential failures with memory protection features. An I^2C bus interface is required for obtaining the sensors measurements. The micro-controller should have also 3 independent PWM outputs for driving the MPPT regulators. The micro-controller should embed at least 64 GPIOs pins for monitoring and controlling the different devices. Finally, the micro-controller should be able to communicate with the OBC through a CAN bus to transfer satellite status, orbital position and attitude and other information.

Therefore, we selected the TMS570LC4357 Hercules Micro-Controller which is based on the ARM Cortex-R Core. The implementation diagram of the micro-controller is represented in figure 6.12 and the external component selection listed in table 6.8. TMS570LC4357 has dual-core lockstep CPUs with ECC-protected caches operating at up to 300MHz with a capacity of up to 500 MIPS. The device core supply is 1.2V while the supply for I/Os is 3.3V, therefore a Linear Drop-Out regulator (LDO) is required to generate the desired 1.2V. The device features also a voltage and clock monitoring module for fault detection. The TMS570LC4357 exhibits several memory protection features such as Memory Protection Unit (MPU), Real-Time Interrupt Timer (OS Timer), Two 2-Channel Cyclic Redundancy Checker (CRC) Modules and Error Signaling Module (ESM) with error pin for detecting and solving bit-flip failures.

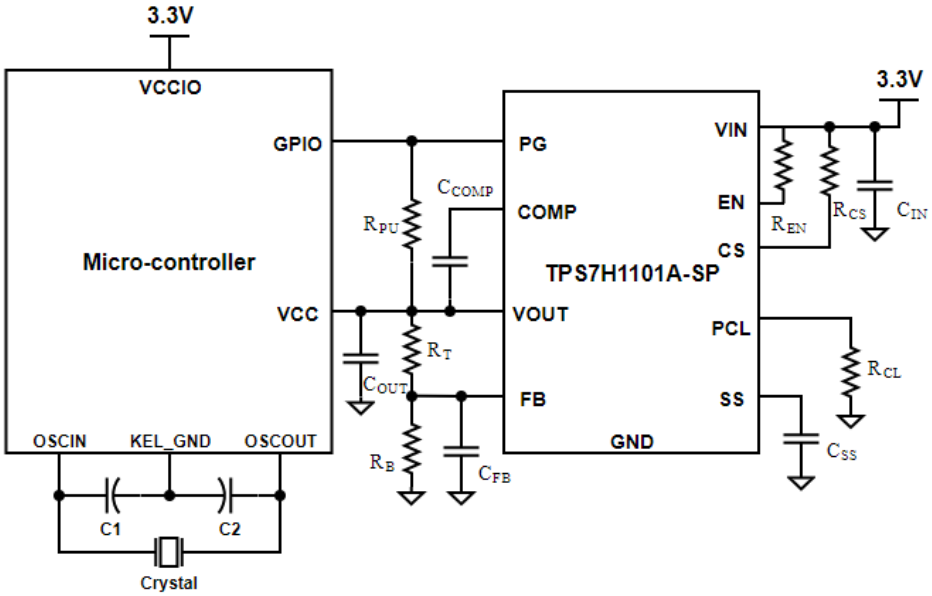

Figure 6.12: Micro-controller implementation using TMS570LC4357

Component	Value	Purpose
C_1	$30pF$	Oscillator capacitor for improved stability
C_2	$30pF$	Oscillator capacitor for improved stability
Crystal	XT46C	Crystal oscillator for main oscillator generation
C_{IN}	$22\mu F$	Input capacitor for supply stability
R_{CS}	$50k\Omega$	Current sense resistor for current foldback
R_{EN}	$15k\Omega$	Enable resistor for pin protection
R_{CL}	$30k\Omega$	Current limit setting resistor
R_{PU}	$10k\Omega$	Pull-up resistor for GPIO pin
C_{COMP}	$10nF$	Capacitor for improved transient response
R_T	$11.3k\Omega$	Top Output voltage setting resistor
R_B	$11.5k\Omega$	Bottom Output voltage setting resistor
C_{OUT}	$22\mu F$	Input capacitor for supply stability
C_{FB}	$22\mu F$	Feedback capacitor for LDO stability

Table 6.8: External components selection for the Micro-controller

The TPS7H1101A-SP has been selected to implement the LDO providing 1.2V for micro-controller core supply. The TPS7H1101A-SP is a radiation hardened LDO regulator with wide input range, low noise and important features such as Soft-Start, Power Good and Adjustable Current Limit. The implementation and external component selection is represented in figure 6.12 and table 6.8.

6.2 Potential failures of space electronic systems

The electronic systems designed for space missions must withstand a broad range of harsh conditions. For instance, the electronics should resist to shock and vibration during launch phase with potential chip damages. During the orbital phase, the electronics should also withstand the vacuum of space that could result in the outgassing of electronic devices. Furthermore, the electronic circuits are subject to a broad range of temperature. For instance, the electronics can be heated up to extreme temperature if located close to the rocket engines and also during orbital phase, the temperature can vary between $-50°C$ and $+100°C$.

The typical potential failures in electronics are therefore open-circuit and short-circuit which are caused by numerous situations. We can also mention that electrical and thermal stresses can occur when the system is subject to large electrical ratings and high temperature respectively. Also electronic devices can experience operation failure which has the effect to perturb and even damage the neighbor devices.

But the major concern when designing space intended electronic systems is the radiation-induced effects. Cosmic rays, solar particle events and Van Allen radiation belts can disturb the embedded electronics and could result in temporary and permanent damages. Space applications require a high mean time between failure (MTBF) due to the incapacity of reparation. Therefore, a special attention should be given to the analysis of radiation-induced effects on the system and the electronic behavior upon high exposure to radiation.

We will explore the different possible radiation-induced effects occurring in semiconductors. In order to understand these critical effects, we will consider the basic building block of any electronic devices which is the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) whose cross-section is represented in figure 6.13.

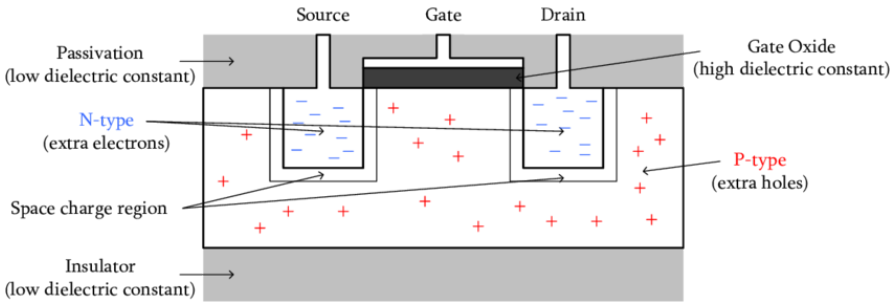

Figure 6.13: Cross-section schematic of N-MOSFET [25]

6.2.1 Total Ionizing Dose

The penetration of a radiation particle can cause either direct or indirect ionization of the semiconductor, both ionization processes result in the same consequences. The indirect ionization causes nuclear reaction in the semiconductor that ultimately result in the ionization.

When an incident particle penetrates through the electronic device (a), the particle interacts with the semiconductor material (b). The particle loses energy as it passes through the material creating electron-hole pairs (c). At last, holes are trapped in the oxide material such as the passivation, insulator or gate oxide (d) [25]. The TID process is represented in figure 6.14.

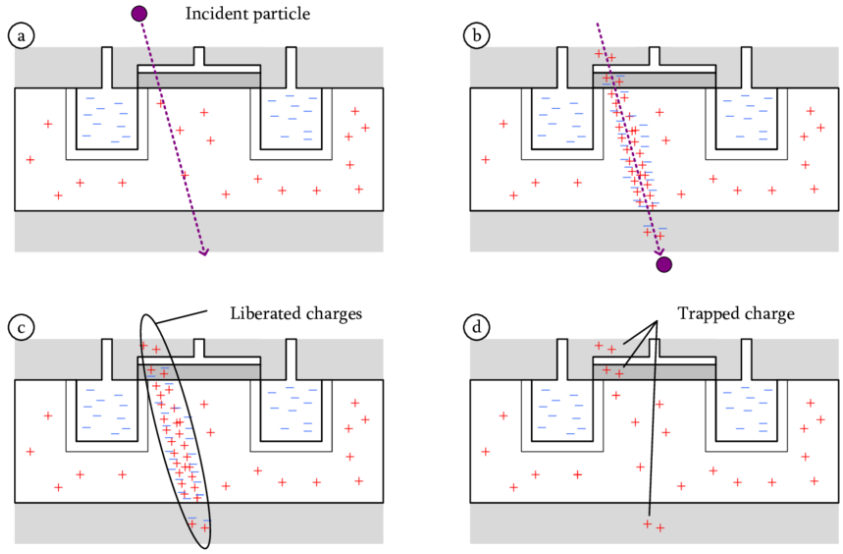

Figure 6.14: Total ionizing dose process in N-MOSFET [25]

The positive charges trapped in the oxide gives rise to deviation of electrical characteristics resulting in performance degradation and ultimately in system failure. The TID effect is a cumulative process which is expressed in Grays [Gy].

The main characteristic subject to TID is the threshold voltage of MOSFETs. As positive particles are accumulated in the gate oxide, it builds up additional positive voltage that reduces the threshold voltage of the transistor. Therefore, the N-MOSFETs are easier to switch on while P-MOSFETs are more difficult to switch off. Short-term effects are the variation of timing margins and the increase in leakage current. Long-term effect is permanent activation of N-MOS devices and permanent de-activation of P-MOS devices leading to system failure.

6.2.2 Single-Event Effects

The Single-Event Effects (SEE) are instantaneous effects and have a certain probability of occurring depending on the particle flux and width of the device. The origins are the same cause as the TID that is the interaction of radiation particle with the semiconductor material (a). Electron-hole pairs are created due to the energy loss of the particle upon material crossing (b). The electrons liberated in the substrate move rapidly to the drain due to their high mobility (c), a current pulse is then sensed at the output of the transistor (d) [25]. The SEE process is represented in figure 6.15.

This current pulse can lead to various types of failure with different severity. Single-Event Transients (SET) and Single-Event Upsets (SEU) are soft failures as they exhibit limited severity. SET are glitches on the signal or clock paths that can result in setup or hold time violations. SEU occurs typically in RAM when one or more stored bits are flipped and this error persists until the flipped bits are re-written. SEU failures can provoke a Single-Event Functionality Interrupt (SEFI) which is a soft failure that causes the device to be reset, locked-up, or malfunction. SEFI occurs in devices with control registers or Finite State Machine (FSM) that are susceptible to SEU.

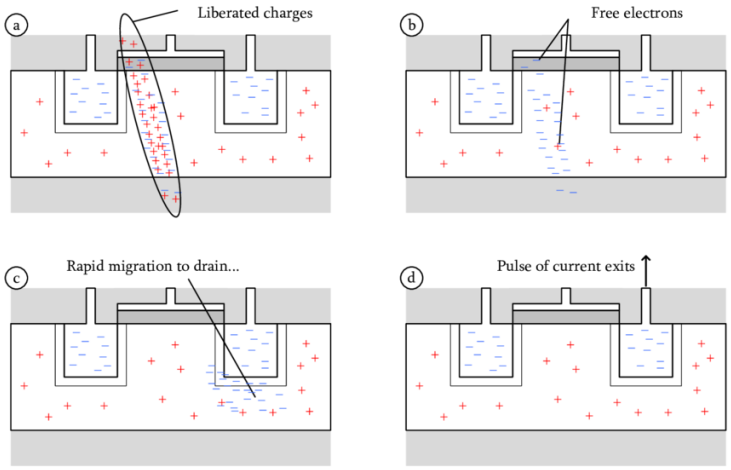

Figure 6.15: Single-Event Effect occurring in N-MOSFET [25]

There are also hard failure modes occurring in CMOS technology. This type of failure is related to the parasitic bipolar transistors located in the substrate of CMOS structure as represented in figure 6.16. If an incident particle inputs sufficient charge to activate the parasitic structure, hard failure modes can occur such as Single-Event Latchup (SEL), Single-Event Burnout (SEB) and Single-Event Gate Rupture (SEGR).

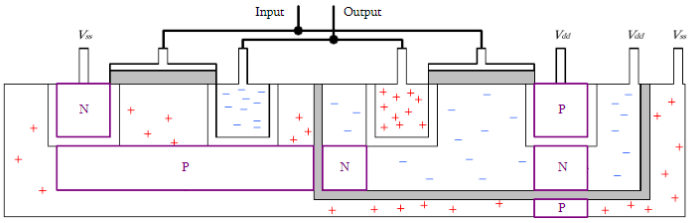

Figure 6.16: CMOS technology with parasitic bipolar transistors in purple [25]

SEL occurs when the parasitic structure is activated creating a short-circuit between supply and ground, ultimately heating up the structure. This short-circuit is locked with the latch-up effect requiring to cycle the supply to be resolved. SEB occurs with the parasitic structure activation, the structure will heat up when high drain-source voltage is applied. SEGR occurs when the particle hits the transistor gate while a high gate voltage is applied, it results in a conducting path through the gate. These hard failures result typically in irreversible damages.

6.2.3 Displacement Damage

The Displacement Damage (DD) comes from the interaction of incident particles with the silicon lattice and its process is represented in figure 6.17. The silicon lattice is made out of silicon molecules which are disposed following a regular pattern revealing a constant inter-molecular space (a). An incident particle penetrates and hits the silicon lattice (b). The particle loses energy during the collision which is redistributed to the silicon molecule which shows a displacement from its initial location (c). This displacement leaves a vacancy and becomes an interstitial by being close to a nearby molecule, this defect is called the Frenkel defect (d) [25]. The Frenkel defect has the impact of reducing the gain of bipolar transistors (MOSFETs being less subject to DD) leading ultimately to a system failure. The DD is a cumulative effect and is measured in terms of total number of 1 MeV equivalent neutrons that have altered the silicon lattice.

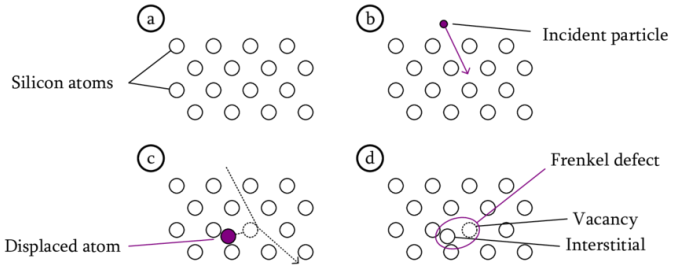

Figure 6.17: Displacement damage in silicon lattice of a semiconductor [25]

6.3 Failure Modes, Effects and Criticality Analysis

The Failure Modes, Effects and Criticality Analysis (FMECA) is a systematic procedure used to study and assess the potential failures that might occur in an operating system. This analysis specifies the failure modes, local and final effects of the failure, potential failure causes, current detection and compensation methods, and recommended actions for improved system reliability. This methodology also specifies a numeric approach by quantifying the severity (SEV), occurrence (OCC), detection (DET) and Risk Priority Number (RPN) of the failures. The decision to implement additional compensation is based on those numbers [45]. The FMECA worksheet template is represented in figure 6.18.

Component	Failure Mode	Local Effects	Final effects	SEV	Failures Causes	OCC	Current detection methods	Current compensation methods	DET	RPN	Actions needed?	Recommended actions
Temperature sensor	Short-circuit	Destruction	No temperature measurements => MPPT algorithm less efficient	2	SEL	5	/	Device radiation hardened (SEL immune to 76 Mev.cm²/mg)	1	10	N	eFuse

Figure 6.18: FMECA worksheet template and example

The failure mode is the way the failure occurs and it also describes the state of the item after the failure has been occurred. Electronic systems are extremely complex to analyze in terms of potential failure modes as the components could fail in countless manners. Therefore, we will constraint the analysis to the failure modes that are most likely to occur in LEO that are short-circuit, open-circuit, thermal stresses, electrical stresses and operation failure. Many other failure modes related to wafer process, assembly process, mounting process also exist but it is considered that these types of failure mode are handled before satellite launch [46].

The local effects of failure are the effects or sequence of effects that the failure induce, while the final effects are the effects on the high-level system operation, performance and status. The local and final effects are dependent on the failure mode, failures causes, component type and its function inside the system.

The severity scale is used to assess quantitatively the impact of the failure on the system. The worst potential effects or sequence of effects should be considered while assessing this number. The severity scale ranges from 1 to 10 depending on the component criticality. The rank and definition of each rank is listed in table 6.9.

Severity scale	Definition
Minor (Rank 1)	The failure will have no impact on the system operation. The control system will not notice the failure due to the minor nature of the failure and the telemetry will most likely not highlight the occurrence of the failure.
Low (Rank 2 - 3)	The control system notices a slight perturbation. The control module will notice a slight reduction of the performance. The telemetry might detect the presence of the failure.
Moderate (Rank 4 - 6)	Failure causes notable impact which may include component degradation or significant reduction of system performance. This failure may result in reduced system operation or component damages.
High (Rank 7 - 8)	System is highly impacted by the failure such as inoperable component or system. The failure may result in loss of features, interrupted system operation, large reduction of the system performance. The system requires a redesign for reducing the failure severity.
Very High (Rank 9 - 10)	Failure affects heavily the satellite operation. The failure may cause the satellite to be left without electrical supply resulting in mission failure. The failure must be compensated and actions are taken to reduce the impact and/or prevent such failures from occurring.

Table 6.9: Severity scale numbering and definition [26]

In LEO, the electronic devices may suffer from solder/pin loss due to vacuum, vibration, shocks, stresses experienced by the satellite. Solar flares, solar winds and other solar activities may produce thermal transients that could result in component failures. At last, the most frequent causes in LEO are the radiation induced effects explained in Section 6.2. The considered radiation effects are SET, SEU, SEFI, SEL, SEGR and SEB that could degrade and damage the semiconductor devices. TID and DD are negligible as the satellite is protected by the electromagnetic shield of the Earth.

The occurrence scale is a quantitative manner to assess the probability of failure occurring. The occurrence scale also ranges from 1 to 10 and each rank is associated with an occurring probability. The occurrence rate are extremely difficult to compute as it depends on numerous parameters. In the analysis, we will assume that the pin loss are remote failures while the thermal transients and SEE have a low probability of occurring. The rank, the definitions and the corresponding probabilities are given in table 6.10.

Occurrence scale	Definition
Remote (Rank 1)	Failure unlikely. No failures ever associated with this component • Rank1: $P(Failure) \leq 5 \cdot 10^{-6}$
Very Low (Rank 2)	Only isolated failures associated with this component • Rank 2: $5 \cdot 10^{-5} \geq P(Failure) \geq 5 \cdot 10^{-6}$
Low (Rank 3 - 5)	Isolated failures associated with similar components • Rank 3: $10^{-4} \geq P(Failure) \geq 5 \cdot 10^{-5}$ • Rank 4: $10^{-3} \geq P(Failure) \geq 10^{-4}$ • Rank 5: $0.01 \geq P(Failure) \geq 10^{-3}$
Moderate (Rank 6 - 7)	This component has occasional failures, but not in major proportions • Rank 6: $0.02 \geq P(Failure) \geq 0.01$ • Rank 7: $0.1 \geq P(Failure) \geq 0.02$
High (Rank 8 - 9)	This component or similar component have often failed • Rank 8: $0.2 \geq P(Failure) \geq 0.1$ • Rank 9: $0.4 \geq P(Failure) \geq 0.2$
Very High (Rank 10)	Failure is almost inevitable • Rank 10: $P(Failure) \geq 0.4$

Table 6.10: Occurrence scale numbering and definition [26]

Afterwards, the analysis studies the detection and compensation methods that are already implemented for counterbalancing the failure effects. The detection scale is used to assess the probability that the system identifies the occurrence of a failure and its ability to automatically compensate the failure. The detection scale ranges from 1 to 10 depending on the current methods. The rank and the corresponding definitions are given in table 6.11.

The Risk priority number (RPN) is a number used to classify the failure with respect to the risk that they represent in terms of mission safety and success. The RPN can be computed as the product of the SEV, OCC and DET numbers. The failures with the highest RPN should be considered in priority.

The RPN will only be used to identify the most critical failures while the decision to implement further actions is taken based on table 6.12. The horizontal axis represents the failure severity while the vertical axis represents the failure occurrence. An action is needed if the combination of row and column (failure criticality) returns Y, while it is not needed if the table returns N. If the table returns a number, the detection rank of the failure should be greater or equal to this number for an action to be required.

Detection scale	Definition
Very High (Rank 1 - 2)	Detection methods will detect the failure mode. The failure is automatically compensated by the current compensation methods.
High (Rank 3 - 4)	Detection methods have a high probability of detecting the failure mode. The failure is then automatically compensated by the current compensation methods.
Moderate (Rank 5 - 6)	Detection methods have a moderate probability of detecting the failure mode.
Low (Rank 7 - 8)	Detection methods have a low probability of detecting the failure mode.
Very low (Rank 9)	Detection methods will not detect the failure but detection methods could be implemented to resolve this problem.
Absolutely No Detection (Rank 10)	Detection methods will not detect the occurrence of the failure and no detection methods are available to resolve this problem.

Table 6.11: Detection scale numbering and definition [26]

O/S	1	2	3	4	5	6	7	8	9	10
1	N	N	N	N	N	N	N	N	Y	Y
2	N	N	N	N	N	N	10	8	Y	Y
3	N	N	N	N	10	7	6	5	Y	Y
4	N	N	N	8	6	5	4	4	Y	Y
5	N	N	10	6	5	4	3	3	Y	Y
6	N	N	7	5	4	3	3	2	Y	Y
7	N	10	6	4	3	3	2	2	Y	Y
8	N	8	5	4	3	2	2	2	Y	Y
9	N	7	5	3	3	2	2	1	Y	Y
10	N	6	4	3	2	2	1	1	Y	Y

Table 6.12: Table for decision making concerning the recommended actions [27]

Now that FMECA basics has been introduced, we can perform a FMECA on the EPS of the nanosatellite. The full FMECA is represented in appendix B. A summary of the FMECA is represented on next page which resumes the most critical failures. The next section will be dedicated to the implementation of compensation methods that are required to increase the chances of mission success based on FMECA resume. We can note that some failure can be compensated by multiple methods. We will select the easiest, cost effective and most suitable recommended actions to continue on the cheap but reliable implementation perspective.

Component	Failure Mode	Local Effects	Final effects	SEV	Failures Causes	OCC	Current detection methods	Current compensation methods	DET	RPN	Actions needed?	Recommended actions
Power monitor	Short-circuit	Component overheating and at last destruction	No voltage and current measurements on channel => no MPPT regulation	8	SEL	5	Sensor not responding	Use current and voltage measurements of other sensors	5	200	Y	eFuse`/ Radiation hardened device
Gate driver	Open-circuit	Disconnection of interconnecting wires	DC/DC converter not driven => Loss of 33% of power	9	Pin loss on VDDB, VSSB, OUTB	1	/	/	9	81	Y	Pull-down resistor on Low-side MOS gate for connecting to GND => DC/DC converters operated in asynchronous mode upon failure
	Short-circuit	Component overheating and at last destruction	DC/DC converter not driven => Loss of 33% of power	8	SEL	5	/	/	9	360	Y	Radiation hardened device / eFuse
	Operation failure	Glitches on OUTA, OUTB	Glitches on MOS gate voltage => Output voltage ripple or short-circuit	8	SET OUTA, OUTB	5	Voltage monitoring on battery bus	/	6	240	Y	Radiation hardened device / eFuse on DC/DC converter input / Replace LO MOS by diode to operate in asynchronous mode
DC/DC converter (solar)	Short-circuit	Component overheating and at last destruction	Short-circuit between Drain and Gate => Loss of DC/DC converter and solar panel	9	SEGR/SEB on High-side MOS	5	Current monitoring on solar panel bus	Large electrical ratings	1	45	Y	Radiation hardened MOS / eFuse on DC/DC converter input
		Component overheating and at last destruction	Short-circuit between Drain and Gate => Loss of DC/DC converter and solar panel	9	SEGR/SEB on Low-side MOS	5	Current monitoring on solar panel bus	Large electrical ratings	1	45	Y	Radiation hardened MOS / eFuse on DC/DC converter input / Replace LO MOS by diode to operate in asynchronous mode
		Component overheating and at last destruction	Loss of DC/DC converter and solar panel => Loss of 33% of power	9	A failure causes the input capacitor to break in short-circuit	4	Current monitoring on battery bus	/	5	90	Y	Self healing capacitor
		Component overheating and at last destruction	Loss of battery bus => Loads not supplied	10	A failure causes the output capacitor to break in short-circuit	4	Current monitoring on battery bus	/	5	100	Y	Self healing capacitor
Battery protection (switches)	Open-circuit	Disconnection of interconnecting wires	Pack disconnection from Battery bus => Loss of 33% of battery capacity	9	Pin loss on VS, GND, OUT, IN	1	/	/	9	81	Y	Parallel redundancy
	Short-circuit	Component overheating and at last destruction	Pack disconnection from Battery bus => Loss of 33% of battery capacity	9	SEL	5	Current monitoring on bus	/	9	405	Y	Radiation hardened device/ eFuse
PWM buck controller	Open-circuit	Disconnection of interconnecting wires	DC/DC converter not driven => Loss of bus	10	Pin loss on VIN, VCC, HB, HO, SW, PGND, AGND,	1	Current monitoring on bus	/	5	50	Y	Parallel redundancy (buck-boost converter + PWM controller)
	Short-circuit	Component overheating and at last destruction	DC/DC convertes not driven => Loss of bus	10	SEL	5	Current monitoring on bus	/	5	250	Y	eFuse
	Operation failure	Component shutdown	DC/DC converter not driven during restart => Bus voltage drops and at last loads shutdown	8	Supply undervoltage condition	4	Voltage monitoring on bus	/	5	160	Y	Supplied on battery bus
		Disconnection of interconnecting wires	Loss of features and at last loss of bus	10	Pin loss on UVLO, RAMP, COMP, FB, RT, RES, SS, CS, CSG	1	/	/	9	90	Y	Parallel redundancy (buck-boost converter + PWM controller)
		Disconnection of interconnecting wires	LO MOS of DC/DC converters not driven => Loss of bus	10	Pin loss on LO	1	/	/	9	90	Y	Pull-down resistor on Low-side MOS gate for connecting to GND => DC/DC converters operated in asynchronous mode upon failure
PWM boost controller	Open-circuit	Disconnection of interconnecting wires	DC/DC converter not driven => Loss of bus	10	Pin loss on Vin, VCC, BST, HO, SW, AGND, PGND	1	/	/	9	90	Y	Parallel redundancy (buck-boost converter + PWM controller)
	Short-circuit	Component overheating and at last destruction	DC/DC converter not driven => Loss of bus	10	SEL	5	Current monitoring on bus	/	5	250	Y	eFuse Radiation hardened device
	Operation failure	Component shutdown	DC/DC converter not driven during restart => Bus voltage drops and at last loads shutdown	8	Supply undervoltage condition	4	Voltage monitoring on bus	/	5	160	Y	Supplied on battery bus
		Disconnection of interconnecting wires	DC/DC converters not driven => Loss of bus	10	Pin loss LO	1	/	/	9	90	Y	Pull-down resistor on Low-side MOS gate for connecting to GND => DC/DC converters become asynchronous in case of failure
DC/DC converter (loads)	Open-circuit	Disconnection of interconnecting wires	Loss of DC/DC converter => Loss of bus	10	Pin loss on High-side MOS, inductor	1	Current monitoring on battery bus	/	5	50	Y	Parallel redundancy (buck-boost converter + PWM controller)
	Short-circuit	Component overheating and at last destruction	Short-circuit between Drain and Gate => Loss of DC/DC converter and battery bus	10	SEGR/SEB on High-side MOS	5	Current monitoring on solar panel bus	Large electrical ratings	1	50	Y	Radiation hardened MOS / eFuse on DC/DC converter input
		Component overheating and at last destruction	Short-circuit between Source and Gate => Loss of DC/DC converter	10	SEGR/SEB on High-side MOS	5	Current monitoring on battery bus	Large electrical ratings	1	50	Y	Radiation hardened MOS / Parallel redundancy (buck-boost converter + PWM controller)
		Component overheating and at last destruction	Short-circuit between Drain and Gate => Loss of DC/DC converter and solar panel	10	SEGR/SEB on Low-side MOS	5	Current monitoring on solar panel bus	Large electrical ratings	1	50	Y	Radiation hardened MOS / eFuse on DC/DC converter input / Replace LO MOS by diode to operate in asynchronous mode
		Component overheating and at last destruction	Loss of DC/DC converter and battery bus	10	A failure causes the input capacitor to break in short-circuit	4	Current monitoring on battery bus	/	5	200	Y	Self healing capacitor
		Component overheating and at last destruction	Loss of bus	10	A failure causes the output capacitor to break in short-circuit	4	Current monitoring on battery bus	/	5	200	Y	Self healing capacitor
Load switches	Short-circuit	Component overheating and at last destruction	Load not supplied	8	SEL	5	Current monitoring on bus	/	5	200	Y	Radiation hardened switch / eFuse
	Electrical stresses	Component degradation and at last destruction	Loss of features and at last load not supplied	6	Supply overvoltage condition	4	/	/	9	216	Y	Clamping diode on bus
Micro-controller	Open-circuit	Disconnection of interconnecting wires	Loss of features and at lastloss of micro-controller	10	Pin loss	1	/	/	9	450	Y	Shock, vibration and vacuum tolerant µC
	Short-circuit	Component ovrheating and at last destruction	Loss of micro-controller	10	SEL	5	Current monitoring on bus	/	5	250	Y	eFuse / LDO
	Electrical stresses	Component degradation and at last destruction	Loss of features and at last loss of micro-controller	8	Supply overvoltage condition	4	Current monitoring on bus	/	5	160	Y	Clamping diode on 5V bus / Radiation hardened LDO
	Operation failure	Component shutdown	Other modules not controlled during restart	10	Supply undervoltage condition	4	/	/	9	360	Y	Supplied on battery bus
		Memory bits flipped	Software code perturbation	10	SEU	5	CRC	CRC, MPU, ESM Software redundancy	3	150	Y	Radiation hardened Watchdog timer
		Glitches on SDA, SCL / SDA locked in pull-down by µC (SEFI)	I2C bus locked => no measurements	9	SET on SDA, SCL	5	Sensors not responding	/	5	225	Y	Power cycling using Watchdog timer

6.4 Final system implementation

This section proposes an improved implementation of the EPS by modifying the design, devices or by adding extra components based on the FMECA results presented in section 6.3. The extra actions have been selected based on the trade-off between complexity and effectiveness. Therefore, when possible, the redundancy is avoided as it is extremely complex to implement. Added complexity means also extra cost, weight and volume, thus simple but effective methods should be considered. Also, if extra components are added to the system, we prefer to select RHA components as we want to prevent additional failures from occurring in these extra components.

We provide the block diagram of the main EPS modules with modifications being highlighted in red. The star next to certain components indicates that the component has been enhanced with self-healing or radiation hardened technology.

6.4.1 MPPT Regulator implementation

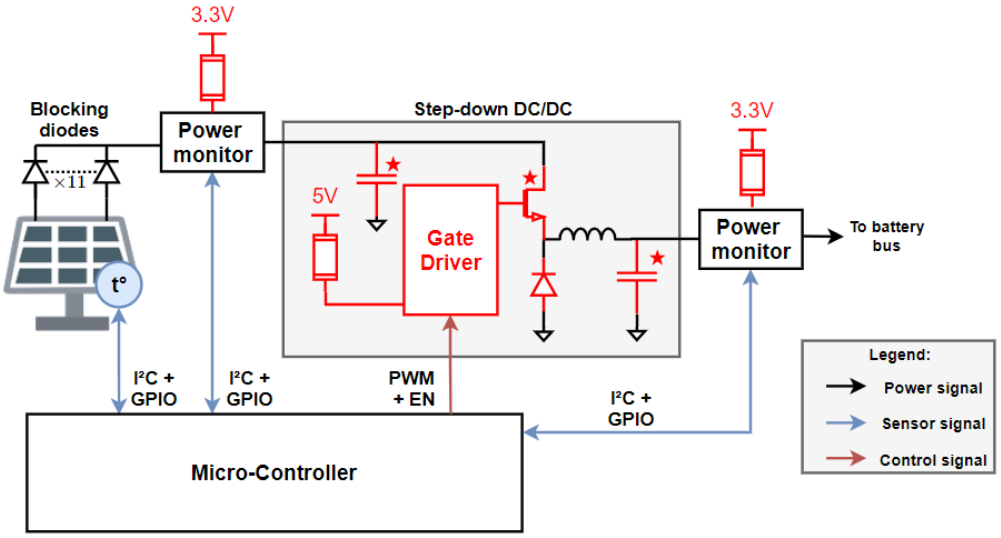

Figure 6.19: Improved implementation of the MPPT regulator

The first modification is the implementation of eFuses on the supply path of power monitors and gate driver as observed in figure 6.19. The eFuse is a power path protection device which is used to prevent over-current and over-voltage fault conditions, preventing device destruction, but also to provide a way to cycle the power in case of SEU or SEFI. We propose to select the TPS25940-Q1 eFuse from Texas Instruments.

The main modification of the MPPT regulator is the replacement of the low-side MOSFET by a diode such that the converter operates in asynchronous mode. Using an asynchronous converter prevents short-circuit in MOSFET but the converter efficiency is deteriorated. Therefore, we need to redesign the gate driver to drive an asynchronous converter and we selected the UCC5310MC device from Texas Instruments which exhibits active Miller clamping which can be used to prevent false turn-on of the power MOSFET. We also need to redesign the diode as the diode ratings have changed. Th V6KL45D4 diode from Vishay satisfies the requirements but exhibits a larger forward voltage increasing the power losses.

The MOSFETs have been replaced by RHA MOSFETs in order to prevent SEGR from occurring in the converter. We propose to use the IRHE57034 MOSFET from Infineon Technologies but the downside is the increase of power losses and extra cost. Finally, self-healing capacitors have been used for input and output capacitors of the DC/DC converter. Self healing capacitor have the ability to clear a fault area where a short-circuit has occurred due to breakdown or over-voltage condition and they are also volume efficient. We propose to use the PM90 R1-R2 capacitor family from Exxelia.

6.4.2 Battery protection and monitoring implementation

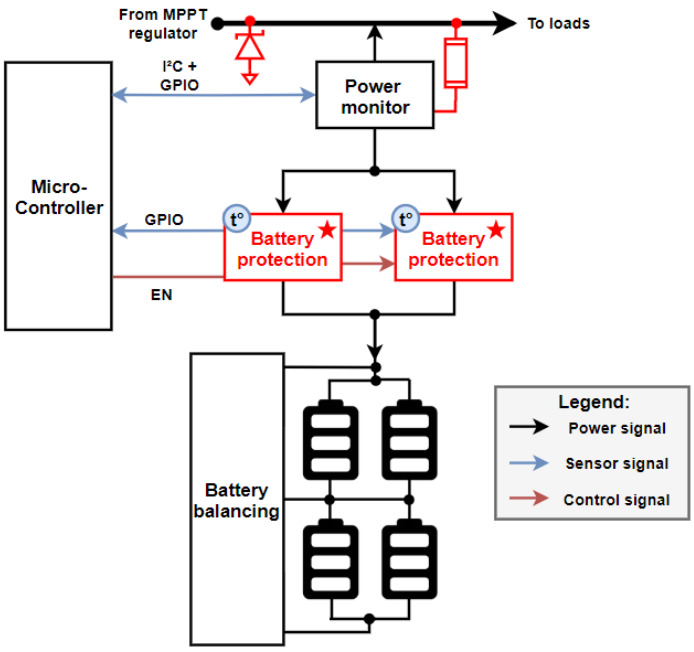

Figure 6.20: Improved implementation of the battery monitoring module

In the battery monitoring module, only few actions are required as reported by the FMECA but we decided to implement more actions as the battery bus is crucial and highly susceptible to failures. We can observe in figure 6.20 that battery protection is doubled to achieve hot redundancy which is a type of redundancy that offers an instant process correction over cold and warm redundancy. The redundancy is used to prevent the pack disconnection from the bus due to pin loss. The redundant battery protections have also been replaced by RHA switches to efficiently prevent radiation-induced failures. We proposed to use the Space-rated TPS7H2201-SP Switch exhibiting the same features as the TPS1H100-Q1 Switch.

Then, an eFuse is used to protect the power monitor from SEL. The power monitor constitutes an additional method for detecting overload and operation failure, and should therefore be protected. We can also use the same eFuse as proposed in the MPPT regulator. At last, a Zener diode connected between battery bus and ground has been implemented. This diode is used to clamp the bus voltage to a maximum voltage and is used to prevent over-voltage condition. We propose to use the MMBZ5237-G Zener diode to clamp the bus to 8.2V.

6.4.3 PDU implementation

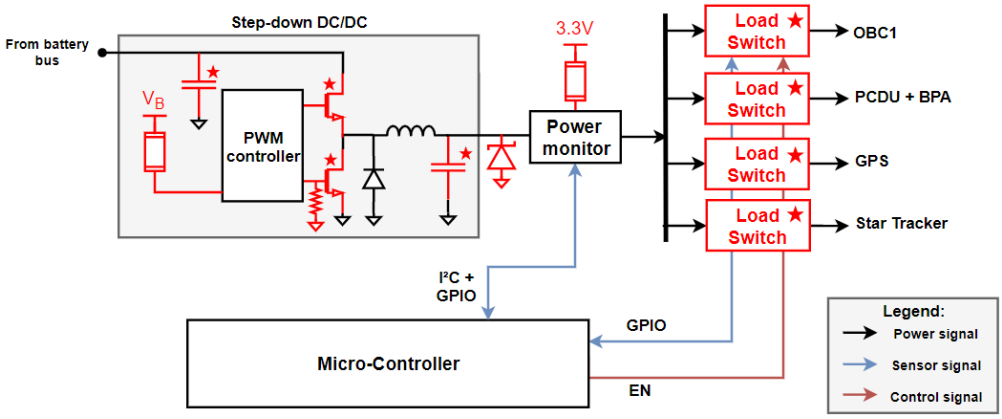

Figure 6.21: Improved implementation of PDU module for 3.3V bus

The first modification is the implementation of eFuses on the supply path of power monitor and PWM controller as it can be seen in figure 6.21. The eFuses are used to protect the devices against SEE on power monitor and PWM controller. We propose to select the TPS25940-Q1 eFuse from Texas Instruments. Unlike in the MPPT regulator, the replacement of the low-side MOSFET is not necessary as the PWM controller features a Hiccup Over-Current Protection that prevents short-circuit and at last destruction of the MOSFET.

Again, the MOSFETs have been replaced by RHA MOSFETs and self-healing capacitors have been used for input and output capacitors. We propose again to use the IRHE57034 MOSFET and the PM90 R1-R2 capacitor family as the same ratings are required. We also implemented a pull-down resistor on the low-side MOSFET gate such that this MOSFET is shutdown permanently in case of floating gate. Therefore, the converter operates in asynchronous mode rather than not working at all. The load switches have also been replaced by RHA switches and we proposed again to use the Space-rated TPS7H2201-SP Switch.

In addition, we implemented a clamping diode on the output of DC/DC converter. This diode is used to protect the load against over-voltage condition. We propose to select the BZX384-G-Series family of Zener diode. Also, the PWM controllers will be supplied on the battery bus instead of the 5V bus such that the loads are supplied in any circumstances. The problem with supplying on the 5V bus is that the bus is shutdown and unable to restart in case of under-voltage condition.

The last modification is the hot redundancy of DC/DC converter and PWM controller in order to prevent a bus loss. The redundancy cannot be avoided as no other compensation method is available and the bus loss has a disastrous impact on the system. A bus loss can occur due to pin loss or device degradation. Therefore, we implemented a buck-boost converter and PWM controller so that it can replace any bus. We need a total of 10 switches in order to implement the hot redundancy. The buck-boost converter is implemented with the same components as the other converters and we propose to use the LM5175-Q1 from Texas Instruments for the PWM controller. The proposed redundancy is represented in figure 6.22.

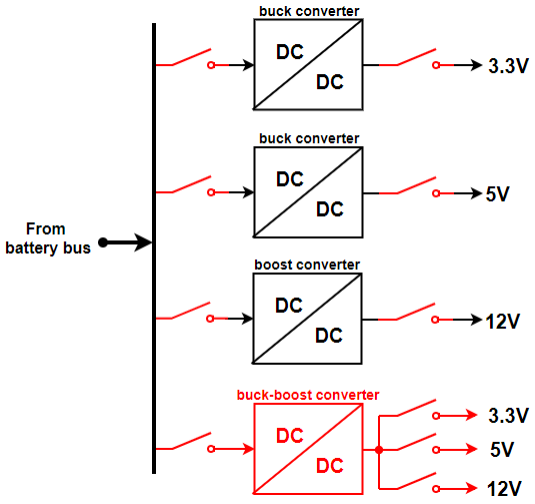

Figure 6.22: Proposed hot redundancy for the PDU module

6.4.4 Micro-controller implementation

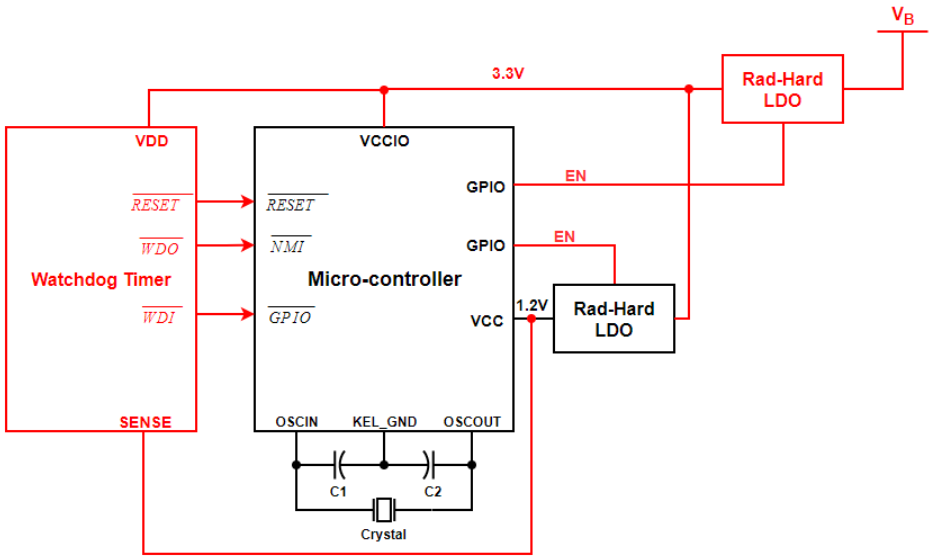

Figure 6.23: Improved implementation of Micro-controller

The first modification is to use a Radiation hardened LDO to supply the Micro-controller with 3.3V as it can be observed in figure 6.23. This action protects the micro-controller against over-voltage condition on the VCCIO pins. Also, the input of this LDO is connected directly to the battery pack such that the micro-controller inputs, VCCIO and VCC, are always supplied even in under-voltage condition where the PDU outputs might be disabled. We propose to use the LM1172ML-SP for the radiation hardened LDO.

The micro-controller is susceptible to be locked due to SEU and SEFI, therefore we used a watchdog timer. The watchdog timer is a module that automatically generates a reset signal when the micro-controller neglects to operate the watchdog timer. Then this device will detect software and hardware faults such as SEFI or SEL and will automatically reset the micro-controller. We propose to use the TPS3850-Q1 for implementing the watchdog timer.

Chapter 7

Conclusion

In this thesis, we addressed the problem of energetic study and optimization of the EPS of a CubeSat based on specifications of an upcoming mission assigned to Aerospacelab. The main contributions of this work are the sizing of power generation and storage cells, the study of power losses and system optimization through configurations selection, and at last we proposed an efficient and reliable system implementation.

A general introduction to satellite, and in particular CubeSat, has been provided. We also discussed the composition, mission purposes, advantages and drawbacks associated with this technology. Then the main modules of a satellite are presented with their function and current implementation in spacecrafts. We elaborate further on the EPS module by detailing the functions, main constituents and topologies, and we provided an overview of the state-of-the-art commercial products.

A discussion on power generation for spacecraft is provided. The solar energy and its conversion to electrical energy is explained. The basics of semiconductors behavior upon photon encounter with an explanation on differences between single-junction and triple-junction solar cell technology is presented. The electrical model and angular response of the cutting-edge triple-junction technology is exposed and the algorithms for extracting a maximum power from the solar cells are exposed.

Different energy storage technologies have been presented with their corresponding principles and characteristics. The Ragone plot is a useful tool for comparing the storage technologies and we explained the superiority of Li-ion batteries in spacecraft applications. The electrochemistry and electronic behavior of Li-ion battery is presented along with typical chemical and electrical equations. The performance degradation associated with this technology and its origins are explained.

The main focus of the thesis was the energetic study and optimization where mission specifications were provided by Aerospacelab. A thorough selection of the solar and battery cells is performed along with an overview of the state-of-the-art products and precise explanations of the selection are given. Afterwards, the energetic study is performed based on mission-specific consumption profiles. The solar panels and battery pack are sized and optimal cells disposition is explored. The system optimization is performed by exploring the system configurations and power losses in each module. Then the system configuration is selected based on the trade-off between efficiency and robustness, and the implications of this selection in terms of system design are presented.

Finally another contribution relies in system implementation. A meticulous selection of the components has been performed for each module constituting the EPS. Implementation diagrams with external components selection and interface with other devices are also provided. Afterwards, the potential failures in space missions are explored with a special attention to the radiation induced effects such as TID, SEE and DD. Based on theses explanations, we introduced the FMECA for assessing the potential failure effects. A complete FMECA has been performed on the EPS and actions have been done on design level of the EPS for reducing the criticality of the main failures.

A wide spectrum of engineering domains were tackled throughout this thesis and the combination of previous courses allows the realization of this thesis. This 5-year engineering knowledge has been build up and takes form in this final work. We can mention the course of semiconductor basics for the power generation module and the general chemistry course for the electrochemical behavior of the batteries. The last two chapters rely mainly on knowledge acquired by both analog and digital electronic courses, with a particular contribution of the power electronics course that introduces and explores in depth the behavior of power converters and the power losses in such components.

This thesis contributes to improving horizontal skills such as organization, communication and project management skills as the thesis was realized in collaboration with Aerospacelab. A feasible and concrete plan of the project was realized and the work was managed around deadlines. The thesis also consists of organizing the information and explaining it in a concise and clear manner. This work provides an opportunity to practice communication skills with colleagues in a wide range of situations, from daily discussions to results presentations and project meetings. It was also interesting to reconcile the points of view of colleagues because a problem can be solved by multiple solutions each of which presents pros and cons.

The overall goal of the thesis was to explore the state-of-the-art and standards in nanosatellite technology, to identify and apply concepts related to power generation and energy storage. The selection and use of appropriate model for each components and a computing tool for addressing the optimization problem constitute parts of the acquired skills. Furthermore, the components selection and implementation, and the failure analysis are also important learning outcomes of this work.

This work sets the ground for optimizing and implementing mission-specific power supplies. But many different design choices, configurations, implementations, tests have been left for the future due to lack of time and also to limit the consistency of this work. For instance, an electrical implementation of the final system, PCB realization, software implementation and measurements can be done to compare the results obtained from the optimization with the actual system performances. Moreover, an analysis and optimization of the digital modules of the EPS could be done, furthermore the design of these modules could be the extension of this work despite being time consuming.

An other future work could be the analysis of satellite telemetry after mission completion. The telemetry is a valuable source of information concerning the actual performance of the system compared to the design performances. The telemetry could help to identify the weak spots of the system and to design a more reliable and robust system. The telemetry can also highlight the occurrence of failures and system behavior upon failure detection.

Finally early in the optimization process, we decided that the MPPT will be the only topology considered. Therefore, an energetic study and optimization of the DET topology could be considered and compared with the results of this work in terms of efficiency, robustness and implementation complexity.

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Appendix A

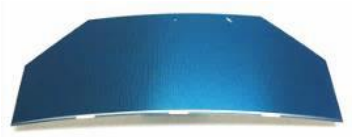
Datasheet of solar cells [1] and battery cells [2]

SPECTROLAB
A Boeing Company

30.7% XTJ Prime
Space Qualified Triple Junction Solar Cell

- **Best in Class - BOL & EOL**
- **AIAA-S111 & AIAA-S112 Space Qualified**
- **Heritage Upright Lattice-Matched XTJ Structure**
- **26.7% EOL, 1E15 1MeV electron****
- **Currently in Full Production**
- **Multiple Sizes Available (27cm² through 84cm²)**

Operates 2° C Cooler
Than Other Space Grade Solar Cells



Cell Thickness = 80μm - 225 μm
Cell Mass = 50 - 84mg/cm²

XTJ Prime Post 1 MeV e- Retention (US Standard AIAA S-111-2005)

Parameters*	BOL	1e14 (10-yr LEO)	5e14	1e15 (15-yr GEO)	1e16
$Efficiency_{mp}$	30.7%	0.94	0.88	0.85	0.65
V_{oc} (V)	2.720	0.94	0.89	0.87	0.78
J_{sc} (mA/cm^2)	18.0	1.00	0.99	0.98	0.93
V_{mp} (V)	2.406	0.94	0.89	0.87	0.76
J_{mp} (mA/cm^2)	17.5	1.00	0.99	0.97	0.86

*** Production average of >100,000 cells; AM0 (135.3 mW/cm², 28ºC)** **(Fluence of 1 MeV electrons/cm²)**

XTJ Prime Post 1 MeV e- Retention (European standard-ECSS**)

Parameters*	BOL	1e14 (10-yr LEO)	5e14	1e15 (15-yr GEO)	1e16
$Efficiency_{mp}$	30.7%	0.94	0.90	0.87	0.70
V_{oc} (V)	2.720	0.94	0.90	0.88	0.80
J_{sc} (mA/cm^2)	18.0	1.00	0.99	0.99	0.94
V_{mp} (V)	2.406	0.94	0.91	0.89	0.80
J_{mp} (mA/cm^2)	17.5	1.00	0.99	0.98	0.88

**** Photon and temperature annealing according to ECSS-E-ST-20-08C** **(Fluence of 1 MeV electrons/cm²)**

QUALITY MANAGEMENT SYSTEM
AS9100
CERTIFIED

ENVIRONMENTAL MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO 14001

Spectrolab, Inc. 12500 Gladstone Avenue, Sylmar, California 91342 USA
● Phone: 800.936.4888 ● Website: www.spectrolab.com ● Customer Service DLSYLCustomerService@Boeing.com

SPECTROLAB
A Boeing Company

30.7% XTJ Prime

Over 320 kW of XTJ Prime Delivered!

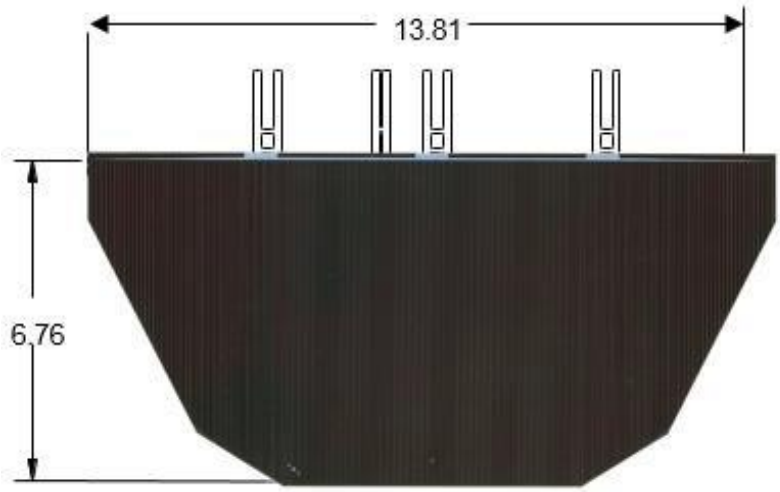
Temperature Coefficients (15ºC - 125ºC)

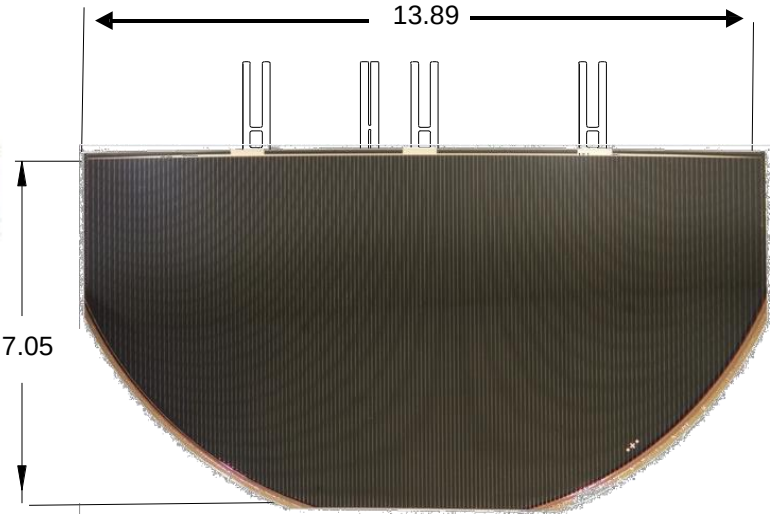
Parameters			BOL	1e14	5e14	1e15	1e16
Open Circuit Voltage	$\Delta V_{oc}/\Delta T$	[mV/ºC]	-5.6	-5.8	-6.2	-6.4	-6.6
Short Circuit Current	$\Delta J_{sc}/\Delta T$	[μA/cm²/ºC]	10.0	10.0	10.3	10.8	11.8
Maximum Power Voltage	$\Delta V_{mp}/\Delta T$	[mV/ºC]	-6.3	-6.4	-6.5	-6.6	-6.6
Maximum Power Curren	$\Delta J_{mp}/\Delta T$	[μA/cm²/ºC]	5.0	6.5	8.9	9.5	12.1

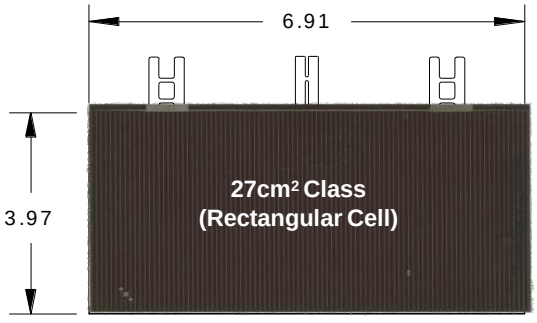
Standard Cell Sizes

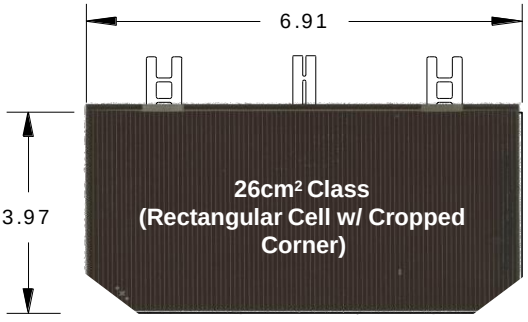
Other cell Sizes Available

Thermal Parameters	Value
Solar Absorptance	0.88
Emittance	0.85









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MP 174565 xtd
Rechargeable Li-ion cell

3.65 V high energy Li-ion cell with extra life and operational temperature

Saft's MP 174565 xtd cell is ideally suited for applications requiring high energy and long operating life, either in calendar, cycling or floating conditions, with excellent performance in unregulated temperature environments from –40°C to +85°C.

Benefits

- Excellent operating life in calendar, cycling and floating conditions
- Unrivalled operating temperature range from –40°C to +85°C
- High level of safety, compatible potentially explosive atmospheres
- Long shelf life with extremely low capacity loss under storage
- Easy integration into batteries
- Smaller environmental footprint than other technologies

Key features

- High energy density (264 Wh/l, and 150 Wh/kg)
- Aluminium casing
- Hermetically sealed
- Operates in any orientation
- Maintenance free
- No memory effect
- Manufactured in EU

Designed to meet all major quality, safety and environmental standards

- Safety: UL 1642 and IEC 62133 Ed. 2
- Transport: UN 3480, UN 3481
- Quality: ISO 9001, ISO 13485 Saft World Class program
- Environment: ISO 14001, RoHS and REACH compliant

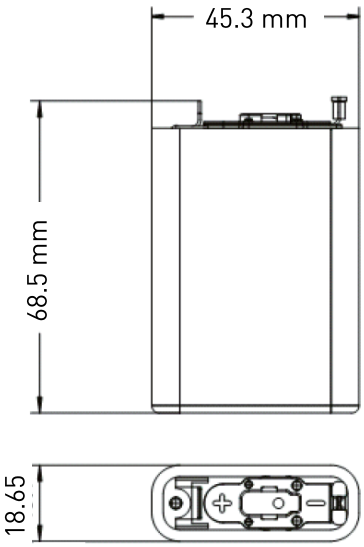
Typical applications

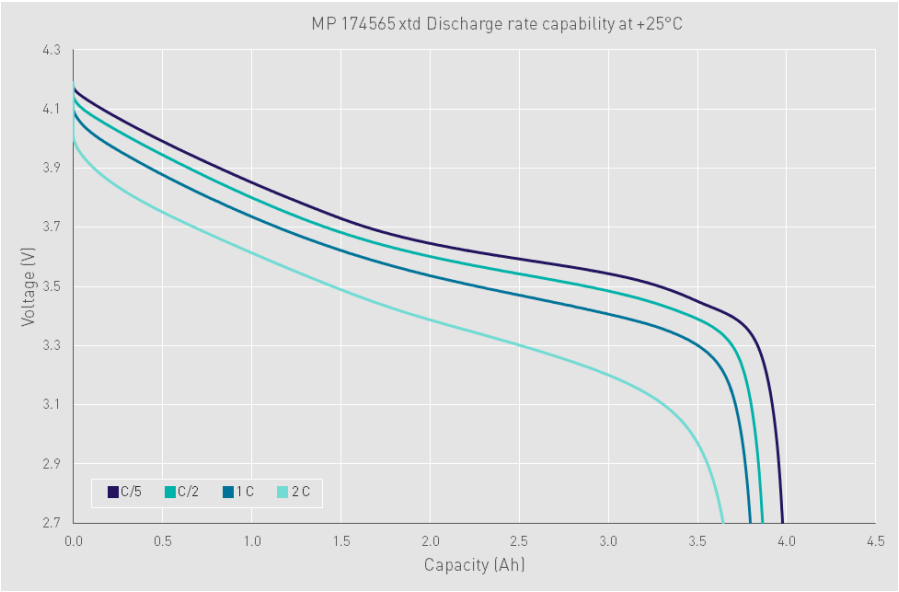
- Backup for industrial equipment
- Medical devices
- Tracking
- Oil & Gas applications
- Internet of Things
- Wireless Sensor Networks
- Lighting & signalling

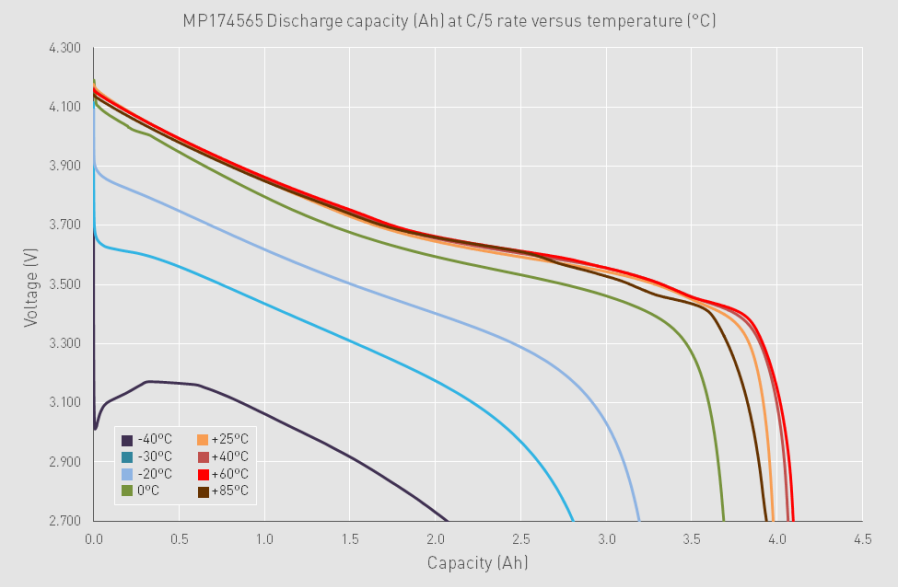
Electrical characteristics		
Typical capacity (at C/5 rate, +25°C, 2.5V cut-off) [i]		4.0 Ah
Nominal voltage		3.65 V
Nominal energy		14.6 Wh
Recommended maximum discharge current [ii]	Continuous	8 A (~2C rate)
	Pulse	16 A (~4C rate)
Physical characteristics (sleeved cell)		
Thickness [iii]		18.65 mm
Width		45.3 mm
Height (including terminals)		68.5 mm
Typical weight		97 g
Volume (including terminals)		0.057 l
IEC cell designation		INP19/46/69
Saft internal cell designation		INT 174565 xtd
Operating conditions		
Typical cut-off voltage		2.5 V
Charging method		Constant current/Constant voltage
Charging voltage		4.2 V
Maximum continuous charge current [iv]		4 A (~1C rate)
Operating temperatures	Charge	-30°C to +85°C
	Discharge	-40°C to +85°C
Storage & transportation temperatures	Recommended	+15°C to +30°C
	Allowable	-40°C to +85°C

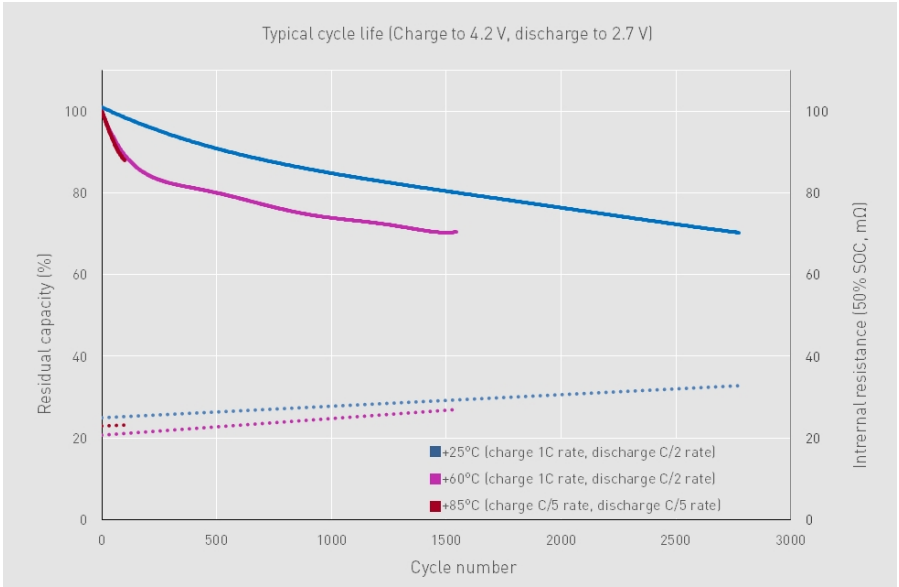
[i] Can vary depending on temperature and discharge rate
[ii] Can vary depending on temperatures. Consult Saft
[iii] At beginning of life, 100% State-of-Charge. May increase with temperature and the cells' calendar life.
[iv] For optimised charging below 0°C and above 60°C, consult Saft

saft









Battery assembly

Individual lithium-ion cells need to be mechanically and electrically integrated into battery systems to operate properly. The battery system includes electronic devices for performance, thermal and safety management specific to each application. Please contact Saft for your specific applications requirements.

Battery-level features

- Saft provides complete battery system designs
- Incorporating several levels of redundant safety features to prevent abuse conditions such as over-charge, over-discharge, and short circuits
- Incorporating electronics for performance and efficiency:
  - charge/floating/discharge management
  - cell balancing
  - temperature monitoring
- Battery protection controller at system level
  Communication for State-of-Charge and State-of-Health

Storage

- The storage area should be clean, cool (preferably not exceeding +30°C), dry and ventilated

Warning

- Do not crush, short-circuit, incinerate, dismantle, immerse in any liquid, heat above +85°C
- Observe charging conditions

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Appendix B

Failure Modes, Effects and Criticality Analysis of EPS

Component	Failure Mode	Local Effects	Final effects	SEV	Failures Causes	OCC	Current detection methods	Current compensation methods	DET	RPN	Actions needed?	Recommended actions
Blocking diodes	Open-circuit	Disconnection of interconnecting wires	Disconnection of solar network => Loss of 4% of total generated power	5	Pin loss on positive or negative terminals	1	Current monitoring on channel	/	5	25	N	Parallel redundancy
	Short-circuit	Solar network connected directly to the bus	Loss of protection against current flowing in reverse in this network => Loss of power	3	Failure causes the diode to break in short-circuit	3	Current monitoring on channel	/	7	63	N	Series redundancy
	Electrical stresses	Component degradation and at last short-circuit failure	Loss of protection against current flowing in reverse in this network => Loss of power	3	Overvoltage condition	4	Voltage monitoring on channel	Large electrical ratings	1	12	N	/
	Thermal stresses	Component degradation and at last short-circuit failure	Loss of protection against current flowing in reverse in this network => Loss of power	3	Thermal transients	3	Temperature monitoring	Large maximum junction temperature	1	9	N	Thermal management Series redundancy
Temperature sensors	Open-circuit	Disconnection of interconnecting wires	No temperature measurements => MPPT algorithm less efficient	2	Pin loss on VS, GND, SDA, SCL	1	Sensor not responding	/	5	10	N	Redundancy
	Short-circuit	Component overheating and at last destruction	No temperature measurements => MPPT algorithm less efficient	2	SEL	5	Sensor not responding	Radiation hardened device	1	10	N	eFuse
	Electrical stresses	Component degradation and at last destruction	Loss of features, accuracy and at last no temperature measurements	2	Supply overvoltage condition	4	/	Wide supply range	4	32	N	Clamping diode on 3.3V bus
	Thermal stresses	Component degradation and at last desctruction	Loss of features, accuracy and at last no temperature measurements	2	Thermal transients	3	Alert pins toggling	Thermal shutdown	1	6	N	Thermal management
	Operation failure	Component shutdown	No temperature measurements during component restart	1	Supply undervoltage condition	4	Sensor not responding	/	4	16	N	/
		Sensor registers modified and at last SEFI	False temperature measurements, false warnings, sensor not responding	1	SEU	5	Software checking with other temp. sensors	Software re-configuration / Radiation hardened device	3	15	N	Power cycling using eFuse
		Glitches on SDA / SDA pulled down by a non-addressed sensor	False temperature measurements / SDA locked in pull-down (SEFI)	1	SET on SDA	5	Software checking with other temp. sensors	Software filtering / Radiation hardened device	1	5	N	SEFI => Power cycling using eFuse
		Glitches on ALERT, THERM	False warnings	1	SET on ALERT, THERM	5	Software checking with other temp. sensors	Software filtering / Radiation hardened device	1	5	N	Power cycling using eFuse
		False detection of remote sensor	False warnings	1	Pin loss on D+, D-	1	Software checking	Ignoring warnings	1	1	N	Redundancy
		I2C address modified	Sensor not responding	2	Pin loss on A0, A1	1	Sensor not responding	Software checking other possible I2C addresses	1	2	N	/
		Disconnection of interconnecting wires	No temperature warnings	2	Pin loss on ALERT, THERM	1	Software checking with other temp. sensors	Software using other sensors warnings	2	4	N	/
Power monitor	Open-circuit	Disconnection of interconnecting wires	No voltage and current measurements on channel => no MPPT regulation	8	Pin loss on VS, GND, SDA, SCL, A0, A1	1	Sensor not responding	Use current and voltage measurements of other sensors	5	40	N	Redundancy with triple channel power monitor
		Disconnection of interconnecting wires	No voltage measurements	5	Pin loss on VBUS	1	Non-coherent voltage measurement	Use voltage measurement of other sensors / MPPT algorithm with temperature and current measurements	2	10	N	Redundancy with triple channel power monitor
		Disconnection of interconnecting wires	No current measurements	5	Pin loss on IN+, IN-	1	No-coherent current measurement	Use current measurement of other sensors / MPPT algorithm with temperature and voltage measurements	2	10	N	Redundancy with triple channel power monitor
	Short-circuit	Component overheating and at last destruction	No voltage and current measurements on channel => no MPPT regulation	8	SEL	5	Sensor not responding	Use current and voltage measurements of other sensors	5	200	Y	eFuse`/ Radiation hardened device
	Electrical stresses	Component degradation and at last destruction	Loss of features, accuracy and at last no voltage and current measurements	6	Supply overvoltage condition	4	/	Wide supply range	4	96	N	Clamping diode on 3.3V bus
	Thermal stresses	Component degradation and at last destruction	Loss of features, accuracy and at last no voltage and current measurements	6	Thermal transients	3	Thermal management	Thermal management	1	18	N	Thermal shutdown
	Operation failure	Component shutdown	No voltage and current measurements during component restart => Loss of efficiency during restart	2	Supply undervoltage condition	4	Sensor not responding	/	4	32	N	/
		Sensor registers modified and at last SEFI	False voltage or current measurements, false warnings, sensor not responding	3	SEU	5	Software checking with other power monitors	Software re-configuration	3	45	N	Power cycling using eFuse / Radiation hardened device
		Glitches on SDA / SDA pulled down by a non-addressed sensor	False temperature measurements / SDA locked in pull-down (SEFI)	5	SET on SDA	5	Software checking with other power monitors	Software filtering	1	25	N	SEFI => Power cycling using eFuse / Radiation hardened device
		Glitches on ALERT	False warnings	3	SET on ALERT	5	Software checking with other power monitors	Software filtering	1	15	N	Radiation hardened device
		Disconnection of interconnecting wires	No warnings	3	Pin loss on ALERT	1	Conversion Ready feature toggles ALERT pin at regular interval	Use warnings of other power monitors	5	15	N	/
	Open-circuit	Disconnection of interconnecting wires	DC/DC converter not driven => Loss of 33% of power	8	Pin loss on PWM, VCC, GND, VDDA, VSSA, OUTA	1	Current monitoring on battery bus	/	6	48	N	Parallel redundacy (DC/DC converter + gate driver)
		Disconnection of interconnecting wires	DC/DC converter not driven => Loss of 33% of power	9	Pin loss on VDDB, VSSB, OUTB	1	/	/	9	81	Y	Pull-down resistor on Low-side MOS gate for connecting to GND => DC/DC converters operated in asynchronous mode upon failure
	Short-circuit	Component overheating and at last destruction	DC/DC converter not driven => Loss of 33% of power	9	SEL	5	/	/	9	405	Y	Radiation hardened device / eFuse
	Electrical stresses	Component degradation and at last destruction	Loss of features, accuracy and at last even DC/DC converter not driven => Loss of 33% of power	7	Supply overvoltage condition	4	/	Wide supply range	1	28	N	Clamping diode on 5V bus
	Thermal stresses	Component degradation and at last destruction	Loss of features, accuracy and at last even DC/DC converter not driven => Loss of 33% of power	7	Thermal transients	3	Thermal management	Thermal management	1	21	N	/

Gate driver	Operation failure	Component shutdown	DC/DC converter not driven during component restart => Loss of 33% of power during restart	3	Supply undervoltage condition	4	Current monitoring on battery bus	/	4	48	N	/
		Disconnection of interconnecting wires	More leakage during nighttime => Battery DoD increased => reduced cycle life	2	Pin loss on DIS	1	/	/	9	18	N	/
		Disconnection of interconnecting wires	Dead time set to 15ns => Short-circuit if both MOS are on => Increase power losses in DC/DC converters and eventually MOS overheating and at last destruction	8	Pin loss on DT	1	/	/	9	72	N	eFuse on DC/DC converter input
		Glitches on OUTA, OUTB	Glitches on MOS gate voltage: Both MOS are off => Output voltage ripple Both MOS are on => short-circuit => MOS overheating and at last destruction	8	SET OUTA, OUTB	5	Voltage monitoring on battery bus	/	6	240	Y	Radiation hardened device/ eFuse on DC/DC converter input/ Replace LO MOS by diode to operate in asynchronous mode
DC/DC converter (solar)	Open-circuit	Disconnection of interconnecting wires	Loss of DC/DC converter => Loss of 33% of power	8	Pin loss on High-side MOS, inductor	1	Current monitoring on battery bus	/	5	40	N	Parallel redundancy (DC/DC converter + gate driver)
	Short-circuit	Component overheating and at last destruction	Short-circuit between Drain and Gate => Loss of DC/DC converter and solar panel	9	SEGR/SEB on High-side MOS	5	Current monitoring on solar panel bus	Large electrical ratings	1	45	Y	Radiation hardened MOS / eFuse on DC/DC converter input
		Component overheating and at last destruction	Short-circuit between Source and Gate => Loss of DC/DC converter	8	SEGR/SEB on High-side MOS	5	Current monitoring on battery bus	Large electrical ratings	1	40	N	Radiation hardened MOS / Parallel redundancy (DC/DC converter + gate driver)
		Component overheating and at last destruction	Short-circuit between Drain and Gate => Loss of DC/DC converter and solar panel	9	SEGR/SEB on Low-side MOS	5	Current monitoring on solar panel bus	Large electrical ratings	1	45	Y	Radiation hardened MOS / eFuse on DC/DC converter input / Replace LO MOS by diode to operate in asynchronous mode
		Component overheating and at last destruction	Short-circuit between Source and Gate => DC/DC converter operate in asynchronous mode	3	SEGR/SEB on Low-side MOS	5	/	Large electrical ratings	5	75	N	Radiation hardened MOS / Replace LO MOS by diode to operate in asynchronous mode
		Component overheating and at last destruction	Loss of DC/DC converter and solar panel => Loss of 33% of power	9	A failure causes the input capacitor to break in short-circuit	4	Current monitoring on battery bus	/	5	180	Y	Self healing capacitor
		Component overheating and at last destruction	Loss of battery bus => Loads not supplied	10	A failure causes the output capacitor to break in short-circuit	4	Current monitoring on battery bus	/	5	200	Y	Self healing capacitor
	Thermal stresses	Component degradation and at last destruction	Reduced efficiency and at last loss of DC/DC converter	6	Thermal transients	3	Thermal management	Thermal management	1	18	N	/
	Operation failure	Disconnection of interconnecting wires	MOS operating in asynchronous mode => Reduced efficiency	3	Pin loss on Low-side MOS	1	/	/	9	27	N	/
		Disconnection of interconnecting wires	Loss of power during Dead Time => Reduced efficiency	3	Pin loss of diode	1	/	/	9	27	N	Parallel redundancy
		Disconnection of interconnecting wires	Large output ripple	4	Pin loss of capacitors	1	/	/	9	36	N	Parallel redundancy
Cell Balancing	Open-circuit	Disconnection of interconnecting wires	Reduced cycle life on 4 battery cells	5	Pin loss on VDD, GND, VC2, VC1,VC1_CB	1	/	/	9	45	N	/
	Short-circuit	Component overheating and at last destruction	Reduced cycle life on 4 battery cells	5	SEL	5	Current monitoring on battery bus / Overcurrent alert of battery protection module toggling	Open up protection switch	1	25	N	Radiation hardened device / eFuse
	Electrical stresses	Component degradation and at last destruction	Loss of features and at last reduced cycle life on 4 battery cells	4	Supply overvoltage condition	4	Voltage monitoring on battery bus / Overvoltage alert of battery protection module toggling	Open up protection switch	1	16	N	/
	Thermal stresses	Component degradation and at last destruction	Loss of features and at last reduced cycle life on 4 battery cells	4	Thermal transients	3	Thermal management	Thermal management	1	12	N	/
	Operation failure	Component shutdown	No current balancing during restart	1	Supply undervoltage condition	4	Voltage monitoring on battery bus	/	4	16	N	/
		Glitches on OUT	False alert of overvoltage condition	2	SET on OUT	5	Software checking with other cell balancing devices	Software filtering	1	10	N	Radiation hardened device
		Disconnection of interconnecting wires	No protection timing on OUT pin => False alert of overvoltage condition	2	Pin loss on CD	1	Software checking with other cell balancing devices	Software filtering/ignoring warnings	1	2	N	/
		Disconnection of interconnecting wires	Cell-Balancing disable => reduced cycle life on 4 battery cells	4	Pin loss on CB_EN	1	/	/	9	36	N	/
		Disconnection of interconnecting wires	No alert of overvoltage condition => Battery cell destruction	5	Pin loss on OUT	1	Software checking with other cell balancing devices / Voltage and Temperature monitoring	Open up protection switch	2	10	N	/
Battery protection (switches)	Open-circuit	Disconnection of interconnecting wires	Pack disconnection from Battery bus => Loss of 33% of battery capacity	9	Pin loss on VS, GND, OUT, IN	1	/	/	9	81	Y	Parallel redundancy
	Short-circuit	Component overheating and at last destruction	Pack disconnection from Battery bus => Loss of 33% of battery capacity	9	SEL	5	Current monitoring on bus	/	9	405	Y	Radiation hardened device/ eFuse
	Thermal stresses	Component degradation and at last destruction	Loss of features and at last Pack disconnection from Battery bus	6	Thermal transients	3	Thermal management	Thermal management, Thermal shutdown	1	18	N	/
	Electrical stresses	Component degradation and at last destruction	Loss of features and at last Pack disconnection from Battery bus	6	Supply overvoltage condition	4	/	Overvoltage shutdown	1	24	N	Clamping diode on battery bus
		Disconnection of interconnecting wires	No warnings	3	Pin loss on ST, DIAG_EN	1	/	Current limiting and thermal shutdown still operating	1	3	N	/
		Disconnection of interconnecting wires	No current limiting => Battery cell degradation => Redcued cycle life	5	Pin loss on CL	1	/	/	9	45	N	eFuse on positive terminal of battery pack
		Glitches on ST	False warnings	2	SET on ST	5	Software checking with other switches	Software filtering	1	10	N	Radiation hardened device
	Open-circuit	Disconnection of interconnecting wires	DC/DC converter not driven => Loss of bus	10	Pin loss on VIN, VCC, HB, HO, SW, PGND, AGND,	1	Current monitoring on bus	/	5	50	Y	Parallel redundancy (buck-boost converter + PWM controller)
	Short-circuit	Component overheating and at last destruction	DC/DC convertes not driven => Loss of bus	10	SEL	5	Current monitoring on bus	/	5	250	Y	eFuse

PWM buck controller	Electrical stresses	Component degradation and at last destruction	Loss of features and at last DC/DC converter not driven => Loss of bus	8	Supply overvoltage condition	4	/	Wide supply range	1	32	N	Clamping diode on 5V bus
	Thermal stresses	Component degradation and at last destruction	Loss of features and at last DC/DC converter not driven => Loss of bus	8	Thermal transients	3	Thermal management	Thermal management	1	24	N	/
	Operation failure	Component shutdown	DC/DC converter not driven during component restart => Bus voltage drops and at last loads (and PWM controllers) shutdown during restart	8	Supply undervoltage condition	4	Voltage monitoring on bus	/	5	160	Y	Supplied on battery bus
		Glitches on HO, LO	MOS gate voltage glitches => Bus voltage Ripple / Both MOS are on => short-circuit => MOS overheating and at last destruction	8	SET on HO, LO	5	Current monitoring on bus	Hiccup Over-Current Feature	1	40	N	Radiation hardened device / eFuse on input of DC/DC converter/ Replace LO MOS by diode to operate in asynchronous mode
		Disconnection of interconnecting wires	Loss of features and at last loss of bus	10	Pin loss on UVLO, RAMP, COMP, FB, RT, RES, SS, CS, CSG	1	/	/	9	90	Y	Parallel redundancy (buck-boost converter + PWM controller)
		Disconnection of interconnecting wires	LO MOS of DC/DC converters not driven => Loss of bus	10	Pin loss on LO	1	/	/	9	90	Y	Pull-down resistor on Low-side MOS gate for connecting to GND => DC/DC converters operated in asynchronous mode upon failure
		Disconnection of interconnecting wires	No current monitoring on bus	6	Pin loss on CM	1	/	Current monitoring on bus using power monitor	1	6	N	Current monitor on each buses
		Glitches on CM	False current measurements	3	SET on CM	5	Software checking with power monitor measurements	Software filtering	1	15	N	Radiation hardened device
PWM boost controller	Open-circuit	Disconnection of interconnecting wires	DC/DC converter not driven => Loss of bus	10	Pin loss on Vin, VCC, BST, HO, SW, AGND, PGND	1	/	/	9	90	Y	Parallel redundancy (buck-boost converter + PWM controller)
	Short-circuit	Component overheating and at last destruction	DC/DC converter not driven => Loss of bus	10	SEL	5	Current monitoring on bus	/	5	250	Y	eFuse Radiation hardened device
	Electrical stresses	Component degradation and at last destruction	Loss of features and at last DC/DC converters not driven => Loss of bus	8	Supply overvoltage condition	4	/	Wide supply range	1	32	N	Clamping diode on 5V bus
	Thermal stresses	Component degradation and at last destruction	Loss of features and at last DC/DC converters not driven => Loss of bus	8	Thermal transients	3	Thermal management	Thermal management	1	24	N	/
	Operation failure	Component shutdown	DC/DC converter not driven during component restart => Bus voltage drops and at last loads shutdown during restart	8	Supply undervoltage condition	4	Voltage monitoring on bus	/	5	160	Y	Supplied on battery bus
		Glitches on HO, LO	MOS gate voltage glitches => Bus voltage Ripple / Both MOS are on => short-circuit => MOS overheating and at last destruction	8	SET on HO, LO	5	Current monitoring on bus	Hiccup Over-Current Feature	1	40	N	Radiation hardened device / eFuse on input of DC/DC converter/ Replace LO MOS by diode to operate in asynchronous mode
		Disconnection of interconnecting wires	Loss of features and at last loss of bus	8	Pin loss on UVLO, COMP, FB, RES, SS, MODE, OPT, SYNCIN/RT,SLOPE, CSP, CSN	1	/	/	9	72	N	Parallel redundancy (buck-boost converter + PWM controller)
		Disconnection of interconnecting wires	DC/DC converters not driven => Loss of bus	10	Pin loss LO	1	/	/	9	90	Y	Pull-down resistor on Low-side MOS gate for connecting to GND => DC/DC converters become asynchronous in case of failure
DC/DC converter (loads)	Open-circuit	Disconnection of interconnecting wires	Loss of DC/DC converter => Loss of bus	10	Pin loss on High-side MOS, inductor	1	Current monitoring on battery bus	/	5	50	Y	Parallel redundancy (buck-boost converter + PWM controller)
	Short-circuit	Component overheating and at last destruction	Short-circuit between Drain and Gate => Loss of DC/DC converter and battery bus	10	SEGR/SEB on High-side MOS	5	Current monitoring on solar panel bus	Large electrical ratings	1	50	Y	Radiation hardened MOS / eFuse on DC/DC converter input
		Component overheating and at last destruction	Short-circuit between Source and Gate => Loss of DC/DC converter	10	SEGR/SEB on High-side MOS	5	Current monitoring on battery bus	Large electrical ratings	1	50	Y	Radiation hardened MOS / Parallel redundancy (buck-boost converter + PWM controller)
		Component overheating and at last destruction	Short-circuit between Drain and Gate => Loss of DC/DC converter and solar panel	10	SEGR/SEB on Low-side MOS	5	Current monitoring on solar panel bus	Large electrical ratings	1	50	Y	Radiation hardened MOS / eFuse on DC/DC converter input / Replace LO MOS by diode to operate in asynchronous mode
		Component overheating and at last destruction	Short-circuit between Source and Gate => DC/DC converter operate in asynchronous mode	3	SEGR/SEB on Low-side MOS	5	/	Large electrical ratings	1	15	N	Radiation hardened MOS / Replace LO MOS by diode to operate in asynchronous mode
		Component overheating and at last destruction	Loss of DC/DC converter and battery bus	10	A failure causes the input capacitor to break in short-circuit	4	Current monitoring on battery bus	/	5	200	Y	Self healing capacitor
		Component overheating and at last destruction	Loss of bus	10	A failure causes the output capacitor to break in short-circuit	4	Current monitoring on battery bus	/	5	200	Y	Self healing capacitor
	Thermal stresses	Component degradation and at last destruction	Reduced efficiency and at last loss of DC/DC converter and bus	8	Thermal transients	3	Thermal management	Thermal management	1	24	N	/
	Operation failure	Disconnection of interconnecting wires	MOS operating in asynchronous mode => Reduced efficiency	3	Pin loss on Low-side MOS	1	/	/	9	27	N	/
		Disconnection of interconnecting wires	Loss of power during Dead Time => Reduced efficiency	3	Pin loss of diode	1	/	/	9	27	N	Parallel redundancy
		Disconnection of interconnecting wires	Large output ripple	4	Pin loss of capacitors	1	/	/	9	36	N	Parallel redundancy
Load	Open-circuit	Disconnection of interconnecting wires	Load not supplied	8	Pin loss on VS, GND, OUT, IN	1	Load not responding	/	5	40	N	Parallel redundancy
	Short-circuit	Component overheating and at last destruction	Load not supplied	8	SEL	5	Current monitoring on bus	/	5	200	Y	Radiation hardened switch / eFuse
	Thermal stresses	Component degradation and at last destruction	Loss of features and at last load not supplied	6	Thermal transients	3	Thermal management	Thermal management, Thermal shutdown	1	18	N	/

Load switches	Electrical stresses	Component degradation and at last destruction	Loss of features and at last load not supplied	6	Supply overvoltage condition	4	/	/	9	216	Y	Clamping diode on bus
	Operation failure	Disconnection of interconnecting wires	No warnings	3	Pin loss on ST, DIAG_EN	1	/	Current limiting and thermal shutdown still operating	1	3	N	/
		Disconnection of interconnecting wires	No current limiting	2	Pin loss on CL	1	/	/	9	18	N	eFuse
		Glitches on ST	False warnings	2	SET on ST	5	/	Software filtering	1	10	N	Radiation shielding
Micro-controller	Open-circuit	Disconnection of interconnecting wires	Loss of features and at lastloss of micro-controller	10	Pin loss	1	/	/	9	90	Y	Shock, vibration and vacuum tolerant µC
	Short-circuit	Component ovrheating and at last destruction	Loss of micro-controller	10	SEL	5	Current monitoring on bus	/	5	250	Y	eFuse / LDO
	Thermal stresses	Component degradation and at last destruction	Loss of features and at last loss of micro-controller	8	Thermal transients	3	Thermal management	Thermal management	1	24	N	/
	Electrical stresses	Component degradation and at last destruction	Loss of features and at last loss of micro-controller	8	Supply overvoltage condition	4	Current monitoring on bus	/	5	160	Y	Clamping diode on 5V bus / Radiation hardened LDO
	Operation failure	Component shutdown	Other EPS modules not controlled during µC restart => 3.3V bus not controlled => µC unable to restart	10	Supply undervoltage condition	4	/	/	9	360	Y	Supplied on battery bus
		Memory bits flipped	Software code perturbation	10	SEU	5	CRC	CRC, MPU, ESM Software redundancy	3	150	Y	Radiation hardened Watchdog timer
		Glitches on SDA, SCL / SDA locked in pull-down by µC (SEFI)	I2C bus locked => no voltage, current and temperature measurements	9	SET on SDA, SCL	5	Sensors not responding	/	5	225	Y	Power cycling using Watchdog timer
		Glitches on PWM of gate driver	DC/DC output voltage ripple	3	SET on PWM	5	Voltage monitoring on bus	/	5	75	N	Radiation hardened µC
		Glitches on DIS of gate driver	Gate driver disabled during short period / Gate driver enabled during nighttime	3	SET on DIS	5	Voltage monitoring on bus	/	5	75	N	Radiation hardened µC
		Glitches on IN of battery protection	Battery pack disconnected from battery bus during short time	3	SET on IN	5	Current monitoring on battery bus	/	5	75	N	Radiation hardened µC
		Glitches on DIAG_EN of battery protection	Battery diagnosis modified	3	SET on DIAG_EN	5	Software checking	Software re-configuration	1	15	N	Radiation hardened µC
		Glitches on IN of load switch	Load not supplied during short time	4	SET on IN	5	Current monitoring on bus	/	5	100	N	Radiation hardened µC
		Glitches on DIAG_EN of load switch	Load diagnosis modified	3	SET on DIAG_EN	5	Software checking	Software re-configuration	1	15	N	Radiation hardened µC

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