UCLouvain

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Wideband On-chip antenna

design, fabrication and testing

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Contents

Abstract

This work present the design of a wideband on-chip antenna on silicon substrate and its capability of beamsteering, the fabrication and measurements results are also presented. An overview of the state of the art of on-chip antenna at higher frequencies in silicon based technology is provided, with an emphasis on the design benefits and challenges. The impact of three silicon based substrates on antenna performance is evaluated during fabrication and testing, the three considered substrate are standard silicon substrate, high resistivity and trap rich silicon substrate. Reflection and transmission coefficients are measured in Welcome lab, results show that the antenna achieve wideband propriety starting from 95 GHz. Simulations show a gain of 6.28 dB, an efficiency of -0.04 dB (99%) and a bandwidth of 25.53 GHz.

Chapter 1

Introduction

On-chip antenna means the combination of antenna and other circuitry in the same chip.All the interest which carries this subject of on chip antenna comes from the fact that the higher the frequency, the lower the size of the antenna, as well as the ease of manufacture which the CMOS technology and specially based on the silicon offers.
World is shifting toward high frequencies with special needs for miniaturization, putting the antennas on the same chip with all needed circuitry will be inevitable.Many technologies are used for fabrication of On-chip antenna like LTTC technology [1]. Silicon is not the only used substrate, Quartz was used in [2] to design an antenna for 300 GHz and SiGe substrate in [3] to design a fully on-chip bowtie shape slot antenna.

1.1 Benefits and challenges

The success of a technology is especially based on the cost, from this point of view the technology of the on-chip antennas allows to drastically reduce the cost and the manufacturing time. The addition of an antenna on a chip does not increase its dimensions, especially since at very high frequencies the antenna has very small dimensions and could be folded to further reduce its size, an example of a folded dipole on chip antenna is given in [1], [4] and [5].
Although this new type of antenna allows to realize complex systems with a relatively low cost when using silicon, This new generation of antenna does not only come with many benefits, but many challenges as well.
An on-chip antenna can eliminate the requirement for bond wires when antennas are off chip and needs to be connected to other integrated circuits. We can build a tiny system that saves a lot of space. The key problem, is to create a really efficient and cost-effective on-chip antenna that meets all of the requirements [6].

The main challenge is caused by the silicon substrate. Due to its low resistivity, which is frequently less than 10 Ω-cm in normal silicon processes, the substrate is lossy. Furthermore, because of the silicon high permittivity (Si∼11.9), the majority of the power is absorbed in the substrate. This is a significant disadvantage for such type of antennas because it prevents energy from radiating efficiently into free space [7].
From some observations in [6], the losses in the substrate account for 85 percent of overall losses, whereas metallization losses account for just 15 percent.

The characterization and measurement of antennas will add another challenge, because of the chip must be installed on a board or specific test fixture to be characterized, another problem is the incorporation of extra radiation during practical measurement. As a result of interference from neighbouring circuits, this causes unwanted radiation that will be measured with the wanted radiation of the antenna.

It is also difficult to end up with a successfully working design that fulfill all the design requirement, as well as design and simulate the antenna and surrounding circuit at the same time in the same simulation tools to better control the effect that one has on the other. Usually the antenna is first simulated and optimized using an EM simulation tool like HFSS or CST, then the S parameters of the antenna are extracted and exported to a circuit simulation tool like Cadence or ADS, this is a way to co-simulate ad optimize the antenna along with the circuit.

1.2 Applications

On-chip antennas are widely used in wireless communication systems, especially in radar applications at higher frequencies [8].On-chip antenna could potentially be used for inter-chip communication and data communication between ICs to lower I/O pin counts, reducing the form factor, packaging costs, and signal delays[9].

1.3 CMOS stack up

Figure 1.1 depicts a typical silicon-based CMOS metal stack. It is made up of six to nine metal layers each of thickness about 500nm embedded in a dielectric layer (SiO2 with a dielectric constant of 4.1), all of which are mounted on a thick silicon substrate (Si11.9) with thickness around 500 μm. Generally, the on-chip antenna is built in the top metallization layer which is the thicker one 1-2 μm nearly, direct radiation into free space is ensured as a result of this. Silicon nitride (Si3N4) or polyimide are usually used as a thin passivation layer on the chip's top surface.

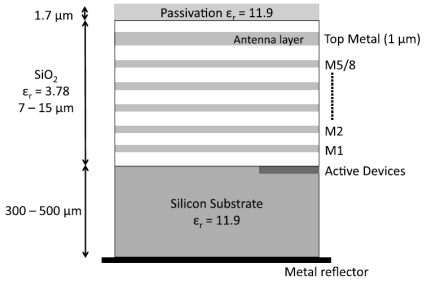


Figure 1.1: Sketched cross-section of a typical CMOS technology [10]

1.4 Silicon effect

Certainly silicon is the best choice for IC manufacturing thanks to its cost and redundancy, although its low resistivity and high permitivity are the major issues in on-chip antenna design. Energy is dissipated in on-chip antennas in both the conductive metal portions and the substrate. Dielectric losses, form a bigger percentage of the loss budget as the operating frequency increases. It has been shown that in the case of extremely lossy substrates like silicon, the substrate-based loss processes exceed the loss due to metallization [10].
A circuit model of an on-chip dipole on a substrate is depicted in Figure 1.2. The compact circuit model is split into two sections: the shunt branch contains C_{ox}, C_{sub} and R_{sub}, this branch models the influence of the silicon substrate and silicon oxide layer, the series branch is composed with L_d, C_d, R_c, R_r and R_{sur} and influences the antenna's radiation performance and losses.

The resistances R_r, R_c, and R_{sur} account for the radiation, conductor, and surface-wave losses of the dipole, respectively. L_d and C_d are the inductance and capacitance of the dipole, respectively. C_{ox} represents the oxide capacitance between the dipole and the silicon substrate. C_{sub} and R_{sub} are the silicon substrate

capacitance and resistance, respectively [11]. The radiation losses depends on the substrate thickness and the width of the metal line dipole, the surface wave losses depends on both the substrate thickness and the operating frequency, while the conductor losses is metal line thickness and frequency dependent, it increases as we go high in frequency.

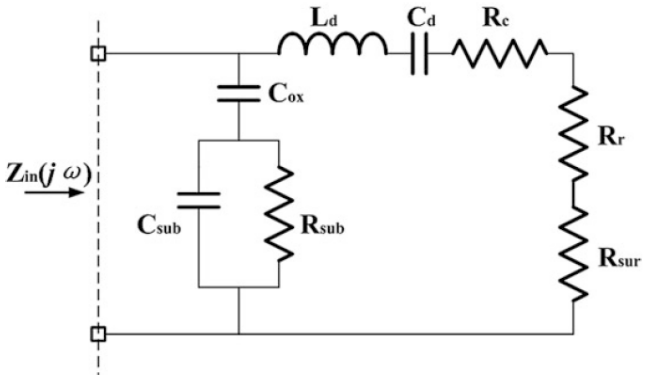


Figure 1.2: Compact circuit model of on-chip dipole antenna with an off-chip ground shield.

1.5 Surface wave

As seen before, the design of on-chip antennas must take into consideration the effect and challenges of the substrate, one of the most important factors resulting from this is the surface waves. These are unavoidable in any substrate slab thickness because their lowest order mode TM0 has no cutoff frequency and their effect on radiation increases with the increase in substrate thickness and dielectric constant. Usually in thin substrate h << λ (h is substrate thickness), surface waves are neglected.

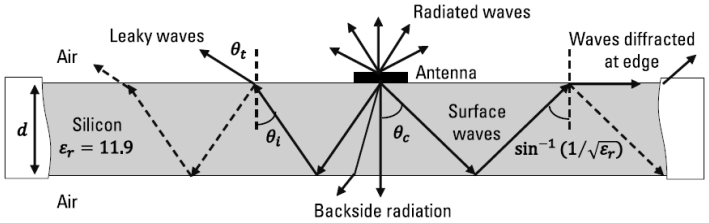


Figure 1.3: Surface waves illustration [10].

In [10] it is stated that the antenna radiates waves into the free space above

and into the dielectric material below. In the dielectric material, these waves are reflected by the boundaries and propagate in a zig-zag path between the dielectric-air interface. Surface waves will be transformed into space waves by diffracting on the edges of the substrate.

1.6 Enhancement techniques

Several approaches with an emphasis on antenna gain/efficiency improvement have been documented in the literatures to overcome the CMOS substrate loss.

1.6.1 Selective etching of Si

To overcome the limitations of the silicon substrate, a selective modification could be done like etching a cavity underneath the antenna to remove a part of the silicon substrate [12]- [13]. Another technique to improve the antenna efficiency is by thinning the silicon substrate to limit the surface wave propagation, as thicker substrate results in more surface wave modes propagation.

1.6.2 Proton implantation

A local or selective proton implantation of the silicon substrate will increase its resistivity from 10 Ω-cm to about 10^6 Ω-cm and thus improve antenna radiation properties.

1.6.3 AMC and PMC

In order to limit the propagation of electric field into the silicon, the antenna has to be physically separated from the substrate, this can be achieved by inserting specialized structures in the metal layers below the antenna that will act as a on-chip reflecting surface. Such structure are called artificial magnetic conductor (AMC) and are designed to behave like Perfect magnetic conductor (PMC).At a specific operational frequency band, an AMC plane can create constructively in-phase reflections with the incoming wave, resulting in greater radiation and larger bandwidth.

1.6.4 Lens and superstrate

Surface-wave power may be converted to useable radiated power using a hemispherical silicon lens with a matching layer [14]. As a result, on-chip antenna's radiation efficiency and directivity are improved. Another approach is to use superstrate like Quartz [2] for example on top of the on-chip antenna.

1.7 Wideband on-chip antenna

When designing antennas, there is always a trade-off between getting a large bandwidth and high gain. Designers used different techniques in order to get a large bandwidth. An engraved air-cavity underneath the antenna into a 150 μm high resistivity silicon substrate in [15] allows to enhance bandwidth (7.1 GHz bandwith around 94 GHz) and radiation efficiency, this is due to the effective permittivity approaching unity in the cavity. Etching out slots from the on-chip antenna was also used in [15] and [16] to achieve ultra wide band characteristics.

1.8 State-of-the-Art designs

Paper in [5] proposes a highly-integrated miniaturized radar SoC operating at 122 GHz with folded dipole antennas and their design techniques. Instead of eliminating the whole silicon layer beneath the antenna, only a tiny portion of it is etched away. This results in a semiconductor with significantly improved mechanical stability, but at the expense of some antenna gain and bandwidth. The implementation of the on-chip double folded dipole antenna using this new technique is shown in Figure 1.4. The ground plane is placed on the bottom metal layer, while the dipoles and their microstrip feeding lines are realized on the thickest top metal layer. The localized back etching technique creates air trenches around the dipoles. Results show a measured -10 dB bandwidth about 20 GHz,a measured gain of 6 dB and a simulated efficiency equal to 54%.

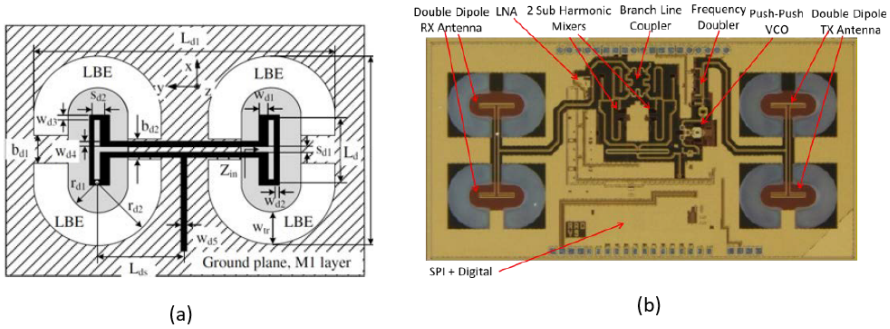


Figure 1.4: Double folded dipole antenna in [5]. (a) Layout, (b) Micrograph of the fabricated 122 GHz radar SoC.

Wael A. Ahmad et al. [8] propose three designs for on-chip antenna with and without localized backside etching (LBE) for 160 GHz for radar applications.First, a planar dipole Figure 1.5 (a) is designed to operate at 165 GHz, the dielectric

between the dipole and the ground plane is made of silicon with 50 Ω-cm resistivity, 11.9 permittivity and 200 μm thickness. A simulated 1 dBi gain with 30% efficiency at 165 GHz are obtained.However this first design is very sensitive to chip size and suffers from surface waves as can be concluded from the distortion of the radiation pattern in Figure 1.5b.

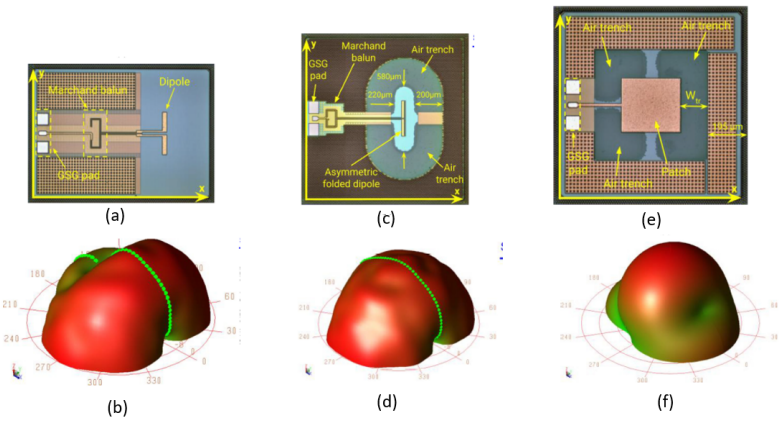


Figure 1.5: Micrograph and 3D radiation pattern of the fabricated antennas. (a) Planar dipole, (c) Folded dipole with LBE air trenches, (e) patch antenna with air trenches at radiating edges [8]

Second, A planar asymmetric folded dipole shown in Figure 1.5 (c) is designed, the silicon bulk is selectively removed by dry etching around the folded dipole, the resonant frequency is pushed from 162 GHz without metal filling to 175 GHz if metal filling are added to satisfy the Design Rules Checking. The gain of the antenna reachs 5 dBi over 165–175 GHz with simulated radiation efficiency of 45% and there is no distortion on radiation pattern, see Figure 1.5 (d).

Third, the patch antenna is simulated and measured, air trenches are introduced directly at the radiating edges of the patch as shown in Figure 1.5 (e), With a small footprint, the patch antenna with LBE performed well.
Debin Hou et al. present in [12] three designs at 130 GHz. First design, the Vivaldi antenna is implemented on the top metal layer which is suspended thanks to the pillars in order to decrease the radiation losses, the antenna is fed using a CPW line which is constructed in the bottom metal layer, the metallic layers are placed on an oxide layer deposited on a silicon substrate with high resistivity (see Figure 1.6 (a) and (b)). The width of the radiator, H, determines both the operation frequency and the bandwidth, while the length L affects the -3 dB bandwidth of the radiation pattern. The measurement and simulation shows good results, The measured -10 dB frequency response of the proposed antenna is from 126

GHz to over 170 GHz, the gain and efficiency are 5.5 dBi and 78% respectively. The second design is a monopole antenna with circular disk depicted in Figure 1.6 (c) and implemented using a stack of three metal layers, with 10 μm BCB sandwiched between each two metal layers, the whole structure is formed on top of a standard silicon with 10 Ω-cm resistivity. To reduce losses, the substrate is etched to get a civity underneath the structure and etched walls are coated with metal to act as a shielding ground plane (see Figure 1.6d). The simulated -10dB bandwidth is 120 GHz to 137 GHz, the gain and efficiency are 6dBi and 88% respectively.

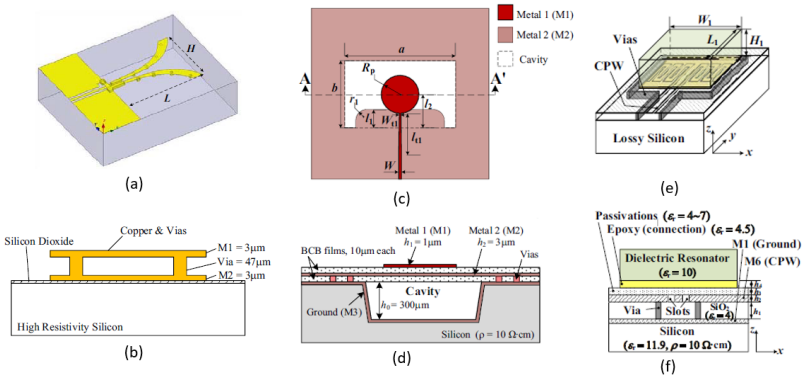


Figure 1.6: Antennas design in [12] (a) 3D view of the modified Vivaldi antenna, (b) Cross-sectional view of Vivaldi antenna, (c) Top view of monopole antenna with backed cavity, (d) Cross-sectional view of the monopole antenna, (e) 3D view and (f) cross-sectional view of on-chip antenna with dielectric resonator.

In [17] the authors propose a cavity-backed slot antenna (see Figure 1.7) implemented in a CMOS stack with six metal layers and a silicon substrate with 12 Ω-cm resistivity, 11.9 permitivity and 275 μm thickness. The cavity is formed by the lowest metal layer (M1) connected to the top metal layer (M6) through vias in between. Two resonance frequency are obtained, the first one at 137 GHz,which is the resonant frequency of mode inside the cavity, and a higher one which depends on the length of the slot, the cavity size and the slot length are optimized in order to get this second resonance frequency approaching the first one to have larger bandwidth and improve both gain and efficiency. Maximum simulated gain and efficiency achieved are –2dB and 18% respectively. To satisfy the CMOS design rule related to metal density, rectangular dummy holes are inserted in the top and bottom surface of the cavity, those holes need to be kept very small to not disturb the obtained radiation results. It is observed that the cavity serves as a shield to block the propagation of radiation both in the substrate and the oxide.

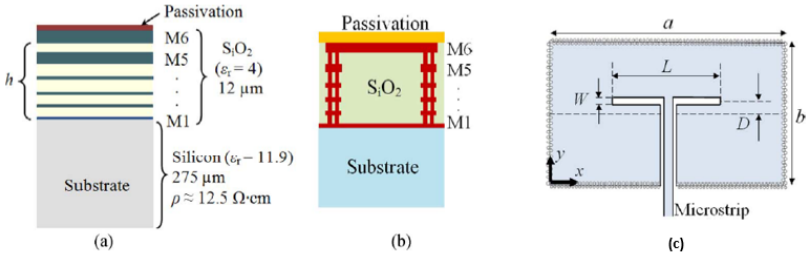


Figure 1.7: Cavity-backed slot antenna[17] (a) Cross-section (lateral) view of CMOS chip, (b) Cross-section view of the cavity M1 as ground., (c) Top view of the cavity and slot antenna fed by a microstrip

Another simple design is presented in [18] where a 4 μm thick Aluminum monopole antenna (see Figure 1.8 (a)) is implemented on standard silicon substrate with 10 Ω-cm resistivity covered by 1.5 μm oxide on top of it. Ion implantation is then done at the end of the fabrication with an energy 4MeV and an effective depth of 175 μm in order to increase the silicon resistivity. The power loss is less than 6% compared to 65% without ion implantation. The measurements show in Figure 1.8 (b) a resonance frequency of 103 GHz with 5 GHz bandwidth.

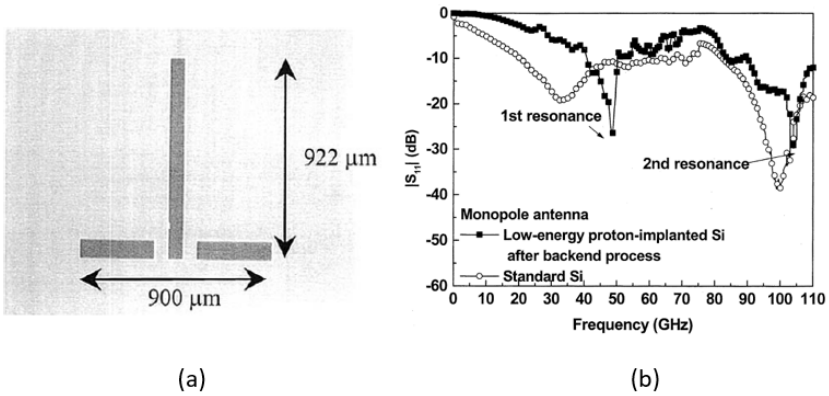


Figure 1.8: Monopole antenna[18] (a) Fabricated monopole antenna, (b) return loss

An on-chip antenna with dielectric resonator designed to resonate at 130 GHz for antenna gain and efficiency enhancement is the third design presented in [12], A grounded coplanar waveguide (GCPW) and a meander slot are used to create the feeding structure, with the meander slot being accomplished using the top metal (M6), insulated by a ground plane (M1), and surrounded by a rectangular metal wall made up of stacked vias from M1 to M6 (see Figure 1.6 (e) and (f)). The epoxy coating, which has a thickness of around 10 μm, is used to fix the dielectric resonator made of alumina, to the chip's surface. The meander slot is optimized

to resonate at a frequency close to that of the dielectric resonator to get larger bandwidth. The measured -10 dB frequency bandwidth is from 122.5 GHz to 138.5 GHz, the gain and efficiency at 130 GHz are 2.7 dBi and 43% respectively.

Instead of using only one dielectric resonator, Debin Hou et al. in [19] suggest and designed an on-chip meander slot antenna using two stacked dielectric resonators (DRs). The suggested on-chip stacked DRA array's configuration can be seen in Figure 1.9. A feeding structure and two DRs make up this system. The classic on-chip DRA explored in [12] is formed by mounting a dielectric resonator (DR1) on the substrate's surface. One more resonators DR2 is arranged vertically on top of the structure and separated by low permittivity support layer to effectively limit the effect of the EM distribution between the DRs, the different resonators are designed to resonate at the same frequency, the DR2 is far enough away from DR1 so that it does not affect its radiation properties and thus its sizing. Both distance between DR1 and DR2 and dimensions of DR2 are optimized in order to achieve the highest possible gain performance.

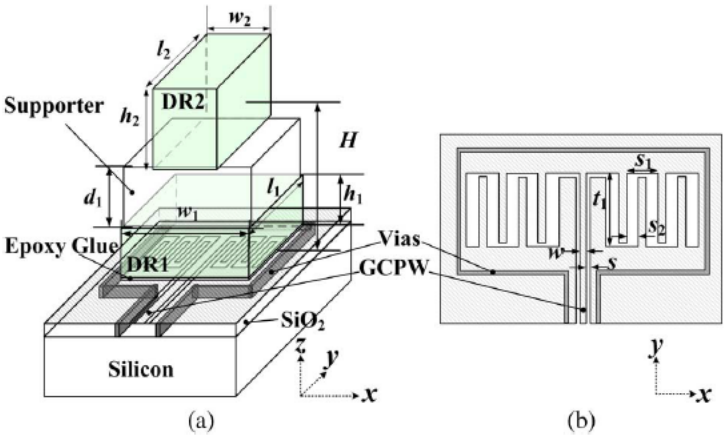


Figure 1.9: 3D on-chip antenna with double dielectric resonators [19] (not in scale): (a) 3-D structure, (b) top-sectional view of the feeding structure.

Figure 1.10 illustrate comparative simulations that are done on antennas without DR, as well as ones with single and double DR in order to compare the gain and efficiency. At 130 GHz, the simulated gain in Figure 1.10 is 4.7 dBi, which is about 2.6 dB and 12.3 dB higher than the antennas with and without a DR, respectively.

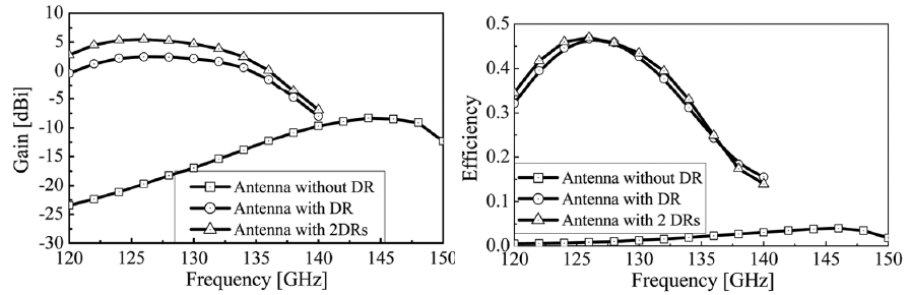


Figure 1.10: Simulated gain and radiation efficiency performances of the three on-chip antennas [19].

A microstrip line fed on-chip slot ring antenna at 140 GHz with silicon lens to enhance gain and efficiency is designed and measured in [14], Figure 1.11 shows the layout of the slot antenna, it has gap at 10 μm and radius R at 158 μm to yield input matching at 140 GHz and optimal efficiency. The mechanical support is silicon substrate with 300 μm thickness. A hyper-hemispherical type Si lens made of high resistivity (HR) Silicon is placed on the backside of the chip to improve the efficiency of the on-chip antenna. This allows the gain to go from -2 dB without the silicon lens to 11.25 dB at 140 GHz with it. The major issue with this design is the alignment between the center of lens and the center of the slot ring antenna, this caused a measured gain of 5.63 dB compared to a simulated gain of 11.25 dB.

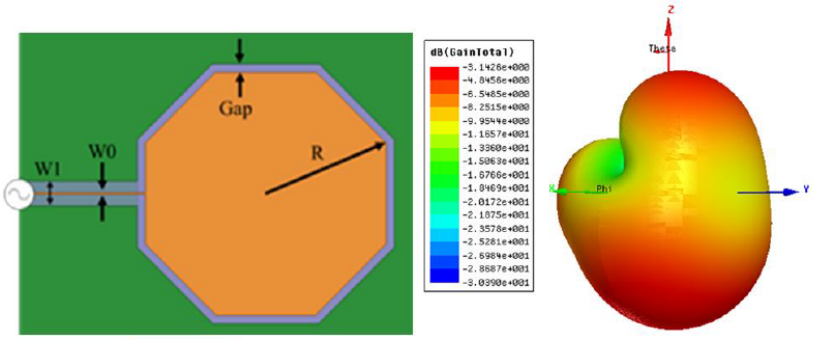


Figure 1.11: Layout and simulated radiation pattern of Microstrip line fed slot ring antenna [14].

A 77 GHz microstrip dipole antenna in [13] exhibit a 3.2 dBi gain and 15 GHz bandwidth at 77 GHz . the antenna is built on a silicon substrate with $\varepsilon_r = 11.9$, electrical conductivity of 2 S/m (resistivity = 50 Ω-cm) and a thickness of 670 μm, covered with SiO2 layer of 11.4 μm. A balun is used to match the microstrip line to the dipole and needs to be designed and optimized together with the dipole, otherwise it will affect antenna radiation characteristics. Dipole and its balun are

implemented in metal layer 5 and ground plane in the first metal layer. Top and side view of the designed dipole antenna with its feeding balun circuit at 77 GHz is shown in Figure 1.12. Etching silicon under the dipole antenna and positioning the ground plane below the etched silicon substrate allows decreasing silicon loss and increasing antenna directivity. Dotted area shows two bars of silicon that are left inside the etched area to increase mechanical robustness of the antenna.

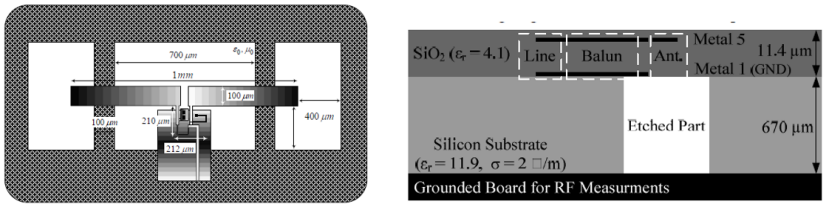


Figure 1.12: Top and side view of the designed dipole antenna with its feeding balun circuit at 77 GHz [13].

Three designs of on-chip antennas are investigated in [20] and shown in Figure 1.13, the three antennas are implemented on a high resistivity silicon 185 Ω-cm in Global Foundries 45nm CMOS SOI Process, all the three achieve higher efficiency and do not need any post processing like substrate thinning, etching or silicon lenses. At 68 GHz, simulations give antenna gain/radiation efficiency of the loop, dipole and slot antenna equal to 3.9 dBi/83%, 4.2 dBi/88%, and 3.9 dBi/85%, respectively. The measured gains of the loop, dipole and slot are 3.7 dBi, 3.9 dBi, and 3.8 dBi, it shows good agreement between measurements and simulations. In Figure 1.13 (a) the top Aluminum layer (LD) of 4 μm thick contains the antennas design, while the the first layers (OA and OB) contains the feeding and matching networks.

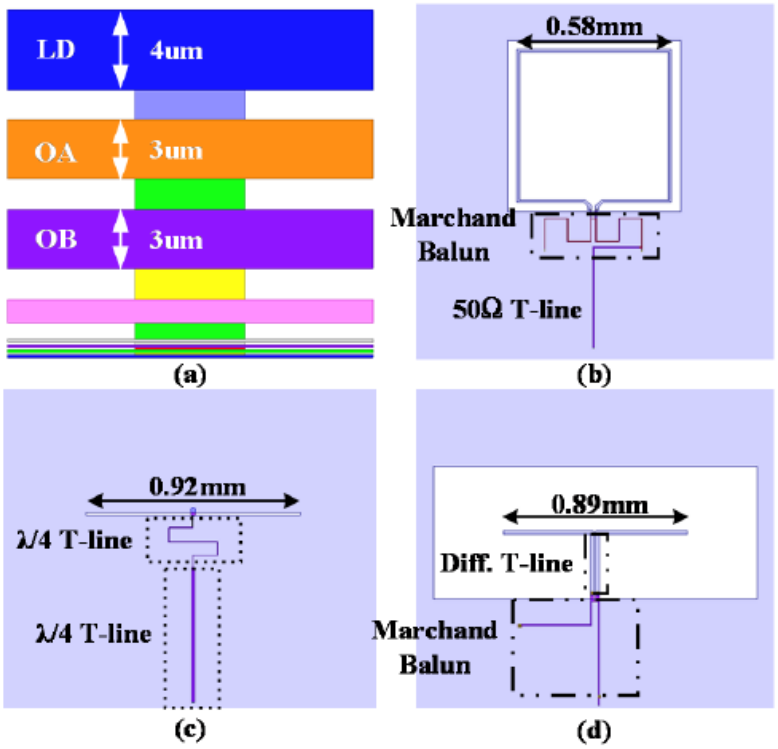


Figure 1.13: Metal stack and 3D EM models of the three on-chip antenna prototypes (b) 1λ square loop antenna, (c) 0.5λ slot antenna and (d) 0.5λ dipole antenna [20].

Figure 1.13 (c) and 1.14 show the 0.5λ slot antenna and its achieved gain and efficiency versus substrate resistivity respectively, it can be seen that the radiation efficiency improves from 46% to 85% and the antenna gain is increased by 2.83dB starting from a conventional substrate (13 Ω-cm) and going up to a high-resistivity substrate (185 Ω-cm).

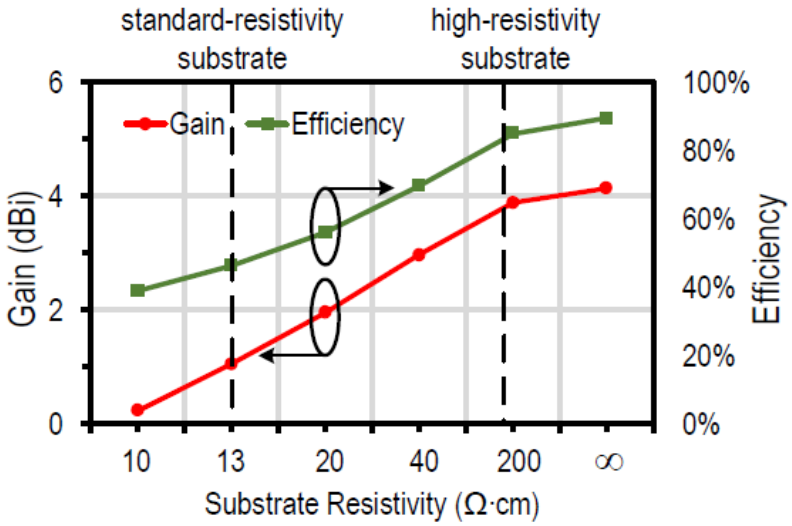


Figure 1.14: 0.5λ slot antenna gain and efficiency vs. substrate resistivity [20].

Table 1.1 gives an overview of the reviewed state of the art.

1.9 Motivation and organization of this thesis

All that has been said, it is clear that the field of silicon based on-chip antennas is very promising, especially if the antenna comes with the possibility of reconfiguring the radiation pattern and make beamsteering possible, this would avoid the use of antenna array that contain many elements and covering large area, adding to that the coupling between the different elements. The goal of this work is to design a wideband on chip antenna at 120 GHz on a silicon substrate for radar applications, we shed the light on the effect of the silicon resistivity on antenna performance. This thesis is organized as follow:

- The first chapter gives an overview of on-chip antennas, their benefits and challenges, reviews the state of the art and proposes some methods used to overcome the limitations of the silicon substrate.
- The second chapter presents the design of the on-chip antenna, the optimization step is discussed as well as the effect of substrate size and resistivity on antenna gain, efficiency and bandwidth.
- The third chapter presents the modification of the design concluded in chapter two to make the antenna capable of beamsteering.
- The last chapter goes through the steps of the manufacturing process as well as the presentation and analysis of the measurement results.

Ref	Frequency (GHz)	Gain (dBi)	Efficiency %	Substrate	Antenna type	Technology
[5]	122	6	54 %	Si	Folded dipole	Metallized back side
[8]	165	1	30 %	Si 200 μm	Dipole	50Ω Metallized back side
[8]	162	5	45 %	Si	Asymmetric folded dipole	-
[12]	130	5.5	78 %	High resistivity Si	Vivaldi	-
[12]	130	6 dB	88 %	Si 10 Ω-cm	Monopole disk	-
[12]	130	2.7	43 %	-	On-chi antenna with dielectric resonator	-
[13]	77	3.2	-	Si 670 μm 50 Ω-cm	Dipole	-
[14]	140	11.25	-	Si 300 μm	Slot ring with silicon lens	-
[17]	137	-2	18 %	Si 12 Ω-cm	Cavity backed slot antenna	CMOS
[19]	130	4.7	44 %	-	Meander slot with two dielectric resonator	-
[20]	68	3.9	83 %	Si 185 Ω-cm	Loop	45 nm CMOS SOI
[20]	68	4.2	88 %	Si 185 Ω-cm	Dipole	45 nm CMOS SOI
[20]	68	3.9	85 %	Si 185 Ω-cm	Slot	45 nm CMOS SOI

Table 1.1: Overview of silicon based on-chip antenna designs.

Chapter 2

Antenna design

After a literature review in the previews section, this chapter describes the design steps of a circular on-chip antenna on a silicon substrate. The three Figures of Merit that are specifically evaluated in this work are bandwidth, gain and efficiency. The approach followed during the design process will be detailed in this chapter, starting from the feeding technique and ending up with optimization.

2.1 Methodology and requirements

A circular disk on-chip antenna on top of a silicon substrate is designed using CST MWS 2019 version for the frequency 120 GHz , the antenna is fed through a 50Ω grouded coplanar waveguide line (GCPW). The suggested design is on one level of metal and suitable for fabrication facilities used in cleanrooms at Winfab. The properties of the silicon substrate used throughout this work are given in Table 2.1. The antenna, the feeding line and grounds material is copper with thickness of 1 μm. Table 2.2 shows the different wavelengths in both air and substrate.

ε_r	Conductivity	Resistivity
11.9	0.01 S/m	10000 Ω-cm

Table 2.1: Silicon substrate propreties.

The requirements that we tried to fulfill during this work are listed below:

- On-chip antenna on top of a silicon substrate with different resistivities to evaluate the effect of the later.
- Maximum efficiency and gain.

Wavelength	air	silicon
λ	2498.27 μ m	724.21 μ m
λ/2	1249.14 μ m	362.11 μ m
λ/4	624.57 μ m	181.05 μ m

Table 2.2: Wavelength in air and Silicon substrate.

- The large possible Bandwith.
- Design without Vias.
- Frequency arround 120 GHz.

The design and simulation of the proposed antenna are performed using the electromagnetic simulation software CST Microwave studio,

2.2 Feeding technique

On-chip antennas are mainly fed using five feeding techniques, namely transmission line, either coplanar waveguide line (CPW) or microstrip line, coaxial cable and aperture coupling. In the context of this work, only the Coplanar waveguide line feed is considered.

The coplanar line (CPW) is one of the transmission lines with a flat geometry, depending on whether it has a ground plane underneath, it is called a grounded coplanar waveguide line (GCPW). Figure 2.1 shows a conventional CPW line, It consists of a central metal conductor with width W and two metalic ground planes on both sides of the centre line with spacing G. the structure relies on a dielectric with a permitivity ε_r and thickness h covered by a metalic ground plane on the back side. The advantage of the coplanar line is that with its grounded geometry, it will allow an easy connection to the measuring device pads.

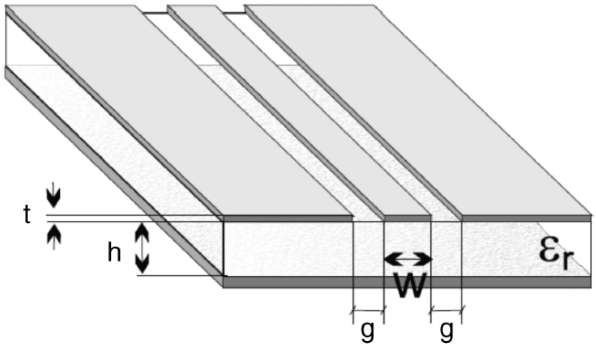


Figure 2.1: Grounded backed coplanar line [24]

The characteristic impedance of such a line depends on the width W of the metal strip, the gap G between central conductor and lateral ground plane and the substrate thickness h and permittivity ε_r. A complete formula could be found in 'Transmission Line Design Handbook' by Brian C. Wadell, page 79, [32].
However for the design, the choice of the substrate was fixed, to calculate the central line width W and the spacing G of the 50Ω feeding line for the design, we did not use this formula, but rather set the W and G parameters using the Macro function of simulation software CST using a silicon substrate with relative dielectric permittivity of 11.9, and a thickness h of 230 μm, the computed line impedance is 49.93Ω for W = 20μm and G = 12μm. The simulated electric field lines of the GCPW are shown in Figure 2.2.

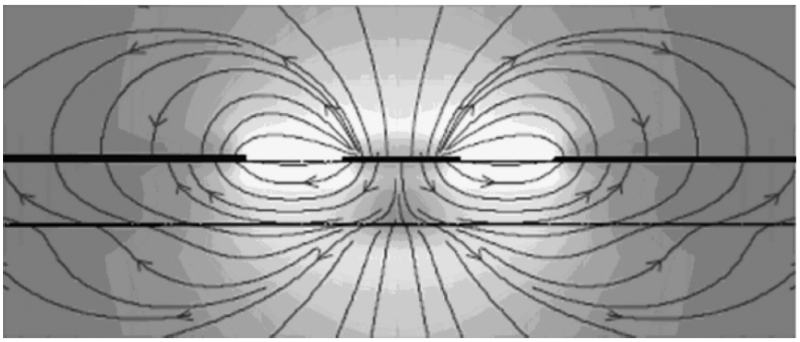


Figure 2.2: Electric field lines of the GCPW [24].

2.3 On-chip antenna

On-chip antennas are a very wide topic with much research being done on how to constantly improve their radiation characteristics. It consists of a very thin

metallic strip whose geometry can vary from the most traditional and basic shapes, such as rectangles or circles, to more complex shapes. The antenna holds on a dielectric substrate whose thickness, permittivity and resistivity strongly affect the radiation characteristics. The back side of the substrate is metallized.

2.4 Design

As mentioned in the beginning of this chapter, the design is performed using the simulation software CST MWS, the fist step was to fix the dimension of the 50 Ω coplanar feed line, the tool that was useful for this is the Macro window in CST. It allows to calculate several parameters, among others the impedance of the line from the width W of the central line, the gap G between the lateral ground plane and the line, the thickness h of the substrate and the dielectric constant of the substrate ε_r. Table below summarizes the parameters of the GCPW line.
The length of the line has been arbitrarily chosen since it does not change the magnitude of the reflection coefficient. This parameter will be fixed during the design optimization. The calculated and line impedance is Z=49.93 Ω.

ε_r	h	W	G
11.9	230 µm	20 µm	12 µm

Table 2.3: CPW and substrate parameters.

2.4.1 Antenna Geometry

The choice of the antenna geometry was not fixed at the beginning of this thesis, so we opted to test several geometries (see Figure 2.3) and make a comparison which allows to have the best results in terms of gain, efficiency and bandwidth. All shapes were placed on a substrate with same size in order to be able to make a comparison only on the radiation properties of the different antennas. After evaluation of the obtained results from the parametric simulations that were carried on the different designs, a circular geometry was chosen.

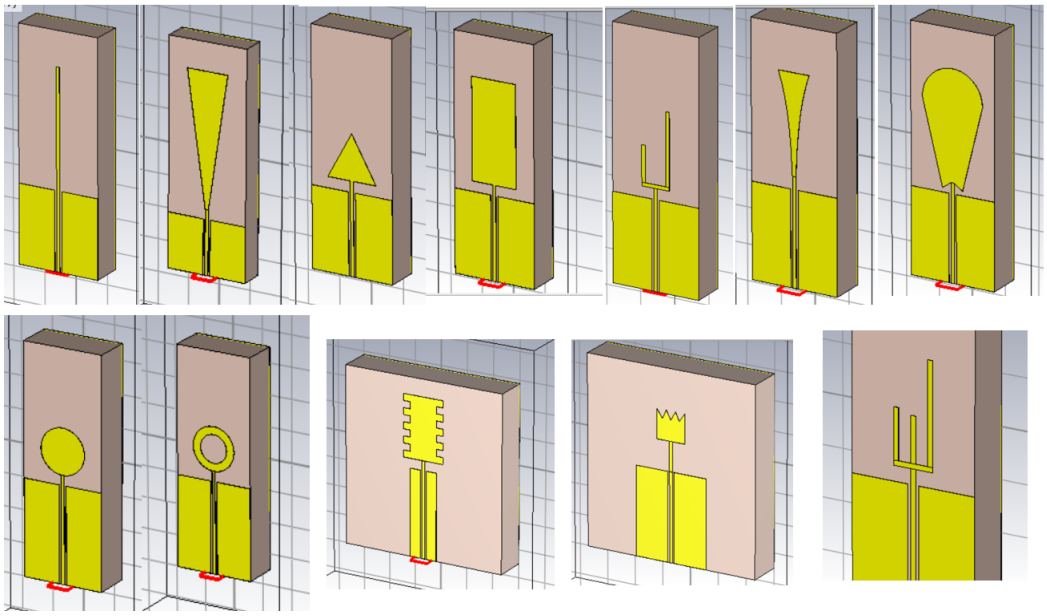


Figure 2.3: Schematic of diffrent antenna geometries.

2.5 Optimization

The choice of the geometry being fixed, a design optimization step is required to further improve the results and to check the limits of the design in terms of gain, efficiency and bandwith. The schematic top view presented in Figure 2.4 shows the different parameters on which we have to play on to carry out the optimization; they are all listed in Table 2.4 with their definition.

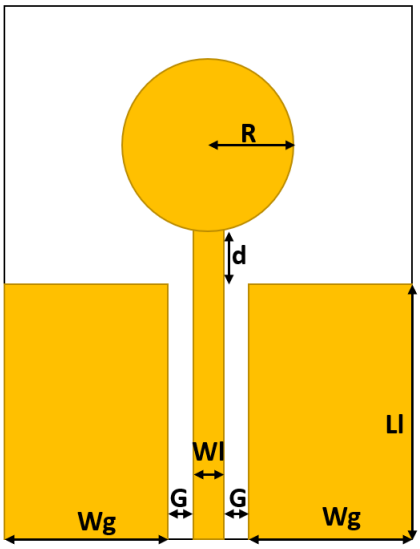


Figure 2.4: Schematic top view of the circular on-chip antenna on silicon substrate.

W_l	GCPW central line width
G	Gap between GCPW central line and lateral ground
W_g	Lateral ground width
L_l	GCPW length
d	GCPW central line extention
R	antenna radius

Table 2.4: Design parameters definition.

It would be interesting to see the effect of each variable on the performance of the design. In the following, we will try to see this by varying one parameter at a time and keeping all other parameters in Table 2.4 fixed, except for W_l and G that were fixed during the first step of design process.

2.5.1 Effect of GCPW length L_l and distance between the circular antenna and GCPW d

First, the coplanar line length L_l is varied, and it is found from the simulation results (see Figure 2.5 and 2.6) that a line length less than 550 μm affects the matching, gain and efficiency. Above that value, the most affected antenna

parameter is the bandwith.
The distance between the GCPW and the circular antenna increases both the imaginary part and real part of the input impedance (see Figure 2.7 and 2.8) and thus essentially affects the matching.

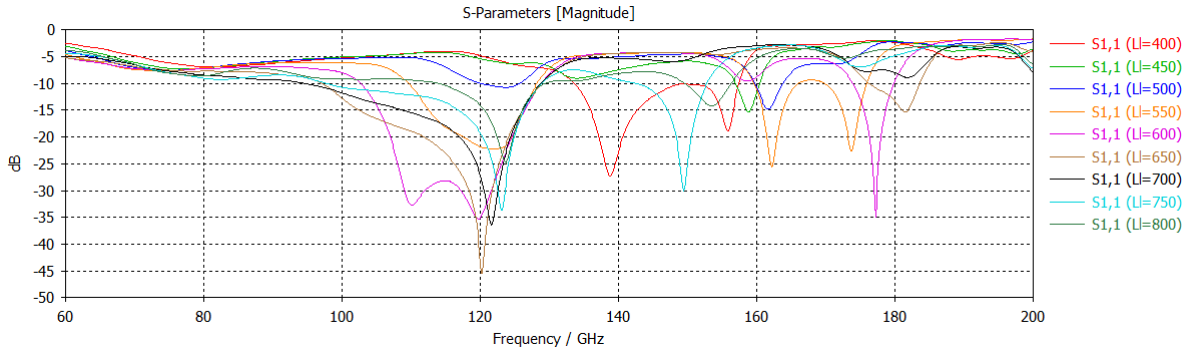


Figure 2.5: S11 resulted from parametric sweep on L_l.

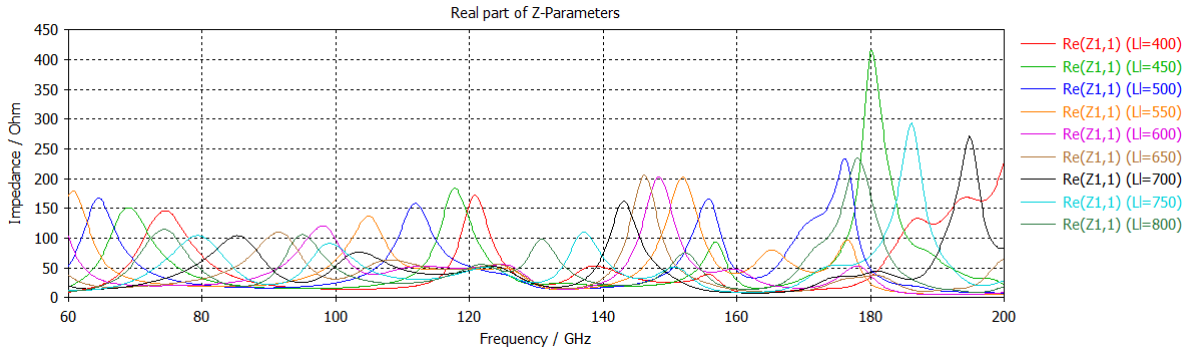


Figure 2.6: Real impedance resulted from parametric sweep on L_l.

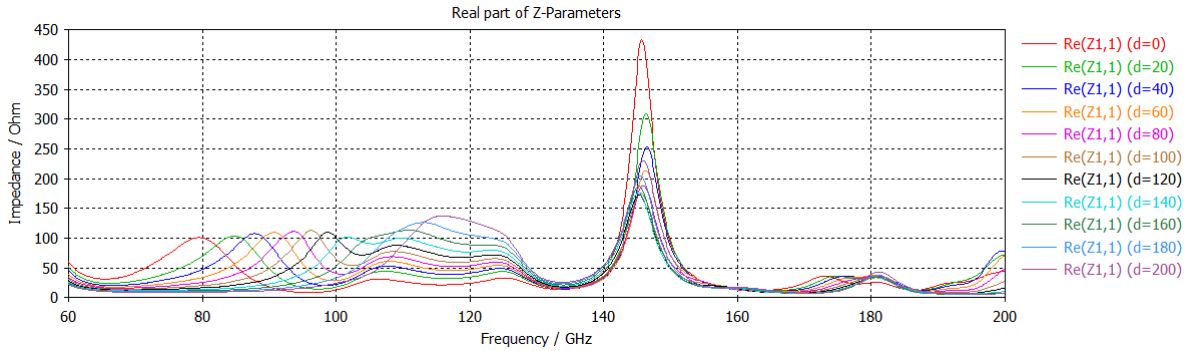


Figure 2.7: Real part impedance resulted from parametric sweep on 'd'.

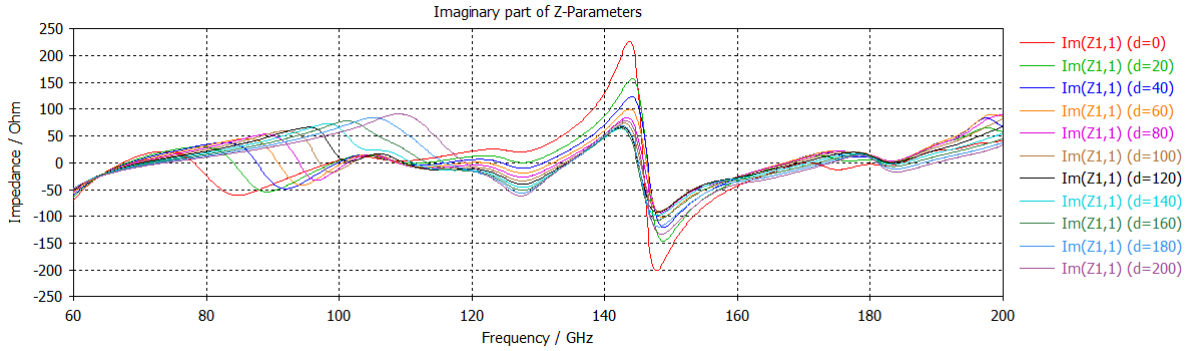


Figure 2.8: imaginary part impedance resulted from parametric sweep on 'd'.

2.5.2 Effect of lateral ground width W_g

When the width of the two lateral ground planes of the GCPW line becomes too small (around 100 μm) it decreases the input impedance value at desired frequency 120 GHz as shown in Figure 2.9 and 2.10.

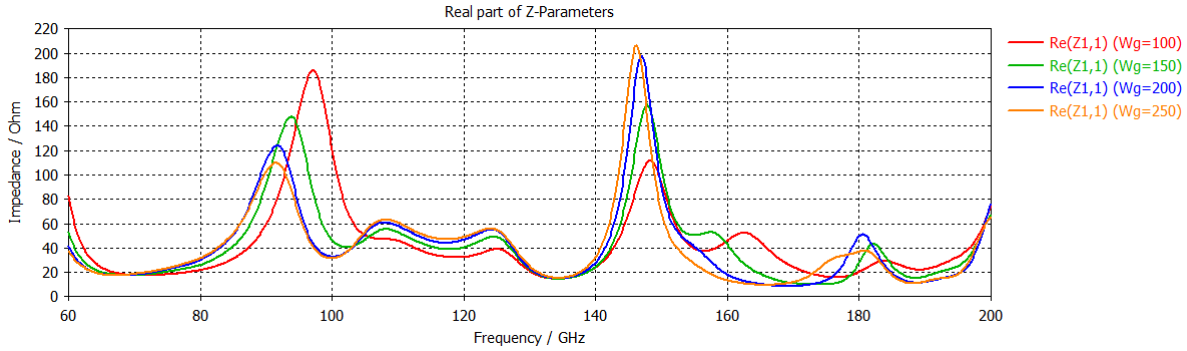


Figure 2.9: Real part impedance resulted from parametric sweep on W_g.

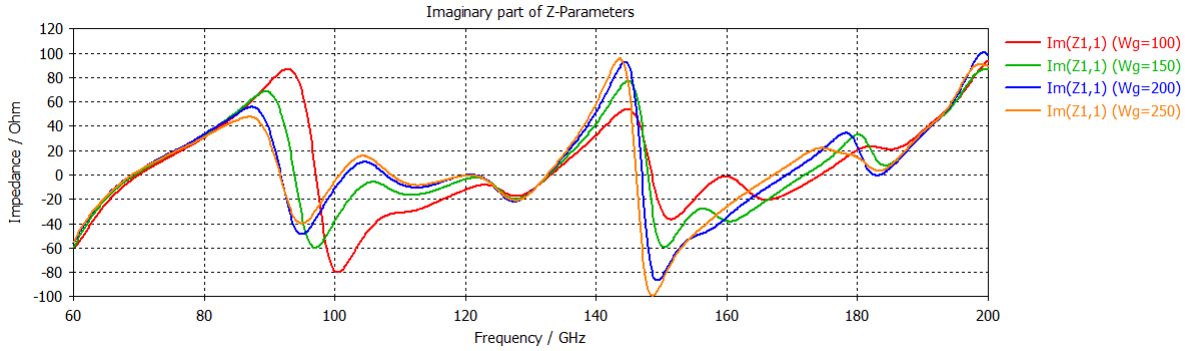


Figure 2.10: imaginary part impedance resulted from parametric sweep on W_g.

2.5.3 Effect of radius R

Figure 2.11 shows the resulted reflection coefficient S11 for different radius values, a good resonance is obtained at the desired frequency of 120 GHz for a radius of 140 µm. The antenna is also very well matched at this frequency.

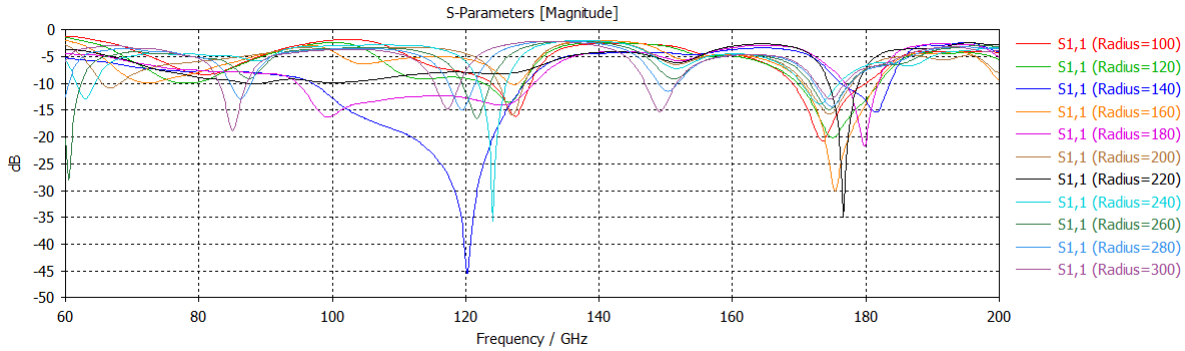


Figure 2.11: S11 resulted from parametric sweep on R.

2.5.4 Intermediate results

In this section we will summarize the results obtained for the parameters set after the optimization, and whose values are given in Table 2.5.

With the proposed antenna, the simulation results show a reflection coefficient of less than -10 dB ranging from 97.4 GHz to 128.7 GHz. That yields a 31.3 GHz bandwidth. Figure 2.13 shows the simulated 3D radiation pattern, the achieved gain and efficiency are respectively 4.42 dB and 81.44%.

W_l	GCPW central line width	20 µm
G	Gap between GCPW central line and lateral ground	12 µm
W_g	Lateral ground width	228 µm
L_l	GCPW length	650 µm
d	Length of the GCPW central line extention	65 µm
R	antenna radius	140 µm
L_s	substrate length	1400 µm
W_s	substrate width	500 µm
H_s	substrate thickness	230 µm

Table 2.5: Design parameters values.

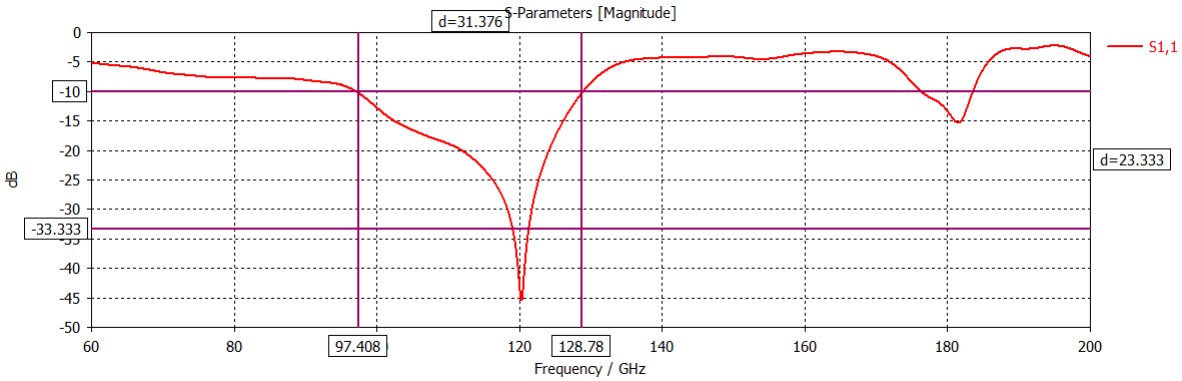


Figure 2.12: Reflection coefficient of circular antenna.

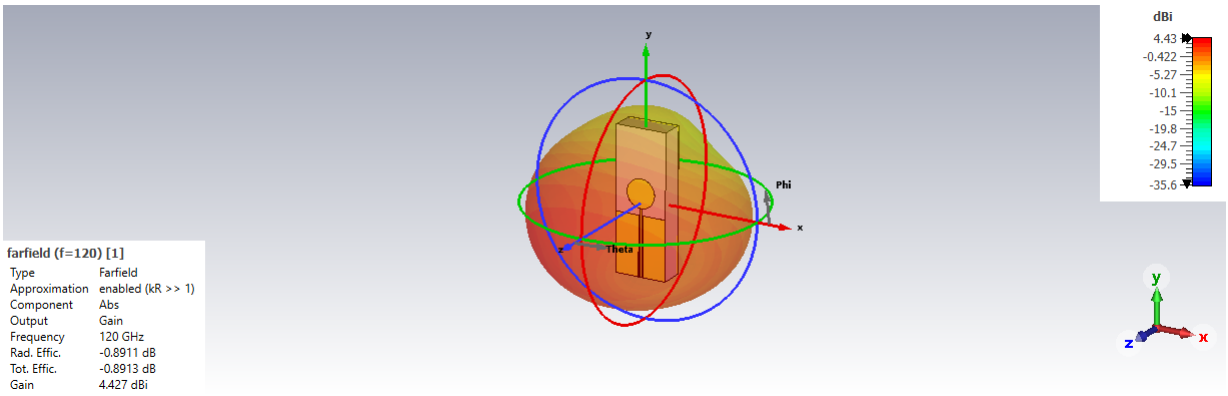


Figure 2.13: 3D far-field radiation pattern.

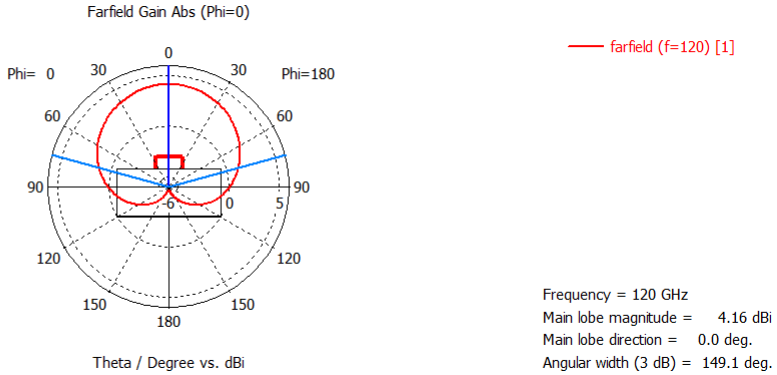


Figure 2.14: H-plane radiation pattern.

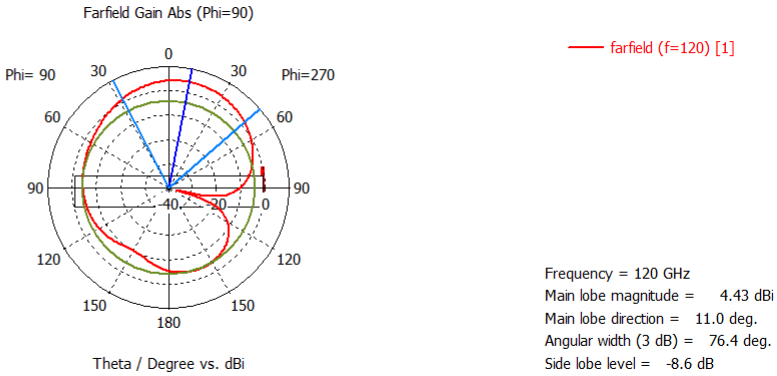


Figure 2.15: E-plane radiation pattern.

2.6 Substrate and ground effect

The primary objective of this work is to evaluate the effect of the silicon substrate on the antenna's performance, the choice of substrate plays a very important role when designing on-chip antennas. A substrate with high permittivity and low resistivity such as silicon will detrimentally affect the gain, efficiency and bandwidth, it will also distort the radiation pattern as was concluded in [8].

2.6.1 Effect of silicon substrate size

In this part we will analyze the impact of the substrate size on the results obtained in the previous section, however we will keep constant the high dielectric constant (11.9) of silicon substrate and the resistivity (10000 Ω-cm) also invariable

for all simulations. Through a parametric study, the width W_s, the length L_s and the thickness H_s of the substrate will be taken into account, the results of the reflection coefficient, and the gain will be exposed.

Looking at the results of the simulations shown below, we can see that the width W_s and the length L_s of the substrate have an impact on both the matching and the gain and thus the efficiency, both the real and imaginary part are affected and the antenna is no longer matched at 120 GHz , which means that we can't study the antenna without taking into account the size of the substrate, it changes all the radiation parameters as well as the matching.

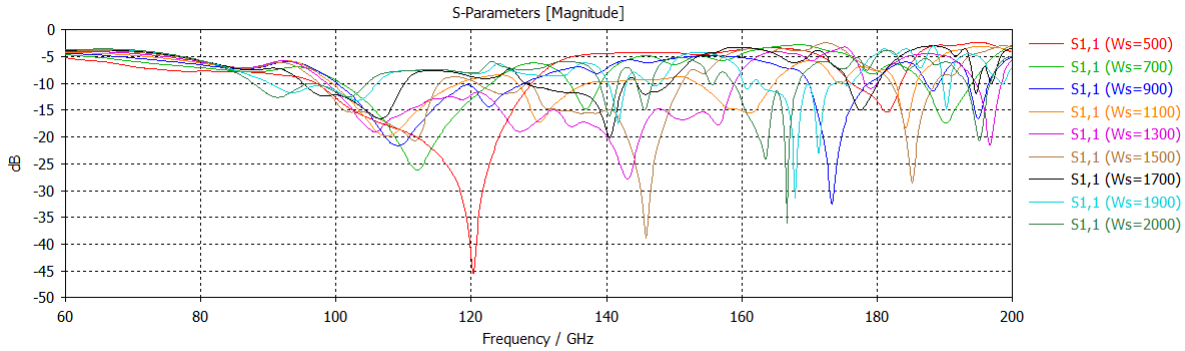


Figure 2.16: S11 with parametric sweep on W_s.

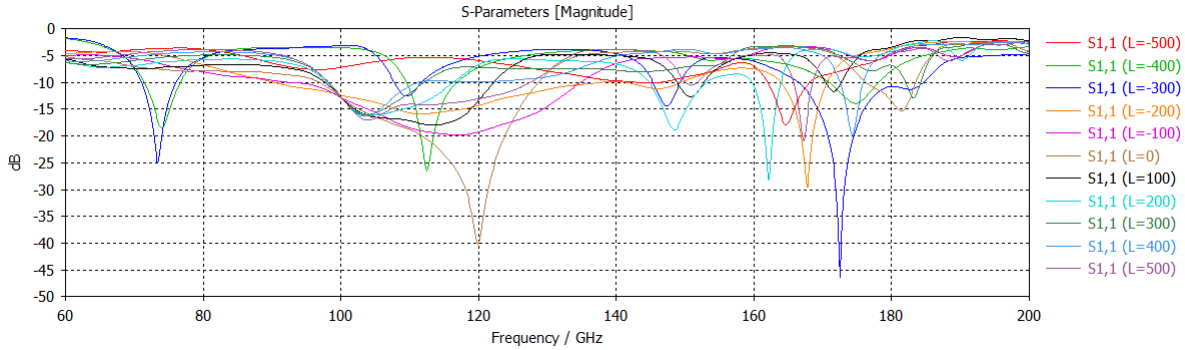


Figure 2.17: S11 with parametric sweep on $L_s = 1400 - L$, .

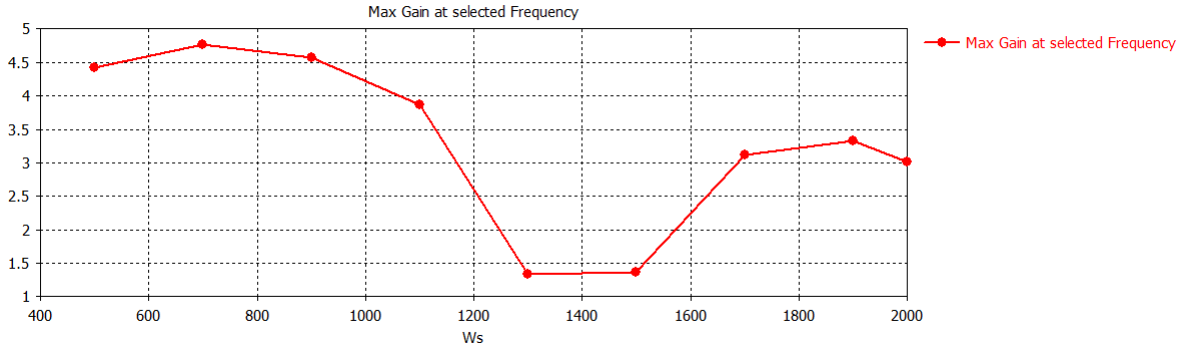


Figure 2.18: Gain with parametric sweep on W_s.

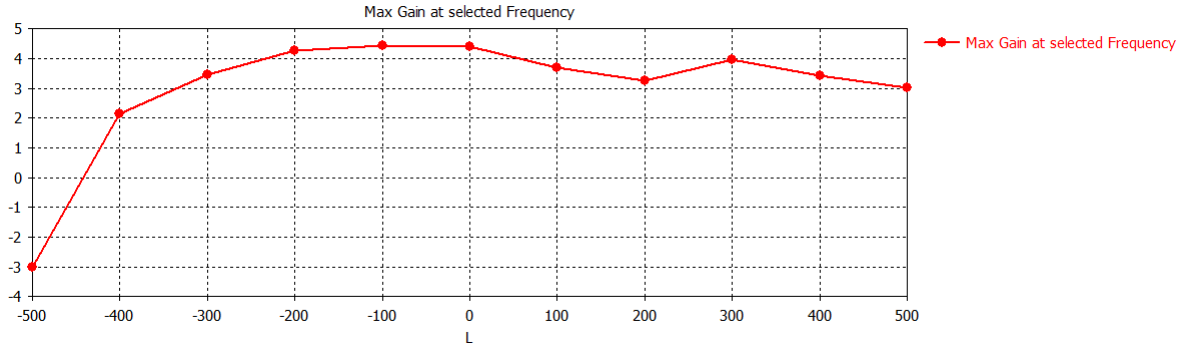


Figure 2.19: Gain with parametric sweep on $L_s = 1400 - L$.

Regarding the effect of substrate thickness, Figures 2.20 and 2.21 shows that there is a shift in the real part of the impedance, the same is noted for the imaginary part of the input impedance whose result is not presented here, while the gain changes with the thickness of the silicon substrate.

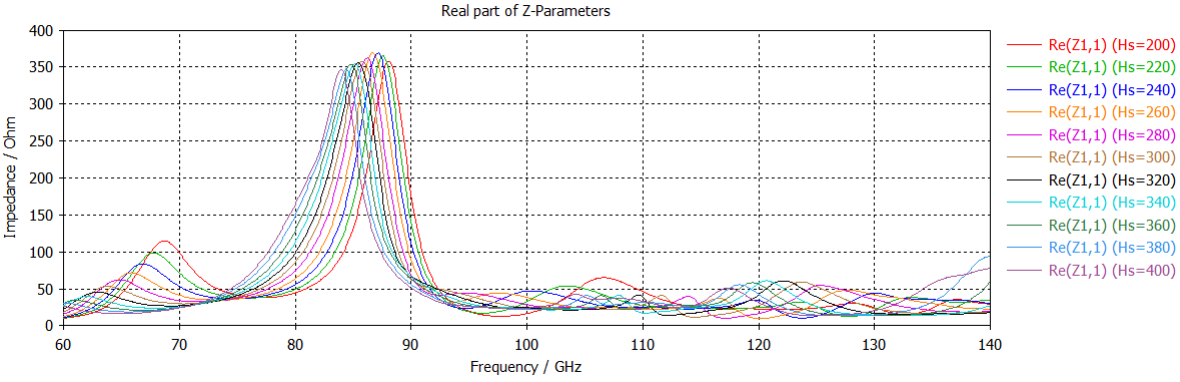


Figure 2.20: Real part of the imput impedance with parametric sweep on H_s.

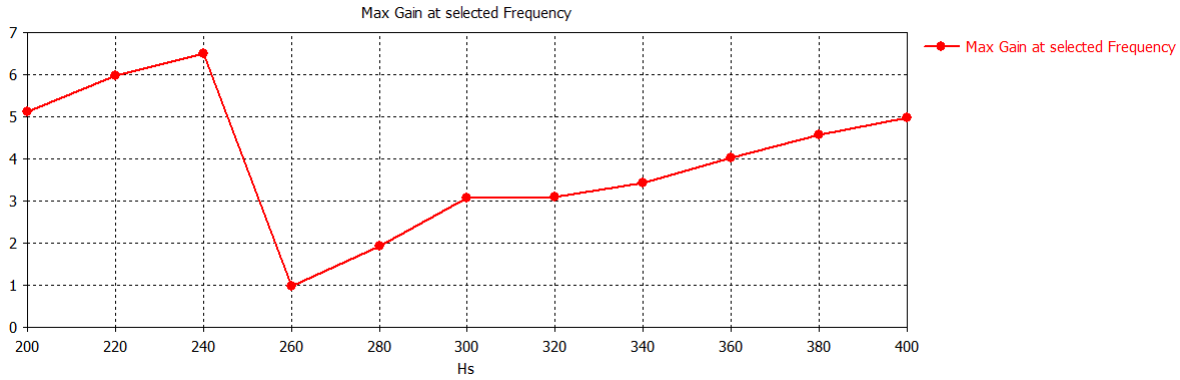


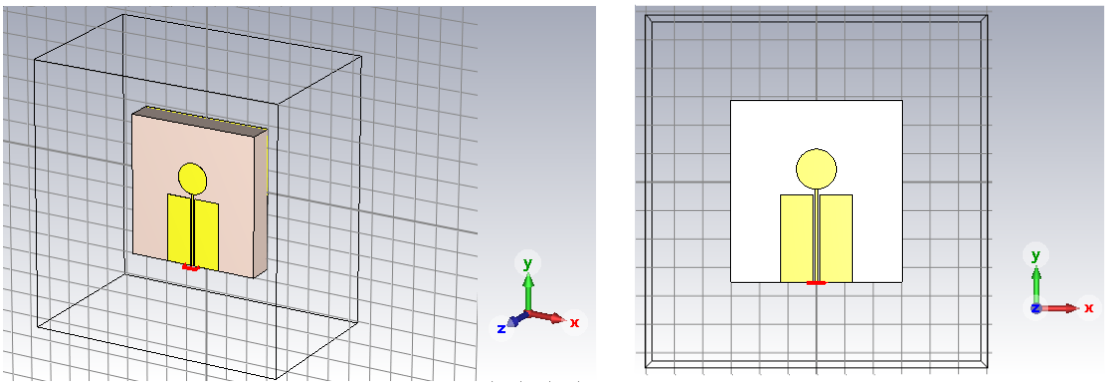
Figure 2.21: Gain with parametric sweep on H_s.

Table 2.6 contains a comparison of the radiation parameters of the circular antenna antenna for two different substrate sizes, all other design parameters remain unchanged, on the first row are the results obtained in the previous section, and on the second row are the results obtained after increasing the substrate size. The gain has increased by 1.82 dB at the expense of losing around 3 GHz of bandwidth.

Substrate size (W_s * L_s * H_s)	Bandwith	Gain	Efficiency
500*1400*230 µm	28.55 GHz	4.42 dB	-0.8883 dB (88.5%)
1195*1270*240 µm	25.53 GHz	6.28 dB	-0.04048 dB (99%)

Table 2.6: Comparison of antenna gain, bandwith and efficiency for two substrate sizes.

A substrate with dimensions 1195 µm * 1270 µm *240 µm is now retained, a final optimization step has been made and the only change is the d-value of the GCPW centreline extension from 65 µm to 40 µm. The reflection coefficient S11 and the radiation pattern are given below. 3-D view and front view of the proposed antenna is given in Figure 2.22.



(a) 3-D view (b) Front view

Figure 2.22: The proposed circular on-chip antenna

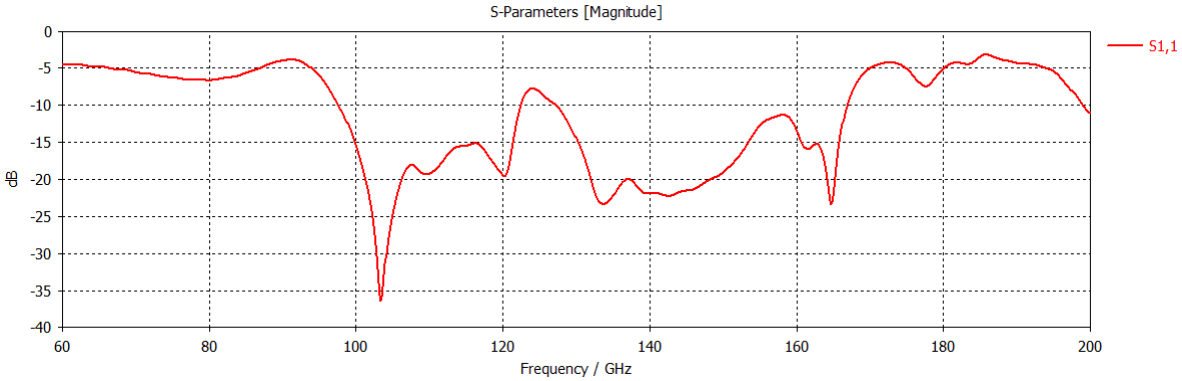


Figure 2.23: Reflection Coefficient of the final antenna design.

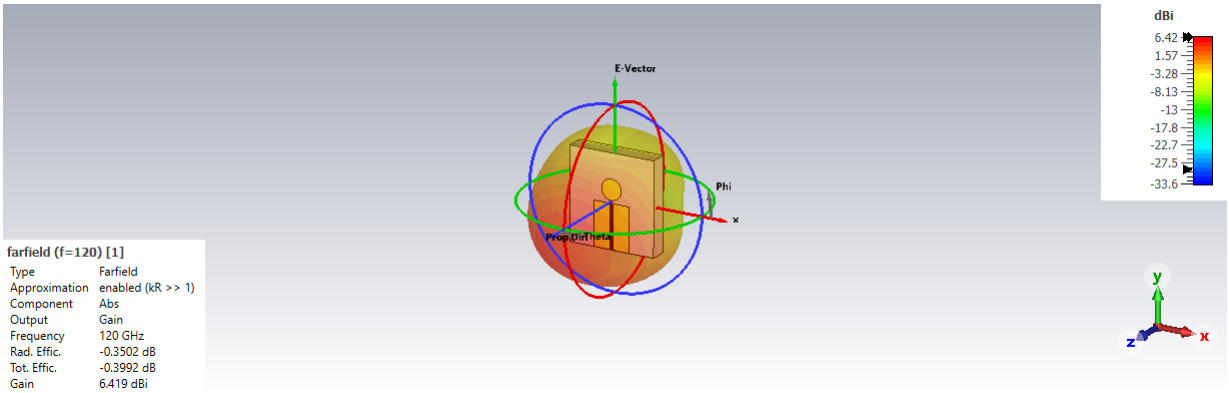


Figure 2.24: Radiation pattern of the final antenna design.

2.6.2 Effect of silicon resistivity

The substrate material presents the most difficulty. To understand its impact on total antenna performance, variables such as substrate resistivity, dielectric constant, and substrate dimensions should be assessed.
Since the dielectric constant $\varepsilon_r = 11.9$ of silicon is kept invariable during this work, the only variable that remains and on which we can play is the resistivity of silicon, during the simulations that have already been done in the previous sections, we used silicon with a conductivity of 0.01 S/m, which corresponds to a resistivity of 10 kΩ-cm.

In the following we will present the results of simulations performed on the final design set in the previous section for three values of silicon resistivity, 10000 Ω-cm, 20 Ω-cm and 10 Ω-cm respectively, only the resistivity is varied while all other design parameters remain unchanged.

Low values of S11 for low resistivity substrate confirm that the losses in the substrate are very high compared to the case of high resistivity substrate,

Indeed the simulated power loss in the dielectric given in Table 2.7 for the three substrate resistivites confirms that dielectric losses are very important in low resistivity silicon, the gain is also very much affected by the low resistivity of the substrate, we see a difference of 5.2 dB of gain between the substrate at 10000 Ω-cm and 20 Ω-cm.

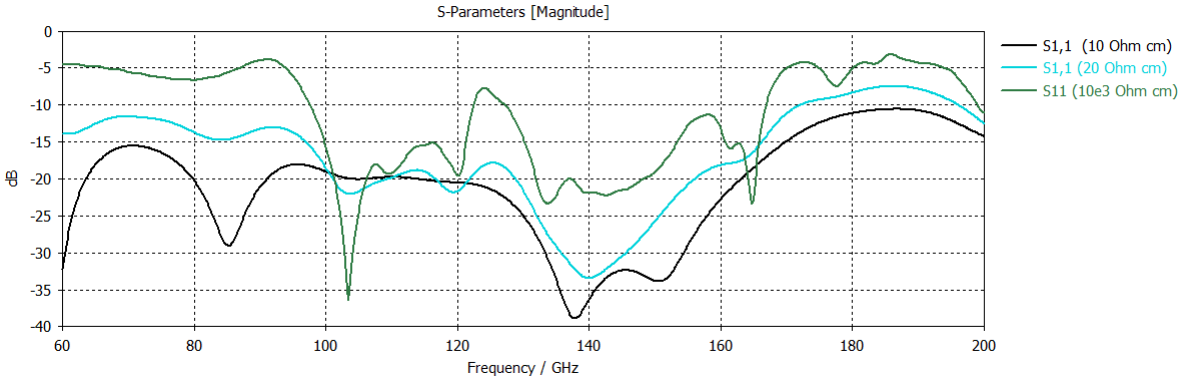


Figure 2.25: S11 coefficient for silicon substrate resistivity of 10000 Ω-cm, 20 Ω-cm and 10 Ω-cm.

Silicon resistivity	Power loss	Gain	Efficiency
10000 Ω-cm	-28.5 dBW	6.42 dB	-0.35 dB
20 Ω-cm	-5.45 dBW	1.22 dB	-4.9 dB
10 Ω-cm	-4.41 dBW	-1.83 dB	-7.5 dB

Table 2.7: Power loss in silicon, antenna gain and efficiency for silicon substrate resistivity of 10000 Ω-cm, 20 Ω-cm and 10 Ω-cm.

2.6.3 Ground effect

The ground plane is not there by accident, but to provide some electromagnetic shielding and reflect the waves that propagate through the substrate towards the desired propagation direction. The ground plane prevents some of the radiation from travelling through the substrate in the opposite direction to that of the antenna radiation.

Extending ground plane

Since it acts as an RF mirror, the presence of an infinite ground plane is desired when simulating antennas, the simulation results displayed in Figure 2.26 show the radiation pattern considering ground plane larger than the size of the substrate, the gain is increased by about 1 dB and the efficiency is reduced by 0.23 dB.

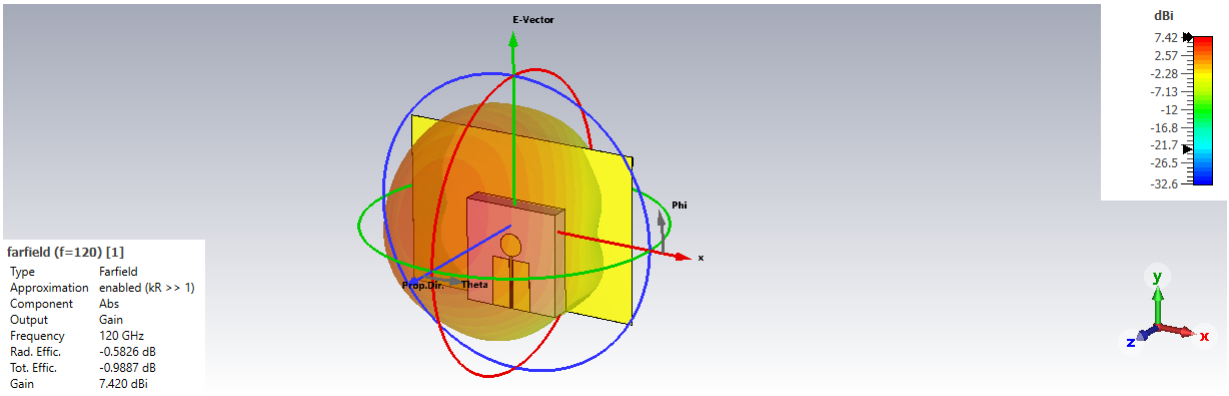


Figure 2.26: Radiation pattern with extension of ground plane

2.7 Gain enhancement: Antenna array and dielectric resonator antenna

As mentioned at the beginning of this report, maximum gain and efficiency should be achieved over the widest possible bandwidth. As part of this work, several techniques have been tested in order to improve the performance of the antenna, in the following we will show the results of the simulations for the more relevant trials.

2.7.1 Antenna array

In [31] a 16 element antenna array allows to reach a gain and efficiency of 11.71 dBi and 70.8% respectively at 300 GHz using a polycarbonate layer on top of a high resistivity silicon. Using the 'Task Array' option in CST, we simulated two arrays, the first is composed of two elements and the second is composed of 4 elements, the resulting radiation diagram of 2 element array is given in Figure 2.27. With an array of two elements we reach a gain of 7.8 dB and an efficiency of -0.8626 dB, while with a network of 4 elements the gain and efficiency are 10.76 dB and -1.055dB respectively.

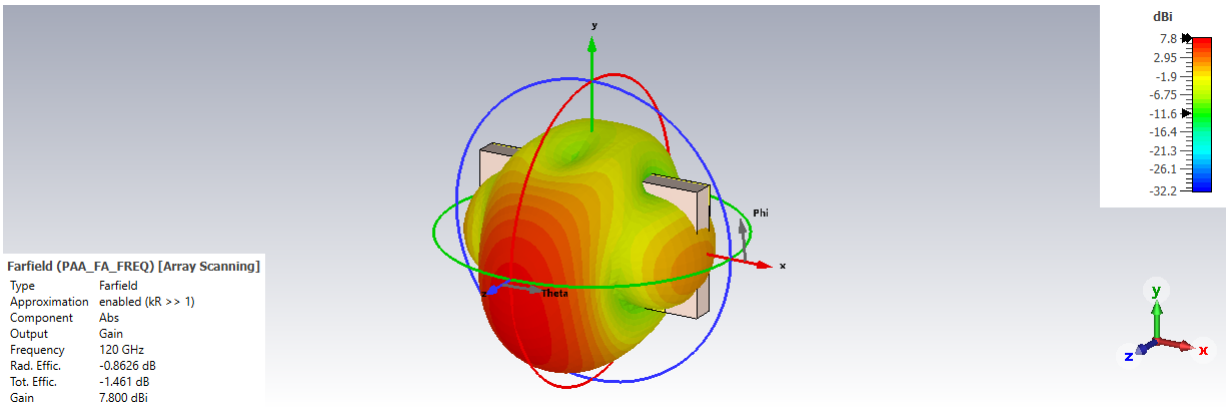


Figure 2.27: Radiation pattern of 2 element array.

2.7.2 Dielectric resonator antenna DRA

The results of the simulation of a circular antenna with an Alumina dielectric resonator shown below show that the use of a DRA allows the gain to be increased considerably, from a gain of 6.4dB for the antenna shown in Figure 2.22 to a gain of 9.16dB, moreover, the size of the substrate has no influence on the antenna performance.

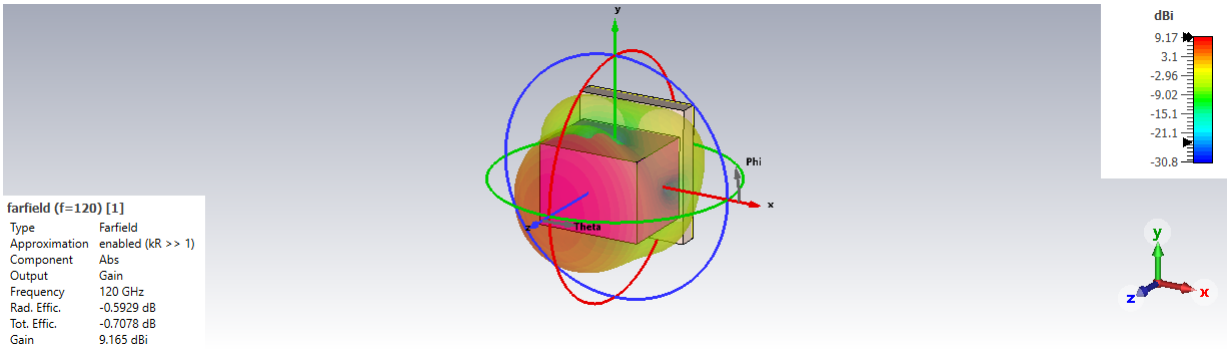


Figure 2.28: Radiation pattern of DRA antenna.

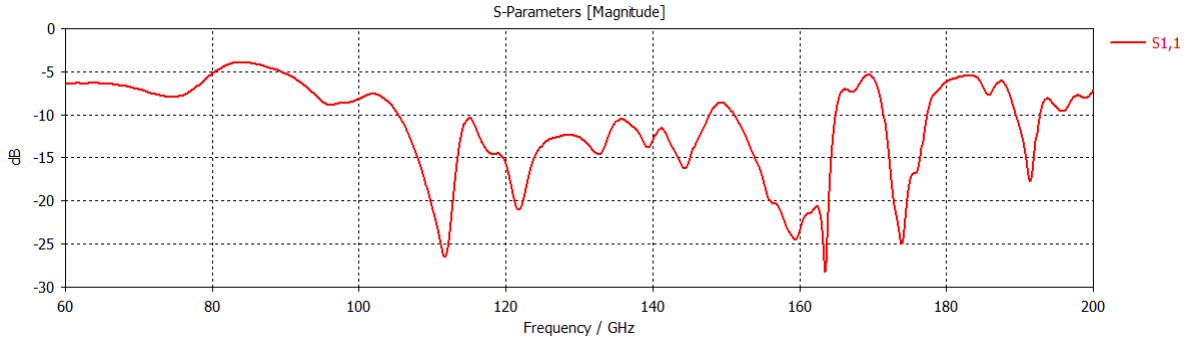


Figure 2.29: S11 of DRA antenna.

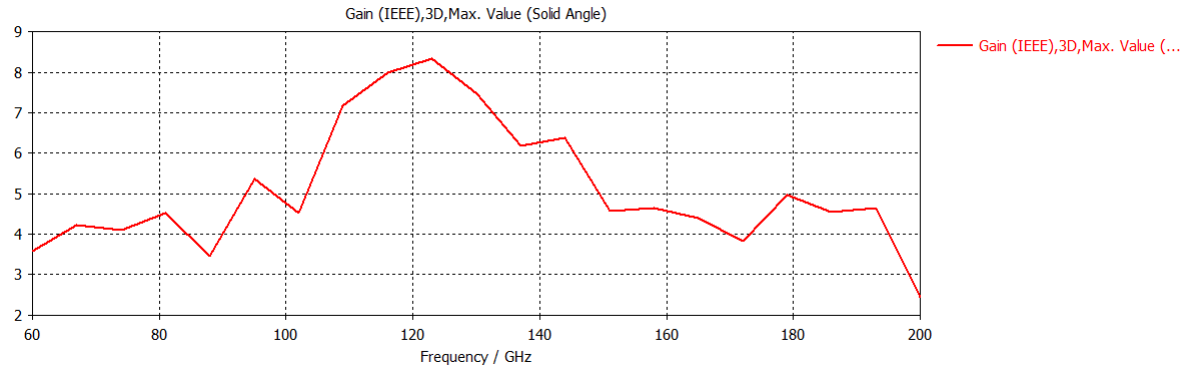


Figure 2.30: Gain over frequency for DR antenna.

Chapter 3

Pattern reconfiguration

Having an antenna that is operational in multiple modes allows to have lighter communication systems with more diversity and capability and makes them more efficient, this has become the new trend that the antenna design field is moving towards. The same antenna designed in the previous chapter was made reconfigurable and capable for beam steering by using parasitic elements. In this chapter, we will first review the literature and the different techniques used in the field of reconfigurable pattern antennas, then we will present the simulation results of our modified antenna.

3.1 State of the art

An antenna is reconfigurable if it has the capability to change its fundamental operating parameters, like switching between several operating frequencies, changing polarization or steering the radiation pattern at different angles. Usually the reconfiguration of one antenna parameter is done while keeping the other parameters unchanged, but this does not prevent the combination of several reconfigurations in a single design.
Reconfigurable radiation pattern antennas can either steer the beam with a change in radiation pattern, or by keeping its shape unaffected and only directing the beam toward different angles, thus avoiding the use of antenna array. Several research projects have been carried out in this area in parallel with the rapid development of on-chip antennas field, in this work we will only focus on the reconfiguration of the radiation pattern.
Several techniques have been used in order to do beam steering of on-chip antennas radiation pattern, among others, varactors, switches, parasitic elements...
In [25] nine directions of the radiation pattern beam of a rectangular patch antenna with a coaxial feed are obtained using four complementary split-ring resonator

(CSRR) etched on ground (see Figure 3.1). For H-plane beam switching, The left and right CSRRs are used and are placed near the non radiating edges of the patch, up and down CSRRs are used for E plane beam switching and are placed near the radiating edges.

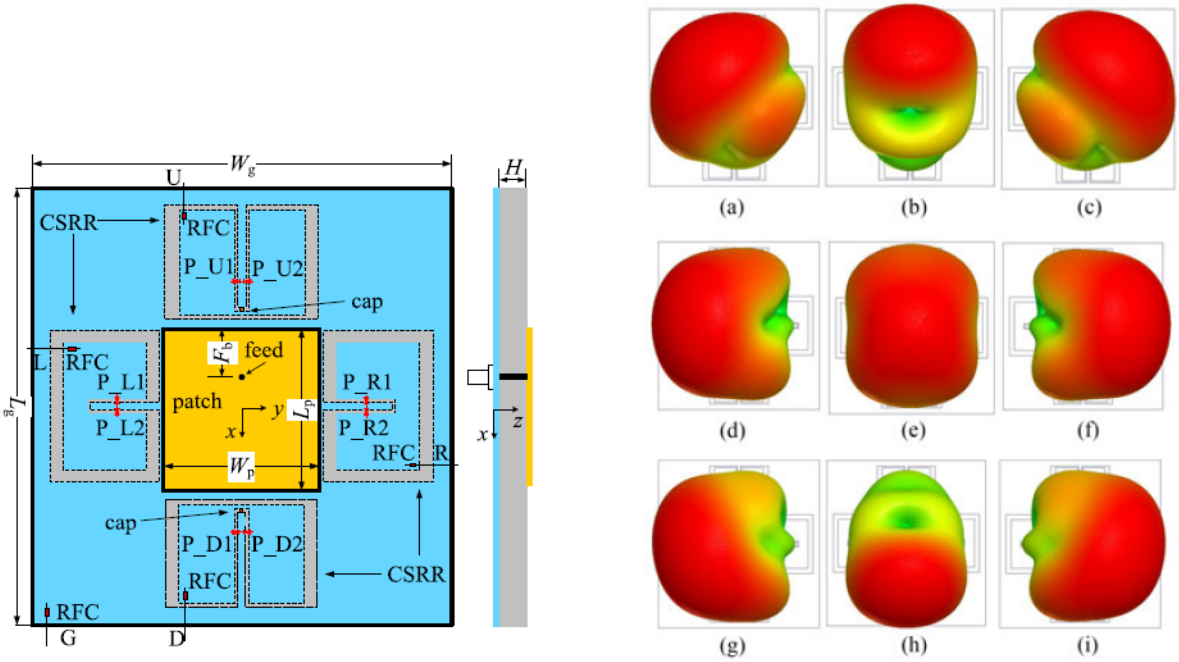


Figure 3.1: Structure of the proposed antenna and pattern of the nine direction [25], (a) left-up, (b) up, (c) right-up, (d) left, (e) middle, (f) right, (g) left-down, (h) down, and (i) right-down.

Combining frequency and pattern reconfiguration was achieved in [26] using radiator with two chip inductors, because the inductors acts as a short and open circuit at lower and upper frequency respectively, the radiator exhibits behavior resembling to both a longer and shorter dipole resonating at two different frequencies. pattern reconfigurability is accomplished using four parasitic reflectors positioned all around the radiator.

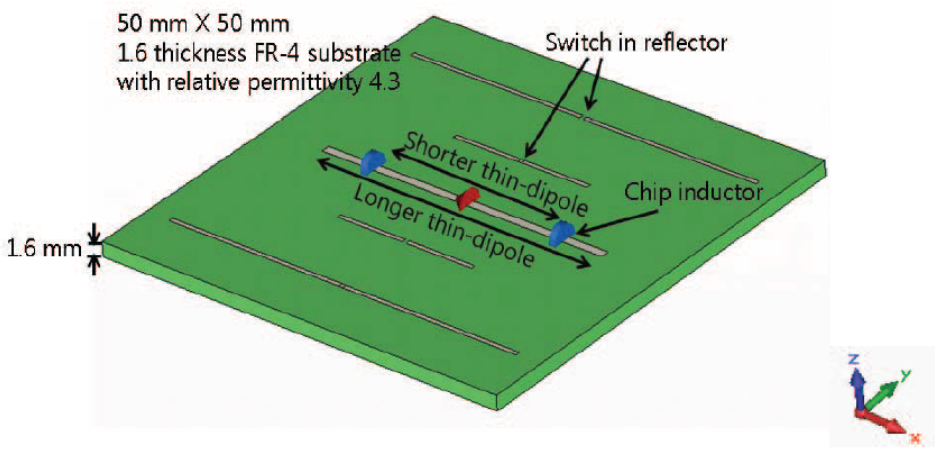


Figure 3.2: The geometry of the antenna in [26].

Parasitic elements were also used in [27], Figure 3.3 shows two parasitic patches set on FR-4 substrate of thickness h2 and located on both side of the patch, the whole is laid on a FR-4 substrate of thickness h1, via holes are used to connect the two parasitic elements to ground. Results shows that both the height and the dielectric constant of the substrate holding the parasitic elements affect the tilt angle.

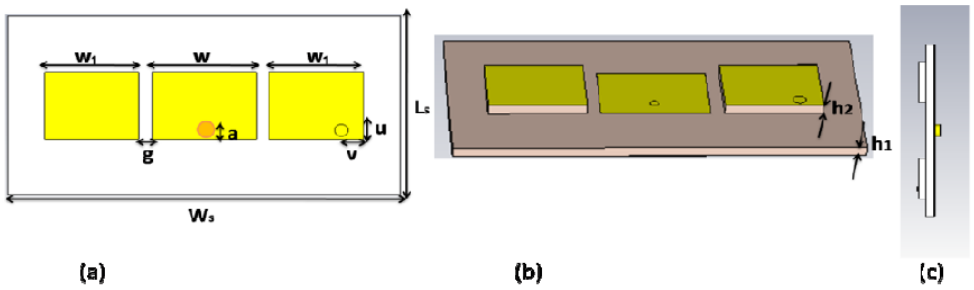


Figure 3.3: (a) Front view, (b) 3-D view and (c) Side view of the proposed antenna in [27].

Paper [28] present frequency and pattern reconfigurable antenna, five diodes (D1-D5), four parasitic elements, an electric-inductive capacitive (ELC) and a closed ring resonator (CRR) are used. For frequency reconfigurability, the diode (D1) is implanted between the ELC and CRR resonators. To produce pattern variety, the remaining four diodes (D2-D5) are implanted between the ground plane and four parasitic components, controlling the electrical length of the ground plane.

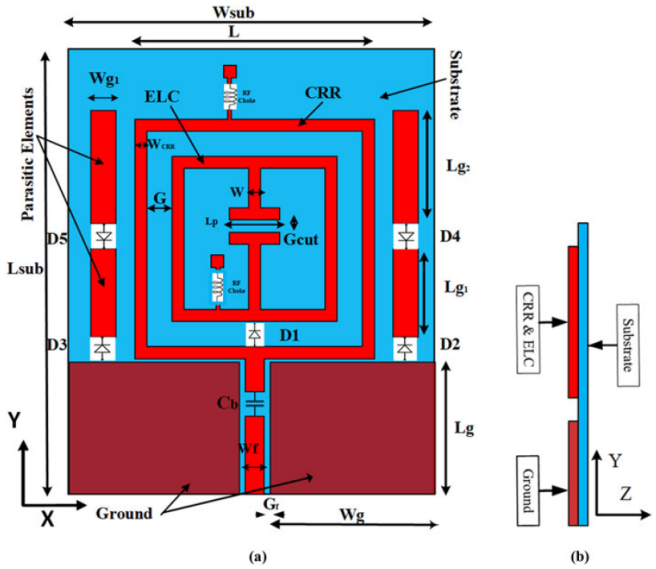


Figure 3.4: (a) Front view and (b) Side view of the proposed antenna in [28].

A planar Yagi-Uda antenna is investigated in [29] and a reconfigurable micro-machined antenna in [30] allows beamsteering on three different angles: –25°, 0°, and 25°.

3.2 Pattern reconfigurable antenna design using parasitic elements

In the following, the design concluded in the previous chapter will be modified in order to achieve a pattern reconfigurable antenna, The circular antenna's ability to change its radiation pattern is made possible by the insertion of a parasitic components in the design.

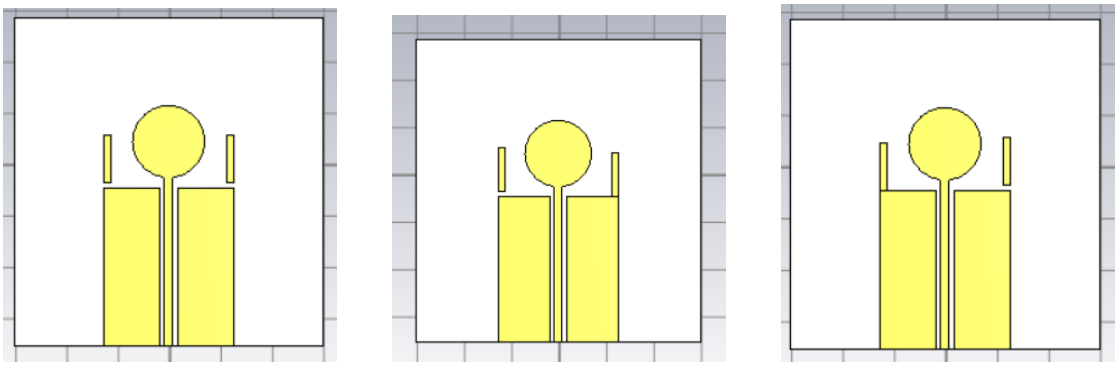
3.2.1 Methodology

All the parameters of the design shown in Figure 2.22 will be kept invariable, the addition of two parasitic elements in the same way as the design given in [28] will be studied in this part, one parasitic element will be added on each side of the circular antenna, we will not use switches to connect the parasitic elements to the ground plane but this will be done manually during the simulation in order to test the connection on the left and on the right of one parasitic element at a time. The goal is to have a beam switching angle of more than 20°over the widest

possible frequency range. The choice of parasitic elements was made after testing several parasitic shapes, the results of the radiation pattern in the H plane and the reflection coefficient S11 will be evaluated.

3.2.2 Design and simulation resuslts

In order to make our design capable of pattern reconfigurability, a rectangular shaped parasitic element has been placed on either side of the circular antenna as shown in Figure 3.5, one bar is connected to the ground plane at a time in order to direct the beam in either direction.



(a) Bars not connected (b) Right bar connected (c) Left bar connected

Figure 3.5: Three designs for reconfigurable pattern antenna

The width 'W', the length 'L', and the distance 'pos' between the element and the circular disk are the three degrees of freedom that will be evaluated in order to have a beamsteering angle of minimum 20° with respect to the direction of the beam given in Figure 3.9 of the original design We can see that the main lobe direction is at 0°.

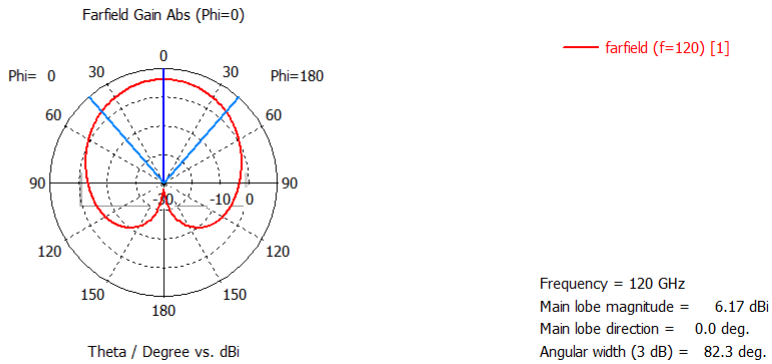


Figure 3.6: H plane of the antenna without parasitic bars.

Both the width and the position of the parasitic elements do not affect the steering angle too much, it is mainly the length L that modifies the results. During the simulations we examined the radiation pattern in the H-plane, we obtain a tilt angle greater than or equal to 20° for a length 'L' equal to 185 μm for the 3 GHz frequency band starting from 117 GHz to 120 GHz, the elements width is W = 25 μm and they are positioned on the extremities of the ground planes as shown in Figure 3.5 . The radiation pattern at different frequencies from 117 to 120 GHz is given in Figures 3.7 to 3.10, comparing those results with the one given in Figure 3.9 it is clear that the beam changes direction.

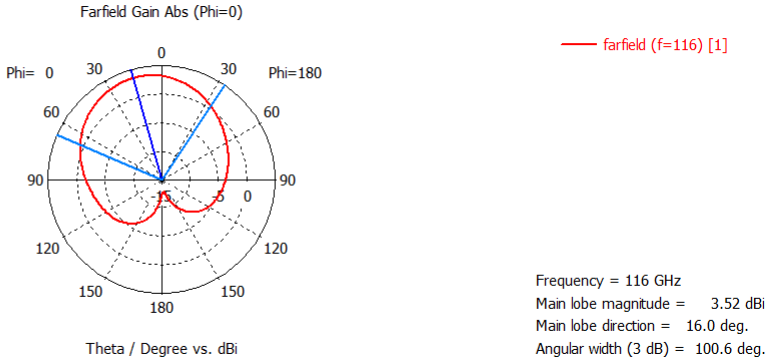


Figure 3.7: H plane at 116 GHz.

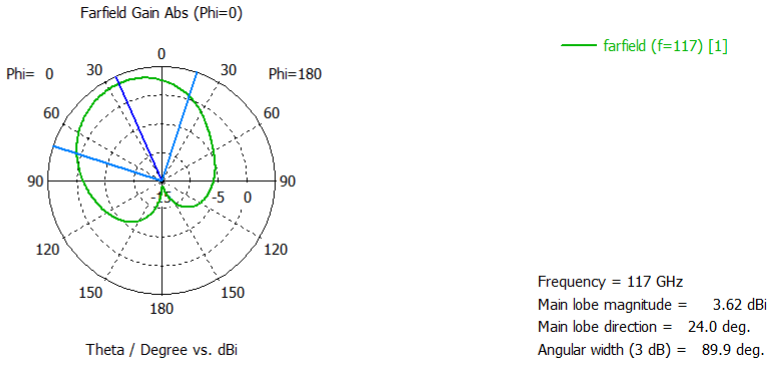


Figure 3.8: H plane at 117 GHz.

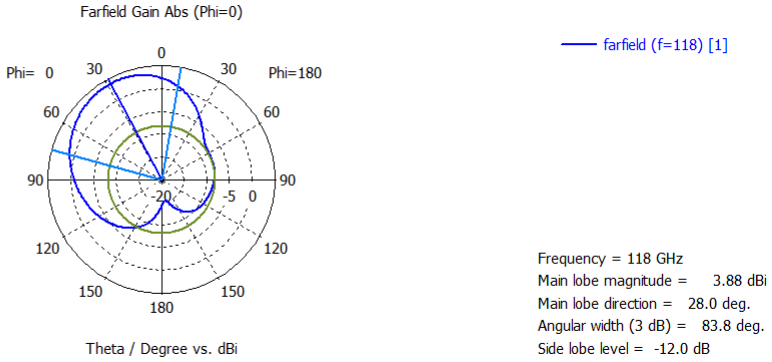


Figure 3.9: H plane at 118 GHz.

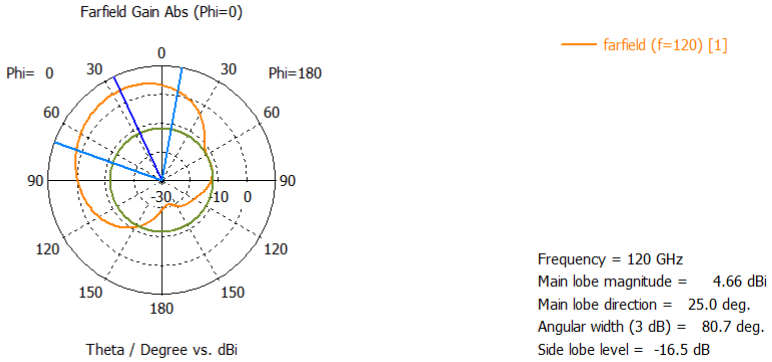


Figure 3.10: H plane at 120 GHz.

The problem with the results is that the reflection coefficient S11 (see Figure 3.11) gets worse once we connect one of the elements to the ground plane, this is due to the change in the input impedance value.

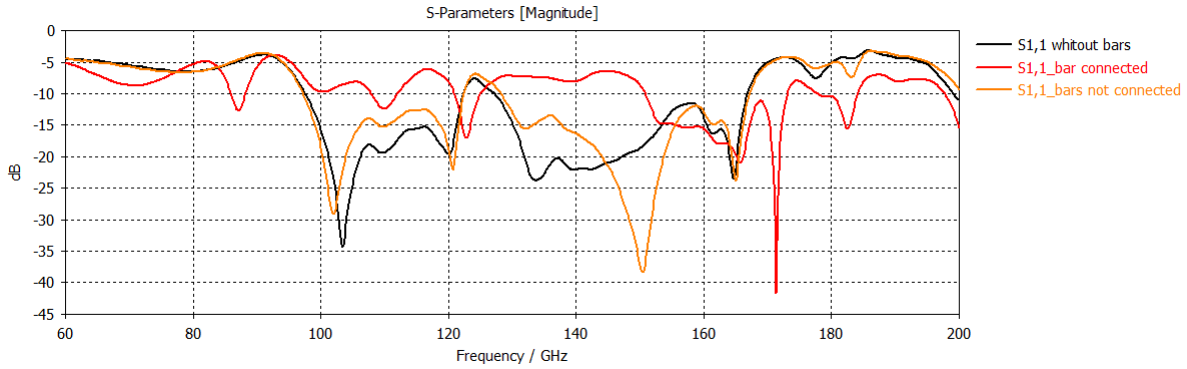


Figure 3.11: Reflection coefficients for design with and without parasitic bars, and with right bar connected.

The current distributions when not connecting any bars, when connecting right bar and when connecting left bar are given in Figures 3.12, 3.13 and 3.14 respectively, it can be seen that the symmetry observed in the case where no bar is connected is no longer there once a connection is established.

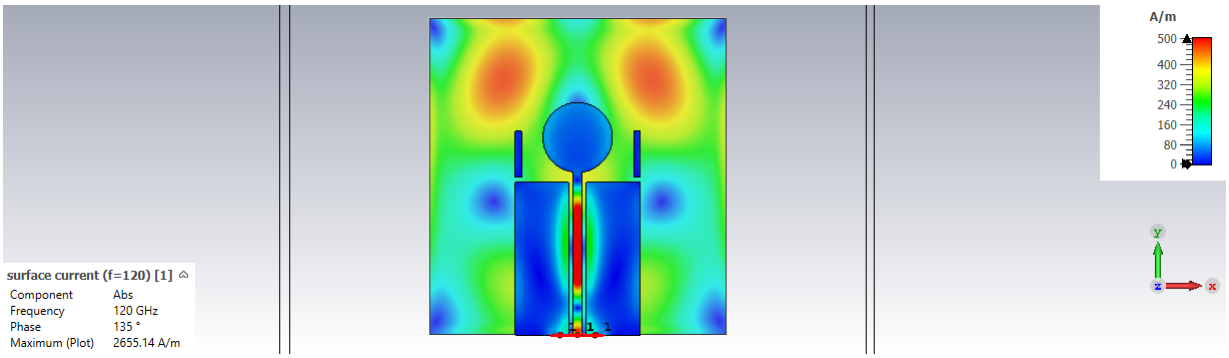


Figure 3.12: Surface currents with both bars not connected.

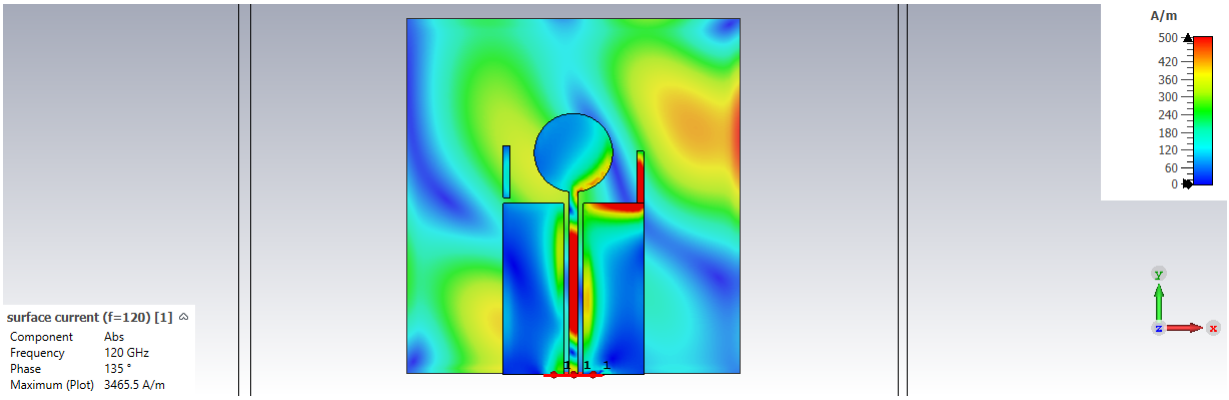


Figure 3.13: Surface currents with right bar connected.

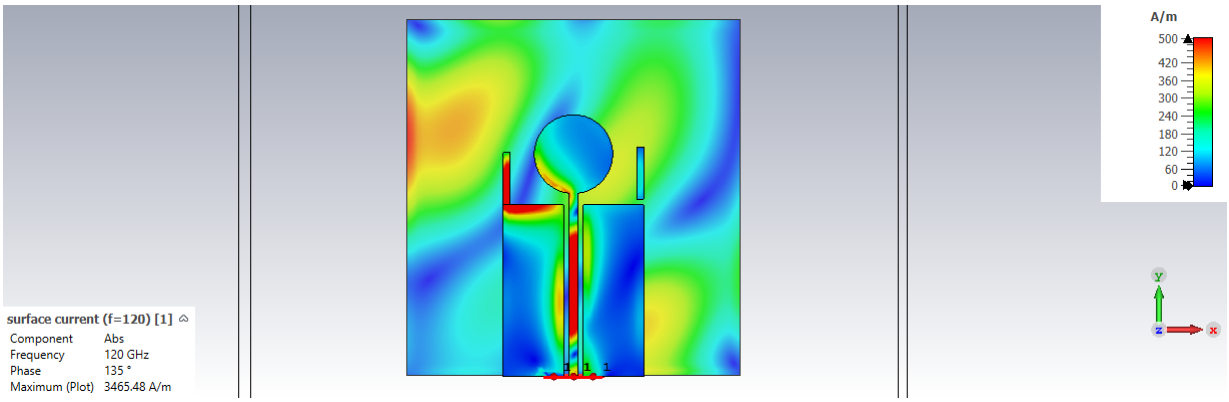


Figure 3.14: Surface currents with left bar connected.

Finally, the final results for a frequency of 120 GHz are given in Figures below, for the three designs given at the beginning of this section in Figure 3.5.the beam switches between two directions to the left and right at an angle of 25°.

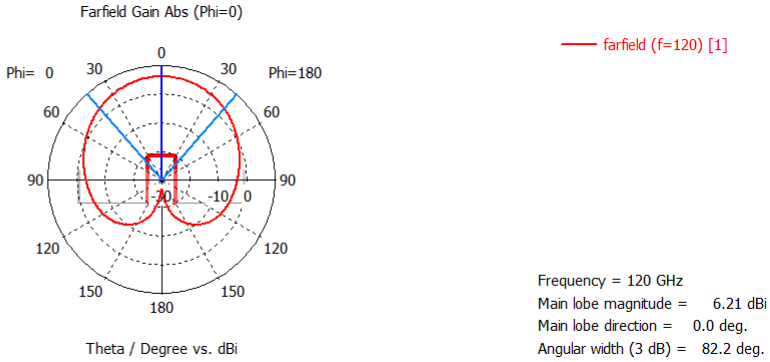


Figure 3.15: H plane at 120 GHz when no connection.

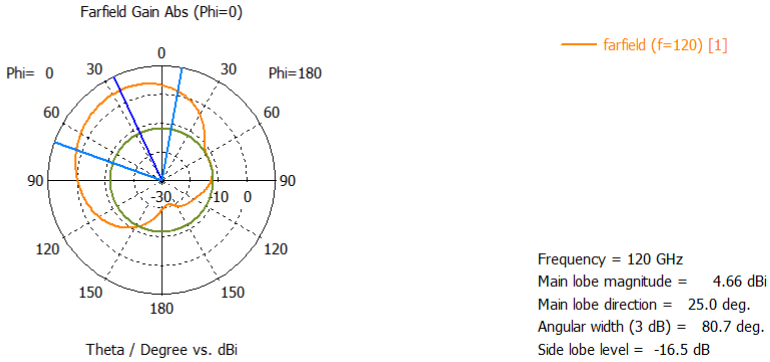


Figure 3.16: H plane at 120 GHz when right element is connected.

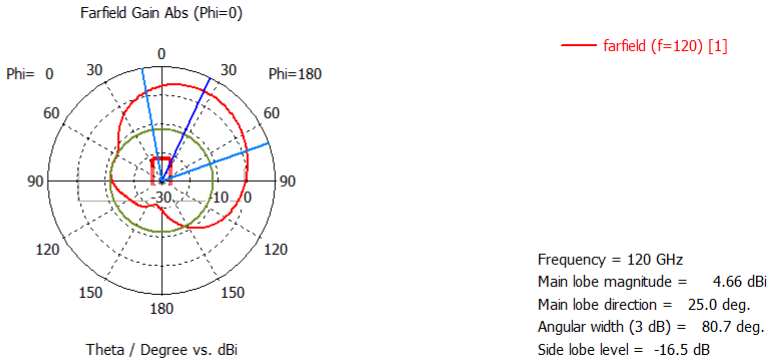


Figure 3.17: H plane at 120 GHz when left element is connected.

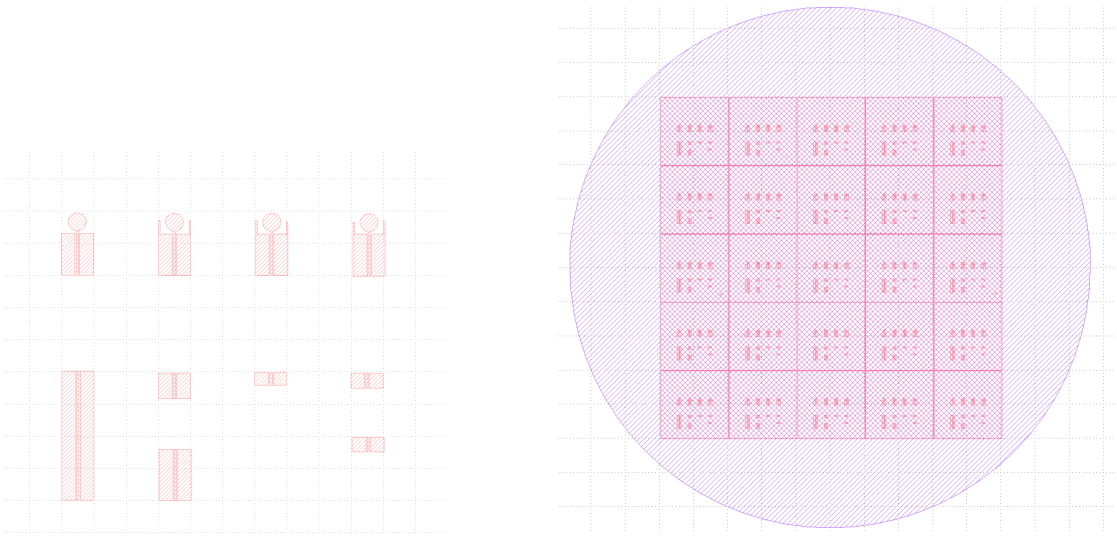
Chapter 4

Fabrication and measurement

This chapter will be devoted to a brief introduction of the fabrication process as well as a presentation of the different designs manufactured, then a presentation and discussion of the measurement results will conclude this chapter.

4.1 Fabrication process

Four antenna designs proposed in the previous two chapters of this report have been fabricated in the Winfab cleanrooms, these are the design proposed in chapter 2 and given in Figure 2.22 and the three configurations intended for beamsteering in chapter 3 and given in Figure 3.5.
The four designs as well as the lines needed for the de-embedding made up the content of the die which will be repeated over the whole wafer surface. Figure 4.1 show the unit cell and the final mask required during the fabrication process.
Three different substrates were used during the manufacturing process, standard silicon with a low resistivity, high resistivity (HR) silicon trap rich silicon (TR) obtained by 500nm of polysilicon deposition on high resistivity silicon wafer .
Before starting the fabrication process, the design of the mask needed for the lithography should be done, it is composed of a unit cell called the die, which is repeated several times. To layout the pattern for the mask, we used the free software 'Klayout' which is developed particularly for chip design.



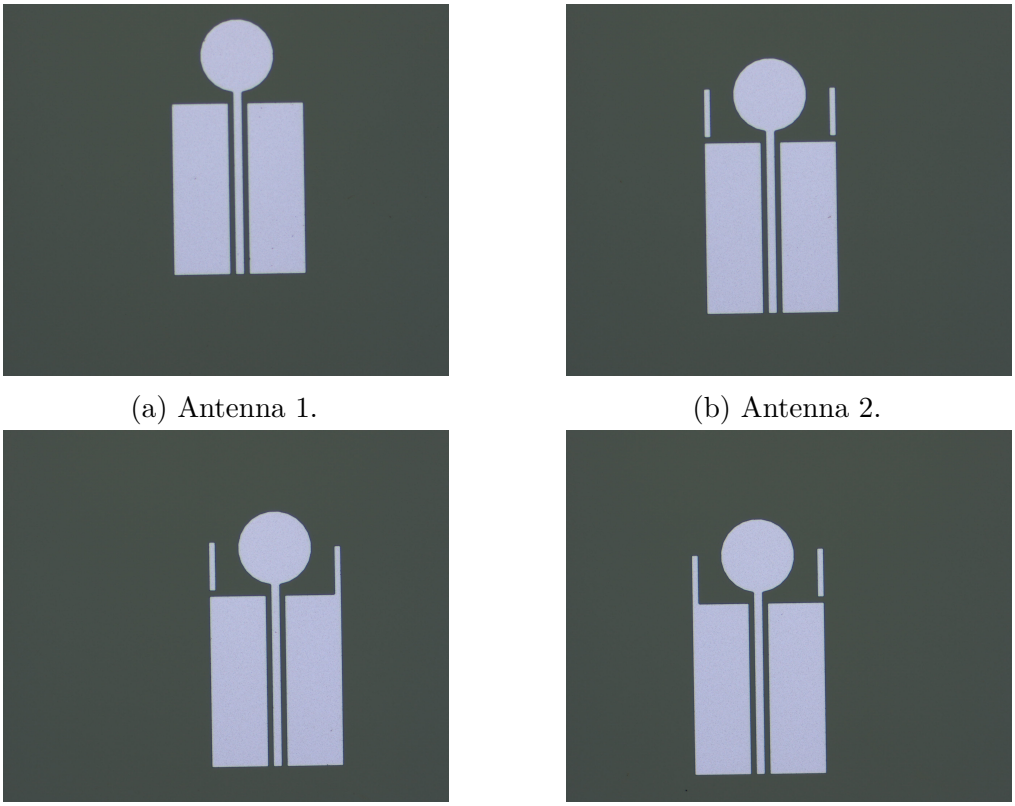
(a) Die (b) Mask

Figure 4.1: Die and masque designed with 'Kalyout'

First, a standard cleaning step of the wafers is composed of a combination of a piranha acid bath and HF batch in order to remove all the organic contaminants and unwanted oxide is done, then a 500 nm polysilicon deposition is performed on the wafers intended to become trap rich before that a 200 nm oxidation is done on all wafers. 1 µm of aluminum is then deposited on the front side of all wafers using the e-beam evaporation technique.
to end up with the different aluminum designs, an etching step is required, but before that, the application of a positive resist on the surface of all the wafers is done, this is followed by a lithography where the wafers are exposed to UV light through the chrome mask which has been fabricated with the design shown in Figure 4.1b, this step has the objective of making the resist non soluble on the parts forming the different antennas and de-embedding lines.the remaining soluble resist will be removed using a developer. The area of the wafer no longer protected by the resist will be etched by wet etching. Phosphoric acid was used as the etchant because of its high selectivity for aluminum, which allows it to etch metal but not silicon oxide.
The thickness of the wafers must be reduced to the target thickness of 240 µm that was fixed during the optimization step, to achieve this, a grinding is performed, the front side which contains the different aluminum dies is protected by a blue resist and a 125 µm thick tape, the different wafers are then placed back side up in a grinding wheel bench shown in Figure 4.2.

Figure 4.2: Wafers grinding

After the grinding step is finished, we decided to keep the tape that protects the front side of the wafers until the end of the fabrication process because the very thin wafers are too fragile and could break easily. The grinded faces are then covered with aluminum layer of 1 μm thickness.Finally, the tape is taken off, and resist is removed using acetone followed by water rinsing and drying.



(a) Antenna 1. (b) Antenna 2.

(c) Antenna 3. (d) Antenna 4.

Figure 4.3: The four fabricated antennas

Figure 4.3 shows the images of the four fabricated antennas, we used the microscope to check if the etching was correct, the measured dimensions shown in Figure 4.4 show that there was indeed an over etch of 3 to 4 μm. Over etching can depend on many things, for example the temperature of the HF acid used during etching, the etching time, it could also vary from wafer to wafer. We also measured the thickness of the aluminum with a profilometer, we found that the thickness varies around 935 um, which means that the deposition was rather uniform.
The oxide thickness measured using ellipsometry shows a thickness of about 195 μm on standard silicon and high resistivity silicon wafers, and around 184 μm for trap rich wafers.

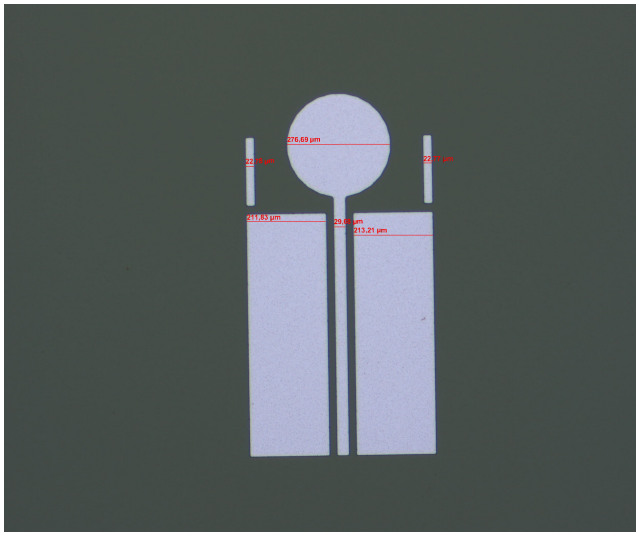


Figure 4.4: Microscope image of the antenna with dimensions.

The following Table shows the measured thickness of each wafer after the grinding process. We can see that there is an error offset of 7 µm more or less.

Std 1	Std 2	HR 1	HR 2	TR 1	TR 2
235 µm	233 µm	237 µm	238 µm	236 µm	233 µm

Table 4.1: Measured thickness of different wafers after grinding process (Std = standard silicon, HR = High Resistivity Silicon, TR = Trap Rich silicon).

4.2 Measurement setup

In order to characterize the different antennas fabricated on the three substrates, measurements were performed in the Welcome lab using an "PNA N5227B 0.9-67 GHz" vector network analyzer with an extension "PNA Millimeter Test Set N5292A", a pair of GSG 110 GHz infinity probes was used as well. The setup measurement is shown in Figure 4.5, Figure 4.6 show the wafer placed on the metallic chuck of the setup. Once the measurement setup is calibrated and the GSG probes are planarized, S-parameter measurements on wafer were performed.

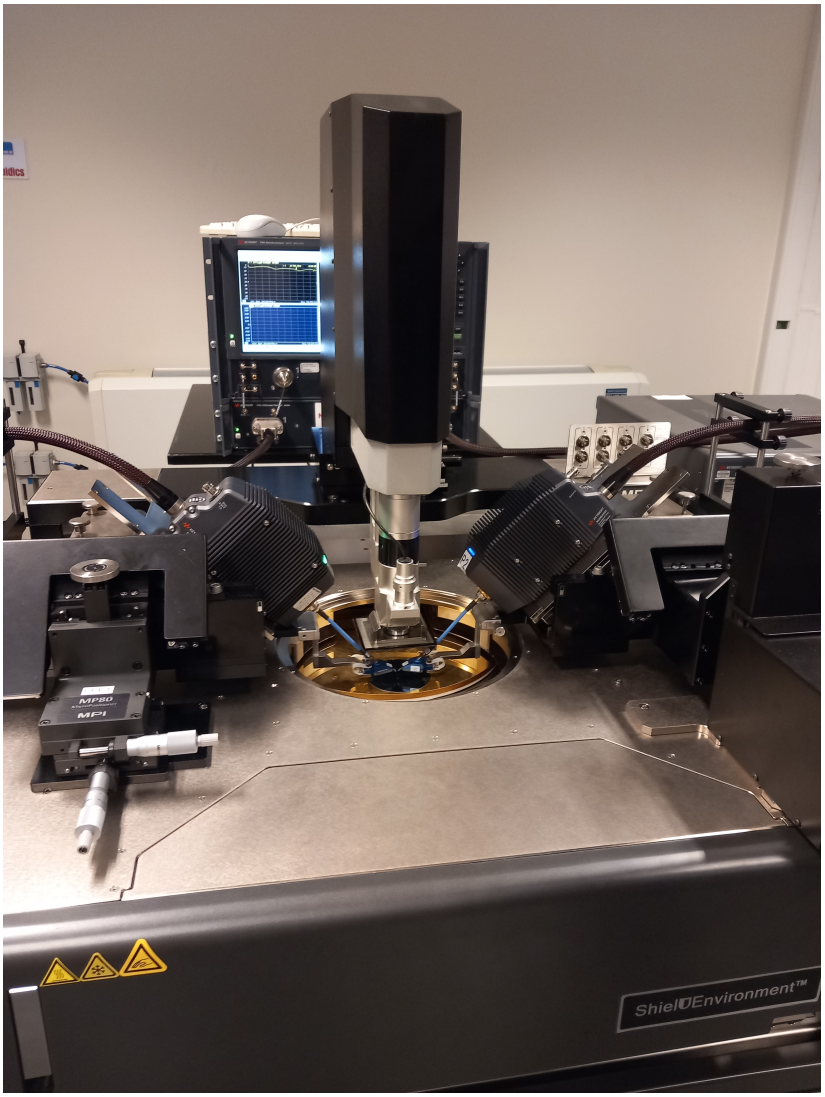


Figure 4.5: Setup measurement in Welcome lab.

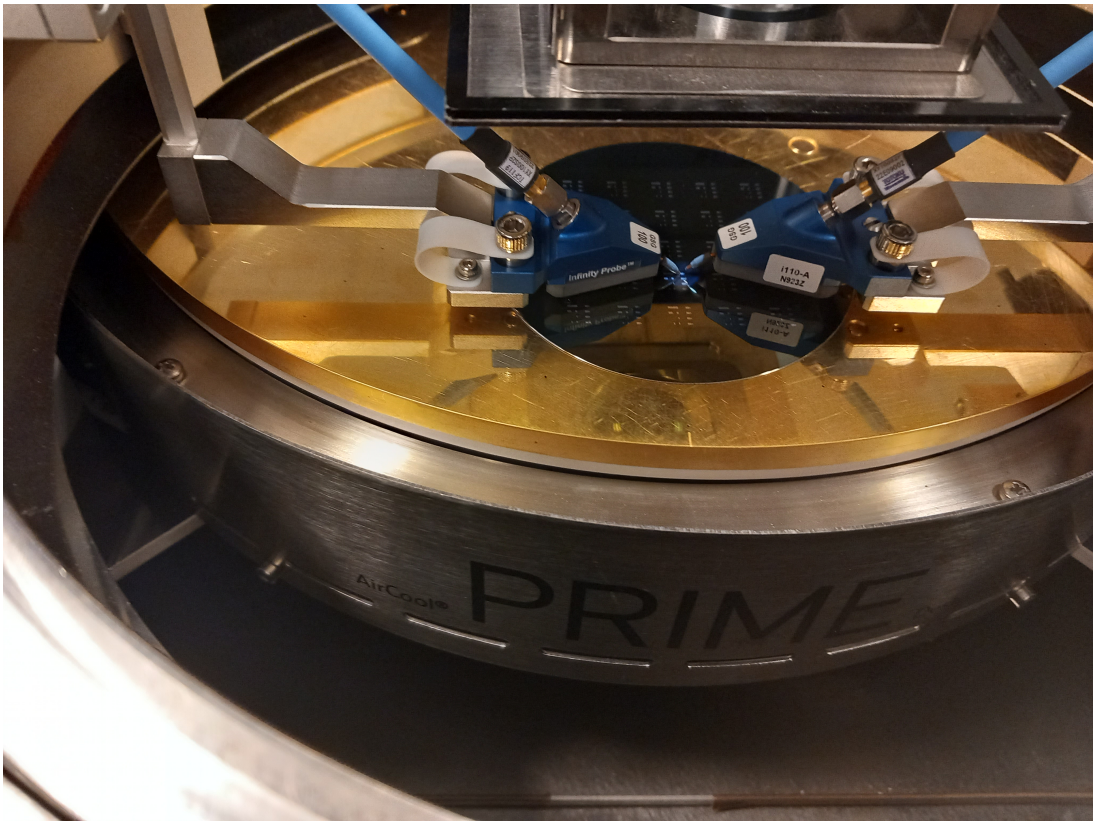


Figure 4.6: On-wafer measurement setup.

4.3 Measurement results

The S parameters measurement were carried out in the frequency range between 0 GHz and 130 GHz, Several dies was measured on each wafer in order to compare results and see if the fabrication process was uniform. It is worth noted that the peak at 120 GHz is due to the setup and cannot be corrected, thus it should be ignored.

4.3.1 GCPW lines measurements and substrate characterization

The S-parameters measurement performed on the GCPW lines allow to extract the needed parameters to characterize the three silicon based substrates: 1) standard silicon; 2) high resistivity silicon and 3) trap rich. Figure 4.7 shows the results of the lineic losses α (dB/mm), the resistivity (Ω-cm), the loss tangent and the effective resistivity for the three considered substrates.

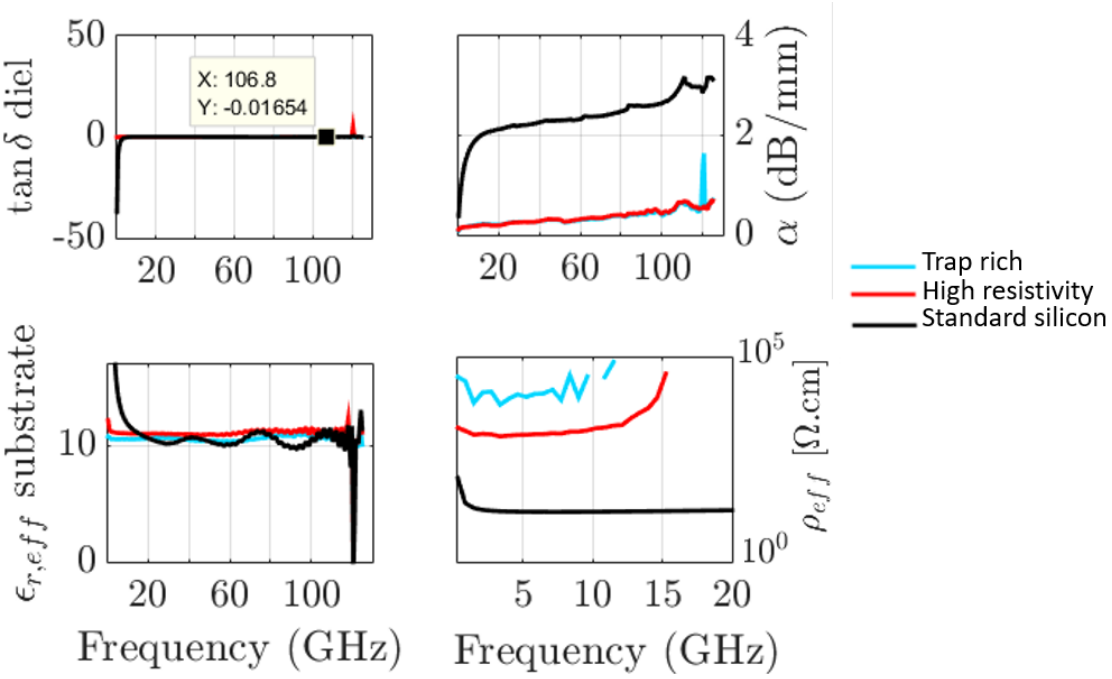


Figure 4.7: Substrates electric parameters.

RF losses are of the order of 2.96 dB/mm at 119 GHz for the STD substrate compared to only 0.55 dB/mm at 119 GHz for the HR and TR substrates, this is due to the low resistivity of the STD substrate which is of the order of 17.45 Ω-cm, that of the HR is 1255 Ω-cm and that of the TR is of the order of 10000 Ω-cm. The extracted effective relative permittivity is 11.23 at 106 GHz.

4.3.2 Reflection coefficient S11 measurements

Only one probe was used for S11 measurements, the three tips of the probe are placed on the CPW feed of each antenna on a chosen die and the S-parameters are measured. The reflection coefficient measurements allow to compare the performance of the silicon based substrates used in fabrication in term of on-chip antenna design. To present the results of the measurements in the next sections, we will use the following nominations for the different antennas and substrates, the four antennas are shown in Figure 4.8 with their nominations.

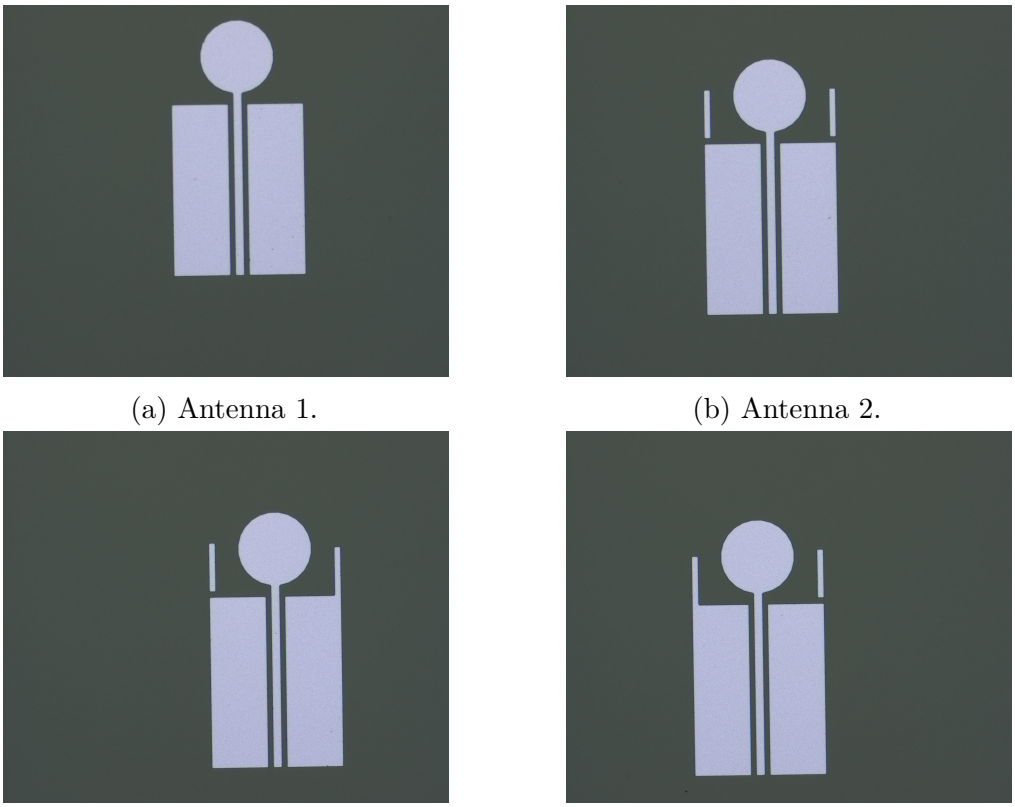
The results of the measurements will be given in the following order:

- First the raw and de-embedded reflection coefficient S11 of the different antennas on each substrate will be plotted, then compared to the simulation results for standard and high resistivity silicon.

Trap rich silicon	TR
High resistivity silicon	HR
Standard silicon	STD
Antenna without bars	Antenna 1
Antenna with not connected bars	Antenna 2
Antenna with right bar connected	Antenna 3
Antenna with left bar connected	Antenna 4

Table 4.2: Nominations of different antennas ans substrates.

- A comparison of the de-embedded reflection coefficients S11 of each antenna on the different substrates will be plotted.



(a) Antenna 1.

(b) Antenna 2.

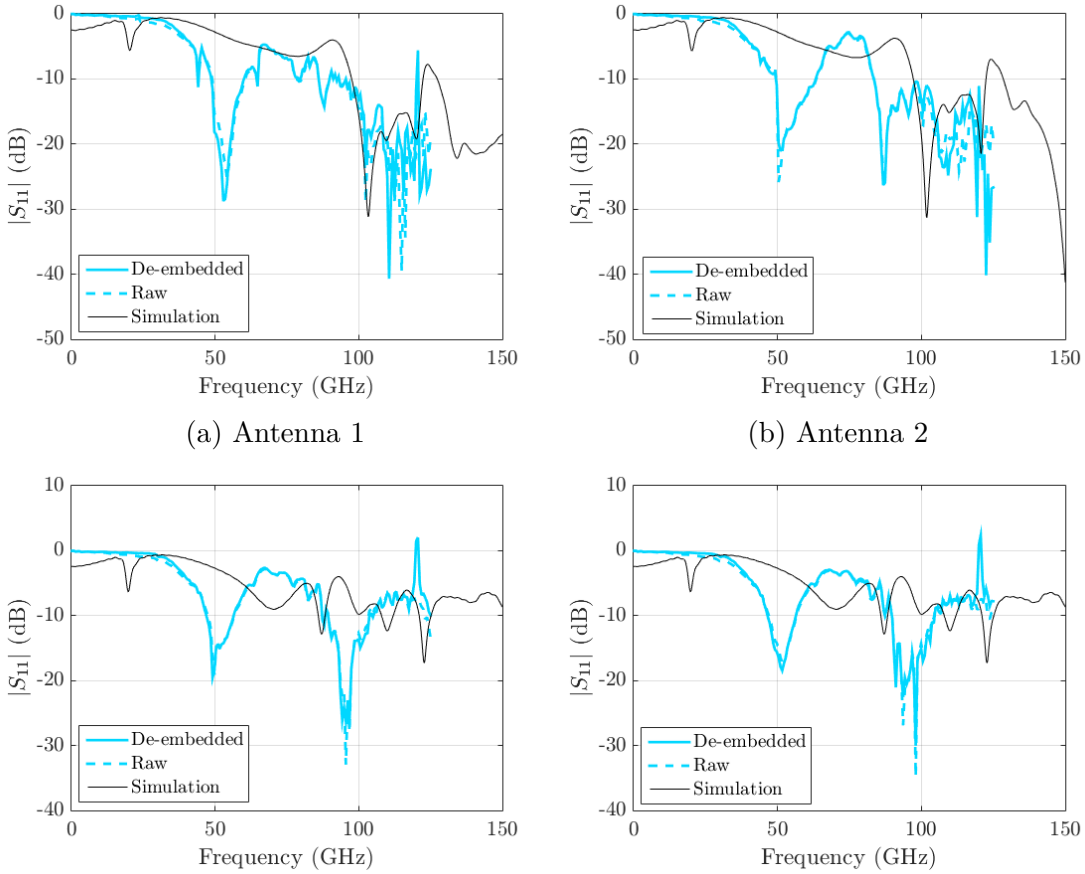
(c) Antenna 3.

(d) Antenna 4.

Figure 4.8: The four measured antennas

Simulated and measured reflection coefficient for the four antennas on TR, HR, and STD substrates are given in Figures 4.9, 4.10 and 4.11 respectively, the measured reflection coefficient does not follow the same behaviour as the simulated one, a measured resonance is observed at 50 GHz for the four antennas patterned on HR and TR substrates and which does not appear in the simulations, another one is measured around 100 GHz for antennas (3) and (4). However, the measurement results on antennas (1) and (2) show a wide bandwidth, which is desired for the designs, the -10 dB reflection coefficient band starts from 95 GHz and 80 GHz for antenna (1) and (2) respectively, this band is even wider than the one obtained by simulation. Considering antenna (3) patterned on standard silicon substrate we can observe good between simulation and de-embedded measurement.

Trap rich (TR) substrate



(a) Antenna 1

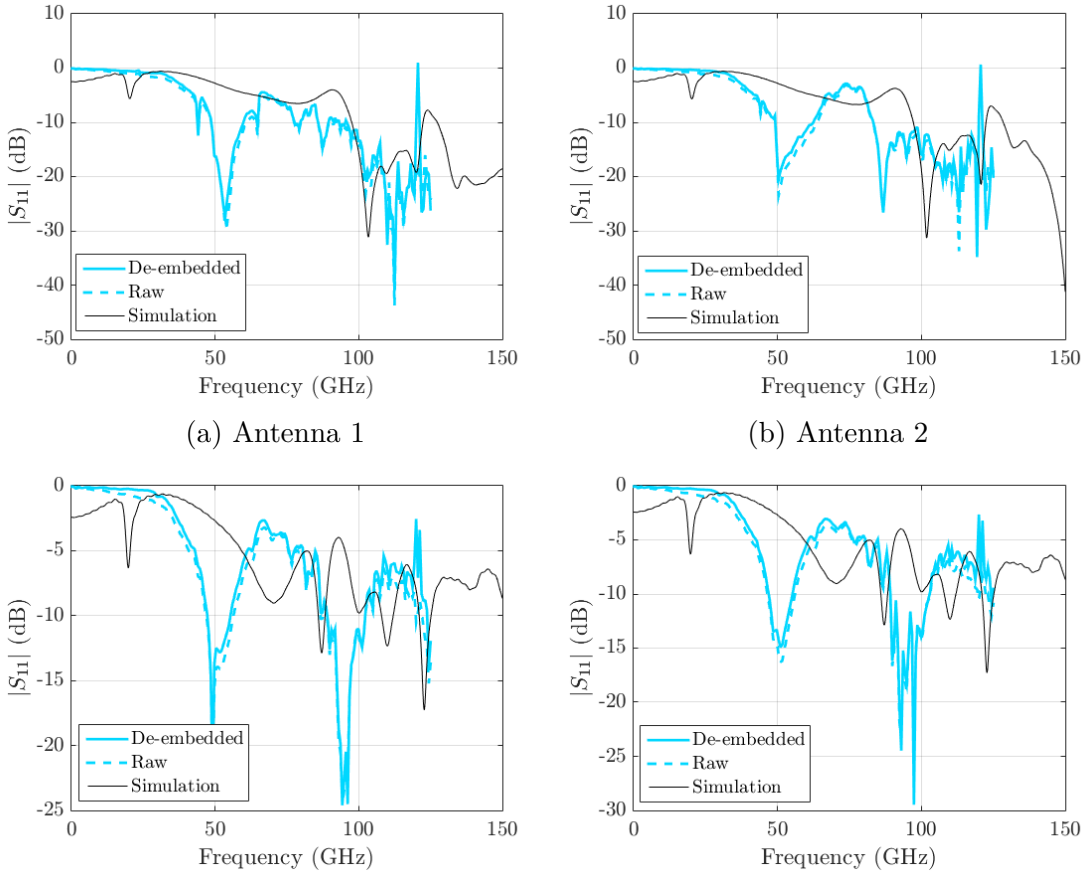
(b) Antenna 2

(c) Antenna 3

(d) Antenna 4

Figure 4.9: Measured and simulated reflection coefficient for antennas on trap rich silicon substrate

High resistivity silicon (HR) substrate



(a) Antenna 1

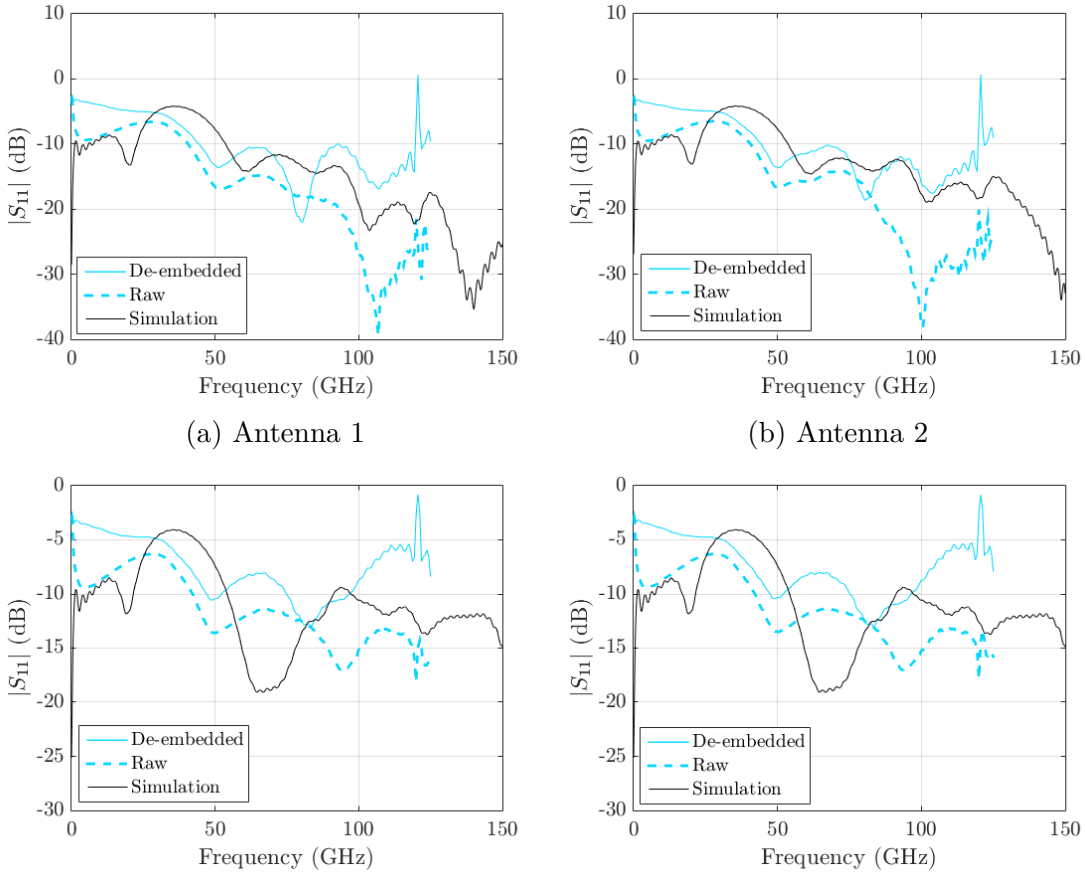
(b) Antenna 2

(c) Antenna 3

(d) Antenna 4

Figure 4.10: Measured and simulated reflection coefficient for antennas on high resistivity silicon substrate

Standard silicon (STD) substrate

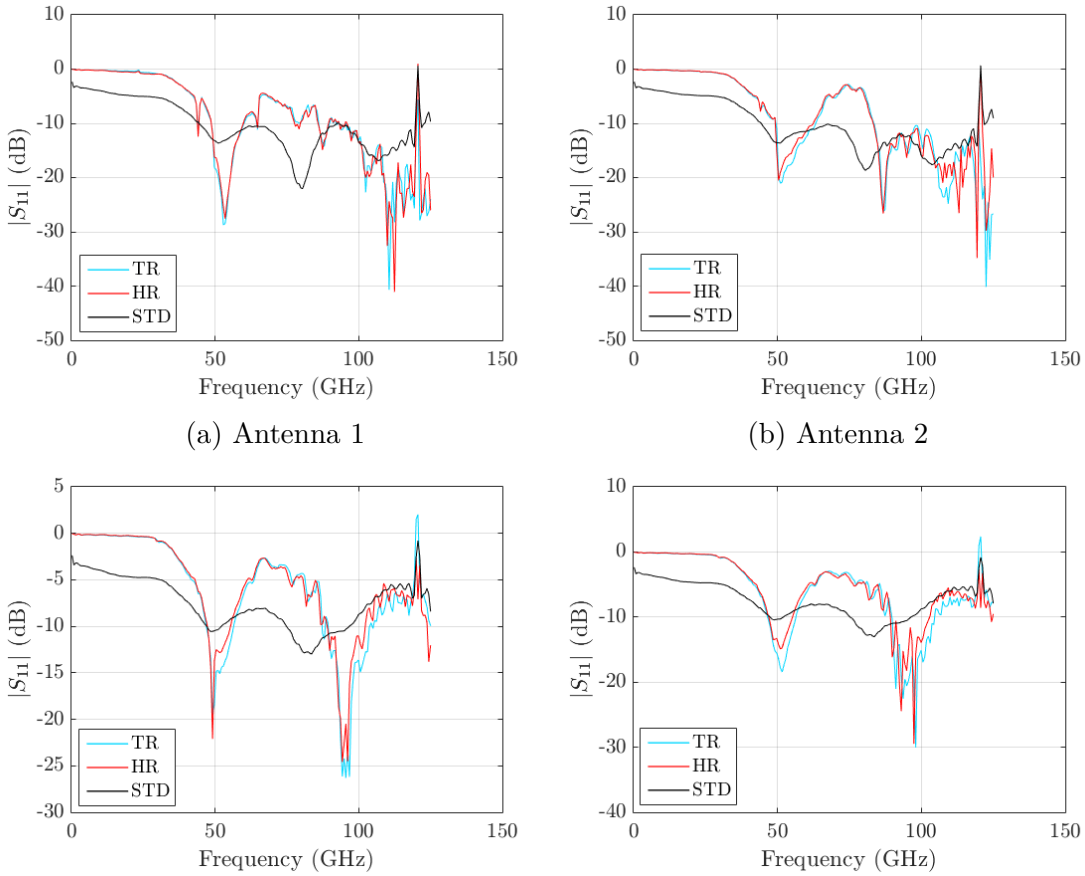


(a) Antenna 1 (b) Antenna 2

(c) Antenna 3 (d) Antenna 4

Figure 4.11: Measured and simulated reflection coefficient for antennas on standard silicon substrate

To see the effect of the substrate on the antenna performance, we plotted the measured and de-embedded reflection coefficient for each antenna on the three considered substrates, Figure 4.12 (a), (b), (c) and (d) shows the measured S11 for antenna (1), (2), (3) and (4) respectively. The results obtained for the patterned antennas on the TR and HR substrate are almost the same, while better results are expected for the trap rich. On the other hand, the very low values of the reflection coefficient obtained with the standard silicon substrate confirm high substrate losses.



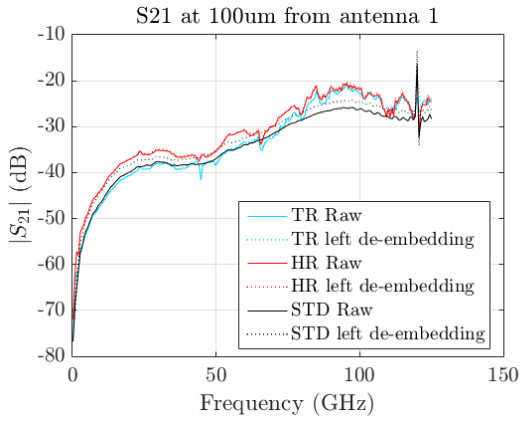
(a) Antenna 1 (b) Antenna 2

(c) Antenna 3 (d) Antenna 4

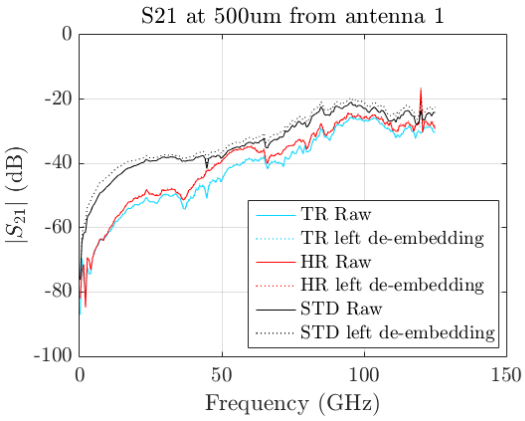
Figure 4.12: Reflection coefficient Measurement on different substrate

4.3.3 Transmission parameter S21 measurements

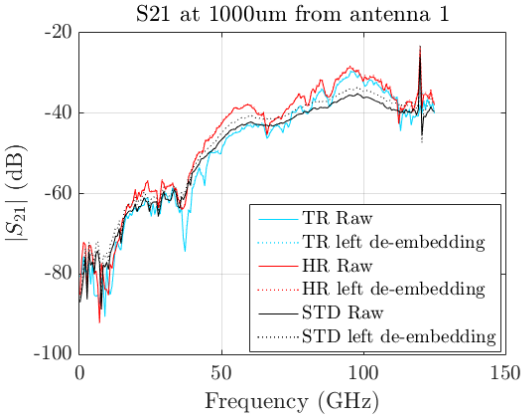
To estimate the additional losses when the substrate is not a trap rich, S21 transmission coefficient measurement were performed between antenna 1 and second probe of the setup measurement located at different distances from antenna 1. Figures 4.13 (a), (b), (c), (d) and (e) show the different transmission measurements when second probe is respectively at 100 µm, 500 µm, 1000 µm, 2000 µm and 3000 µm, both raw and de-embedded measurements are plotted. The trap rich substrate is assumed to give the best values of the S21 transmission coefficient, however the opposite can be seen in Figure 4.13 (b) where the standard silicon substrate is better, thus the results at 500 µm are not considered for further analysis.



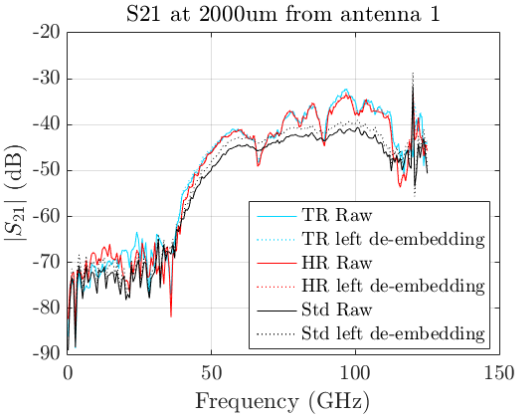
(a) 100 µm



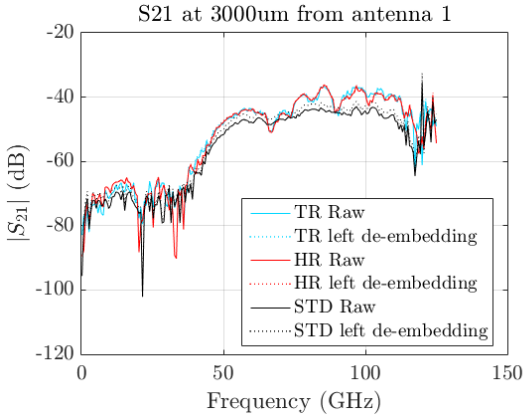
(b) 500 µm



(c) 1000 µm



(d) 2000 µm



(e) 3000 µm

Figure 4.13: S21 Measurement at different distance from antenna 1

The S21 coefficient is maximum around 100 GHz, Table 4.3 shows the values of

S21 extracted at this frequency, the values at 100 µm and 2000 µm are ones that seem more correct since the trap rich is better than the high resistivity substrate, which in turn is better than standard silicon substrate. Table 4.4 contains the values of losses between trap rich and high resistivity silicon, high resistivity and standard silicon, and finally between trap rich and standard silicon at 100 µm and 2000 µm. It can be concluded that the amount of power lost is too high when the substrate is a standard low resistivity silicon.

Distance from antenna 1	TR	HR	STD
100 µm	-21.94 dB	-22.92 dB	-26.15 dB
1000 µm	-33.34 dB	-30.85 dB	-36.11 dB
2000 µm	-34.73 dB	-37.94 dB	-41.48 dB
3000 µm	-38.19 dB	-37.94 dB	-41.48 dB

Table 4.3: Transmission coefficient S21 at various distances from antenna 1 at 100 GHz for Trap rich, high resistivity and standard silicon substrate.

Distance from antenna 1	TR / HR	TR / STD	HR / STD
100 µm	0.98 dB	4.21 dB	3.23 dB
2000 µm	3.21 dB	6.75 dB	3.54 dB

Table 4.4: Difference in dB between transmission coefficient S21 between the different substrate at 100 µm and 2000 µm .

To conclude this chapter, several challenges must be taken into account in analyzing the measurement results :

- The problem of poor contact with the left probe of the measurement setup, we had to make a larger over-travel of the tips to overcome this issue.

- The measurements were made at the end band of the device, resulting in an uncertainty and unreliability in the measurement results.

-The variability of the manufacturing process can also alter the measurement results, especially the over etching of the s patterned on aluminum and the lack of accuracy during grinding step.

Chapter 5

Conclusion and future work

Designing on-chip antennas faces several challenges, some of them were addressed in this thesis as well as some alternative techniques to mitigate these difficulties. The lossy silicon substrate is by far the most serious problem faced. Although excellent for integrated circuits, silicon's high permittivity and low resistivity cause on-chip antenna to have fundamentally poor gains and efficiencies. The reviewed designs and simulation results show that the high-resistivity silicon substrate allows for efficient antenna radiation improvement.
In this thesis, an on-chip antenna was designed on a high resistivity silicon substrate. According to the simulation results, the substrate plays a very important role in the obtained results, the size of the substrate, its resistivity and its permittivity will influence the radiation performance of the antenna. The final design of the antenna placed on a high resistivity silicon substrate allows to achieve a gain of 6.28 dB, an efficiency of -0.04 dB and a bandwidth of 25.53 GHz.
The design is then made capable of beamsteering by adding two on-chip parasitic elements, The problem faced in this part of the work is the degradation of the reflection coefficient when a left or right contact is made, the use of switches has not been addressed as well. Finally, a beamsteering angle greater than 20° is obtained for the frequency band between 117 GHz and 120 GHz.
The various prototypes were then fabricated in the Winfab cleanrooms, three based silicon substrates were used during fabrication in order to evaluate how the based silicon substrates affects the antenna performance. The measurements results show effectively the advantage of using high resistivity trap rich substrate compared to standard silicon substrate. Wide bandwidth has been obtained, and the limitation of the reflection coefficient in the case of antennas with connected parasitic elements has been observed.

The following points summarize some of the direction to be conducted to expand on the ideas discussed in this thesis:

- Redo the measurements with device going up to frequency higher than 130 GHz.
- Measurement of the radiation proprieties would allow to have more results on the antenna performance and validation of the beamsteering capability.
- Take into account the integration of switches in order to connect parasitic elements to the ground plane.
- Try to separate the antenna from the silicon substrate by bringing up the ground plane on the top of the substrate, using multi-level metals and a thick oxide layer.

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