

École polytechnique de Louvain

Radiation effects on ultraviolet enhanced backside-illuminated Single Photon Avalanche Diode

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Abstract

A backside illuminated Single-photon Avalanche Diode has been developed at UCLouvain, specially tuned to present a high sensitivity for light with ultraviolet and near-UV wavelengths. These devices are particularly effective for applications such as biophotonics or positron emission tomography (PET). Research are also being made regarding the viability of SPADs for space missions. In these different types of applications, the photodetectors are located in harsh environment with ionizing radiations. The aim of this thesis is to assess the damage suffered by SPADs under radiation and to determine if critical changes are made to their characteristics. This analysis is done both by simulation and experimentally, on devices fabricated for the occasion. It is shown that most SPADs present a slight increase in dark current (factor 2) and a shift (either to the left or to the right) in voltage breakdown, ranging from 10s to 100s of mV when irradiated at a dose of 100 krad. These changes are not negligible, but they can be considered minimal when compared to the stronger influence of temperature on these specific parameters.

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Introduction

The Single Photon Avalanche Diodes (SPADs) are photodetectors that are able to detect extremely low levels of light, down to the photon. This very high sensitivity, combined with high Signal-to-Noise Ratio (SNR)[52], a wide variety of designs and lower production costs thanks to 15 years of research and improvements have popularized SPADs. They are now implemented in a wide variety of applications, such as biophotonics (Fluorescence lifetime imaging microscopy)[6], quantum photodetectors (for quantum communication), [43], light detection and ranging (LiDAR)[42], positron emission tomography (PET)[54] and they are currently being studied for possible space applications[35]. A lot of these applications take place in harsh environments where important levels of radiation are present. This thesis focuses on the impact of radiations on the operation of SPADs. This analysis is based on a specific type of SPAD developed at UCLouvain, with an enhanced sensitivity for light in the UV and near-UV range.

The first chapter of this work presents the main concepts associated with Single Photon Avalanche Diodes, such as their working principle, some of principal Figure of Merits and some theoretical notions about their operation and the effects of radiations. Then, an extensive comparison between different UV-enhanced SPADs is presented.

Chapter 2 focuses on the fabrication process of the UV BSI SPAD. A complete presentation of the structure and the different variations between the fabricated devices is made. Then, some important fabrication techniques are briefly presented to give context to the fabrication process. This work resumes and concludes the process flow of an SOI wafer. The complete fabrication is then described in details.

The third chapter introduces basic characterization of the fabricated devices. It also presents the irradiation campaign and the experimental setup. The measurement of devices of interest are shown for the different irradiation stages, and the evolution of their parameters are discussed.

Finally, chapter 4 describes the modelisation of the UV-enhanced SPAD with the Silvaco software. The radiation effects are simulated and discussed. Finally, the influence of radiations is put into perspective with other parameters to determine its importance and whether it can be a source of limitation regarding the possible applications of SPADs.

Finally, the conclusion of the thesis is presented and future works regarding the irradiation of SPADs are proposed.

Chapter 1

State of the art

In this section, the working principle of the Single Photon Avalanche Diode (SPAD) is presented, as well as the operation of a Silicon Photomultiplier (SiPM) cell. The most important figure of merits (FOMs), used to assess the performances of different SPADs architecture are then presented. Some useful theoretical principles are then introduced with regards to the aforementioned FOMs. This section concludes with a comparison of different commercially available or research SPADs and their relevant figures of merit.

1.1 Principle of operation

1.1.1 SPAD

A Single Photon Avalanche Diode (SPAD) is a photodetector based on a simple PN junction that is operated in reverse bias. The diode is biased above its breakdown point V_{BD} and is working in a region called the Geiger mode. At voltage levels exceeding V_{BD} , the electric field is high enough for a single photo-generated carrier to set off a chain reaction called an avalanche breakdown[5]. This avalanche (figure 1.1) is a self-sustaining mechanism that outputs a macroscopic current that can be processed and interpreted by the appropriated readout circuitry.[57] The avalanche breakdown is a phenomenon initiated by the generation of an electron-hole pair when a photon is absorbed in the fully-depleted depletion region. Due to the important magnitude of the electric field, there is an important probability for an electron-hole pair to multiply the amount of carriers in the depletion region via impact ionization[24]. Impact ionization refers to the absorption of kinetic energy of another electron or hole to generate an electron-hole pair. This avalanche is sustained until the operation voltage is brought below the breakdown value V_{BD} . [12]

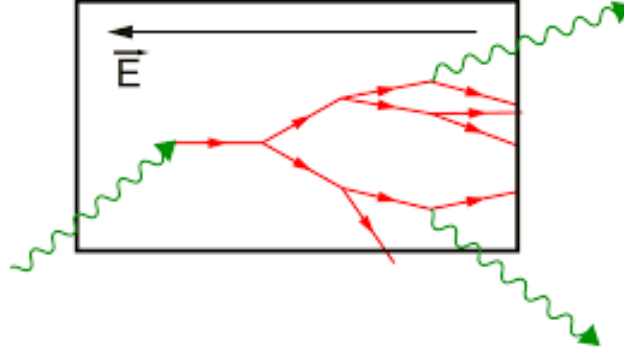


Figure 1.1: The principle of the avalanche breakdown

The operation cycle of a SPAD cell is comprised of three distinct phases that are presented below (see figure 1.2):

1. Avalanche phase : the SPAD is reverse biased at a voltage greater than its breakdown voltage V_{BD} . In this state, a single photon has a probability to trigger an avalanche breakdown and the current rises to macroscopic levels very rapidly (the rise time is in the order of the hundreds of picoseconds). This makes it possible to time the detection of photon in an accurate manner.
2. Quenching phase : to stop the self-sustaining avalanche from reaching current levels that could be destructive to the device, the SPAD biasing has to be lowered at a voltage level that is below the breakdown voltage V_{BD} . This is done with the help of a resistance placed in series, called the *quenching resistance*[8].
3. Recharge phase : after the quenching phase, the SPAD is unable to detect new photons. In order to be reach the avalanche phase, the SPAD has to be re-biased at an excess voltage above the breakdown voltage. During this re-biasing phase, the sensitivity of the SPAD is gradually increasing until it reaches its standard value[10].

It is important to note that the SPAD cell is nearly insensitive during the quenching and re-biasing phase. The time spent for these two phases is called the *recovery time*[46]. A SPAD behaves like a 'all or none' switch and produces a binary output. It is not proportional to the amount of photons intercepted in the avalanche phase due to its unstable biasing above the threshold voltage, and an information on the magnitude of light intensity is not available.

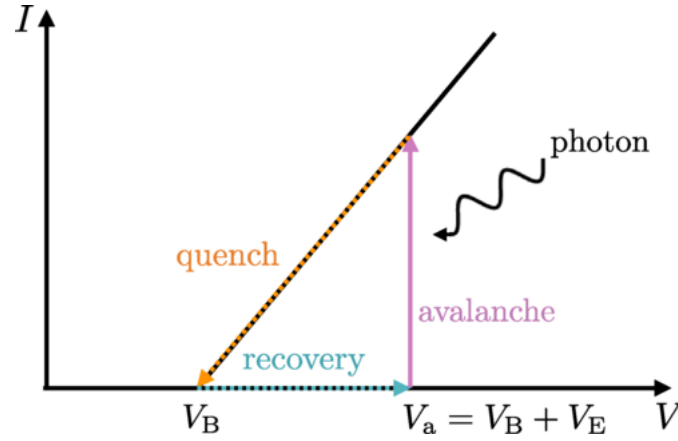


Figure 1.2: The qualitative operation cycle of a SPAD. From [31]

1.1.2 SiPM

A Silicon Photon Multiplier (SiPM) is a device made of a great amount of SPADs connected in parallel to each other. All of the SPADs have their own quenching resistance, which makes it possible for each separate device to detect individual photons and to go through a full operation cycle while the neighboring SPADs are active and ready for detection.[13]

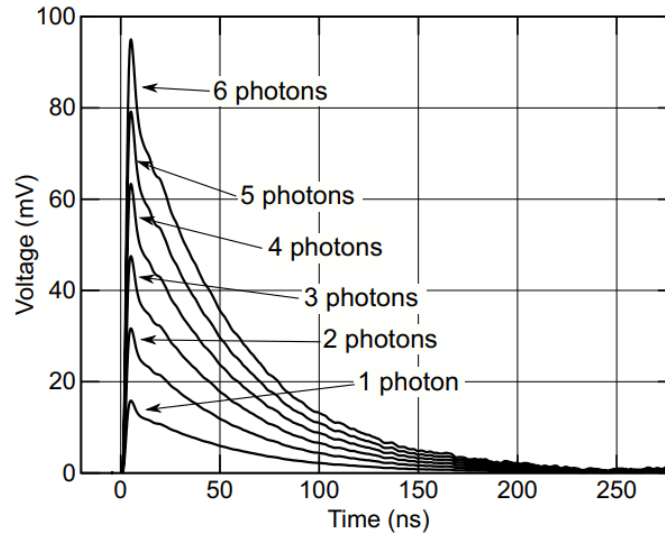


Figure 1.3: Proportional voltage outputs of a SiPM. From [50]

The main interest of the SiPM structure is its ability to produce outputs that

are proportional to the detected light over the photosensitive area of the device. Since each SPAD cell is autonomous and independent with regards to the others, several avalanche can occur concurrently in different SPAD cells. Since they are all parallelized, the output of the SiPM is equivalent to the sum of the discrete current levels of each triggered SPAD, and it is therefore proportional to the magnitude of the detected photon flux.

1.2 Figures of Merit and parameters

To characterize and compare the performances of different devices or architecture, it is important to understand the main figures of merit (FOM) associated with Single Photon Avalanche Diodes. The behavior of the SPAD can be affected by different parameters that are presented below.

1.2.1 Breakdown Voltage

The breakdown voltage is the bias point where the device operates in Geiger mode and where an avalanche breakdown can occur. From a device perspective, the theoretical breakdown voltage can be defined as the voltage where the multiplication factor of carriers approaches infinity[58] . The practical breakdown voltage has to take into account the effects readout circuitry and of the quenching resistance, and is therefore defined differently than the theoretical one. There can be different ways to define the breakdown voltage :

- By looking at the IV curve of the SPAD, the breakdown voltage V_{BD} can be defined where the current increases rapidly by several orders of magnitude. One could, for example, define the breakdown voltage at the point where the cathode currents reaches a discrete value that would be orders of magnitude higher than the leakage current, usually at a dark of approximately 10 μA [40].
- By plotting the derivative with regards to the voltage of the logarithm of the current over the reverse voltage ($\frac{d \log(I)}{dV}$ -V curve) : this makes it possible to observe the voltage values where the current is rising the faster, and this point can be considered to be the breakdown voltage[62]

Once the breakdown voltage has been defined, the leakage or dark current can also be specified. It is the resident electric current flowing in the photo-detector without illumination, and is present at cathode voltage values that are below the breakdown level.

1.2.2 Dark count rate

SPADs are very sensitive devices, able to detect very low levels of light down to a single photon. However, this high sensitivity comes with a drawback : the existence of dark count rate (DCR). DCR happens when an avalanche breakdown is triggered despite the absence of photon being sensed on the photosensitive area. It can be seen as a sort of noise, and it is measured in count per second (cps). These false positives happen because generated carriers trigger the avalanche mechanism. There are three different mechanisms for the apparition of these carriers[65].

- The Shockley-Read-Hall thermal generation transports a charge carrier from the valence band to the conduction band in two steps, due to defects within the structure. This transport mechanism is called trap-assisted-tunneling (TAT).
- Some carriers are transported directly from the valence band to the conduction band due to a phenomenon called *band-to-band tunneling*. It is highly proportional to the magnitude of the electric field in the depletion region[25] .
- Carrier diffusion can also be the cause of dark count. Some minority carriers can indeed diffuse from the quasi-neutral regions towards the depletion region and moderately increase the DCR. Contrarily to the two other mechanisms, carrier diffusion does not take place in the

Shockley-Read-Hall thermal generation can be mitigated by low-temperature operation and the other mechanisms can be limited by avoiding as much as possible the presence of defects during the fabrication process.

1.2.3 Afterpulsing Probability

The phenomenon called afterpulsing is the triggering of an avalanche breakdown during the recovery time. It is a factor contributing to the DCR and is caused by the release of trapped carriers during the re-biasing phase. This FOM is measured in percent and represents the probability that afterpulsing might occur. A secondary type of afterpulsing can be caused by the generation of secondary photons during the avalanche breakdown, that can be re-absorbed by the active region, creating a fake event.[61]

1.2.4 Photodetection probability

The Photodetection Probability (PDP) is a figure of merit that describes the detection efficiency of SPADs. It only takes into account the active area of the SPAD and describes the efficiency with which a photon striking this active area

is able to trigger an avalanche, according to its wavelength. Therefore, the PDP is highly dependent on the wavelength of the incident light[2]. There are several ways a photon might not be detected properly :

- Reflection at the surface : an incoming photon might be reflected at the surface of the photodetector and never even generate an electron-hole pair in the depletion region
- Passing through the device : photons with longer wavelength can completely go through the SPAD without triggering an avalanche
- Recombination of the charge carriers : it is also possible that once the electron-hole pair generated inside the depletion region, the charge carriers might recombine via different mechanisms before reaching the multiplication region. It would therefore not trigger an avalanche and the detection will be 'missed'.
- Stochastic nature of the avalanche : even when all the conditions are met and a charge carrier reaches the multiplication zone, an avalanche might not trigger. It is a stochastic mechanism and therefore has a probability distribution[38].

1.2.5 Dead time

A SPAD cell is not active and ready to detect photons at all times, as described in section 1.1. The dead time is a figure of merit used to determine the amount of time between the detection of two events. It is consisting of the successive impact ionization resulting in the avalanche, the subsequent quenching and the re-biasing up to the nominal voltage level. Note that it is possible that a photon might be sensed before the re-biasing phase is completed, which can lead to unpredictable behavior of the device[37]. This can be avoided when designing an active quenching circuit.

1.2.6 Time jitter

The SPAD timing jitter is defined as the statistical spread of output on-set in comparison with the true photon arrival time[9] . It is a measurement of the amount of uncertainty in the time accuracy of photon detection. First of all, it should be noted that the temporal response relevant with the absorption of a photon in the depletion region has a Gaussian distribution. The timing jitter includes the detection delays in different delays, caused by different mechanisms[56] :

- When a photon generates charge carriers in the depletion region, the charges have to be accelerated over a certain distance for them to gather enough energy to create an avalanche. This time taken by the acceleration is called the *avalanche buildup time* and contributes to the total dead time.
- When the carriers are photo-generated in the "neutral region" of the SPAD, the minority carriers have to be displaced all the way across the boundary of the depletion region. This is the origin for a supplementary timing jitter contribution related to the Gaussian tails of the distribution.

1.3 Theory of the SPAD cell operation

In this section, some theoretical aspects of Geiger-mode avalanche photodiodes are presented, and some of the concepts used in further chapters are introduced.

1.3.1 Impact ionization

The mechanism of impact ionization occurs when charge carriers, highly accelerated by electric fields of high magnitude, ionize one of the silicon atom from the crystal lattice. With sufficient energy, this ionized atom generates an electron-hole pair, which will both be accelerated against or in the direction of the electric field, respectively. The energy level that has to be reached is called the ionization threshold[64]. This value is dependent on the material and it is different for electrons and holes. It has been found by *Kane* that in silicon, the threshold is considered to be *soft* : both the energy loss and scattering rate are individually dependent on the energy of the electron. A popular model of this mechanism is the Selberherr's model that describes more accurately the impact ionization for small size devices and takes into account dependence regarding important parameters such as temperature[22].

1.3.2 Avalanche multiplication

The excess voltage applied to the reverse biased p-n junction and, by extension, the very high electric field accelerates the photogenerated electron-hole pair. These carriers gain enough energy to ionize other silicon atoms, generating secondary, then tertiary electron-hole pairs. This chain reaction is called the avalanche multiplication and is a positive feedback mechanism[45].

If we consider a p-n junction with a depletion region with boundaries denoted by x_n and x_p for the n-type and p-type part of the junction respectively. Since the

junction is reverse biased, we know that the generation of an electron-hole pair in the depletion region will lead to the displacement of the electron towards x_n and of the hole towards x_p . Along this distance and granted they attain the ionization threshold, both of these carriers will be able to generate new electron-hole pairs along the way. We define $M(x)$ as the total amount of charge carriers that will flow out of the depletion zone when a single electron-hole pair has been generated initially. We obtain :

$$M(x) = 1 + \int_{x_n}^x \alpha_n M(x') dx' + \int_x^{x_p} \alpha_p M(x') dx' \quad (1.1)$$

By differentiating with regards to x , we obtain :

$$\frac{dM(x)}{dx} = (\alpha_n - \alpha_p) M(x) \quad (1.2)$$

Equation 1.2 has the following solutions :

$$M(x) = M(x_n) \exp \left(\int_{x_n}^x (\alpha_n - \alpha_p) dx' \right) \quad (1.3)$$

$$= M(x_p) \exp \left(- \int_x^{x_p} (\alpha_n - \alpha_p) dx' \right) \quad (1.4)$$

With these equations[55], we can obtain both the multiplication gain for pure electron or hole injections, M_n or M_p . For example, by substituting (1.4) in (1.1), we obtain the multiplication gain :

$$M_n = \frac{1}{1 - \int_{x_n}^{x_p} \alpha_n \exp \left(- \int_{x'}^{x_p} (\alpha_n - \alpha_p) dx'' \right) dx'} \quad (1.5)$$

1.3.3 Breakdown voltage

As mentioned earlier, the avalanche breakdown is theoretically defined as the point where the multiplication gain becomes infinite. Taking (1.5), this condition is fulfilled when the denominator tends towards 0, so when :

$$\int_{x_n}^{x_p} \alpha_n \exp \left(- \int_{x'}^{x_p} (\alpha_n - \alpha_p) dx'' \right) dx' = 1 \quad (1.6)$$

in the case of pure electron injection. The equivalent exists for pure hole injection as well, and these two statements are the conditions for the avalanche breakdown to occur. When the integral from (1.6) is larger than one, then the junction is biased above its breakdown voltage. The mathematical model presented above suggests that the self-sustaining breakdown current is infinite, however it is practically

limited by the series resistance and the space charge resistance. The breakdown voltage V_{BD} can be obtained mathematically via an iterative method : by evaluating the field profile at a certain bias voltage, the ionization coefficients and then the ionization integrals can be evaluated. The bias voltage is then adapted whether the ionization integral is higher or lower than one, until it reaches one[4]. The voltage bias at which it occurs is the breakdown voltage V_{BD} .

1.4 Total ionizing dose effects

1.4.1 Radiation effects in silicon dioxide

In a silicon-based device, the most sensitive parts to radiations and ionizing particles are the oxide insulators. The radiation-induced effects on oxides are very complex and are a combination of several different mechanisms that will be described in this subsection.

When radiations are going through an oxide with a certain energy, it generates electron and holes that present different mobilities. Just after the electron-hole generation, some of these carriers will recombine and cancel each other. The holes that did not recombine, having lower mobility than the electrons and being relatively static in the silicon dioxide, will induce a temporary positive oxide charge. However, some of these holes are swept towards the silicon-oxide interface. This is called a *dispersive* process[53] because it is highly dependent on several parameters such as the electric field, temperature and oxide thickness and also because it requires a time-span orders of magnitude higher than the generation/recombination.

Some of the holes that are transported to the Si/SiO₂ interface might reach deep trap states with long lifetimes. These positive charge carriers can stay trapped for very long periods of time. They contribute to the interface charge of the device and can induce voltage threshold shifts. These trapped charge can however get released because a slow annealing mechanism is present, even at room temperature. Finally, there is a buildup of traps at the interface when it becomes irradiated. These traps can become negatively or positively charged. These traps present energy levels in the silicon band-gap.

These four mechanisms can both reinforce or oppose each other and the sum of their contribution leads to positive or negative voltage shifts in the operation of different devices, including an increase of Dark Count Rate for Single Photon Avalanche Diodes.

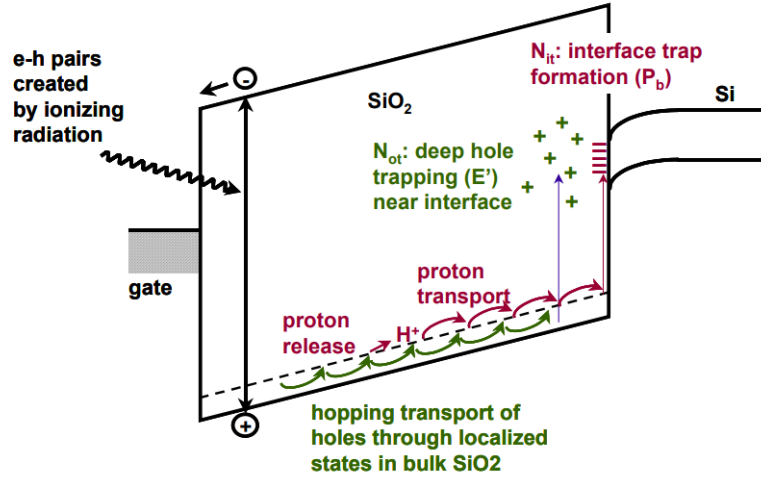


Figure 1.4: Main radiation-induced effects in an oxide. From[48]

1.5 UV-enhanced SPADs comparison

In this section, different SPAD cells that are commercially available or referenced in the literature are presented. The main selection criteria to ensure a relatively fair comparison of the different devices with the Ultraviolet Enhanced Backside Illuminated (UV BSI) SPAD developed at UCLouvain are :

- A high photo-detection probability around the blue light and UV wavelength range (400nm)
- Similar orders of magnitude with regards to the size of the device
- A reasonable value of the excess voltage at which the PDP is measured.

Table 1.1 regroups the main characteristics, performances and figure of merit of different devices and compare them to the UV BSI SPAD developed with SOI technology.

The SPAD of interest, presented at the bottom of table 1.1 has a high photodetection probability at 400nm compared to the other devices, as well as a low breakdown voltage. It is however less optimized with regards to other figure of merits such as the dark count rate, that is unfortunately higher than the other devices compared in table 1.1.

Reference	Peak PDP	PDP at 500 nm	DCR (cps/ μm^2)	AP (%)	Dead time (ns)	Time Jitter (ps)	Breakdown voltage (V)	Excess voltage (V)	Size (μm)	Technology
[21]	62 %	46 %	0.1	0.97	0.97	52	32	7	8.8 (diameter)	55nm BCD
[26]	23.8 % (420 nm)	-	233	-	3.5	139	-	0.5	10 (diameter)	65nm standard CMOS
[28]	73 % (440 nm)	64 %	12.6	0.15	3000	68	17.2	5	78.5 μm^2	110nm CIS
[59]	34.47 % (450 nm)	33 %	50	-	-	127	14.1	1	23.75 (pitch)	130nm CIS
[49]	48 % (480 nm)	46 %	0.19	0.14	0.9	75	26.5	5	10 (diameter)	160nm BCD
[66]	47.8 % (520 nm)	47 %	0.49	0	25	106	22	5	28.5 (pitch)	180nm CIS
[33]	33.5 % (500 nm)	33.5 %	2.5	0.21	10	88	23	6	3 (diameter)	180nm CIS
[34]	26.7 % (520 nm)	26 %	0.4	-	-	-	-	3.3	9.4 (pitch)	180nm CIS
[20]	55 % (480 nm)	51 %	0.23	<3	50	16	22	6	50 (pitch)	180nm CIS
[7]	49 % (550 nm)	48 %	9	2	8.3	35	-	5	50 (diameter)	Custom
[3]	67 % (420 nm)	52 %	0.71	<1	55	75	32.5	6	40 (diameter)	-
[51]	50.5 % (420 nm)	-	0.5	0.75	45	75	24.5	2.5	35	-
[36]	54 % (450 nm)	45 %	0.55	1	55	75	53	3	50 (pitch)	-
[60]	55 % (420 nm)	45 %	0.079	4	20	75	25	6	50 (diameter)	-
[41]	51.2 % (400 nm)	-	0.75	5	100	160	26	3	25 (diameter)	-
[39]	55 % (400 nm)	-	0.3	1	100	23	22.1	2	-	180nm CMOS
[30]	50 % (480 nm)	39 %	73	1	55	158	9.6	1	4 (diameter)	65nm CMOS
[47]	69.51 % (423 nm)	25 %	156.8	-	-	-	8.5	3	36 (diameter)	SOI 0.65 μm

Table 1.1: Comparative table of different blue light/UV enhanced SPAD cells.

Chapter 2

UV BSI SPAD fabrication process

This chapter presents in detail the fabrication process and the different architectures of the Ultraviolet Enhanced BSI SPADs and SiPM made with SOI wafers. First, the general stack and the various designs are introduced. Then, some crucial microfabrication techniques are presented in detail and the accent is put on the fabrication steps most relevant with the radiation campaign presented later. Finally, the complete fabrication process is shown, with some remarks of interest and important advices.

2.1 Overview of the structure and architectures

The UV Enhanced Backside-Illuminated SPAD developed at UCLouvain presents several design specificities related to its wavelength detection range that are described in this section.

2.1.1 Structure

The device is fabricated on a Silicon-On-Insulator (SOI) wafer with a 1 μm Buried Oxide (BOX) and a 0.65 μm top, high quality silicon layer. This silicon layer constitutes, once patterned, the active region of the SPAD. Its general structure is presented in figure 2.1. The most important part of the structure is the diode that is made of a shallow n++/p-well junction. Both the n+ and the p+ implant also serve as low resistivity sinkers for electrons and holes, respectively. The thinness and doping profiles of the junction are specifically selected to improve the photodetection in the ultraviolet and blue light wavelength range. The size of this junction is a square with a length of 13 μm and it is called the active area. The anode is located all around this junction and is made of a highly doped P++ zone, with a 7 μm width.

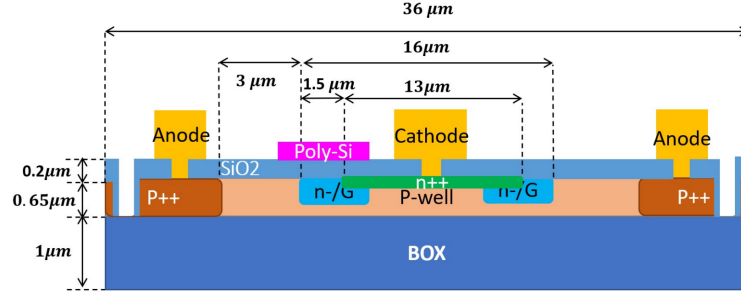


Figure 2.1: Structure of the BSI SOI SPAD developed at UCLouvain. From [23]

To avoid the phenomenon of edge breakdown, caused by the presence of a more intense electric field at the edges of the diffusion zone, locally doped zones called *guard rings* are implanted on the sides of the diffusion zone. For this device, guard rings are made with n-type doped zones around the p-n junction. A slight overlap is present with the p-n junction, effectively extending the active area of the SPAD as a secondary purpose, up to a $16 \times 16 \mu\text{m}$ square. An integrated passive quenching polysilicon resistor is connected to the anode. It has a high resistance of approximately $300 \text{ k}\Omega$. A thin SiO_2 passivation layer of $0.2 \mu\text{m}$ is grown on top of the silicon. On top of this, a thick silicon nitride (Si_3N_4) layer is deposited on the SiO_2 . Although Si_xN_y groups can sometimes introduce compressive stresses, a tensile layer of Si_3N_4 is deposited to balance out the compressive stress caused by the different SiO_2 layers. It is important for this device to be globally under tension to avoid buckling of the membrane which would render it unusable.

2.1.2 Different architectures

The designed SPAD and SiPMs have been derived in several different versions that will be presented here. First of all, there are 3 different architectures for the SPAD cell named by their respective sizes : the 36, 46 and 52 architectures. The '36' design is made of a central cathode, overlapped by a guard-ring. An anode in the form of a squire with a length of $36 \mu\text{m}$ surrounds the cathode. The polysilicon quenching resistor is connected to the anode and serves as the passive quenching circuit. The '46' architecture is based on the design of the '36' SPAD with a total length of $46 \mu\text{m}$ from one end of the anode to the other and a wider cathode. The goal of this second design is to increase the active area (and consequently the fill factor). Finally, the '52' design has a different geometry, with a $19 \mu\text{m}$ hexagonal cathode surrounded by a $52 \mu\text{m}$ hexagonal anode.

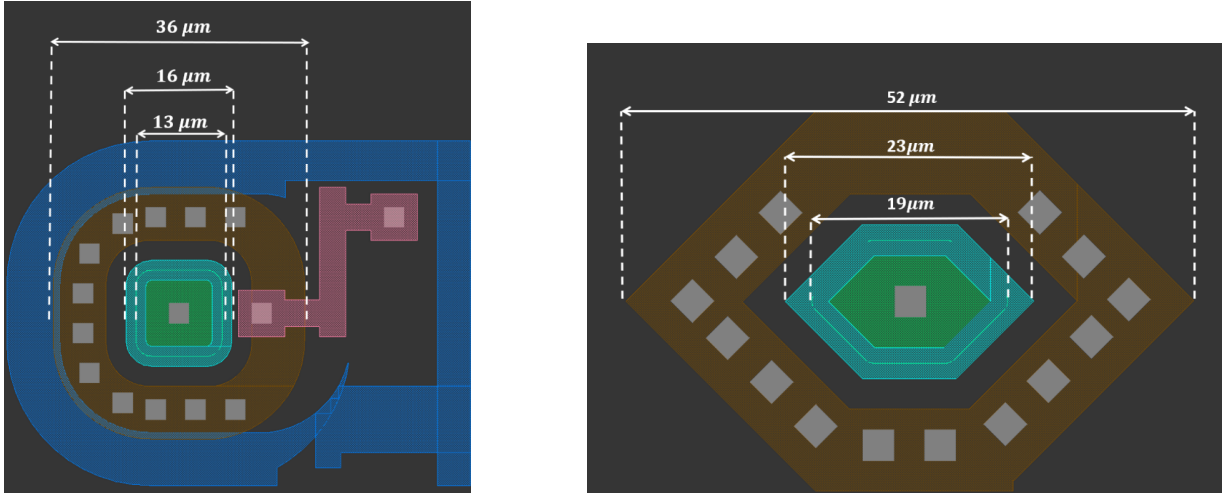


Figure 2.2: Two main architectures of the BSI SOI SPAD. From [23].

The three different designs presented earlier are furthermore declined in two distinctive architectures regarding the isolation from one device to another; these will be called 'trench' and 'mesa'. The trench used for this device is not exactly similar to the Shallow Trench Isolation (STI) technique often used in CMOS technologies. In this scenario, the different SPADs are separated from one another by etching a narrow portion of the silicon layer on the outer side of the circular or hexagonal anode, down to the BOX. Half of the devices on the wafer are designed with these trenches. On the other hand, the 'mesa' architecture is made by etching all of the silicon down to the BOX between the different devices[32]. This way, the SPADs are isolated by being completely separated from each other.

2.2 Microfabrication techniques

A key part of this master's thesis has been the work done on the fabrication of the devices in the WinFAB facility at UCLouvain. In this section, the most important microfabrication techniques are presented in details.

2.2.1 Wafer cleaning and pre-processing

We are working with a Silicon-On-Insulator (SOI) wafer from SOITEC made of a 380 μm silicon support (handle), a BOX of 1 μm and an high-quality top Si layer of 650 nm. The wafer has to undergo a process called 'standard cleaning' before being processed to remove the different contamination sources such as dust, organic

particles or metallic contamination. The procedure is comprised of a first bath in a solution nicknamed "piranha" comprised of sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2). During this first bath, a little bit of oxidation takes place on the surface of the silicon and a thin layer of SiO_2 is formed. This oxide grown at room temperature is called *native oxide*, and the wafer is plunged into a 2% hydrofluoric acid (HF) bath to remove this silicon dioxide layer via etching[19]. The wafer is then rinsed with deionized water and dried with pressurized N_2 .

2.2.2 Ion implantation

To produce the very precise and specific doping profile of the SPADs, ions are directly implanted in the silicon layer. This method offers more flexibility and precision than doping via diffusion. For this fabrication technique, dopant atoms are volatilized, ionized and accelerated towards a silicon wafer. The implanted ions are stabilized in the crystal lattice by losing their initial energy via collisions with the silicon atoms.

To select the areas where the ions will be implanted, a lithography step can be done to mask the silicon areas where implantation is not wanted with photoresist. The implanted ions are decelerated and stopped in the silicon lattice by collisions with nuclei from the crystal and by electronic attraction. This process is stochastic and there is a spatial probability distribution of the ions ΔR (the straggle) around the projected range R_p . These collisions and attractions also make the atoms undergo some lateral straggle, R_L . This distribution is shown in figure 2.3. The depth at which the dopant atoms penetrate the silicon (and the photoresist, which has to be thick enough to completely stop the ions, even the tail of the distribution) is proportional to the implantation energy, which usually ranges between 10 and 200 keV, and inversely proportional to the weight of the ion[15].

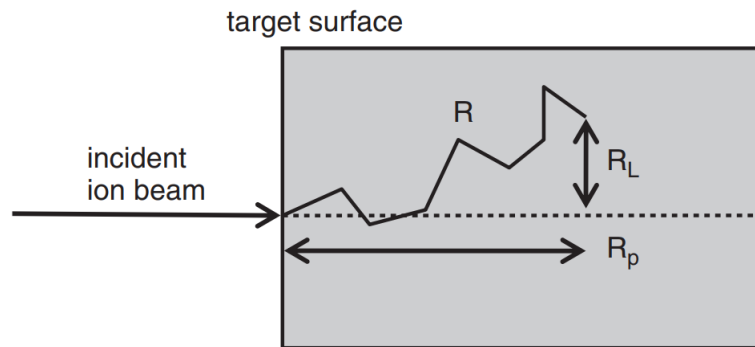


Figure 2.3: The range and straggle of an implanted ion. From [15]

There are several advantages to direct implantation over diffusion :

- Reduction of lateral spread under the mask : it is approximately one third of the vertical depth for direct implantation whereas depth and sideways diffusion are identical for the diffusion process.
- Better control over the doping concentration
- More flexibility : it is possible to dope a silicon wafer through an oxide layer, to shift the peak of the distribution probability at the expected depth.

Implanting through a thin oxide also protects the silicon from a possible metallic contamination caused by metal atoms sputtered from the different sources like the chambers walls or the wafer holders. It is also useful to prevent *channeling*, because the oxide randomizes the direction of the incoming ions. Channeling is a phenomenon that describes the absence of significant scattering of the ions which leads to a deeper implantation than initially wanted. It happens because of the crystalline structure of silicon, where ions can travel through long-range open space and only undergo glancing collisions with the atom rows or planes. It is more pronounced for the $\langle 100 \rangle$ plane which presents a very open structure. To prevent channeling, the wafers are often tilted at a 7° angle to avoid the major planes, and rotated to guarantee a symmetrical doping.[63]

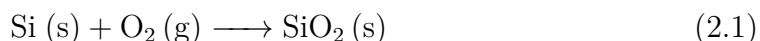
After each implantation step is done, damages are caused to the silicon crystal lattice. The defects can range from vacancies and interstitial, to the formation of dislocation loops for doses above a level of 10^{14}cm^{-2} . In this state, the wafer can be so damaged that its electrical behavior is modified due to trapped charges and its resistivity becomes higher. A specific annealing step has to be done to repair the silicon while minimizing the diffusion of the dopant. Since the energy level required to repair the damaged lattice is higher than the activation energy for diffusion, the wafer has to be heated to very high temperatures (around 1000°C) for short amount of times (less than 100s). This is called Rapid Thermal Annealing (RTA)[15], where wafers are repeatedly and rapidly introduced in a furnace with a specific thermal gradient.

2.2.3 Thermal oxidation

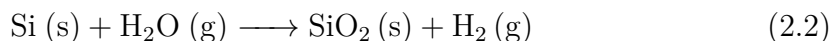
Silicon is a semiconductor material that presents the advantage of being easily oxidized : a native oxide grows on its surface at room temperature over time, and it is possible to grow high quality, stable and controlled oxides at higher temperatures. It is said to be 'grown', because the silicon used for the silicon oxide layer is

directly coming from the wafer itself, as opposed to it being deposited from an external source. Thermally grown silicon oxides present a high quality interface with a low density of defects[44] and good properties such as high resistivity, exact stoichiometry and etching selectivity.

There are two main ways to grow a controlled oxide on the surface of a silicon wafer : wet and dry oxidation. Both process are usually done in a resistively heated furnace (a quartz tube) under a pure dry nitrogen (N_2) flow to prevent a native, uncontrolled oxidation layer to grow. Dry oxidation is described by the following reaction :



Wet oxidation is a bit different and follows :



where the H_2O is formed by the reaction of $H_2 (g)$ and $O_2 (g)$ or by injecting the latter in liquid water. During the oxide formation, approximately 45 % of the total thickness of the SiO_2 is consumed from the silicon[18]. For this fabrication process, a precise control of the flow of the reactant gas is not necessary since because the rate is determined by processes at the interface or in the oxide.

Thermal oxidation produces a uniform oxide layer across the whole surface of the wafer at the cost of a lengthy process. A mathematical model has been developed to estimate the thickness of the oxide with regards to the time it spends in the furnace. Called the Deal-Grove oxidation model, it works very well for single-crystal silicon and thick oxides. The model gives the thickness $x(t)$ according to the following formula [1] :

$$x(t) = \frac{-A + \sqrt{A^2 + 4(B)(t + \tau)}}{2} \quad (2.3)$$

where A and B are specific constants, t is the time and τ is the time-equivalent of an eventual initial oxide layer. The Deal-Grove model firstly predicts (when $(t + \tau) \ll \frac{A^2}{4B}$) a linear growth rate, followed by a parabolic growth rate for thicker oxides (see Figure 2.4). The quadratic and linear reaction rate constants are respectively given by :

$$B = B_0 \exp(-E_{A_1}/kT) \quad (2.4)$$

$$\left(\frac{B}{A}\right) = \left(\frac{B}{A}\right)_0 \exp(-E_{A_2}/kT) \quad (2.5)$$

where B_0 , $(\frac{B}{A})_0$ are constants dependent on the crystal orientation and the type of oxidation, and where $E_{A_{1,2}}$ are the activation energy (also different for dry/wet

oxidation).

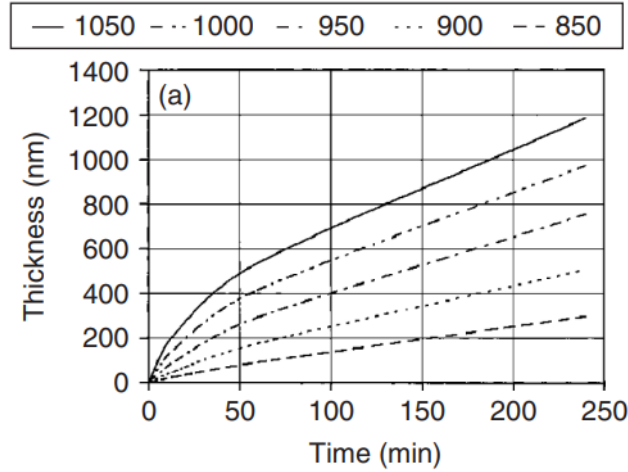


Figure 2.4: Wet oxidation rate of $\langle 100 \rangle$ silicon. From [18]

As mentioned above, this process is quite slow, and the thicker the oxide, the slower the growth. This is because the O_2 or H_2O molecules take more and more time to reach the silicon and react with it, the thicker the oxide is. To illustrate the time taken by the process, it has been calculated by [18] that wet thermal oxidation has a grows only 130 nm for 1 hour at 900°C , and dry oxidation is even slower with only 30 nm formed for identical parameters.

2.2.4 Photolithography

Photolithography is one of the most common and important step in any fabrication process. It is a technique that makes it possible to precisely pattern a wide variety of materials efficiently. An optical lithography step is made up of the following operations :

0. Adhesion promotion (optional step) : especially important for materials that present poor adhesion to resists like metals or polysilicon, it is done via the application of hexamethyl disilazane vapor (HMDS) and its subsequent heating at 100°C . HMDS reacts with the dangling OH bonds at the surface of the material and leaves CH_3 groups.
1. Resist deposition : photoresist is deposited on a wafer rotating at a low speed. It is then spun at high velocity (up to 5000 RPM) to spread it across the whole surface evenly, and this process is called 'spin-coating'. The resist can either be either positive or negative

2. Pre-exposure bake : the photoresist is then baked on a hotplate to get rid of the solvent still present. The baking temperature cannot be too high to prevent the degradation of the photosensitive properties of the resist.
3. Alignement : the wafer is placed in a holder and is lined up with the alignment marks from previous lithography steps. The first lithography step is often done to place the so-called 'zero-level alignment marks'.
4. Exposure : once aligned, the photosensitive resist is exposed to UV light through the pattern of a opaque mask. The best resolution is offered by vacuum contact between the mask and the wafer, but other modes exist.
5. Post-exposure bake : the resist is once again heated at approximately 100°C for a short amount of time to harden the unexposed resist and make sure it stays in place.
6. Development : a liquid developer is poured on the wafer and dissolves the exposed parts of the positive resist or the unexposed part of a negative resist.
7. Hard bake : a third heating phase, usually for a bit longer and at a slightly higher temperature, that hardens the remaining resist and improves its adherence in preparation for the following microfabrication process (often etching or implantation)

There are two main different types of photolithography processes : the positive and negative one. For the positive lithography, the exposed parts of the resist used becomes soluble and are removed during the development step. Negative resists is made from a different material that becomes polymerized through cross-linking when exposed under UV light and they become insoluble[16]. Positive lithography is therefore an image of the opaque parts of the mask whereas negative lithography is a direct copy of the transparent patterns of the mask (see figure 2.5).

The photomasks are plates usually made of fused quartz that are patterned with thin chromium layers of approximately 100 nm, made with a beam writer. Quartz is selected as a base for the masks because of its good transmission of light in the UV range and because its coefficient of thermal expansion (CTE) is low[17]. Two general types of masks exist : it is called a light-field mask if it is mostly covered in chromium and there are some transparent patterns, and it is called a light-field mask in the opposite case. There are also identical alignment marks on the different masks of a same series.

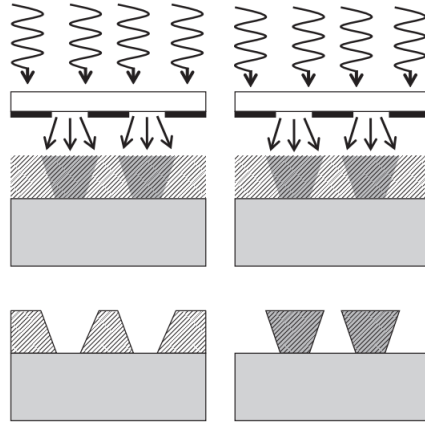


Figure 2.5: A schematic example of positive (left) and negative (right) lithography. From [16]

2.2.5 Etching

Etching is the process of chemically or physically removing a specific material. It is often done after a lithography step, where some areas are protected by a masking material that is insensitive to the etching process and other areas are removed from the structure to create patterns. One of the most important quality of an etching process is the high selectivity between the different materials that will be in contact of the process. Ideally, the etching would entirely remove the wanted material and would leave the resist, the protected areas of the material and the underlying film intact. Different techniques with variable accuracy can be used depending on the material and the criticality of the current step.

Etching mechanisms can be separated in two distinct categories following the type of etchant used. **Wet etching** uses, as indicated by its name, a liquid etchant that will dissolve the unprotected areas of the wafer. The rate at which this mechanism happens can be limited either by surface reactions or by the etchant conduction and diffusion mechanisms themselves. Wet etching is quite a slow process, but it is available for most materials and is the cheapest of the alternatives. The concentration and temperature of the wet etchant must be adapted depending on the nature and thickness of the protection layers used (photoresist, Si_3N_4), etc) to maintain their integrity. **Plasma etching** uses reactive gas excited by RF fields in a vacuum chamber to bombard the material to be etched and react with it. It is a complex combination of chemical and physical processes that makes it possible to produce closely-spaced structure and etch vertical walls without undercut. The ions that are bombarding the surface do not reach the vertical walls and therefore the etching rate in that direction is reduced[14].

One of the most critical aspect to take into consideration when selecting which technique to use is its etching profile. Isotropic etching has an equal etching rate in every direction and its etching front is spherical. This type of profile leads to undercut because material below the mask is etched at the same rate as the exposed material. This phenomenon can be limited in anticipation by sizing the mask features differently, but it is sometimes willingly used to create specific structures. Anisotropic profiles have different etching rates in the vertical and horizontal directions, and it is used to design high aspect ratio structure. Both wet and plasma etching processes can present isotropic or anisotropic etching profiles.

2.3 Complete process

2.3.1 Initial process flow

The fabrication done in this work is based on unfinished wafers left over from the *CQIntegre* project. The steps presented below were already completed prior to this work. They are described in this subsection with the help of the annotated process sheet used during the first run of the *CQIntegre* project. As this process is quite lengthy, some modifications were made to make the process flow easier to follow and understand. First of all, several fabrication steps are grouped together to simplify the global process and ease their schematic representation. The repeated metrology steps such as ellipsometric spectroscopy, profilometer measurements and the observations with the optical microscope were removed from the list of fabrication steps. The ellipsometric spectroscopy is done with a Sentech SE850 device on a test wafer after every deposition and etching steps to ensure that the process took place as intended. For simplicity, lithography is listed as a single step, but as described in section 2.2.4, it contains a lot of preparation and development steps. A detailed lithography step is presented in table 2.3.

Step	Sequence	Parameters	Machine
1	Standard cleaning	All baths	-
1	Thermal oxidation	27 nm, T=950°C	Koyo 1
1	Lithography (alignement marks)	Mask : M1 - Hard bake	Suss MA/BA6
1	SiO2 wet etching - BHF	Backside is hydrophobic	-
1	Si etching - ICP RIE	25s, 300nm. 50W RF 800W ICP	Corial 210IL
1	Photoresist stripping	Plasma descum - 500W	TePla 300E
2	Standard cleaning	Without HF	-
2	Ion implantation (P-well)	Boron, E=20keV, dose=5E13, tilt=7°	IBS facility
2	SiO2 wet etching - BHF	1 min, hydrophobic backside	-
3	Standard cleaning	All baths	-
3	Thermal oxidation	27 nm, T=950°C	Koyo 1
3	Lithography (anode)	Mask : M2 - 165J/cm ² , hard bake	Suss MA/BA6
3	Ion implantation (P++ anode)	Boron, E=20keV, dose=5E15, tilt=7°	IBS facility
3	Photoresist stripping	Plasma descum - 500W	TePla 300E
4	Standard cleaning	All baths	-
4	Degassing under N2	T=700°C, 30 min	Tempress
4	Lithography (trench)	Mask : M5 - 165J/cm ² , hard bake	Suss MA/BA6
4	SiO2 wet etching - BHF	40s	-

Table 2.1 continued from previous page

Step	Sequence	Parameters	Machine
4	Si etching - ICP RIE	700 nm, down to BOX	Corial 210IL
4	Photoresist stripping	Plasma descum - 500W	TePla 300E
5	Standard cleaning	All baths	-
5	Thermal oxidation	27nm, T=950°C	Koyo 1
5	Lithography (guard ring)	Mask : M3 - 165J/cm ² , hard bake	Suss MA/BA6
5	Ion implantation (N-guard ring)	Arsenic, E=60keV, dose=1.3E13, tilt=7°	IBS facility
5	Photoresist stripping	Plasma descum - 500W	TePla 300E
5	SiO ₂ etching - BHF	45s	-
6	Standard cleaning	All baths	-
6	Thermal oxidation	27nm, T=950°C	Koyo 1
6	Lithography (cathode)	Mask : M4 - 165J/cm ² , hard bake	Suss MA/BA6
6	Ion Implantation (N++ cathode)	Arsenic, E=20keV, dose=5E15, tilt=7°	IBS facility
6	Rapid Thermal Annealing	Under argon, 1 min, T=950°C	IBS facility
6	Photoresist stripping	Plasma descum - 500W	TePla 300E
6	SiO ₂ etching - BHF	25s - protection of the exposed Si	-
7	Standard cleaning	All baths	-
7	Degassing under N ₂	T=600°C, 15 min	Tempress
7	SiO ₂ via PECVD	330 nm, 440s	Oxford Plasmalab
7	Polysilicon deposition via ALD	325 nm, 2 hours, T=620°C	Cambridge Fiji
7	SiO ₂ via PECVD	50 nm	Oxford Plasmalab
7	Lithography (Resistor)	Mask : M6 - degassing at 600°C, HB	Suss MA/BA6
7	Polysilicon etching	-	-
7	Photoresist stripping	Plasma descum - 500W	TePla 300E
7	SiO ₂ via PECVD	300 nm	Oxford Plasmalab
8	Lithography (Contact holes)	Mask : M7 - Hard bake	Suss MA/BA6
8	SiO ₂ etching - BHF	Depth : 600nm	-
8	AlSi sputtering	Thickness : 1300 nm	VST - TFDS 462
9	Lithography (Metal)	Mask : M8 - Hard bake	Suss MA/BA6
9	AlSi etch - ICP RIE	Depth : 1300 nm	Corial 210IL
9	Photoresist stripping	Plasma descum - 500W	TePla 300E
9	Annealing (forming gas)	T=450°C, 30 min	-

Table 2.1: Fabrication completed prior to this work

The first step in most fabrication processes is for the wafers to undergo standard cleaning to get rid of all possible contamination sources and to prepare them for thermal oxidation. A 27nm SiO₂ layer is thermally grown to protect the wafer before the first lithography step. The first mask is then used to create the alignment marks that are directly etched into the Si after development of the exposed photoresist and etching of the SiO₂.

The second stage begins with a new standard cleaning procedure that is here done without fluorhydric acid (HF) to avoid damages that could be caused because of the newly etched marks. The wafers are then sent to IBS for ion implantation over the entire surface, that is still covered by the thin oxide. Boron species are implanted at a dose of 5E13 at/cm³ and an energy of 20 keV through the silicon oxide. In most of the implantation steps that were made for this fabrication process, a thin sacrificial oxide layer is used to shift the peak of the ion distribution in the silicon to obtain the required doping profile. The 27 nm of SiO₂ is then etched in a bath of Buffered HF (BHF).

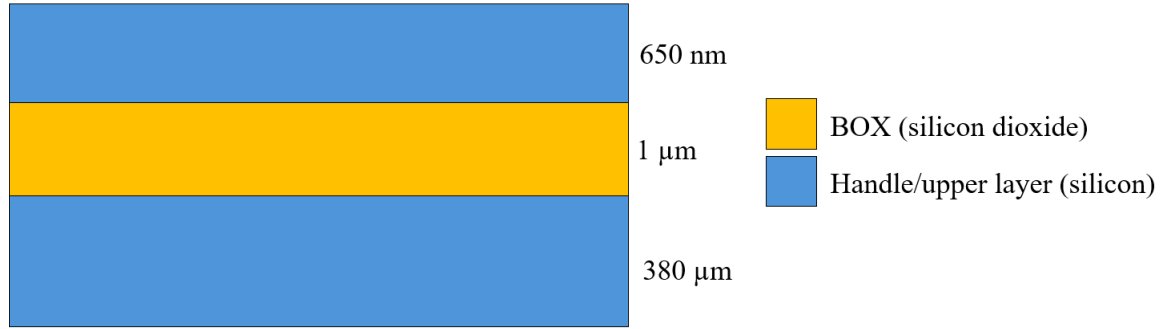


Figure 2.6: Initial wafer structure

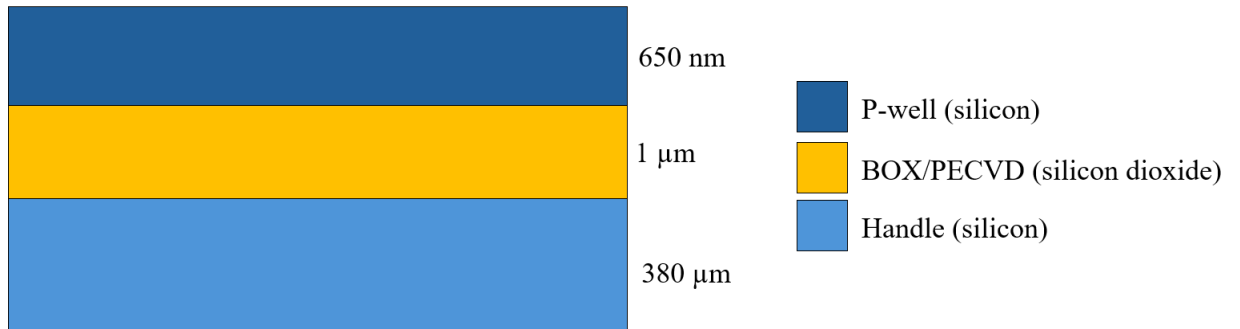


Figure 2.7: Structure after step 2.

Step 3 represents a typical cycle of operations that have to be made to locally dope certain areas of the device in fabrication. After another standard cleaning process, a new thin layer of SiO_2 is thermally grown on the silicon to prepare the ion implantation step. Here, a lithography step is carried out with a dose of $165\text{J}/\text{cm}^2$ to pattern the anodes of the different SPADs on the photoresist. The wafers are then sent at IBS for a new implantation step. The patterned areas are also doped with boron atoms at an energy of 20 keV, but this time with a higher dosage of $5\text{E}15\text{ at}/\text{cm}^3$. The anodes are now correctly doped and the photoresist is stripped with plasma in the TePla 300E.

The fourth step is where trenches and mesas are being etched in silicon. After the standard cleaning and a new lithography to pattern the trenches or isolate the devices, the exposed SiO_2 is removed via wet etching. The wafer is then put into the Corial 210IL to anisotropically create the trench/mesas via Reactive Ion Etching. The silicon is removed over 650nm (down to the BOX) and the photoresist

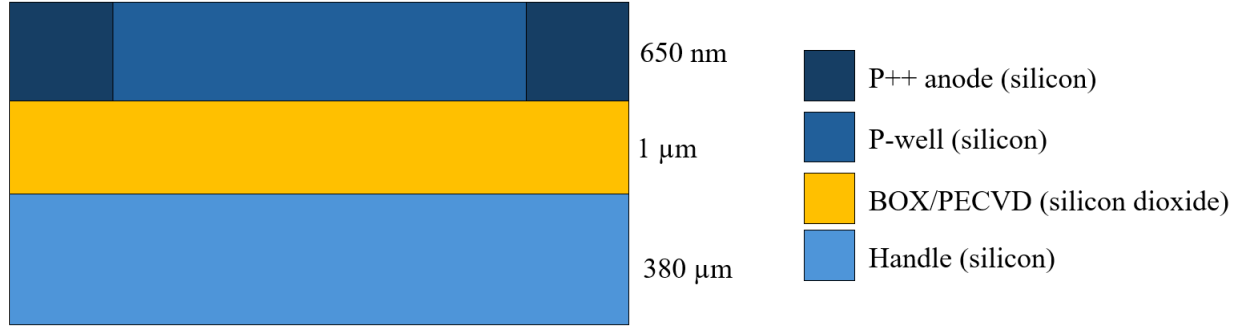


Figure 2.8: Structure after step 3.

is stripped. The devices are now isolated from one another and the difference between the mesa architecture and the trenches is now observable on the optical microscope.

The last two cycles of ion implantation are then done to define zones with specific doping : the guard-ring and the cathode. The guard-rings are designed very similarly to the anode in step 3, with a different mask and a different implantation. Here, arsenic species are implanted with an energy of 60 keV at a dose of $1.3\text{E}3$ at/cm². The thin sacrificial silicon dioxide layer is always removed after these kinds of precise implantation process to prevent them from naturally diffusing the dopants they gathered into unwanted areas of the device. The creation of the cathode is the last process of the fabrication that requires the wafer to be sent at IBS for implantation : after being cleaned, the wafers undergo a new thermal oxidation to create a brand new, dopant-free SiO₂ layer. After the lithography step that patterns the cathode, arsenic species are implanted at an energy of 60 keV and a dose of $5\text{E}15$ at/cm³. The highly doped N++ cathode are now defined on the devices and no more implantation steps will be required. To repair the damage caused to the Si crystal by these successive doping processes, the wafer undergo a Rapid Thermal Annealing (RTA) step during 1 minute at 950°C in Argon. The photoresist is then stripped and the oxide is etched away with BHF while protecting the trenches/mesa.

Step 7 implements the quenching resistor to the SPAD and SiPM devices. After a standard cleaning procedure, the wafer are degassed under nitrogen (N₂) to remove any volatile contaminants from the surface of the wafer. This ensures that the deposition of 350nm of SiO₂ via Plasma-Enhanced Chemical Vapor Deposition (PECVD) is well made. The oxide is deposited instead of being thermally grown to avoid the diffusion of the precise doping profile that would naturally occur

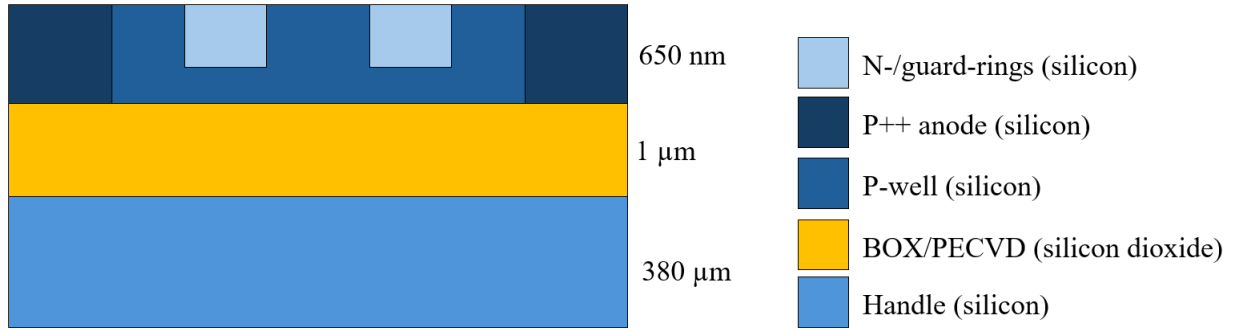


Figure 2.9: Structure after step 5.

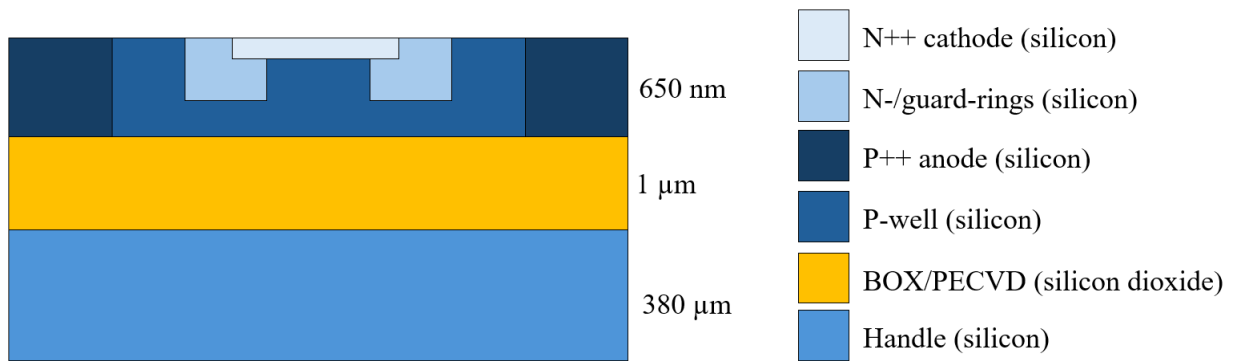


Figure 2.10: Structure after step 6.

would the wafer be exposed to high temperatures for a long period of time. The polysilicon layer that will constitute the resistance is deposited on top of the SiO_2 for 2 hours at a temperature of 300°C via Atomic Layer Deposition (ALD) and a thin oxide layer (50nm) is deposited on top of it. Then, a lithography step is carried out to protect the polysilicon under the resistance pattern from being etched. The photoresist is then removed with O_2 plasma, and a last layer of silicon dioxide is deposited via PECVD with a thickness of 300 nm, encapsulating the resistance between oxide and electrically isolating it.

Finally, the metallic interconnections for the anode, cathode and resistor are made. A first lithography sequence is performed to isolate the contact holes, that are then etched through some of the SiO_2 layer. For the anode and cathode contacts, all of the 680 nm of oxide are etched whereas only 350nm have to be etched to reach the polysilicon resistance. Al-Si_{1%} is deposited via sputtering on the whole surface of the wafer. With a thickness of 1300 nm, it completely fills the contact holes and

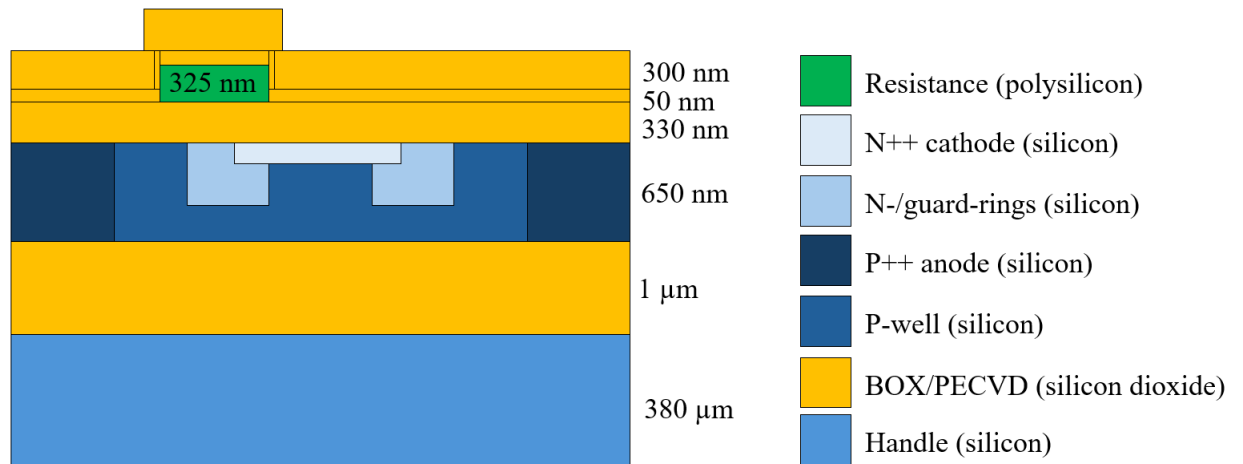


Figure 2.11: Structure after step 7.

leaves a substantial layer on top of it. A lithography step is performed to pattern the frontside metal connections on the $\text{AlSi}_{1\%}$. The 1300 nm of exposed metal are then removed by anisotropic dry etching to limit underetching and the photoresist is stripped away. An annealing step is necessary to improve the connection between the $\text{Al-Si}_{1\%}$ and the silicon/polysilicon by breaking native oxide bonds. The wafers are annealed under H_2 and N_2 for 30 minutes at a temperature of 450°C .

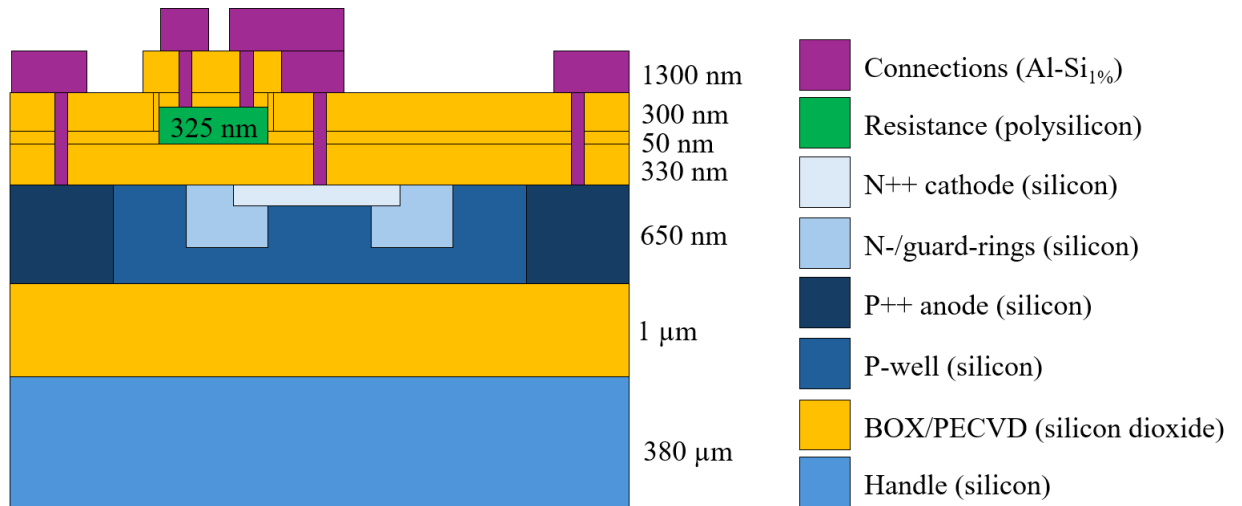


Figure 2.12: Structure after step 9.

2.3.2 Continuation of the process

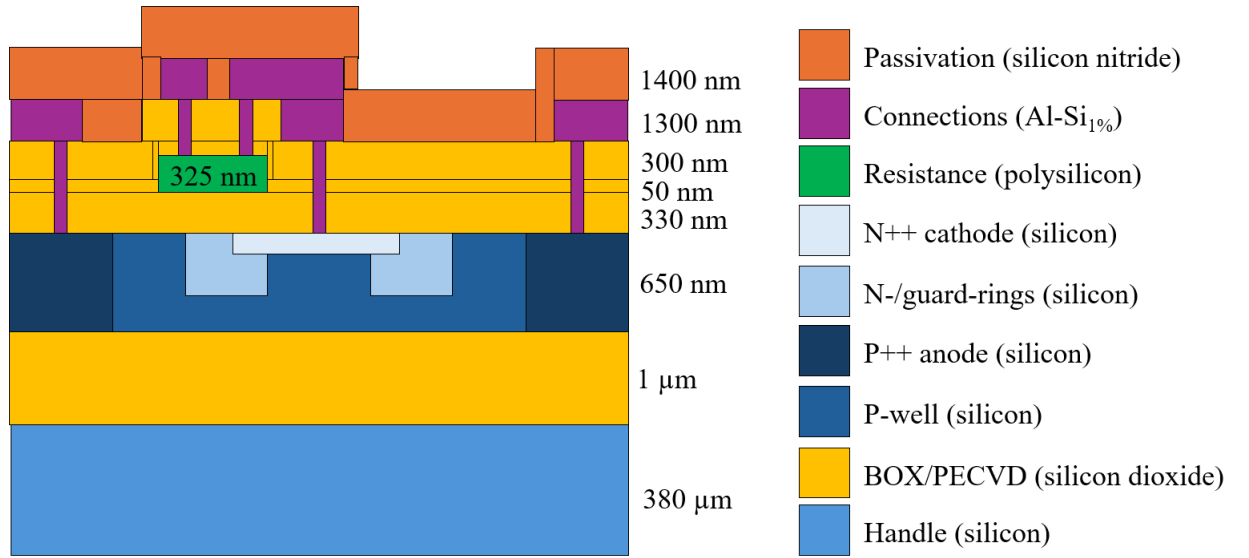
This subsection describes the completion of the SPADs fabrication process that was done in the scope of this report. Some of the steps are therefore described in more details. The process flow is shown on table 2.2. The steps in italic are only done for the "released devices".

Step	Sequence	Parameters	Machine
10	Si ₃ N ₄ via PECVD	T=300°C, 1400 nm (69 min 45 s)	Oxford Plasmalab
10	Ellipsometric spectroscopy	Frontside - 1402 nm	Sentech SE850
11	Lithography (contact pads)	Mask : M10 (darkfield)	Suss MA/BA6
11	Si ₃ N ₄ etching (SF ₆)	10', p = 15 mtorr, RF = 30 W	Oxford Plasmalab
11	Ellipsometric spectroscopy	Frontside - 0 nm	Sentech SE850
12	Resist coating	Frontside - T = 130°C, 120 s	Suss Gamma 80
12	Grinding - backside	Target : 280 µm, blue tape frontside	G&N MPS 2R 300S
13	Chemical polishing	Backside	Mecapol P600
14	Al-Si via PVD	300 nm, T = 250°C	VST - TFDS 462
14	Degassing under N ₂	T = 120°C, 2 h 30 m	Tempress
14	Lithography (membrane)	Mask : M11 (darkfield)	Suss MA/BA6
14	Al-Si etching - H ₃ PO ₄	300nm, T = 55°C, 30 + 30 m	Tempress
15	Dicing	Dies with individual devices	Tempress 602
16	Photoresist stripping	Plasma descum - 500W	TePla 300E
17	<i>Die preparation</i>	Blue resin manual deposition	-
17	<i>Si etching - XeF₂</i>	27 cycles, 30" per cycle, 400 Pa	SPTS Xactix
18	<i>Resist removal + membrane release</i>	Acetone, isopropanol	-

Table 2.2: End of the process flow

First, a layer of silicon nitride is deposited on top of the wafer via Plasma-Enhanced Physical Vapor Deposition. The goal of this Si₃N₄ layer is to balance the compressive stress caused by the SiO₂ layers. Especially for the devices that will be 'released', it is important for the membrane to be under tensile strength to avoid buckling. Inconclusive tests had been carried in previous project with 500 nm layers, therefore the thickness of 1400 nm has been chosen. The deposition has been made in the Oxford Plasmalab 100 at a temperature of 300°C for 69 minutes and 45 seconds, after the recipe was defined on a test wafer. The thickness of the deposited film is checked via ellipsometric spectroscopy afterwards.

A lithography step is then carried out on the frontside of the wafer to pattern the Si₃N₄ layer and expose the aluminum contact pads for the characterization of the device. It is done with a 'darkfield' mask which makes the alignment slightly more challenging through the crosshairs. This specific lithography process is described in table 2.3. The developed areas are then dry-etched for 10 minutes with SF₆ to uncover the aluminum contact pads. The following parameters were used in the



Oxford machine : 15 mtorr of pressure and 30 W of RF power. A verification is made by ellipsometry to make sure that all of the 1400 nm of Si_3N_4 were correctly etched.

Operation	Parameters	Machine
Adhesion promotion	HMDS	LPIII Oven
Resist deposition	Azmir, 2000 rpm	Suss Gamma 80
Pre-exposure bake	T = 90°C, 90 s	Suss Gamma 80
Alignment	-	Suss MA/BA6
Exposure	Vacuum contact, 165 mJ/cm ²	Suss MA/BA6
Post-exposure bake	T = 110°C, 90 s	Suss Gamma 80
Development	60 s, no shaking	Suss Gamma 80
Hard bake	T = 120°C, 120 s	Suss Gamma 80

Table 2.3: Lithography process (step 11).

In preparation for the following steps that will only concern the backside of the wafer, the frontside has to be protected to avoid any damage. A blue resist is therefore applied and then baked 130°C for 120 s with the Suss Gamma 80 coater. A blue protective tape is then added on top of the resist to improve the protection. The backside of the wafer, made from the silicon handle, has to be grinded as its supporting role is not needed anymore. The grinder is operated at rates of 20 µm/s

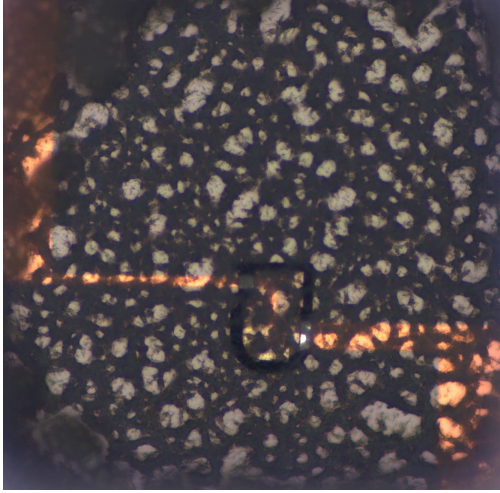
or 10 $\mu\text{m/s}$ for the 'fine speed' mode. A silicon layer of 280 μm is estimated to be left on the backside of the wafer after grinding. It is then mechanically polished to smooth its surface and improve the adhesion of the next material that will be deposited on the backside.

A 300 nm layer of Al-Si₁% is deposited on the backside of the wafer by Physical Vapor Deposition. The metal, vaporized under very low pressure at 250°C with a technique called 'electron-beam evaporation', condensates on the surface of the wafer in VST chamber. The wafers then undergo degassing in a N₂ atmosphere in preparation for the next step. A new lithography sequence is carried out on the backside to pattern the aluminum in preparation of the release of the membranes. It is very similar to the one presented in table 2.3 but with a different mask. Afterwards, the wafers are immersed in a bath of H₃PO₄ at a temperature of 55°C for 2 x 30 minutes to etch away the 300 nm thick aluminum patterned areas at the backside of the membrane.

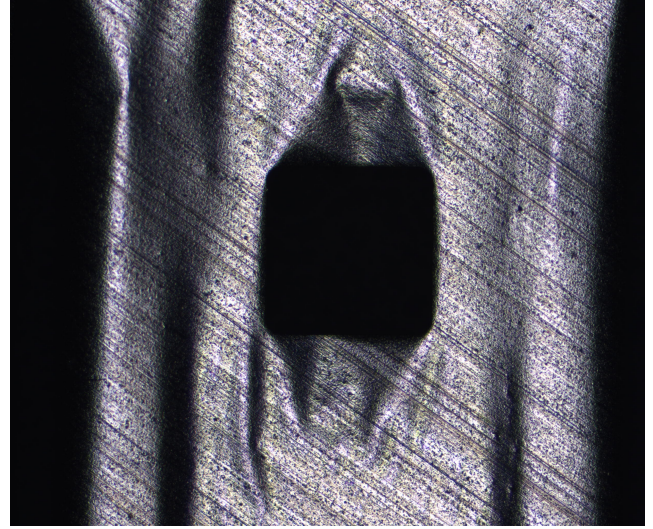
The different diodes, SPADs and SiPMs are then individually diced by Miloud Zitout with a G&N MPS 2R 300S. The blue tape that was applied earlier holds the different dies together. The dicing was done before the release of the membranes for two main reasons. First of all, it makes it possible to characterize and compare 'released' and 'unreleased' SPADs, as will be shown in chapter 3, and it was required as other devices unrelated to this work and located on the center of the wafer had to be diced for an alternative end of fabrication. The dies are then taken away from the blue tape by hand and put for one cycle in the plasma barrel to get rid of the photoresist still preset on the backside. At this point the devices that will not be released are ready for characterization, and we can consider their fabrication process done (figure 2.15a). Note that their backside is made of aluminum and a thick silicon layer that makes it impossible for them to be backside-illuminated.

Some of the devices are released, and some more steps are still required. First of all, the dies have to be carefully prepared before the etching of the silicon. Due to the shared nature of the wafer and the dicing operation happening before the end of the process, each dies presents a substantially higher area of visible silicon on its sides. To release the membrane, the backside Si that is not covered by aluminum has to be etched away, while the silicon visible on the sides has to stay in place to avoid the possibility of an important underetch. The preparation of the dies consists of the usage of blue resist to position dies on a glass tab while protecting the frontside of the wafer. One has to make sure that the borders of the dies are well covered in blue resist, and a covering by hand might be necessary if it is not the case. The resist is then heated at 120°C for 5 minutes. The glass tabs with

the exposed backside of the dies is then inserted into the SPTS Xactix 1 machine which is able to perform isotropic dry-etching with XeF_2 gas.



(a) Cobweb-like structures of oxidized silicon

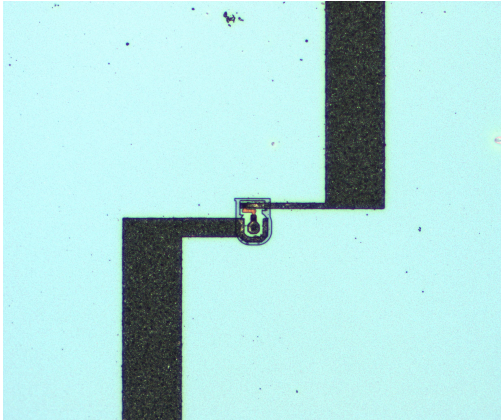


(b) Delamination of the backside Al-Si₁% film

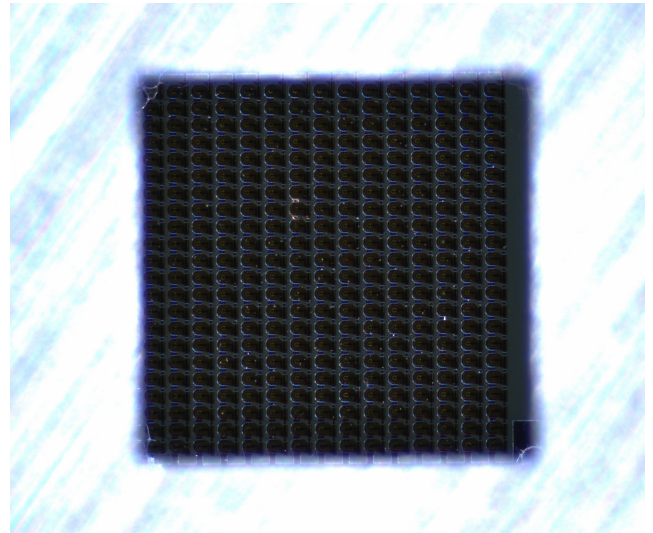
Figure 2.14

A few test dies have been used to determine the correct length and amount of cycles to completely etch the thick silicon layer. The recipe consists in 27 cycles of 30s at a pressure of 400 Pa. Optical microscope observation of the dies after an inferior number of cycle is not recommended, because some of the etched silicon is exposed to the ambient atmosphere of the cleanroom and immediately starts to grow a native oxide that is not etched by the XeF_2 anymore, leading to the presence of 'cobweb structures' limiting the optical transparency from the backside (see figure 2.14a). A failure to correctly protect the sides of the die leads to a partial delamination of the aluminum layer due to severe underetching of the silicon (see figure 2.14b).

With the right preparation of the dies and the correct recipe for the isotropic dry etching, the results are satisfying, with an optically transparent backside (figure 2.15b). At this point, the membranes can finally be released by immersing the glass tabs in acetone and then isopropanol to get rid of the blue resist. With this final step, the fabrication process of the SPADs is complete.



(a) Frontside of a fabricated SPAD 36



(b) Backside of a properly released SiPM 36

Figure 2.15

Chapter 3

SPADs characterization and irradiation campaign

3.1 Pre-radiation characterization

After the complete fabrication process described in the previous chapter, an initial characterization of the devices has been made to obtain a reference measurement with which the irradiated SPADs will be compared. First, the selection of devices that will undergo radiations is presented. Then, the measurement setup and the I-V curves are shown for the different architectures and dimensions.

3.1.1 Devices selection

All the devices produced (presented in chapter 2) are not selected for the radiation campaign. Several reasons motivate this decision:

- Space limitation : devices from different projects are exposed to the radioactive sources during this irradiation campaign. To ensure an homogeneous exposure of the different devices, they are located in a specific square area that has been defined by all parties involved. To accommodate for these specifications, the different SPADs are not mounted on PCBs nor wire-bonded.
- Time limitation : several intermediate measurements are made to observe the evolution of the behavior of the different devices. However, annealing mechanisms that reverse the damages caused by radiations occur even at room temperature. To limit the impact of these effects and ensure proper analysis, a maximum time slot of 3 hours has been determined for the measurements to be made. The amount of devices that are irradiated is chosen proportionally to the time taken by the individual measurement of each die.

The SPADs are selected so that different sizes, designs and architecture can be compared fairly. A reference design is chosen, and the other devices measured only present a single different characteristic with the reference SPAD. The changing feature can be the design/size, the presence or absence of a resistor, the trench/mesa architecture or the fact that the membrane has been released. The reference design selected is the **36TR** (following the simple nomenclature where *36* is the architecture, *T* indicates a trench variation and *R* indicates the presence of a quenching resistance). As a precaution, two of these reference SPADs were part of the selection in case one of them became damaged.

Since the devices were not mounted on a PCB, the high amount of manipulation of the dies with tweezers and the repeated probing of the pads to characterize them and take the intermediate measurements oriented the selection towards the unreleased devices because they are more robust than their released counterpart. Therefore, only two released SPADs (36TR and 46TR) are part of the selection to observe potentially different behaviors. The list of devices that measured and irradiated is presented in table 3.1.

Device	T	TR	M	MR
36	2x	2x + 1x released	-	1x
46	1x	1x	-	-
52	-	1x	-	1x

Table 3.1: SPADs selected for the irradiation campaign

3.1.2 Measurement setup

Since none of the dies are PCB-mounted, they are individually measured in the dark with a Microtec PM8 PS prober. The IV measurements are made with a strict current compliance of 10 nA to prevent the complete avalanche breakdown to occur.

3.1.3 I-V measurement

Important parameters of the fabricated devices can be obtained by making DC measurement without illumination. The reverse I-V curve is obtained by varying the cathode voltage between -2 and 15V while observing the current at the cathode. It is one of the most important measurement to define the operating

characteristics of a SPAD, such as its breakdown voltage and its leakage current. The current-voltage curves of the different devices are presented in figure 3.1 in the form of a semi-log plot. This representations doesn't show the negative cathode current for the forward bias, but it allows for a better visualization of the leakage current and breakdown voltage. Several different behaviors are observed on this

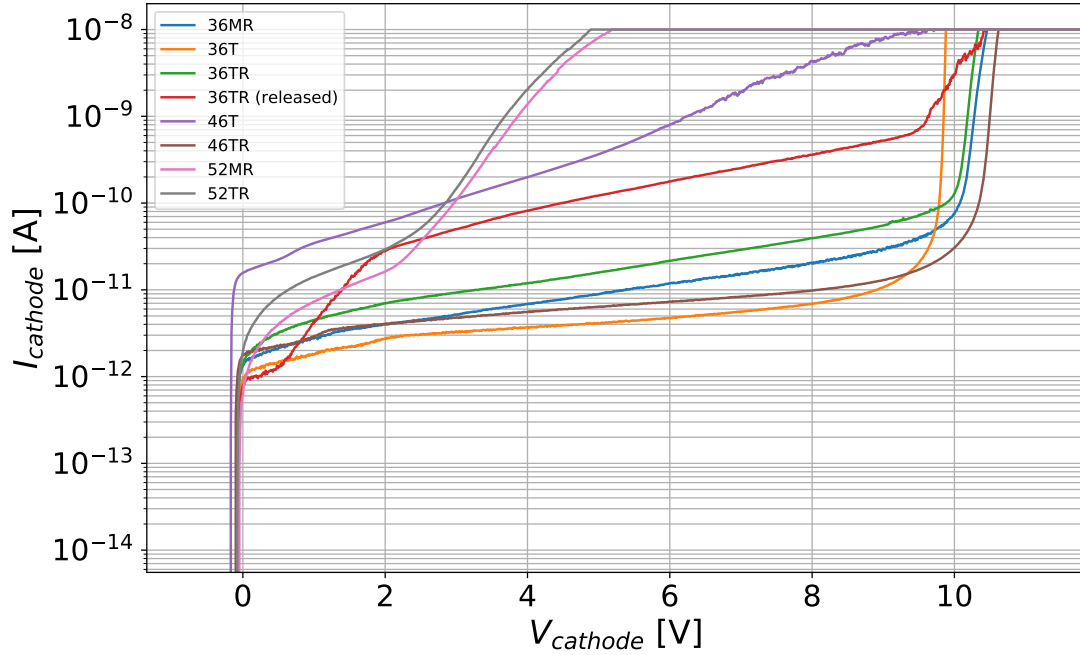


Figure 3.1: Reverse biased I-V measurement of the selected devices (semi-log plot)

plot. Devices 36MR, 36TR and 46TR present the most typical and expected curve for a reverse bias operation, with a low leakage current around $I_{leakage} = 10^{-11}$ A and a sudden current rise at their respective breakdown voltages around 10V, limited by the machine compliance. The same behavior is observed for the diode 36T, where the absence of resistance makes the breakdown voltage steeper. The released device presents a less distinct breakdown knee, and both device 46T and itself have important dark currents, orders of magnitude higher than expected. We also observe that the devices with the hexagonal design (52MR and 52TR) present an abnormal behavior, with the cathode current rising at around 2.5V. Understanding the exact reason for these unexpected behaviors is not easy, but fabrication defects including short-circuits (or low-resistance paths) between the anode and the cathode are possible and have been visually observed in some of the defective devices.

To confirm that these measured curves do not reflect a standard behavior, the current-voltage can be observed in a linear plot where a clear difference is observable between devices 36MR - 36TR - 36T - 46TR and the other ones. Contrary to the semi-log plot, it is also possible to observe the forward bias behavior of the diodes, with an important positive anode current after the anode threshold voltage.

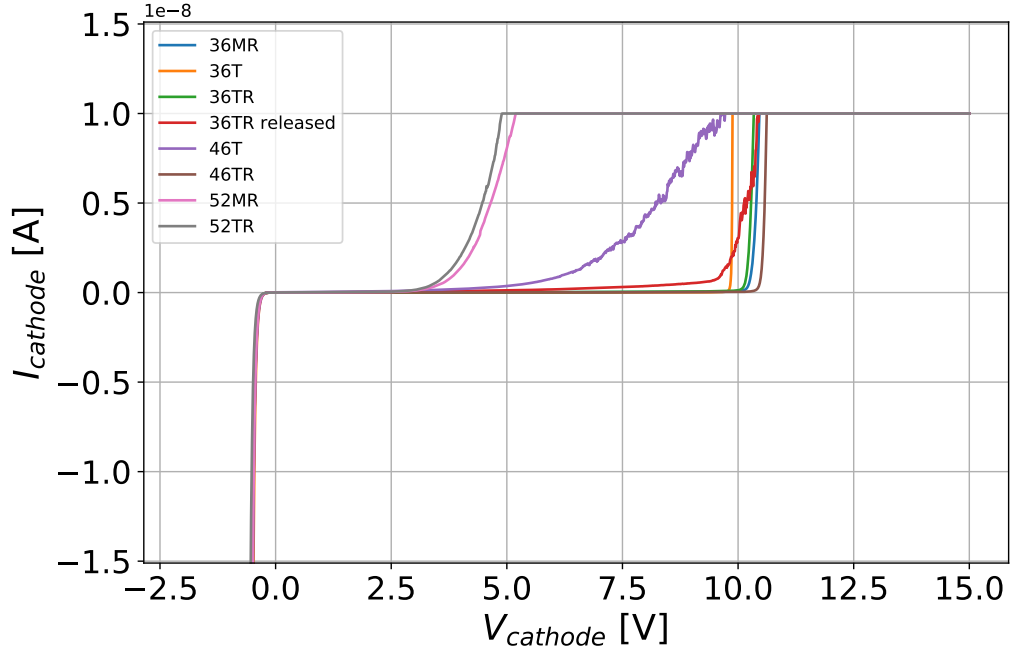


Figure 3.2: Reverse biased I-V measurement in a linear plot

These different experimental measurements can be evaluated in comparison with the expected values presented in [47], [23]. Regarding the breakdown voltage, slightly higher values are observed for these devices compared to the one presented in previous characterization but they are still relatively close. It is also important to note that a lower current threshold is used in this report work to determine the value of V_{BD} , at only 10 nA. Whereas an average breakdown voltage of 9.78V is reported in [23] for SOITEC wafers, we obtain an average value of 10.2V. The dark current values are similar to the measured one, between 1 and 10 pA.

3.2 Irradiation campaign

The selected devices were irradiated at the Cyclotron facility in Louvain-la-Neuve to observe potential effects on their performances that should be taken care of or anticipated with regards to their applications.

3.2.1 Experimental setup

The devices were placed in a closed small plastic box on a slightly adhesive material covering the inside of the box to guarantee that they do not move and accidentally shield each other from the radiations. As specified in a previous section, other devices from different projects were part of the same irradiation campaign. A specific square area of $5 \times 5 \text{ cm}^2$ is designated as the *area of interest* where the devices have to be located to ensure homogeneous radiation doses for all parties concerned (figure 3.3). The support of the dies for the different project are then taped to a piece of cardboard to facilitate its swift positioning in the irradiation room as well as its transport from the *Cyclotron* facility to the *Welcome* characterization laboratory. None of the materials used are shielding the exposed devices, ensuring the fidelity measured radiation doses. The irradiation room consists of three Cobalt-60 sources,

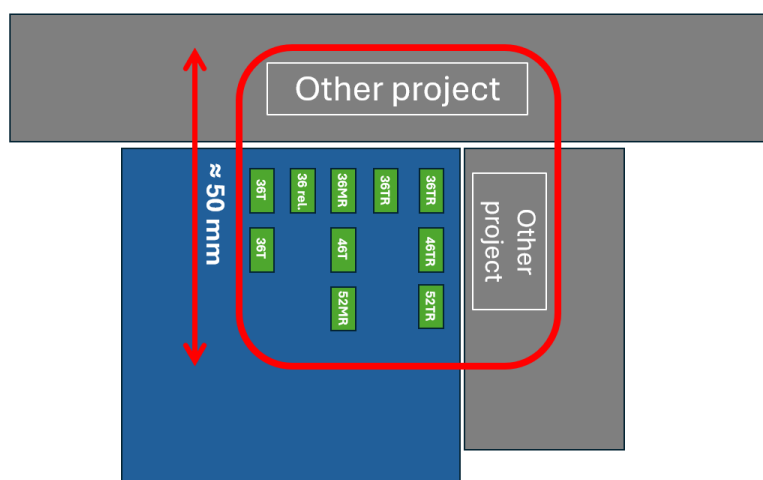


Figure 3.3: Position of the devices for the irradiation. The area of interest is represented in red.

producing gamma radiations. One of the source was depleted at the time of the campaign, so only two of them are effectively producing γ rays. The devices are placed on a stand, a few dozens of centimeters from the ground, at a certain distance from the sources determined by the technicians (figure 3.4).

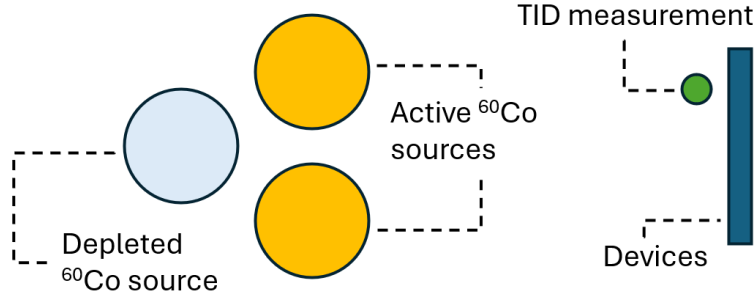


Figure 3.4: Layout of the radiation room

3.2.2 Irradiation schedule

The samples were irradiated at a rate of approximately 512 rad/hour during 11 days, to reach a Total Ionization Dose above 100 krad. The exact schedule is presented in table 3.2. The different measurements are not done at 'round' amounts

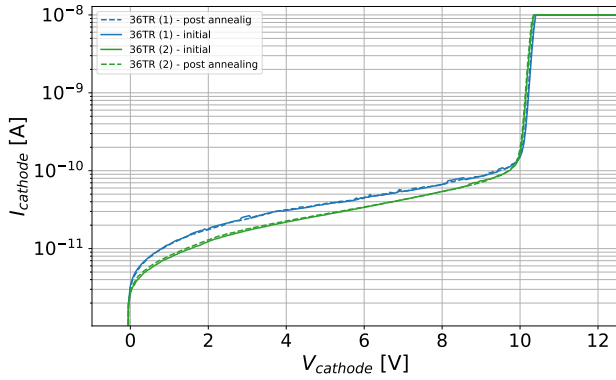
Step	Start	End	Duration [hour]	Dose rate [rad/hour]	Accumulated dose [Gy]	Accumulated dose [krad (Si)]
1	06/05 - 11:45	07/05 - 12:00	24:15	518	139.8	12.582
2	07/05 - 15:00	08/05 - 12:50	21:50	528	267.9	24.111
3	08/05 - 16:01	13/05 - 08:08	112:07	526	924	83.160
4	13/05 - 11:15	15/05 - 09:02	45:47	523	1189	107.100
5	15/05 - 12:04	17/05 - 13:07	49:03	522	1474	132.660

Table 3.2: Complete irradiation schedule of the SPADs

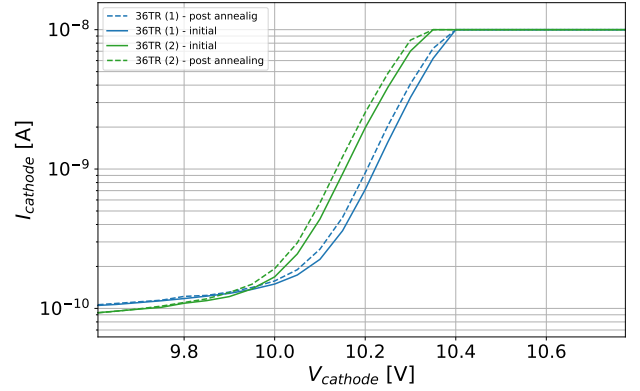
of accumulated doses due to schedule constraint with the Cyclotron facility. The accumulated dose is measured at every radiation step and is given in grays. To obtain the silicon-equivalent Total Ionizing Dose, a factor of 0.9 is applied and the unit is changed to krad. A maximum TID of 132 krad is reached at the end of the irradiation campaign. Note that an important part of the devices measured at the first step of radiation (TID = 12.6 krad) are not exploitable due to technical problems encountered with the PM8 PS prober. Since most of these measurements are extremely noisy or incoherent, it has been decided not to present them in the next section.

As presented earlier, the maximum amount of time allocated to the transport and measurement of the devices is 3 hours, to minimize the effects of room temperature

annealing. These possible annealing effects have been quantified after the last radiation step by making an I-V measurement of the first quantified SPAD (36TR) 3 hours after getting the samples out of the GIF (Gamma Irradiation Facility) and comparing it to the characterization done as fast as possible after starting the measurements. The results are presented in figure 3.5. We observe a slight annealing process already taking place in under 3 hours. The leakage current is quite similar before and after the time duration period, at values ranging between 10 and 100 pA. Regarding the voltage breakdown, a slight shift (in the range of 10 - 20 mV) is observed towards the left. This phenomenon is present and similar for both 36TR SPADs. To prevent this annealing from affecting the measurements, the SPADs are measured in the same sequence at every step to ensure that the annealing time is identical.



(a) Complete IV curve before and after RT annealing



(b) Zoom on the breakdown voltage

Figure 3.5: IV curves of two SPAD 36TR at the beginning and at the end of the measurement session

3.3 Post-irradiation characterization

To observe possible variations in the parameters of the fabricated devices, I-V measurements are made for every device after each irradiation step. For each of these current-voltage plots, both the complete curve and a zoomed version on the breakdown phenomenon are presented and discussed.

3.3.1 I-V measurement

The evolution of the current-voltage curves of devices 36TR, 36MR and 36T are presented in figures A.1 to 3.8. For device 36TR, only measurements from steps

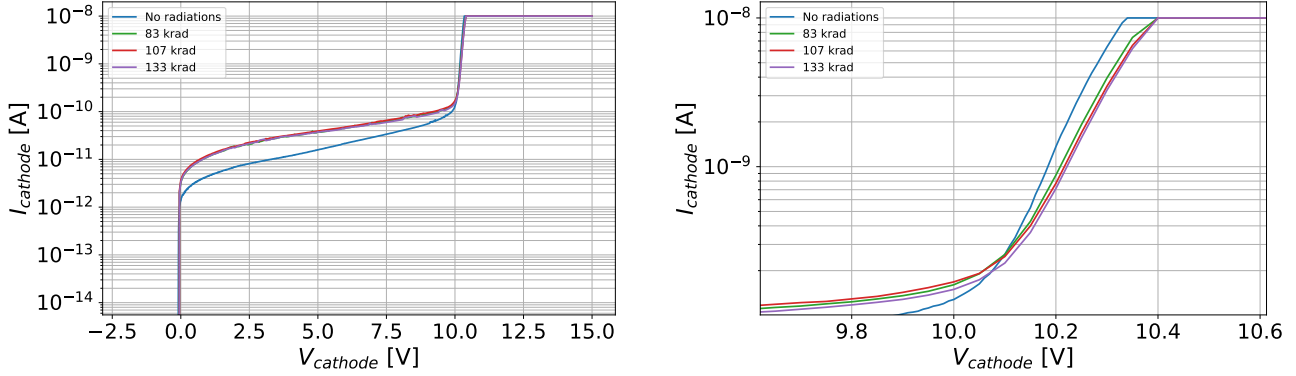


Figure 3.6: IV curves of SPAD 36TR at different irradiation stages

3 to 5 were correct and could be analyzed. Two main effects of the radiations can be observed : first of all, the dark current is now present at a higher level, with a factor ranging from 2 to 3. We do not observe significant differences of dark current between the different levels of radiations. Regarding the breakdown voltage, different interpretations can be made depending on the definition used to determine the breakdown voltage. With an arbitrarily fixed voltage limit such as 1 or 10 nA, we could observe a shift towards the right of a few 10s of mV. This shift seems to be proportional to the increasing Total Ionizing Dose, with increasingly higher breakdown voltage values. It should however be pointed out that the slope of the curve around this breakdown voltage is lower for the irradiated devices. This might indicate some sort of effect of the gamma rays on the polysilicon resistance. The steeper slope could also be a visual artifact due to the fact that the leakage current evolution is slightly more important for the device before irradiation : an identical breakdown 'knee' would therefore result in an apparently steeper slope relatively to the other curves presented in figure A.1.

For the 36MR device (figure 3.7), similar behaviors are observed. The leakage current is also more important at each irradiation step. The voltage breakdown happens to be shifted once again towards the right, in this case by magnitudes higher than 100 mV, 10 times more than previously observed for the 36TR SPAD. We observe that the shift is not equal in amplitude for the different devices or architecture. However, the influence of the resistance on the shape of the breakdown

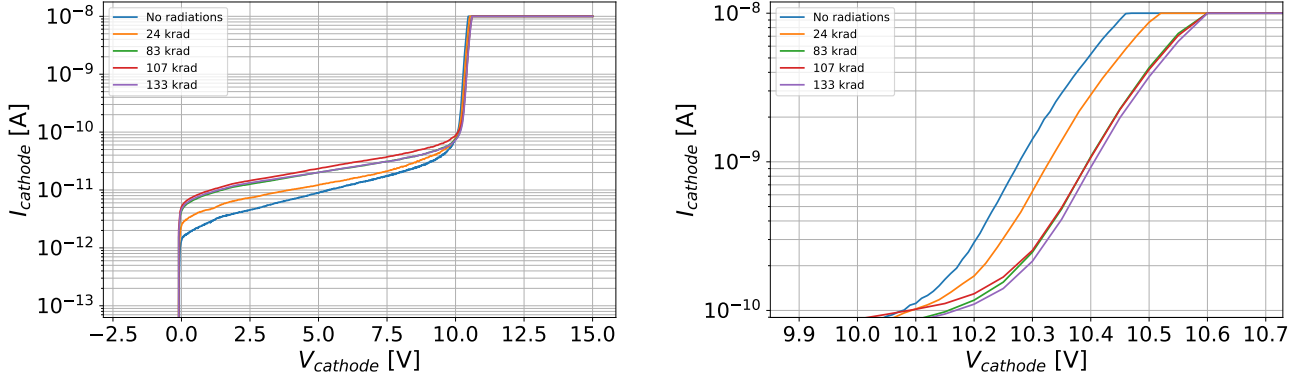


Figure 3.7: IV curves of SPAD 36MR at different irradiation stages

knee is still not clearly defined.

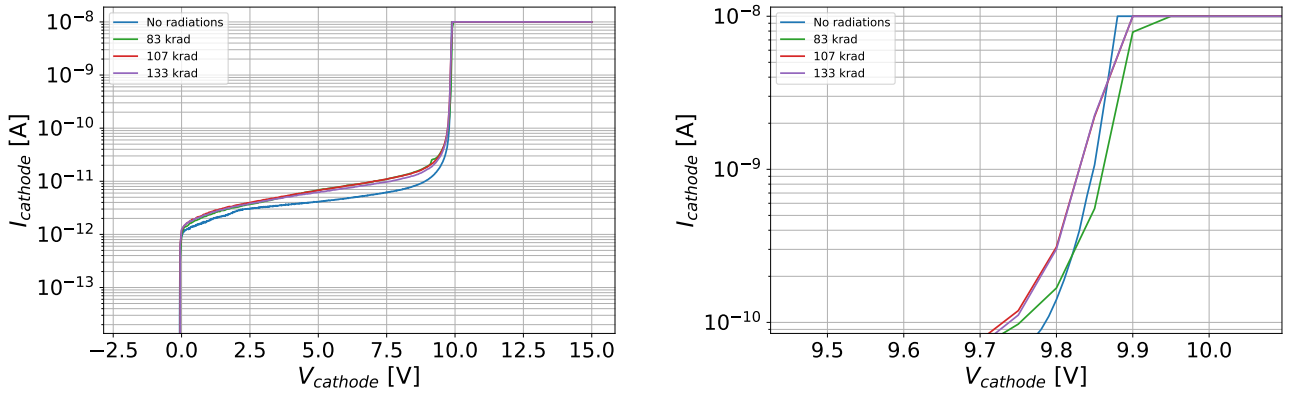


Figure 3.8: IV curves of SPAD 36T at different irradiation stages

To get a better understanding of its potential impact, a device without resistor is analyzed. The I-V plot of diode 36T (figure 3.8) is interesting because it confirms the increase in dark current with radiation levels, as well as the more gradual slope of current around the breakdown voltage. We can conclude from this observation that the resistance is not the cause for this increase in the slope. Whereas we usually observe a shift of the curve around V_{BD} towards the right, the behavior is less distinguishable for this device, as the slope after complete irradiation is somehow on the left of the slope after only two irradiation steps.

All these observations are however limited by a number of factor due to the experimental nature of this chapter : defective devices due to the fabrication process, failed measurements due to poor connexion between the probes and the metal pads, impossibility to check the validity of measurements due to timing constraints, etc. It is therefore of interest to try to replicate these behavior via TCAD simulation.

Chapter 4

Modelisation of the radiation effects

To get a better understanding of the effects first observed in chapter 3, a modelisation of a SPAD with the architecture 36 is made with Silvaco, a TCAD software made to develop electronic devices by simulating their fabrication process and electrical behavior. In this chapter, the model of the device is presented as well as the different simulation parameters used. Then, simulations aimed at re-enacting the electrical behaviors observed earlier in this work are made and discussed. Finally, the effects of radiation with regards to leakage current and voltage breakdown are quantitatively put in perspective with other parameters that can have an influence on SPADs.

4.1 Modelisation of the 36 SPAD

Models of the UV-enhanced BSI SOI SPAD have already been made in previous works ([23], [27]) with Silvaco tools *Athena* and *Atlas*. *Athena* is a process simulator that generates a very faithful model of the device by precisely simulating each microfabrication steps. For this work, a simpler model has been made with *Atlas* to improve the simulation speed and avoid repeated convergence problems. It is based on a model developed by Tom Klauner, and it has been updated with his help to be as close as possible to the fabricated devices presented in chapter 2. This model reproduces the correct device dimensions and includes the addition of the thick silicon nitride layer. The objective of this modelisation is to understand the intrinsic behavior of the device after irradiation. Therefore, resistances and readout circuits are not included. Furthermore, the diode is only simulated in 2D for simplicity and time efficiency.

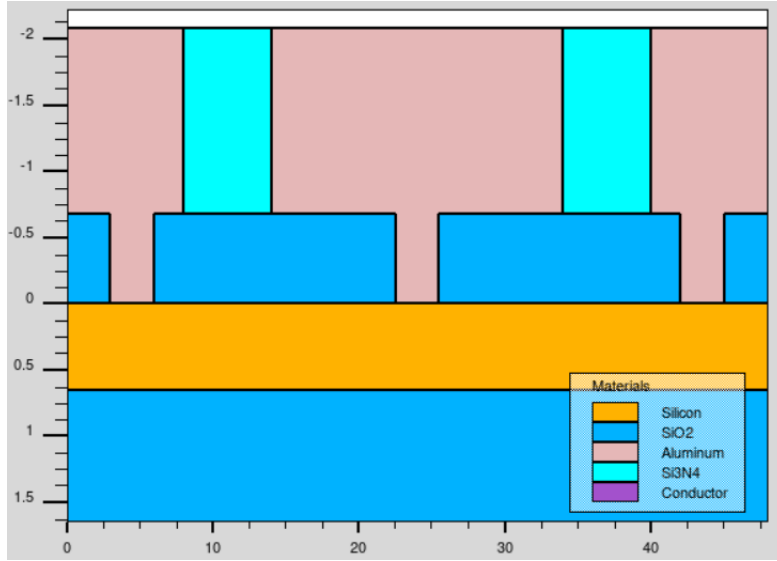


Figure 4.1: Structure simulated with *Atlas*

The updated model is presented in figure 4.1. The dimensions are similar to the fabricated device (figure 2.13). However the doping profiles have been adapted to fit the current-voltage curves to the experimental measurements. Without these precautions, a breakdown as early as 7 V can be observed, which does not match the experimental measurement. *Atlas* models are enabled to take a variety of physical effects into account. This selection is based on [23]

- Transport : the drift-diffusion model is used. The system is solved with Poisson's equations, current continuity and drift-diffusion equations.
- Recombination : Shockley-Read-Hall recombination using concentration dependent lifetimes and Auger recombination accounting for high level injection effects
- Carrier statistics : the Boltzmann approximation is used because simulations are done at room temperature, as well as the bandgap narrowing model to take into account the dependence of the bandgap with high doping concentration
- Mobility : the concentration dependent mobility mode is used to model the loss of momentum of carriers relative to the doping profile and the lateral electric field-dependent mobility model takes into account the velocity saturation of the carriers.
- Impact ionization : the Selberherr's model is recommended by the *Atlas* manual for most cases and it presents temperature dependent parameters,

which are of particular for the last section of this work.

To obtain the current-voltage curve, the cathode voltage is increased from 0.1 to 15V, with an imposed current compliance of 1 μ A to limit the simulation time (and because the observable effects are already present at this current level). The I-V curve of the SPAD 36 model is presented in figure 4.2 and compared to the experimental measurement. We observe a dark current steadily increasing from $2E-13$ A to $1E-11$ A and a breakdown happening at a voltage of 10.0 V. These results are close matches to the measurements made on the diode 36T. The model is satisfying and will be used to simulate the irradiation effects.

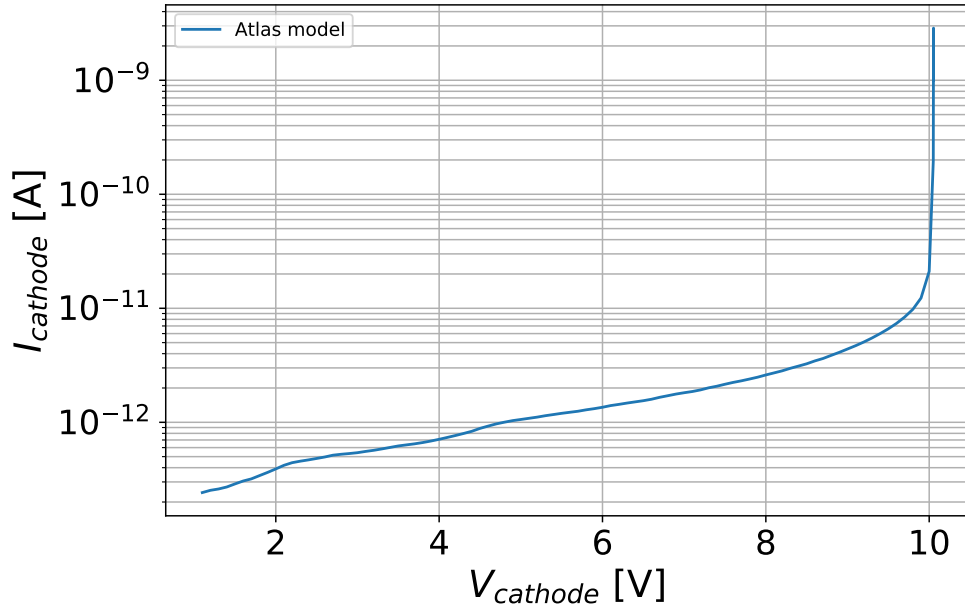


Figure 4.2: Simulated IV curve

4.2 Simulation of radiation effects and discussion

There are two ways to reproduce the effects that radiations have on the devices. The first one consists of using the Radiation Effects Module (REM) from Silvaco while specifying the source and the rate of the radiation source. However, convergence problems were encountered very often when using this module on the modeled SPAD, making this solution unreliable. The second option consists of manually introducing the effects caused by radiation. We know from section 1.4 that charges are trapped in the oxide layers and that interface states are created. Therefore, to

emulate the behavior of irradiated devices, oxide charges and interface traps are manually added to the structure of the device.

Typical orders of magnitude for the oxide charges N_{ox} and interface traps N_{it} are found in the literature[67] and are respectively ranging from $1E17\text{cm}^{-3}$ to $5E17\text{cm}^{-3}$ and $1E12\text{cm}^{-2}$ to $5E12\text{cm}^{-2}$, for radiation doses up to 1 kGy (100 krad). Simulations were carried out on the SPAD 36 model for increasing values of oxide charges and are shown on figure 4.3 These manual insertion of charges in the

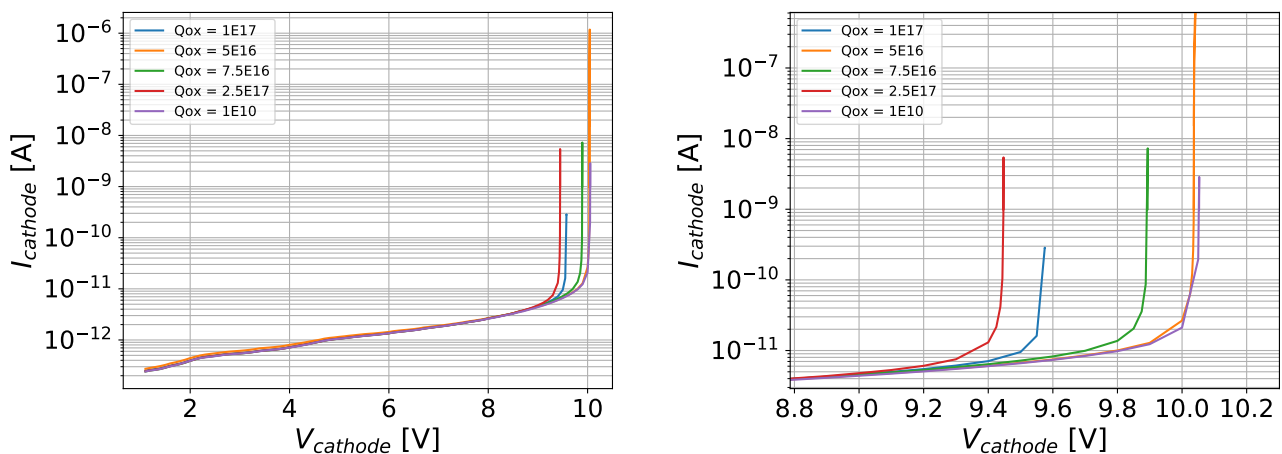


Figure 4.3: IV curves of simulated SPAD 36 with fixed charge oxides

oxide produce unexpected results, with close to no difference in the dark current and a very important shift of the breakdown voltage towards the left. These results are not similar to the one observed in chapter 3, but they could however explain breakdown voltage shift towards the left for device 46TR.

The simulated curves for increasing concentration of interface traps did not show any difference, which leads to the impression that the SPAD model or the implementation of these interface traps might faulty. However, it has been found in the literature[11] that interface traps can slightly increase the breakdown voltage. It could be possible that both these effects counteract each other and that the behaviors observed in chapter 3 are dependent on which one of them is dominant. The dark current is also expected to increase with radiations due to the presence of defects leading to the presence of deep acceptor levels in the bandgap[29].

4.3 Influence of other parameters

The observed increase in dark current and the shift of voltage breakdown both seem to happen after irradiation. However, their quantification is quite complex. To at least be able to compare them to other physical phenomenons, an analysis of the behavior of SPADs for varying temperature is made. The oxide charges and interface traps are removed and the temperature is modified by steps of 20°K. The results are presented in figure 4.4. We observe a clear increase of the dark

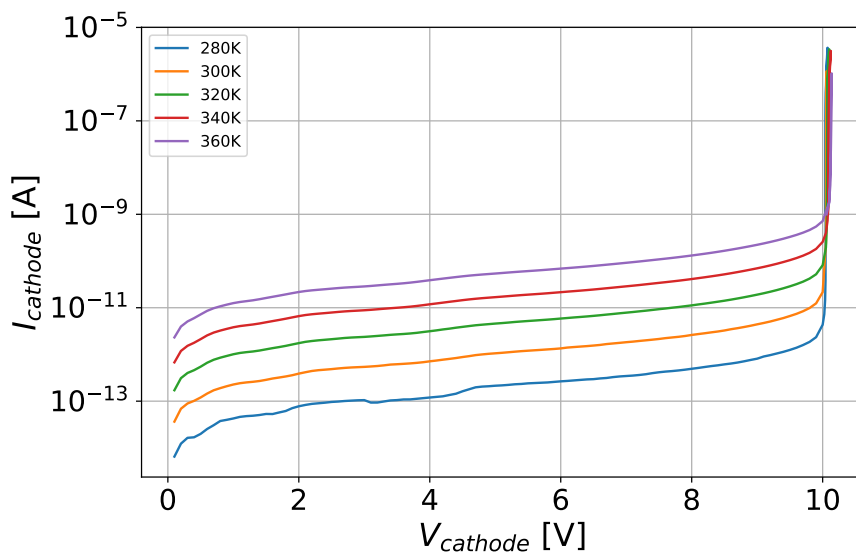


Figure 4.4: IV curves of simulated SPAD 36 at different temperatures

current, several orders of magnitude more important than the one observed during the measurements. At higher temperature, several mechanisms contribute to this phenomenon, such as the thermal generation of carriers, an exponential increase in intrinsic carriers concentration and a higher mobility of charge carriers. No effects on the breakdown voltage are observable on this plot. However, it has been reported that the breakdown voltage increases with increasing temperature due to the decrease of the ionization rate (figure 4.5)[47]. We observe that It appears quite clearly that the model and the simulations used for this chapter could be improved. They provide incomplete information on the trends observed in chapter 3. Their analysis is not easy, but they still bring quantitative information on the intrinsic behavior of UV-enhanced BSI SPAD.

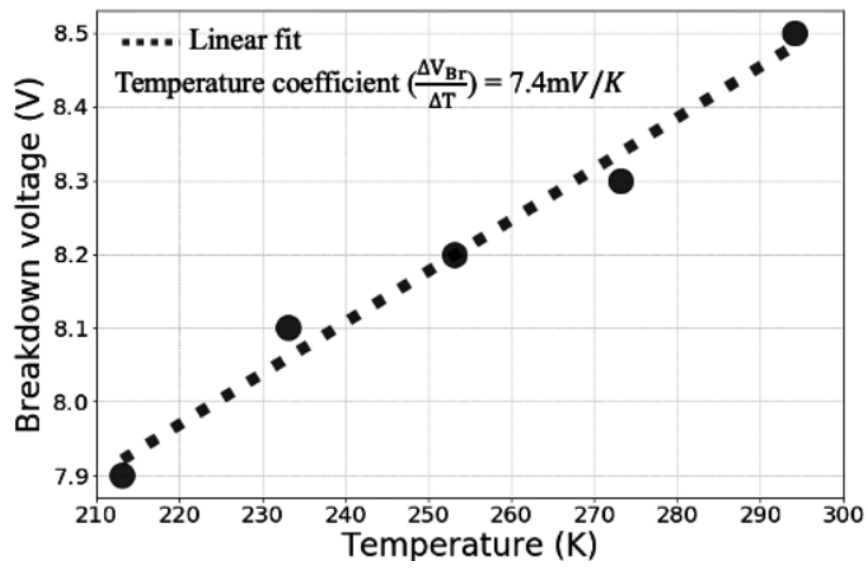


Figure 4.5: Relationship between the breakdown voltage and temperature. From [47]

Conclusion and perspectives

In conclusion, this work presents experimental results regarding the characterization and irradiation of a UV-enhanced backside illuminated SPAD developed at UCLouvain.

In the first part of this thesis, an extensive description of the SPADs fabrication process is given. All of the steps are presented with the associated parameters and the different machines used. The risks regarding the backside operations are discussed, and solutions are presented to avoid making mistakes or damaging dies in the future fabrication processes.

The results from the irradiation campaign are then discussed and compared with each other. The radiation effect are qualitatively described and trends are highlighted. It is established that the leakage current is increased in irradiated devices and that the voltage breakdown undergoes a shift of several tens of milivolts either towards the left or the right.

Then, an TCAD model of the SPAD 36 is introduced, with updated dimensions to match the fabricated devices. Irradiation effects are simulated by introducing fixed oxide charges and interface traps, but resulting IV curve only show isolated parts of the total observed effect. To put the importance of radiations in perspective with regards to the breakdown voltage and the leakage current, a simulation is carried out with varying temperature. It is shown, although qualitatively, that the increase in dark current is at least 2 bigger for a 20°K shift in temperature than it is for a 100 krad irradiation. It is also shown that temperature shifts the breakdown voltage point of a SPAD at quite a high rate and in a defined direction. It is therefore concluded that radiations are not the most dominant phenomenon regarding shifts in electrical behaviors for SPADs.

Future works could address in detail the possible differences between the various SPADs architectures and designs. A quantitative comparison was not made in this work due to the numerous time and material limitations that would not have

allowed for a fair comparison. A complete analysis of degradation of the Dark Count Rate (DCR) due to irradiation could also be undertaken, as well as a research on the healing methods for radiation damages.

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Appendix A

IV measurement

For the device 46TR, a shift of the breakdown voltage towards the left can be observed.

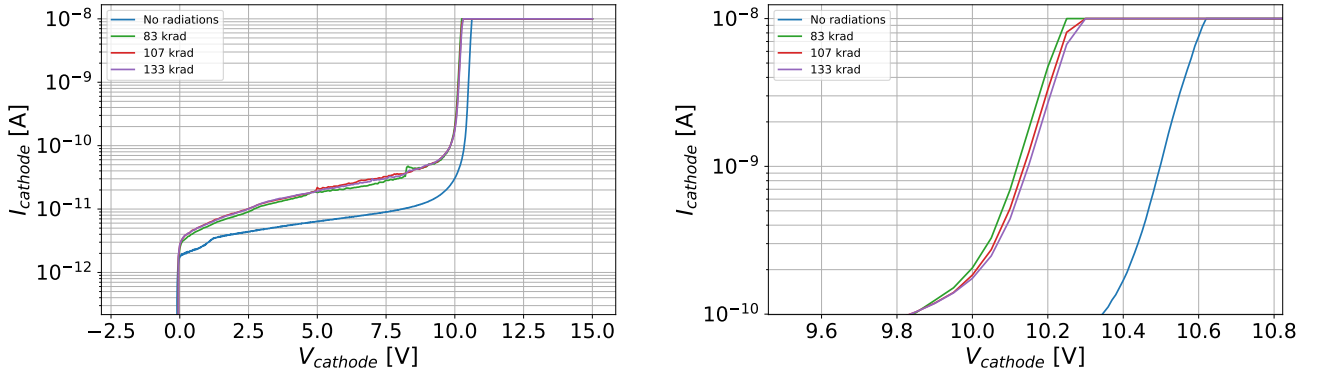


Figure A.1: IV curves of SPAD 46TR at different irradiation stages

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