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Design of a radio frequency energy harvesting circuit with an incorporated solar cell

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To conclude, I would like to deeply thank my parents without whom it wouldn't have been possible for me to get where I'm now.

Abstract

This work presents a radio frequency energy harvesting circuit designed to harvest RF energy at 2.45GHz with the help of an incorporated solar cell. The levels of RF energy targeted are between -30dBm and -20dBm. The off the shelf solar cell of this work is the dye sensitized solar cell from *3gsolar* that can provide a constant voltage of 500mV for indoor condition operations (between 50lux and 500lux). The simulated Power Harvesting Efficiency (PHE), RF + solar, can reach 43% for -30dBm of RF input power at 500lux of irradiance and 38.3% at 50lux for the same level of RF input power.

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Chapter 1

Introduction

This work present the design of a Radio Frequency Energy Harvesting (RFEH) circuit working at $2.45GHz$ with an incorporated off the shelf solar cell designed for indoor condition purposes. The main idea behind the use of the solar cell inside the RFEH circuit is to collect solar energy for hybrid energy harvesting but also to enhance the efficiency of the circuit that harvests the Radio Frequency (RF) energy.
Figure 1.1 represents the chain of blocs that compose a traditional RFEH circuit (without solar cell) to supply energy to a load (a sensor in this example). The circuit harvests the RF signal with an antenna. This antenna converts the electromagnetic waves into a useful AC signal for the circuit. This AC signal is converted with a rectifier into a DC voltage for the Power Maganement Unit (PMU) that performs MPPT to supply a constant DC voltage at the sensor.

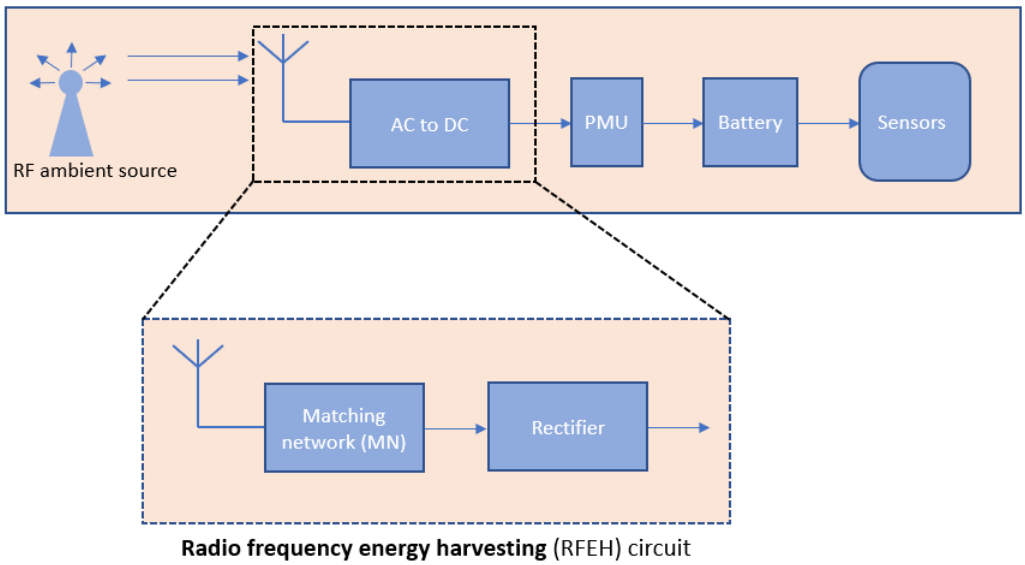


Figure 1.1: Representation of the traditional chain of blocs that compose a RFEH circuit.

One of the main challenge when designing a RFEH circuit is the low level of input power that lies usually between -40dBm and 30dBm depending on the type of the RF source and the distance at which the energy is harvested. To be able to supply energy

to a load: sensor, power management unit, battery inside a Wireless Sensor Network (WSN), etc, the ouput voltage of the circuit should be high enough to meet the voltage requirement for proper operation condition. This is not an easy task since the input power is low and the losses inside the circuit with the high operation frequency decrease the available output power.

The incorporation of the solar cell in the RFEH circuit can boost the ouput voltage and decrease the losses inside the RFEH circuit by improving the matching between the impedances that compose the circuit.

This document begin with a description of the specifications that the final RFEH circuit need to respect. After that, the state of art of each sub circuit that compose the proposed RFEH circuit is presented. Equations and exemples from different recent papers are presented to explain the challenges of designing a RFEH circuit.

The following chapter present the proposed topology of the circuit with incorporated solar cell with the overall design. The electrical equivalent circuit of all the blocs that compose the circuit are presented with the associated value for the lumped components and equations: solar cell, antenna, power management unit, rectifier and matching network.

Onced each bloc is designed, the second to last chapter presents all the simulations perfomed with the proposed circuit. The justification for the incorporation of the solar cell is presented through ADS plots and the Power Harvest Efficiency (PHE) of the overall circuit is computed for different parameter values.

The final chapter present the conclusion of this work and future modification that can be done to increase the efficiency.

1.1 Goal of the master thesis

Most of the RFEH circuits proposed in the litterature that work with microwave frequencies cannot harvest energy below -25dBm with enough ouput voltage (above 1V) to supply a battery or a load. For that reason, the idea of incorporating a solar cell was decided to increase the available ouput voltage and enhance the RF energy efficiency.
The goal of the master thesis is to prove that with the help of a low power solar cell, the efficiency of a circuit that harvest low power RF signals can be enhanced. Simulation are provided at the end of this work to prove the feasibility of the concept.

1.2 Design procedure

Onced all the bloc that composed the RFEH circuit are modeled, the reverse global analysis technique from Pengcheng Xu[46] is used to design the parameters that composed those model for the simulation.
This procedure consist of using the output parameters from the RFEH circuit: ouput voltage, ouput power and internal voltage inside the circuit to quantify the level of RF input power needed to supply the load or Power Management Unit (PMU) at the ouput of the circuit.

Chapter 2

Specifications

To be able to incorporate the RFEH circuit inside a WSN, the dimensions of the circuit need to be restricted. For that reason, they are limited here by choice at 5x5x5cm. Because most of the available ambient signals operate at microwave frequencies, the targeted frequency of operation for the circuit is $2.45GHz$ with an input power below -25dBm. As explain in the introduction, the main purpose of the solar cell is to enhance the efficiency of the RF signal harvested. For that reason, a low power solar cell is used here with the dimension of 36x38x4.5 mm for the width, length and height respectively and a weigth of 7.7g from *3gsolar*. This solar cell is designed for indoor condition environement and can work between 50lux and 1000lux. The Power Management Unit (PMU) from *epeas* is used as a voltage regulator at the end of the RFEH circuit. The ouput voltage and power of the circuit are imposed by the cold start condition of the PMU.

Table 2.1 summarize the specifications targeted here for the design of the circuit:

Specifications	
Dimension	5x5x5cm
Input frequency	2.45GHz
RF input power	-30dBm to -20dBm
Solar input power	50lux to 500lux
Output voltage	380mV
Output power	3uW

Table 2.1: Specifications of the RFEH circuit with incorporated solar cell.

Chapter 3

State of the art

This chapter present the state of art of Radio Frequency Energy Harvesting (RFEH) circuit and hybrid energy harvesting of solar and Radio Frequency (RF) energy.

The first section describes the architecture of the conventional RFEH circuit and displays the main blocs that compose it.

The second section describes the main sources of RF energy that can be harvested by a RFEH circuit.

The remaining sections of this chapter present the state of art of each individual bloc that compose the conventional RFEH circuit, with the addition of the solar cell. The theory associated with each bloc is presented and some key equations that are important to understand the design choices of the circuit are explained.

3.1 Topology

The conventional topology of a Radio Frequency Energy Harvest (RFEH) circuit (without the solar cell) can be seen in Figure 3.1:

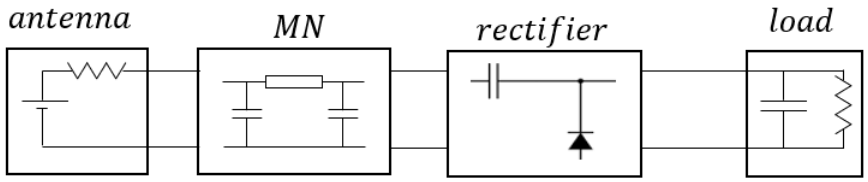


Figure 3.1: Representation of the conventinal topology of a RFEH circuit

The circuit of Figure 3.1 is composed of four main blocs: the antenna, the matching network (MN), the rectifier and the load. The antenna represents the part of the circuit that harvest the electromagnetic waves from the source to convert it into useful electrical power for the circuit. The matching network bloc is composed of various passive electrical elements like inductors and capacitors, to ensure proper power transmission, with maximum efficiency, from the antenna to load. The rectifier bloc convert the AC power from the matching network into DC power for the load.

The nature of the load from the conventional RFEH circuit varies with the application of the circuit. For simulation purposes, the load is usually replaced by a simple resistor to compare the efficiency of the circuit for different antenna or rectifier design. For practical implementation, this load can represent a Power Managment Unit (PMU) who performs DC voltage regulation[46] if the device that the RFEH circuit is suppose to power has specific voltage requirement.

If the RFEH circuit does not include a pre build PMU but still has some voltage constraint to respect at the load, a DC-DC converter can be incorporated between the rectifier and the load.

The main challenge when designing a RFEH circuit for very low input power is the losses inside the circuit. The metric used to quantify the efficiency of the RFEH circuit is the Power Harvest Efficiency (PHE) defined as the ratio between the RF input power $P_{in.RF}$ that comes from the RF source and the output DC power $P_{out.rec}$ that is fed to the load:

$$PHE = \frac{P_{out.rec}}{P_{in.RF}} = \frac{P_{load}}{P_{in.RF}} \tag{3.1}$$

with $P_{load} = P_{in.RF} - P_{loss}$ where P_{loss} represent all the energy lost inside the circuit. Thoses losses are represented in Figure 3.2:

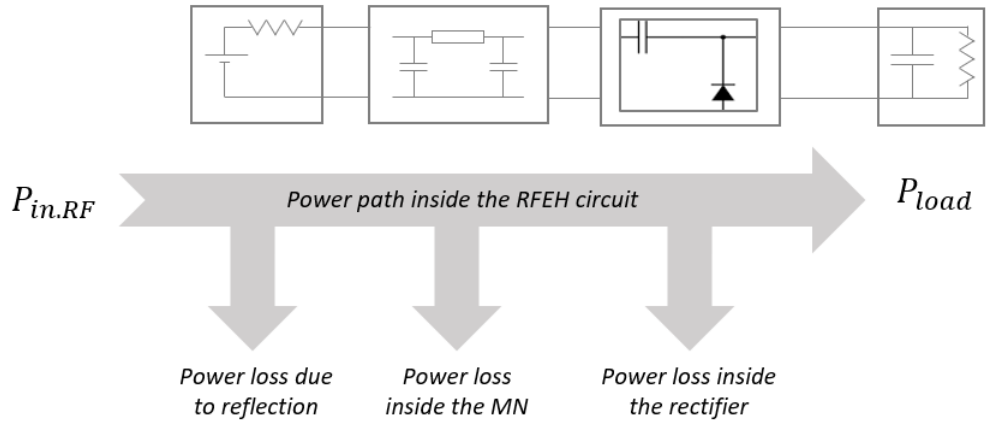


Figure 3.2: Representation of the power path inside the RFEH circuit and the different losses from the antenna to the load

In order to increase the PHE from expression (3.1), the losses inside the circuit need to decrease.

Proper antenna and matching network design can reduce the losses due to reflection. At very low input power, those losses are important due to the presence of parasitic effects who appears at microwave frequencies.

The losses inside the matching network and rectifier are due to the non ideality of the elements that compose those blocs: capacitors, inductances and non linear elements (diode or MOSFET). Some of those losses can be attenuated by using compensation techniques such as Self-V_{th} cancellation (SVC) for a CMOS implementation of the rectifier.

3.2 Radio frequency source

3.2.1 Common source of RF energy

The main purpose of the RFEH circuit is to harvest electromagnetic waves from the surrounding devices that generate radio frequency radiation. Those radiations come at different power levels and frequencies depending on the type of source and the level of radiation emitted.

Most of the signals harvested by a RFEH circuit working under low input power condition have their frequencies that lie between $3kHz$ and $3GHz$. Figure 3.3 from [38] summarize the main available sources and frequencies at which RF energy can be harvested by common RFEH circuit and the level of power associated with it.

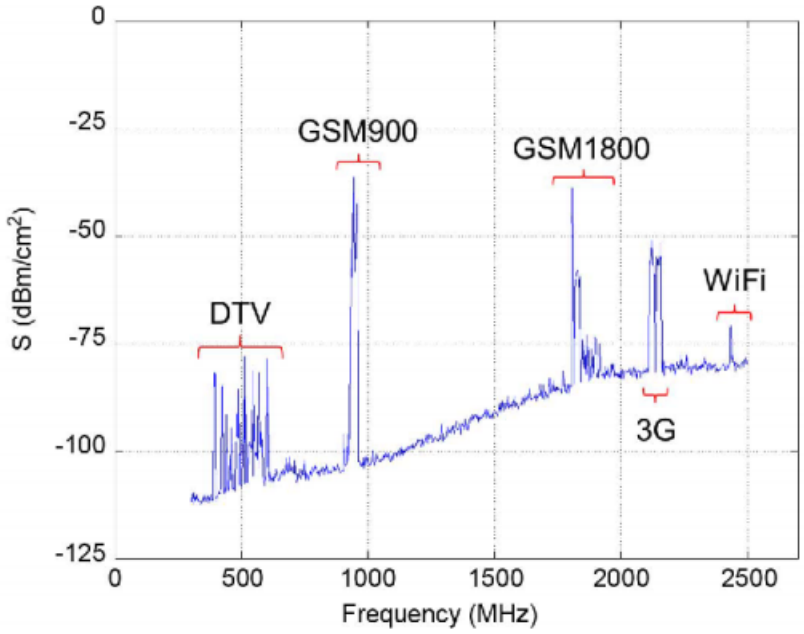


Figure 3.3: Power level of different common RF sources in function of the frequency [38].

Nowadays, the number of signals that can be harvested by a RFEH circuit is high due to the increasing number of wireless application such as GSM900 (890-960MHz), GSM1800 (1710-1885GHz), GMS1900 (1850-1990MHz), LTE2300 (2300-2400MHz), Wi-Fi/WLAN (2400-2450MHz), Wi-MAX3500 (3300-3600MHz) and many more[39]. For that reason, those type of frequencies are targeted during the design of the RFEH circuit.

Because RF energy transfert is used for wireless sensor network, communications and data transfert, the effective distance at which the RF energy can be harvested goes from several centimeters to several meters depending on the frequency and the sensitivity of the RFEH circuit[39]. For that reason, either a specific RF source is targeted when designing the RFEH circuit or the circuit is designed with the purpose of harvesting ambient RF energy (usually 2 or more frequencies) from its surrounding.

3.2.2 Leaky feeders

A leaky feeder or also called a radiating cable is a communication system used to propagate a RF signal from a location of strong signal availability to an other location were that same RF signal couldn't reach without the help the radiating cable. So in order to amplify the level of a RF signal in locations with low signal availability, e.g.: underground mining, some spaces in buildings and tunnels, leaky feeders are used.
Leaky feeders is an exemple of specific RF source that a RFEH circuit can harvest energy from. An example of lealy feeder from [11] can be see in Figure 3.4:

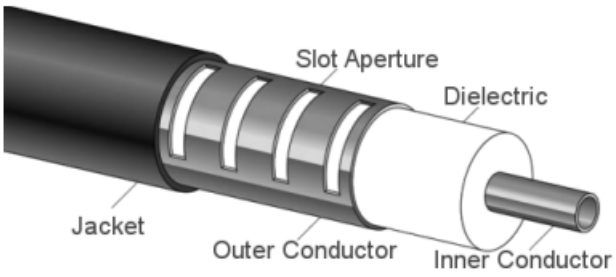


Figure 3.4: Representation of the structure of a standard radiating cable from [11].

The RF signal that propagates through the cable is leaked from the slot aperture of the cable inside the jacket. Those slots on the outer conductor of the cable act as antennas that generate Electrmagnetic Wave (EM).

3.3 Antenna

The antenna bloc of Figure 3.1 represent the physical antenna from the circuit that harvests the electromagntic waves. Those electromagnetic waves originate from different sources according to the environment where the circuit will belong (e.g. indoor or outdoor). The role of the antenna, is to convert the electromagnetic energy into electrical energy that can be delivered to a load. The type of antenna used in the design of the circuit will depend on the frequency of the electromagnetic waves, the level of power that need to be harvested and the polarisation of the wave [16]. They are two popular designs used in RFEH circuit:

- Small wire antenna or monopole/dipole antenna
- Microstrip antenna or patch antenna

Figure 3.5 and 3.6 represent respectively an exemple of a dipole antenna and a patch antenna from [16].

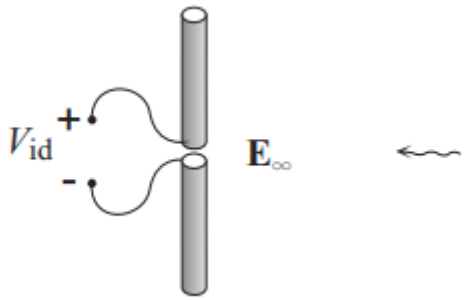


Figure 3.5: Representation of a dipole antenna generating a voltage V_{id} due to the harvested electric field $\mathbf{E}$ from [16].

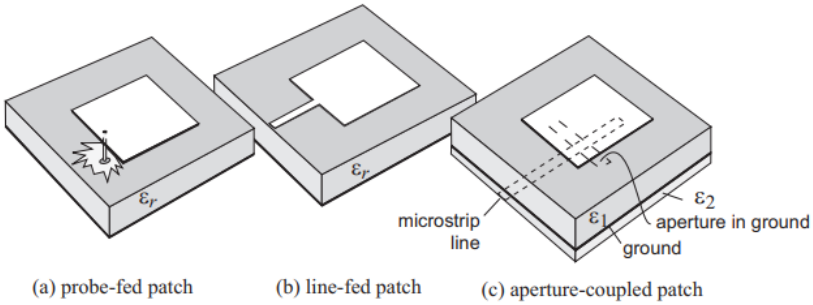


Figure 3.6: Representation of a patch antenna with multiple feed configuration from [16].

When working at microwaves frequencies, above $1GHz$, the patch antenna is preferable compare to the dipole antenna for the design of RFEH circuit.

In term of antenna size, the final RFEH circuit should be relatively small depending on the application. The length of the dipole antenna is usually equal to:

$$L_{dipole} \approx \frac{\lambda}{2} \tag{3.2}$$

with $\lambda(m)$ beeing the wave length in free space, to achieve the desired caracteristic antenna impedance [16]. This mean that in order to work at microwave frequencies, the dipole size should exceed $30cm$ which is not conceivable in most RFEH circuit. Concerning the size of a typical patch antenna, a first approximation of the length can be computed with the following expression from [30], if the antenna is monted on a dielectric substrat:

$$L_{patch} \approx 0.49\frac{\lambda}{\sqrt{\epsilon_r}} \tag{3.3}$$

with ϵ_r the dielectric constant of the PCB. So for the same frequency condition $f = 1GHz$ as the dipole length antenna computed above, if a typical FR4 material is used to design a patch antenna ($\epsilon_r = 4$), the patch length would be equal to $7cm$ which is less than the dipole length for the same frequency condition.

In term of cost and design, the patch antenna is low cost and has ease of manufacturing compared to the dipole antenna [8].

3.3.1 Available power and antenna gain

The average power received at the antenna can be computed with expression (3.4):

$$P_{av} = SA \tag{3.4}$$

where A represent the antenna effective area that depends on the antenna type and S the power density. This power density can be computed with expression (3.5) from [2]:

$$S = P_{Tx}G_{Tx}G_{Rx}L_c\left(\frac{\lambda}{4}\pi r\right) \tag{3.5}$$

where P_{Tx} represent the transmitted power, G_{Tx} the transmitting antenna gain, G_{Rx} the received antenna gain, λ the wave length, L_c the path loth and r the distance between the emetting source and the antenna receiving the electromagnetic waves. Because the antenna of the RFEH circuit is usually designed to harvest ambient energy, the transmitted power P_{Tx} cannot be design to achieve high efficiency for the circuit. In order to increase the available power, the gain G_{Rx} need to increase through the design of the antenna.

This antenna gain can be computed with expression (3.6) from [16]:

$$G_{Rx} = e_{rad}e_{pol}e_{ap}D_{max} \tag{3.6}$$

with e_{rad} the total radiation efficiency, e_{pol} the polarization efficiency, e_{ap} the apparture efficiency and D_{max} the maximum available directivity. In order to get a high antenna gain for the circuit, the directivity of the antenna should be high. Because of their radiation pattern, patch antenna can usually achieve better directivity than dipole antenna, making them more suitable for low power applications

An example of comparaison between the performances of a patch antenna and dipole antenna can be found in [44]. In their paper, Alan Wong and Yang Tan present the measurement result of a patch antenna design for Wi-Fi application. The geometry and dimension of their antenna can be seen in Figure 3.7.

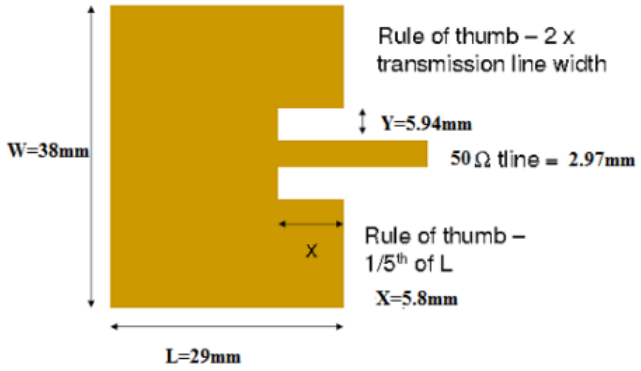


Figure 3.7: Representation of the patch antenna from [44] with the dimensions

The measurements they made in their paper were realised using the patch antenna of Figure 3.7, and a reference dipole antenna, by injecting a sinusoidal signal of $17dBm$ at $2.45GHz$ using the Hameg HM8135 RF Synthesizer. Their results show that the patch antenna has a maximum gain of $8dBi$ at the main lobe which is $6dB$ higher than the dipole antenna.

The radiation pattern of their patch antenna and the reference dipole antenna can be seen in Figure 3.8.

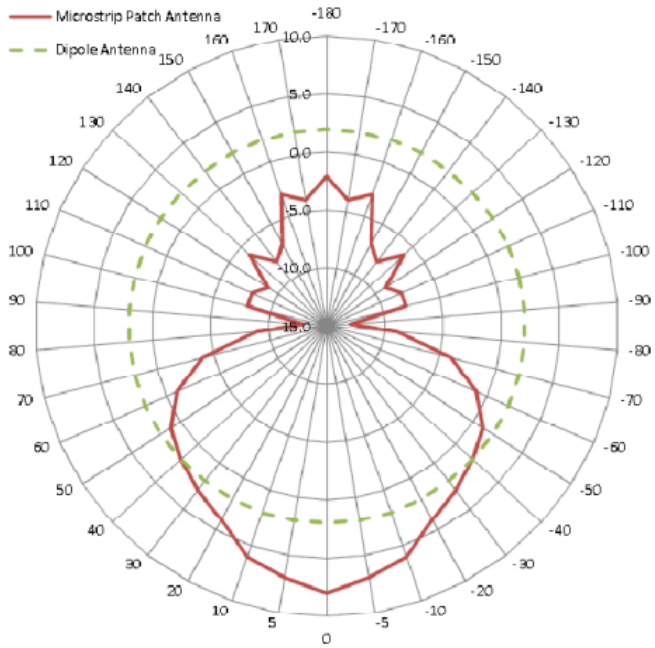


Figure 3.8: Polar plot of the radiation pattern of the patch antenna in red and dipole antenna in green from [44].

3.3.2 Antenna design in the litterature

For some application of RFEH circuit, if a specific frequency or a defined bandwitdh need to be achieved to harvest the RF energy, a specific geometric can be used to design the antenna of the RFEH circuit. The remaining part of this section shows 3 examples from the litterature where a specific design for the antenna was made to meet specifications.

Mamta Kurvey and Dr. Ashwini Kunte [24] present in their paper a RFEH circuit with a specific designed antenna, see Figure 3.9, to harvest RF energy at $1.8GHz$. The monopole antenna of Figure 3.9 is designed on FR4 substrate ($\epsilon_r = 4.4$) with a rectangular patch and microstrip line and can reach a gain of $4dBi$ at $1.8GHz$.

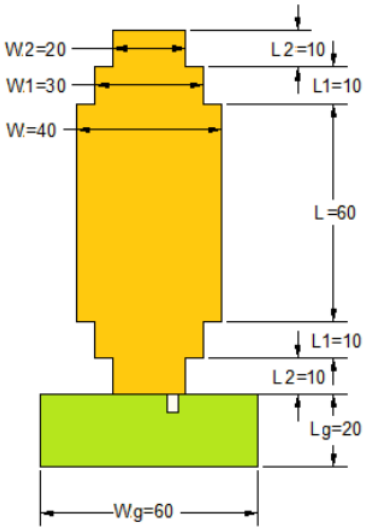


Figure 3.9: Representation of the monopole antenna working a $1.8GHz$ from [24]

Sanchari Sen Sarma and M. Jaleel Akhtar [35] present in their paper a high gain printed dual-band meandered dipole antenna on Figure 3.10. This dual band antenna is designed to harvest energy at $1.8GHz$ and $2.45GHz$. The specific design of the antenna was made that way in order to harvest energy a two frequencies while maintaining a small antenna size. The antenna is fabricated on a FR4 substrate with a permitivity of $\epsilon_r = 4.4$.

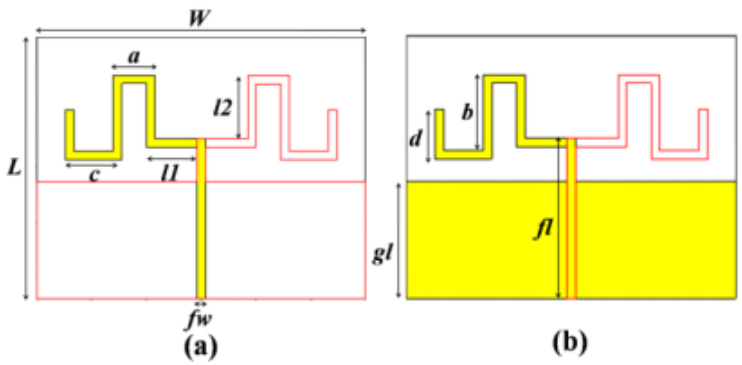


Figure 3.10: Representation of the dual-band antenna, front side (a) and back side (b), working a $1.8GHz$ and $2.45GHz$ from [35]

Sangkil Kim [17] presents in his paper a flexible loop antenna with incorporated balun designed to harvest far-field RF energy, see Figure 3.11. The antenna is designed to work at a frequency of $880MHz$ and is fed by a balun to convert the 50Ω unbalanced line into a 100Ω balanced differential line. The substrat material used to design the antenna is a 100μm thick polymer, Melinex 339, with a permitivity $\epsilon_r = 2.4$. At the operation frequency, the estimated average antenna gain is 2.5dBi

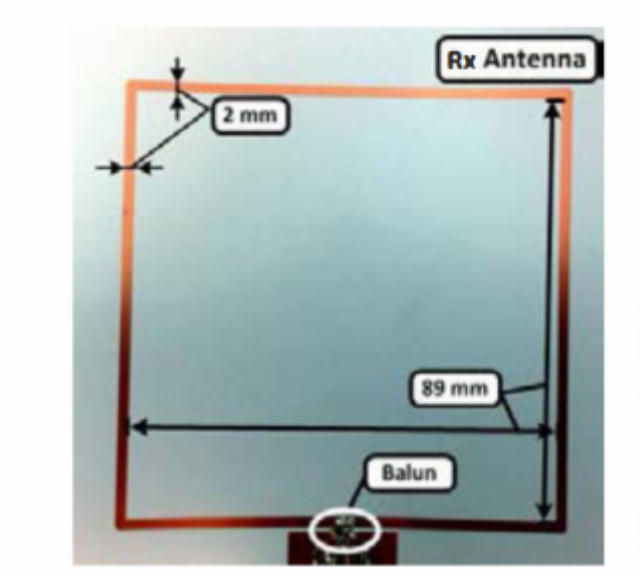


Figure 3.11: Representation of the quare loop antenna from [17] working at a frequency band of 80MHz (850-930MHz)

3.4 Matching network

One source of power losses in a conventional RFEH circuit is the power reflected into the circuit due to the mismatch between the antenna impedance and the input equivalent impedance of the rectifier [9]. In order to reduce the power loss due to reflection, a matching network is needed to perform impedance matching.

3.4.1 Impedance matching

In order to maximize the power delivered to a load by a electrical DC source, the impedance of that load need to be equal to the impedance of the source. Figure 3.12 represent a conventional DC voltage source V with a source impedance R_S and a load impedance R_L :

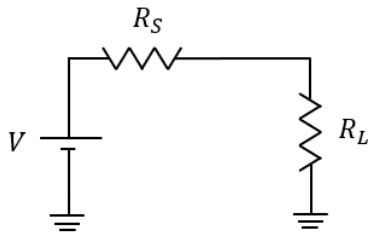


Figure 3.12: Electrical DC circuit with a source and a load

The power delivered to the load can be computed with the following equation:

$$P_{load} = \left(\frac{V}{R_S + R_L}\right)^2 R_L \tag{3.7}$$

To compute the value of the load resistor that maximize the power transfer from the voltage source to the load, the derivative of equation (3.7) is necessary:

$$\frac{dP_{load}}{dR_L} = V^2 \left(\frac{(R_S + R_L)^2 - 2R_L(R_S + R_L)}{(R_S + R_L)^4}\right) \tag{3.8}$$

by equalizing the derivative of the load power to zero, the value of the load resistor that maximize the power transfert to the load can be found [14]:

$$\frac{dP_{load}}{dR_L} = 0 \Longrightarrow R_S = R_L \tag{3.9}$$

The equality from equation (3.9) show that in order to transfert the largest amount of power from the source to the load, the resistor of the load needs to be equal to the resistor of the source. So in order to get the maximum power to the load, the impedance R_L needs to match the impedance R_S.

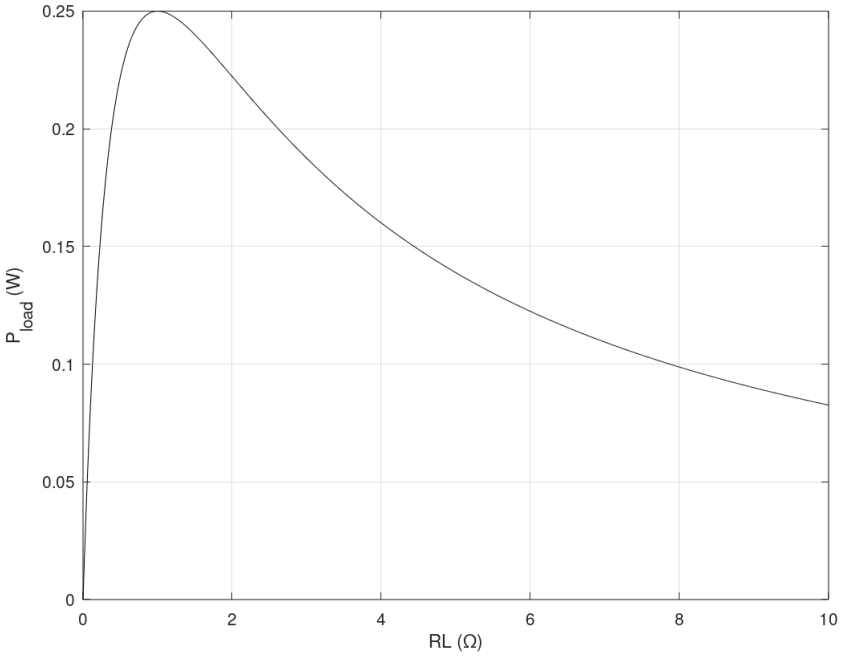


Figure 3.13: Represention of the power available at the load from Figure 3.12 in function of the load value from equation (3.7).

Figure 3.13 represent equation (3.7) with $V = 1(V)$ and $R_S = 1(\Omega)$. The maximum power at the load occurs when $R_S = R_L = 1(\Omega)$ has predicted by (3.9).

In the case of the conventional RFEH circuit of Figure 3.1, the impedance matching needs to be made between the real impedance $Z_{ant} = R_{ant}$ of the antenna and the complexe impedance seen at the input of the rectifier Z_{rec}. In order to do that, the matching network bloc needs to be tuned to ensure that the rectifier impedance seen from the antenna side is equal to the complex conjugate of that same antenna impedance:

$$Z_{rec} = conj\{Z_{ant}\} = Z_{ant}^{*} \tag{3.10}$$

Figure 3.14 represent a part of the conventional RFEH circuit where the matching network is tuned to perform impedance mathcing between the antenna and the rectifier.

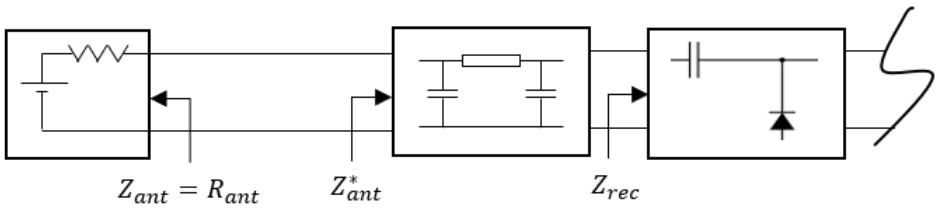


Figure 3.14: RFEH circuit with perfectly tuned matching network to perform impedance matching

3.4.2 Matching network design: L-type, T-type, π-type

In order to tune the matching network (MN) to perform impedance macthing, passive components need to be used: capacitors C and inductors L. There are 3 types of configuration to design the matching network using lumped elements: L-type (Figure 3.15), π-type (Figure 3.16) and T-type MN (Figure 3.17):

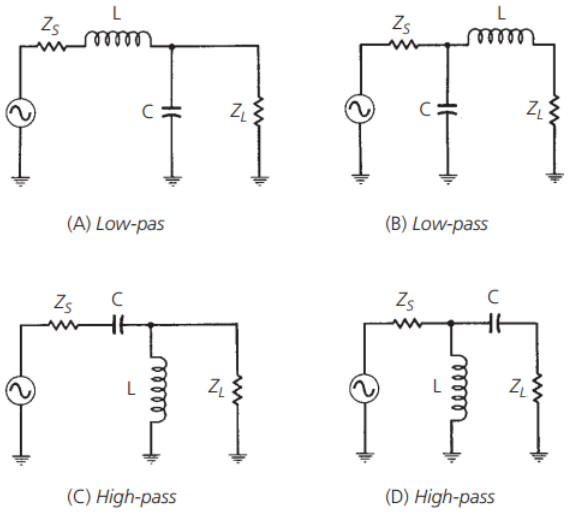


Figure 3.15: L-type MN configurations from [6]

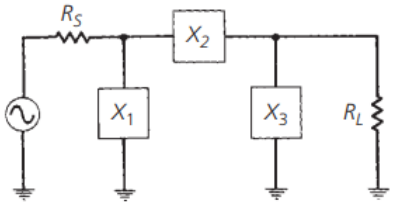


Figure 3.16: π-type MN configuration from [6]

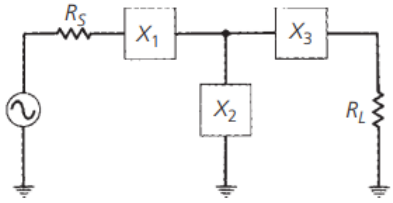


Figure 3.17: T-type MN configuration from [6]

The selection of one configuration compared to another depend on multiple factors: the input power received at the antenna by the RFEH circuit, the value of the impedances

that need to be matched together, the parasitic elements on the circuit that influence the value of the complex impedances, the frequency of the input signal from the antenna and the value of the desired Q factor of the MN that is defined has:

$$Q = \frac{f_c}{f_2 - f_1} \tag{3.11}$$

where f_c represent the center frequency and $f_2 - f_1$ the bandwidth selectivity of the MN [6][3][46]. If the RFEH circuit is design to harvest energy from a single source with a fixed known frequency, the Q factor of the macthing network should be high (with low bandwidth) in order to filter the parasitic frequencies from the surrounding and enhance the overall efficiency of the RFEH circuit. On the other hand, when dealing with RFEH circuit that harvest energy from multiple sources, the Q factor should be low (with high bandwidth) to ensure that the signals from the different sources are harvested and not filtered by the MN. This high Q factor in RFEH circuit increase the ouput voltage at the load and make the circuit more sensitive to different input frequencies [27].

If the L-type matching network design is choose for impedance matching, the Q factor is fixed by the real part of the source and load impedance. If R_S is defined has the real part of the source impedance and R_L the real part of the load impedance, then the Q factor is computed with the following relation [6]:

$$Q = \sqrt{\frac{R_L}{R_S} - 1} \tag{3.12}$$

Expression (3.12) show that if the L-type design is choose, the Q factor of the MN is not a design parameter but a fixed value imposed by the impedances that need to be match together.

If the π-type matching network design is choose for impedance matching, the Q factor can be computed with relation (3.13):

$$Q = \sqrt{\frac{R_H}{R} - 1} \tag{3.13}$$

where $R_H = max(R_L, R_S)$ and R a virtual resistor use for the design of the π-type MN (see Section 4.5 on MN design). Compared to the L-type MN, the π type topology allows the modification of the Q factor through the value of the virtual resistor to meet the design specification in term of MN bandwidth.

If the T-type matching network design is choose for impedance matching, the Q factor can also be tuned with the following expression (3.14):

$$Q = \sqrt{\frac{R}{R_{small}} - 1} \tag{3.14}$$

where $R_{small} = min(R_L, R_S)$ and R the virtual resistor.

3.4.3 Matching network design: distributed impedance matching

If the use of lumped element for the design of the MN is not allowed due to specification constraint, the distributed impedance matching method can be used. Indeed, at microwave frequencies, the parasitic influence of the lumped elements become more noticeable [23], so the distributed impedance matching is required. This method consist of doing some structural modification to the RFEH circuit by the means of microstrip lines, stubs, quarter wave transformer and balun to modify impedances. The distributed technique for impedance matching works for high Q factor has well has low Q factor [33]. Figure 3.18 represent an exemple of two microstrip patch antennas that use distributed impedance matching, transformer and stub, to perform impedance matching.

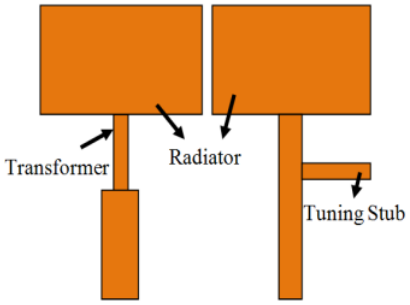


Figure 3.18: Representation of the implementation of the distributed impedance macthing technique with two microstrip patch antennas from [33]

Impedance transformer

There is two ways of performing impedance matching with impedance transformer in function of the desired bandwidth/Q factor and impedances to match: the single quarter wave transformer (high Q factor) and the multisection quarter wave transformer (low Q factor), see Figure 3.19.

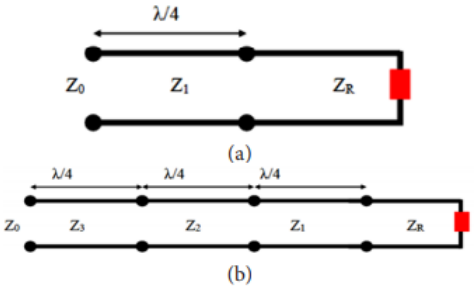


Figure 3.19: Representation of a single (a) and multisection (b) quarter wave transformer from [33]

When two real impedances need to be match together, Z_0 (feed line impedance) and Z_R (antenna impedance) in this exemple, the single quarter wave transformer is used

(circuit (a) of Figure 3.19). The equivalent input impedance Z_{in} seen at the input of the quarter wave transformer is computed has [12]:

$$Z_{in}(L) = Z_1 \left(\frac{Z_R + jZ_1 tan\left(\frac{2\pi}{\lambda}L\right)}{Z_1 + jZ_R tan\left(\frac{2\pi}{\lambda}L\right)} \right) \tag{3.15}$$

If the length of the transformer is exactly $\lambda/4$ then equation (3.15) can be written as:

$$Z_{in}(L = \lambda/4) = \frac{Z_1^2}{Z_R} \tag{3.16}$$

From equation (3.16), by selecting the proper characteristic impedance of the line Z_1 that compose the transformer, the matching between Z_0 and Z_R can be done:

$$Z_0 = Z_{in} = \frac{Z_1^2}{Z_R} \tag{3.17}$$

Equation (3.17) represent the condition that ensure the matching between two impedances Z_0 and Z_R for a single quarter wave transformer of caracteristic impedance Z_1.

When broadband (low Q factor) matching network is needed, the multisection quarter wave transformer is used (circuit (b) of Figure 3.19). This multisection transformer is composed of multiple single quarter wave transformer with different size that are put together in series. Figure 3.20 from [33] represent a multisection (two section) quarter wave transformer implementation.

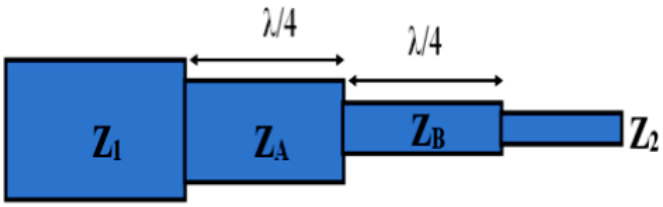


Figure 3.20: Representation of a two section quarter wave transformer of length $(2 \times \lambda/4)$ from [33]

To perform impedance matching between Z_1 and Z_2 on Figure 3.20, the caracteristic impedances of the multisection transformer need to be equal to:

$$Z_A = Z_1 \left(\frac{Z_2}{Z_1}\right)^{1/4} \tag{3.18}$$

$$Z_B = Z_1 \left(\frac{Z_2}{Z_1}\right)^{3/4} \tag{3.19}$$

Tapered line

Another impedance matching technique that allows broadband design for the MN is tapered line. An example of 3 different tapered lines can be see in Figure 3.21 from [33]. The geometry of the structures for the tapered lines of Figure 3.21, are designed to have continuous varying impedance along their length.

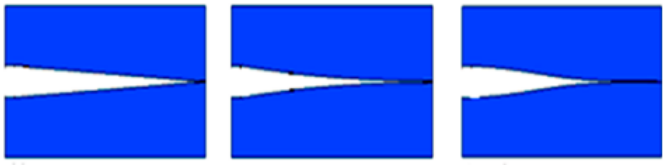


Figure 3.21: Representation of 3 different tapered lines structure (from left to right): exponential, triangular and Klopfenstein from [33]

To perform impedance matching with tapered line, the length is adjucted to meet the required impedance value to perform the matching between a load impedance and a line or source impedance.

The way the impedance along the length varies depend on the structure of the tapered line.

Stubs

Using stubs to perform impedance matching is one of the most used method to design matching network [33]. Figure 3.22 represent an AC electrical circuit with a line impedance Z_0 that is matched with to a load impedance Z_R thanks to the stub of length l (represented in red on the Figure).

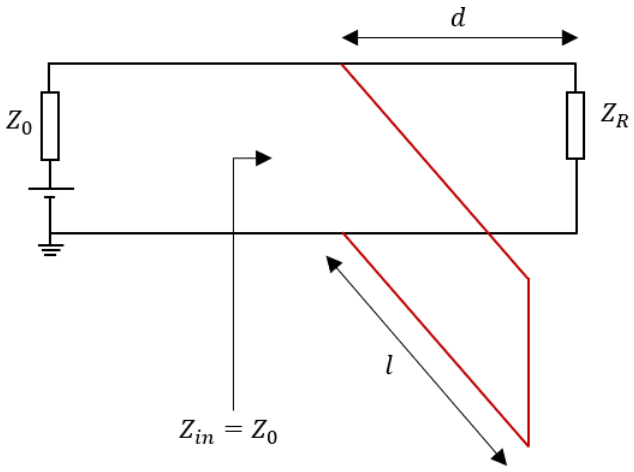


Figure 3.22: Schematic view of a stub performing MN impedance matching between a line impedance Z_0 and a load impedance Z_R

The length l of the stub is choose to cancel out the capacitive or inductive reactance of the load Z_R. In that way, the distance of connection d of the stub can be selected to

have an input impedance Z_{in} equal to the real line impedance Z_0 that we need to match to the complex load Z_R.

An exemple of stub impedance matching in a RFEH circuit working with GHz frequencies can be found in [41]. In this paper, Jérôme Tissier, Mohamed Latrach, and Zoya Popovic present a RFEH circuit design to harvest ambient RF signal at $1.84GHz$ with an incident power of $-20dBm$ and a load of $7k\Omega$. The stub circuit they implemented to perform the impedance matching with the 35Ω patch antenna and the load can be see in Figure 3.23.

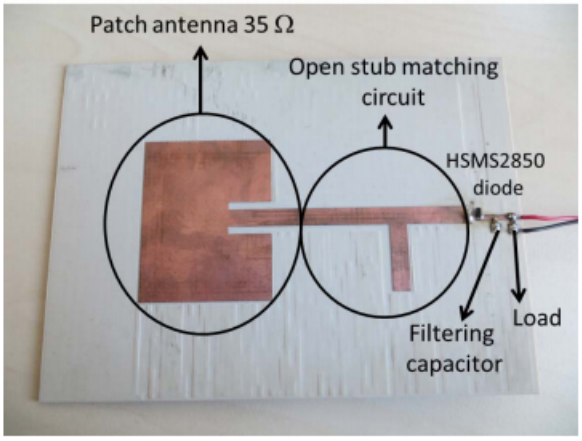


Figure 3.23: Illustration of the implemantation of a stub matching network from [41]

3.5 Rectifier: AC to DC conversion

The rectifier bloc of the conventional RFEH circuit of Figure 3.1 turns the AC signal from the Matching Network (MN) bloc into a DC signal to delivers eletrical energy into the load. The rectifier is usually made of non linear elements like diode and MOFFET from a defined CMOS technology. Due to those elements, the rectifier will dissipate power through heat.

To minimise this effect, special kind of diode, Schottky diode, are used. Those diode have low serie resistance and low junction capacitance for fast switching speed to work with microwave frequencies. They also have low threshold voltage (150-250 mV for the HSMS-285x series) to reduce the voltage drop and thus reduce the losses inside the rectifier [40][28]. For the CMOS implementation of the rectifier, diode connected MOSFET are used [42]. Those MOSFET were introduce to reduce even more the voltage drop compared to the diode type rectifier [25] and thus reduce the losses inside the rectifier while increasing the output voltage when the RFEH circuit works under low input power condition [45]. The diode connected MOSFET also provide a better resistance to temperature variation than the diode [21].

Multiple topologies are possible to implement the rectifier. In this section, the 2 most popular topologies are presented: the Greinacher topology and the Cross-Coupled Differential Drive (CCDD) topology.

3.5.1 Power conversion efficiency

The efficiency of a AC to DC rectifier is measued with the power conversion efficiency (PCE). This PCE is defined as the ratio between the ouput power and the input power of the rectifier:

$$PCE = \frac{P_{out.rec}}{P_{in.rec}} = \frac{P_{out.rec}}{P_{out.rec} + P_{losses}} \tag{3.20}$$

where $P_{out.rec}$ represent the DC ouput power of the rectifier, $P_{in.rec}$ the AC input power and P_{losses} the power losses inside the rectifier. When working under low input power condition, which is the case for most RFEH circuit, equation (3.20) can be approximated by [19]:

$$PCE \approx \frac{V_{out.rec}}{V_{out.rec} + V_{TO}} \approx \frac{V_{in.rec} - V_{TO}}{V_{in.rec}} \tag{3.21}$$

where $V_{out.rec}$ represent the DC ouput voltage of the rectifier, $V_{in.rec}$ the peak voltage amplitude of the AC input voltage of the rectifier and V_{TO} the turn on voltage of the diode inside the rectifier. This turn on voltage is approximated by the threshold voltage V_{th} if diode connected MOSFET are used to design the rectifier. This is why, in order to achieve high PCE, compensation techniques are used when the rectifier is design with CMOS techology [19][47].

3.5.2 Greinacher rectifier

The Greinacher topology for the rectifier can be seen in Figure 3.24. This topology is made out of two sub circuit: the Villard doubler and a peak detector. Both sub circuit

are composed of one capacitor and a non linear component symbolise by a diode. This diode symbol either represent a Schottky diode or a diode connected MOSFET.

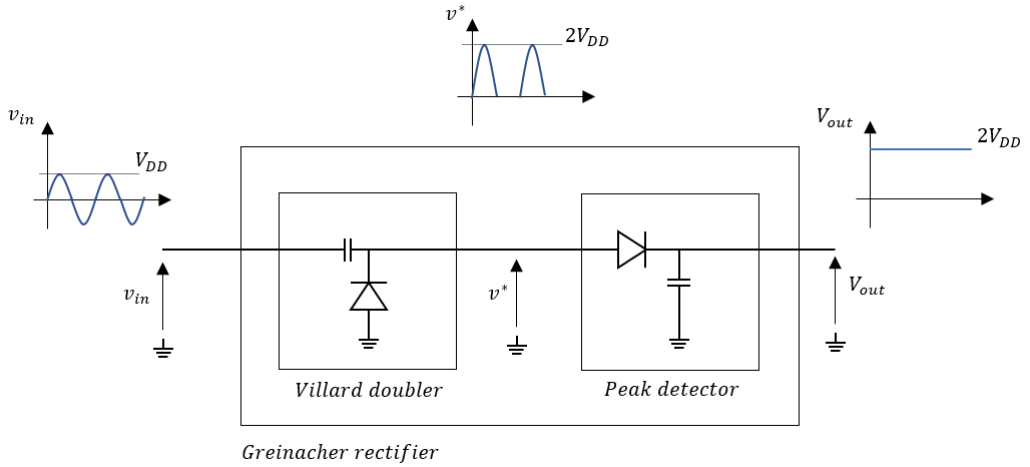


Figure 3.24: Representation of a Greinacher AC to DC rectifier

The Villard doubler inside the rectifier can also be called a voltage doubler. This voltage doubler inside the Greinacher topology works in two steps depending on the sign amplitude of the input signal v_{in}:

- negative half cycle ($v_{in} < 0$): the diode from the villard doubler is forward biased and the amplitude of the input voltage is equal to $v_{in} = -V_{DD}$. A current flows from the diode through the capacitor until the voltage across the capacitor is equal to $V_C = v^* - v_{in} = V_{DD}$.
- positive half cycle ($v_{in} > 0$): the diode from the Villard doubler is reverse biased and the amplitude of the input voltage is equal to $v_{in} = V_{DD}$. The voltage at the output of the Villard doubler is the addition of the input voltage v_{in} and the voltage across the capacitor (that was previously charged during the negative half cycle): $v^* = v_{in} + V_C = 2V_{DD}$.

The output signal of the Villard doubler, v^*, is an AC signal with only positive peaks that have twice the amplitude of the input signal v_{in}, see Figure 3.24.

The second sub circuit inside the Greinacher rectifier is a peak detector. This peak detector holds the highest point of the input signal that is feed to him on the capacitor [13], in this exemple: the peak amplitude of the signal v^*, $2V_{DD}$. The ouput voltage of the peak detector, and so the Greinacher rectifier, is the DC voltage across the charged capacitor of the peak detector bloc $V_{out} = 2V_{DD}$, see Figure 3.24.

The complete expression of the output voltage of the Greinacher rectifier (if the losses inside the diodes are taken into account) is:

$$V_{out} = 2V_{DD} - 2V_{TO} \tag{3.22}$$

where V_{TO} is the turn on voltage of the diodes that compose the rectifier: voltage drop of a Schottky diode or threshold voltage of a diode connected MOSFET. In expression (3.22), the voltage drop across the diodes is taken into account in the final value of the output voltage (the capacitors are considered ideal in this expression).

3.5.3 N-stage Greinacher/Cockcroft-Walton rectifier

In order to achieve higher output voltage at the load, N-stage rectifier topologies can be used. Figure 3.25 and 3.26 represent respectively a 2 stage Greinacher rectifier (also called Dickson rectifier in some papers) and a 2 stage Cockcroft-Walton rectifier.

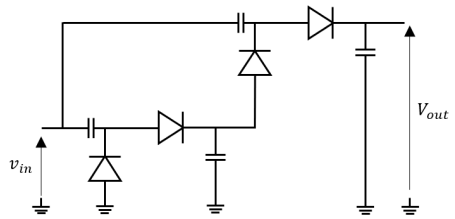


Figure 3.25: Two stage Greinacher rectifier

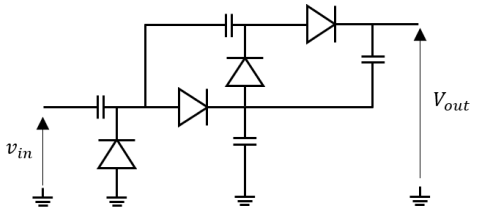


Figure 3.26: Two stage Cockcroft-Walton rectifier

Those two topologies are based on the same 1 stage Greinacher topology of Figure 3.24, the only difference between the two are the points of connection. The output voltage of an N-stage rectifier, Greinacher or Cockcroft-Walton, can be compute with expression (3.23):

$$V_{out} = 2N\left(V_{DD} - V_{TO}\right) \tag{3.23}$$

with N beeing the number of stage, V_{DD} the peak value of the input signal of the rectifier and V_{TO} the turn on voltage: voltage drop of a Schottky diode or threshold voltage of a diode connected MOSFET. If the number of stage increase inside the rectifier, the output voltage will also increase. On the other hand, more diodes are needed inside the rectifier which will cause more voltage drop due to the turn on voltage V_{TO} which mean more losses inside the rectifier. There is this trade off to take into account when designing multiple stage rectifier. When working under low input power, below $-10dBm$, one stage rectifier can achieve better PCE than multistage rectifier for the same output voltage [3]. Above 0 dBm multistage rectifier provide higher ouput voltage than the one stage rectifier topology.

Table 3.1 summarize the different AC to DC rectifier from the recent litterature that are used inside RFEH circuit for different input power, frequencies and topologies.

	[43] 2009 sim.	[15] 2013 meas.	[32] 2018 meas.	[31] 2018 meas.	[45] 2019 sim.
Technology	diode	diode: HSMS2852	diode: HSMS286k	diode: SMS7630	CMOS
Topology	Cockcroft-Walton	Greinacher	Greinacher	Greinacher	Greinacher
Number of stages	20	1	2	2	1
Frequency	2.4GHz	868MHz	866MHz	2.45GHz	2.45GHz
RF input power	-37dBm	-10dBm	-5.5dBm	-30dBm to 0dBm	-15dBm
PCE	NA	49.7%	NA	NA	82.85%
Ouput voltage	1.03V	0.705V	0.633V	27mV (@-20dBm)	1.62V
load	$200M\Omega$	$10k\Omega$	RFID tag	$100k\Omega$	$100k\Omega$

Table 3.1: Comparaison of the different rectifier performances inside RFEH circuit from the litterature.

3.5.4 CMOS cross-coupled differential-drive rectifier

Expression (3.21) from section 3.5.1 shows that in order to increase the PCE for a fixed RF input power, the turn on voltage V_{TO} of the non linear element that compose the rectifier need to decrease. CMOS implementation of an AC to DC rectifier can manage to reduce the turn on voltage better than a diode type rectifier by the means of static or dynamic V_{TO} cancellation mechanism [20].

The conductance of a MOSFET can be computed with the following expression [36]:

$$g = \mu C_{ox} \left(\frac{W}{L} \right) v_{OV} \tag{3.24}$$

where μ represent the mobility of the electrons or holes (depending on the MOSFET type), C_{ox} the oxyde capacitance, W and L the width and length of the MOSFET and v_{OV} the overdrive voltage. The cancellation techniques aim to increase the conductance of the MOSFET by increasing the overdrive voltage in expression (3.24). This can be done by increasing (for the NMOS) or decrasing (for the PMOS) the gate voltage of the transistor to compensate for the fixed threshold voltage:

$$v_{OV,nmos} = v_{GS} - V_{th,n} \tag{3.25}$$

$$v_{OV,pmos} = v_{SG} - |V_{th,p}| \tag{3.26}$$

Figure 3.27 represent a one stage Greinacher rectifier from [22] implemented with diode connected MOSFETs that uses Self-V_{th} Cancellation (SVC) technique to perform threshold voltage compensation. The NMOS has his gate connected to the ouput of the rectifier V_{DC}, the PMOS has his gate connected to the reference voltage (ground in this example). By performing this type of connections for the gate of the transistors, the effective threshold voltage of the transistors inside the rectifier are decreased according to expressions (3.25) for the NMOS and (3.26) for the PMOS. This compensation method is refered as static compensation because the gate of the transistors are biased with DC voltages.

If the threshold voltage is over compensated due to execive biasing, the effective threshold voltage of the diode connected MOSFET becomes negative. This as the effect of increasing the reverse leakage current flowing inside the diode connected MOSFET which lead to a decrease of charges that are transmitted to the ouput load, and so, a decrease of PCE.

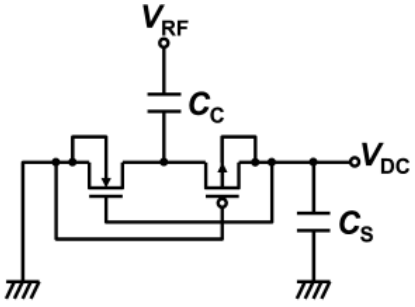


Figure 3.27: Representation of a Greinacher rectifier implemented with diode-connected MOSFET performing static V_{th} compensation from [20]

To limit the effect of reverse leakage current inside the rectifier, dynamic V_{th} cancellation techniques can be used. Figure 3.28 show the topology of a Cross-Coupled Differential-Drive (CCDD) rectifier implemented with MOSFET from [20] that performs dynamic V_{th} compensation.

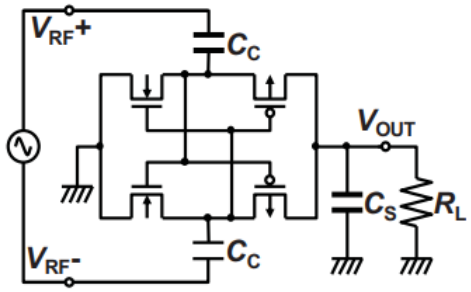


Figure 3.28: Representation of a CCDD rectifier implemented with diode-connected MOSFET performing dynamic V_{th} compensation from [20]

When $V_{RF}+$ is negative and $V_{RF}-$ positive, the gate of the NMOS transistor from the upper part of the CCDD circuit is biased with positive voltage and the compensation is made, this allow the transfert and accumulation of charges on the capacitor C_c from the upper part of the circuit. The PMOS from the upper part is turn off due to his gate connection with the NMOS. The PMOS beeing turn off, the effect of reverse leakage current is reduced. For the lower part of the CCDD circuit, the NMOS is turn off and his gate voltage is negative, reducing the reverse leakage current. The PMOS is biased due to the negative voltage at the gate and the V_{th} compensation is made. This allow the transfert of charges from the lower capacitor C_c of the rectifier to the load R_L.

When $V_{RF}+$ is positive and $V_{RF}-$ negative, the same phenomenon occurs with the 4 MOSFET of the CCDD rectifier but with opposit effects. The NMOS from the upper part is now turn off with no V_{th} compensation and the PMOS is turn on due to the negative voltage $V_{RF}-$. The charges that were accumulated on the upper capacitor C_c are transfered through the upper PMOS to the output load. For the lower part of the CCDD rectifier, charges are flowing though the turn on NMOS to the lower capacitor C_c and the PMOS is turn off.

Figure 3.29 from [20] shows the volution of the PCE in function of the RF input power for multiple rectifier topologies at a frequency $f_{RF} = 953MHz$ and for a load $R_L = 10k\Omega$. At very low input power, the CCDD rectifier, the red curve of Figure 3.29, that performs dynamic V_{th} compensation show a better PCE than the SVC rectifier that uses static V_{th} compensation.

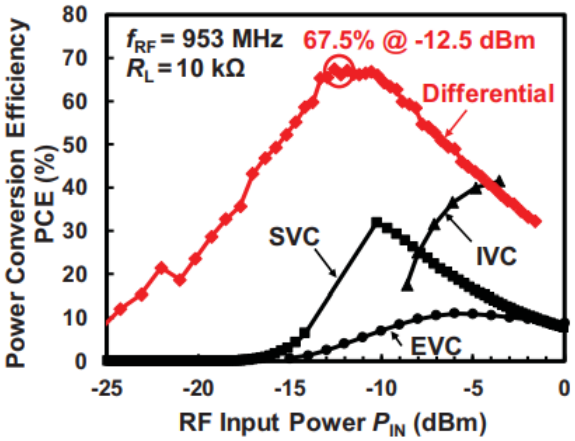


Figure 3.29: Represention of the evolution of the PCE in function of the RF input power for different rectifier topologies from [20].

Table 3.2 summarize the different AC to DC rectifier implemented with CMOS technology from the recent litterature that are used inside RFEH circuit for different input power and frequencies.

	[37] 2015 sim.	[34] 2016 sim.	[26] 2018 sim.	[7] 2019 meas.	[20] 2019 meas.
Technology	CMOS: 0.13um	CMOS: 130nm	CMOS: 130nm	CMOS: 0.18um	CMOS: 0.18um
Topology	CCDD	CCDD	CCDD	CCDD	CCDD
Number of stage	6	1	1	7	1
Frequency	2.45GHz	2.4GHz	900MHz	900MHz	953MHz
RF input power	-24dBm	-20dBm	-15dBm	-6dBm	-12.5dBm
PCE	NA	55% (PHE)	66.28%	42.3%	67.5%
Ouput voltage	1.5V	0.267V	0.4V	≈1V	0.62V
load	50M	13k	10k	10k	10k

Table 3.2: Comparaison of the different CCDD rectifier performenaces inside RFEH circuit from the litterature.

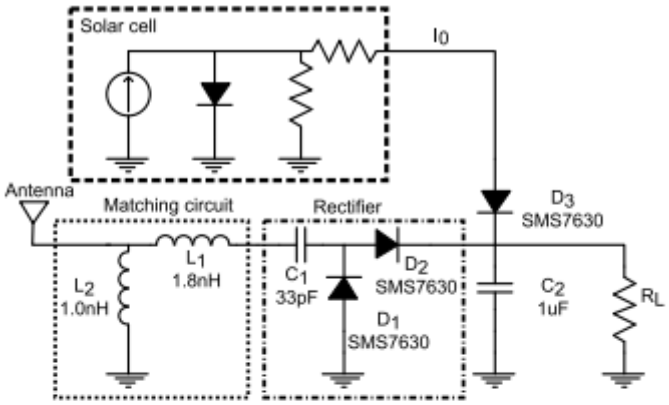
3.6 Hybrib solar and radio frequency energy harvesting

Most of the hybrid circuits in the litterature that combine solar and RF energy harvesting are designed to combine effectively the energy from the 2 sources to feed a load or a Power Magagment Unit (PMU). This can be done in two ways:

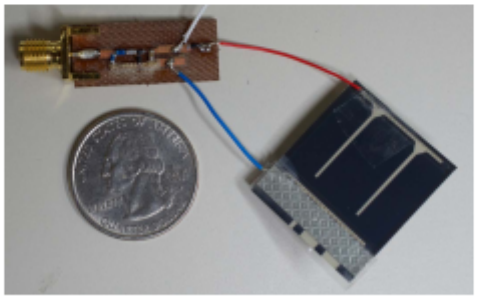
- case $n°1$: The hybrid circuit is divided into two sub circuits where each part is harvesting one specific source of energy, solar or RF.
- case $n°2$: The classical topology of the RFEH circuit of Figure 3.1 is modified by the incorporation of the solar cell to perform hybrid energy harvesting.

3.6.1 Case n°1: sub circuit implementation

An exemple of a sub circuit implementation for hybrid energy harvesting can be found in the paper wrote by Jo Bito[4]. The circuit of Figure 3.30 is design to harvest ambient RF energy at $2.45GHz$ and solar energy.



(a)



(b)

Figure 3.30: Representation of the schematic of the hybrid circuit (a) and a image of the implemented circuit (b) from [4].

The harvested solar and RF energy have different path inside the hybrid circuit to drive the ouput PMU. The solar cell, represented here be a single-diode model, is connected to the ouput node through the diode D3. The RF signal, goes through the L-type matching network and Greinacher rectifier, implemented by 2 Schokkty diode SMS7630, before reaching the load. The purpore of the hybrid circuit is to drive the bq25504 IC PMU who requires a input voltage of 330mV and a power of 15μW to perform the cold start.

The solar cell choose for the design of the prototype was the Power Film MP3-25 solar cell with the dimensions 114mm×24mm an open voltage $V_{oc} = 4.1V$ and a short circuit current $I_{sc} = 48mA$. In order to respect the specifications, only one fifth of the solar cell length was used to realised the prototype, see picture (b) of Figure 3.30.

3.6.2 Case n°2: solar cell incorporation

An exemple of an hybrid energy harvesting system incorporating the solar cell inside the RFEH circuit topology can be found in the paper wrote by Kyriaki Niotaki[29]. The circuit they implemented can be see in Figure 3.31:

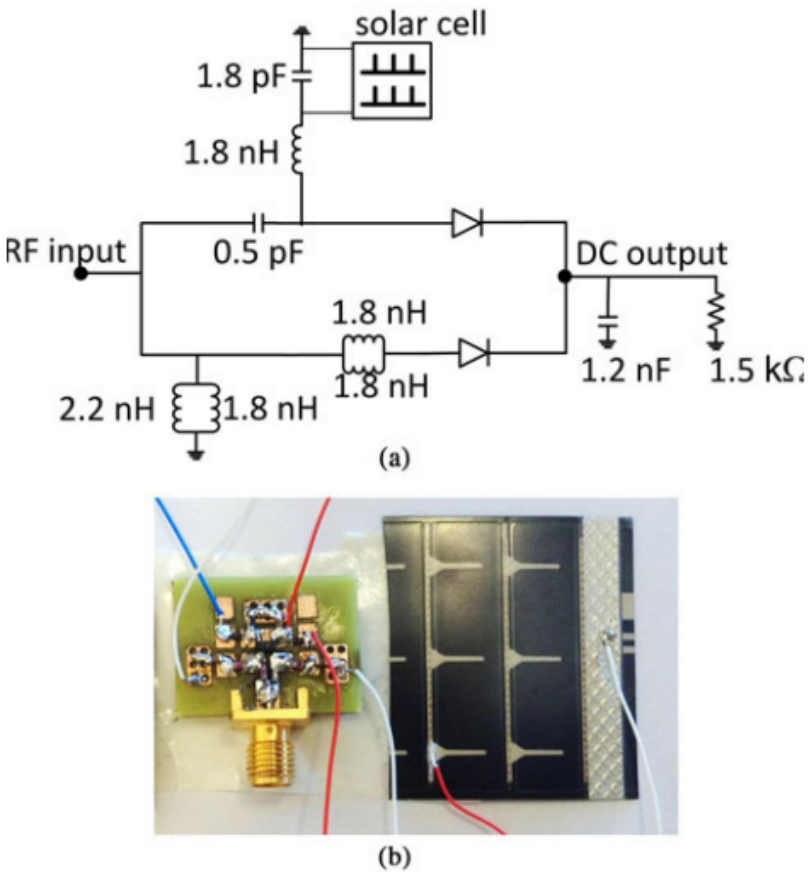


Figure 3.31: Representation of the schematic of the RFEH circuit incorporating a solar cell (a) and a image of the implemented circuit (b) from [29].

The proposed circuit combines the RF energy and solar energy before delivering them to the load. A second branch to harvest the RF energy alone is designed in case there is a change in the irradiance of the solar cell that could provoque mismatch. Each one of the branches has a proper matching network.

The SIW cavity-backed slot antenna of the circuit is made on in FR4 substrat of 1.6mm height with a dielectric constant $\epsilon_r = 4.4$ and is designed to harvest RF energy at $2.45GHz$. The a-Si solar cell is directly incorporated on top of the antenna structure.

Chapter 4

RFEH circuit design

In this section, the proposed RFEH circuit with incorporated solar cell is presented. At first, the composition of each bloc that compose the proposed circuit is describe. After that, each bloc is designed with the proper equations to be able to simulate the proposed circuit with ADS simulations.
The modelisation of the solar cell from *3gsolar* is also presented.

4.1 Proposed RFEH circuit

The proposed RFEH circuit with the incorporation of a solar cell can be seen in Figure 4.1. The circuit is composed of an antenna with a 50Ω impedance, a π-type matching network (MN), a Greinacher based rectifier with Schottky diode, a power maganement unit (PMU) and the solar cell.

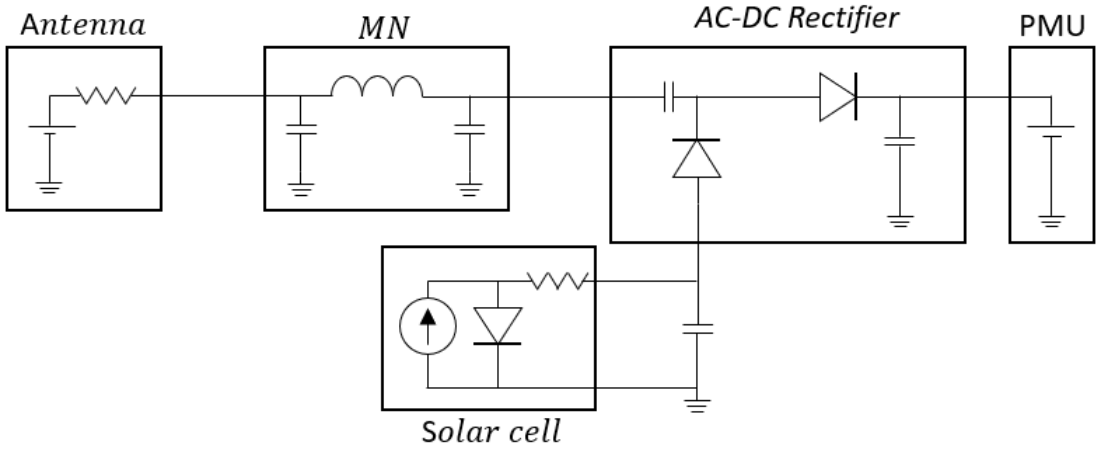


Figure 4.1: Representation of the proposed RFEH circuit with the incorporation of the solar cell

Antenna

The antenna choose here to harvest the RF signal is a patch antenna with a 50Ω real impedance. As explain in the state of art in section 3.3, the patch antenna is more suitable than the dipole antenna when it comes to low input power condition. It is also easier to manufacture than the dipole antenna and respect the dimension imposed by the specification for the overall circuit.

Matching network

A π-type Matching Network (MN) is choose to perform impedance matching between the antenna impedance and the equivalent input impedance seen at the rectifier. At very low input power, the effect of parasitic capacitor become important and can't be neglected when designing the matching network. For that reason, the π-type MN is choose over the L-type in order to have flexibility on the design to allow the matching at $2.45GHz$ despite the parasitic effects.

AC-DC rectifier

For the rectifier bloc of the RFEH circuit, a one stage Greinacher rectifier is choose to perform the AC to DC conversion of the signal coming from the antenna. The rectifier is design with Schottky diode from the HSMS-286x series. Those diodes are choose because of their low voltage drop during forward biased operation: 250-350mV and low junction capacitor: 0.18pF.

Solar cell

The solar cell choose to perform the simulation is the dye sensitized solar cell from *3gsolar*[1]. This solar cell was designed for indoor condition and can provide an ouput voltage of $0.439V$ with an input power as low as 50lux. This solar cell was choose for its ability to provide voltage under low irradiance (indoor condition) and for its samll dimensions, see Figure 4.2.

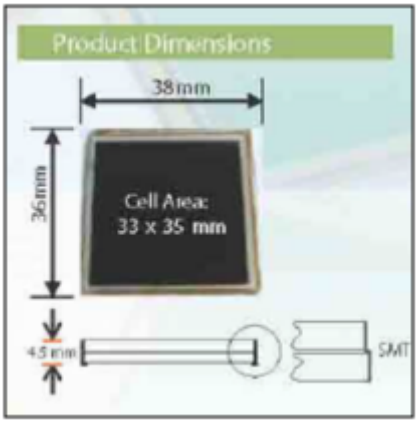


Figure 4.2: Representation of the Solar cell from *3gsolar* and its dimensions.

Power managment unit

The Power Managment Unit (PMU) used to regulate the ouput power of the rectifier is the AEM30940 from e-peas[10]. This PMU performs open circuit voltage sensing every 0.33s for MPPT and can supply low voltages 1.2V or 1.8V or high voltages 4.1V to a specific load or battery at the end of the RFEH circuit.
To be able to perform the cold start of the PMU, the output of the rectifier needs to provide at least 380mV of input voltage to the PMU and 3μW of power. During the voltage regulation, the PMU can sustain operation with an input voltage of 50mV.

4.2 Power management unit model

The role of the PMU inside the RFEH circuit is to perform voltage regulation to provide a constant DC voltage to a load or a battery even if the level of RF input power varies at the antenna.
To perform DC-DC conversion and regulate the output voltage at the load or the battery, the PMU fixes the output voltage of the rectifier as a ratio of the open circuit voltage:

$$V_{out.rec} = \gamma V_{oc.rec} \tag{4.1}$$

where γ represent the open circuit voltage ratio of the PMU, 50%,65% and 80%, and $V_{oc.rec}$ the open circuit voltage at the ouput of the rectifier when no load or PMU is connected.

For that reason, the PMU can be modelised by a constant DC voltage source to perform ADS or SPICE simulations, see Figure 4.3.

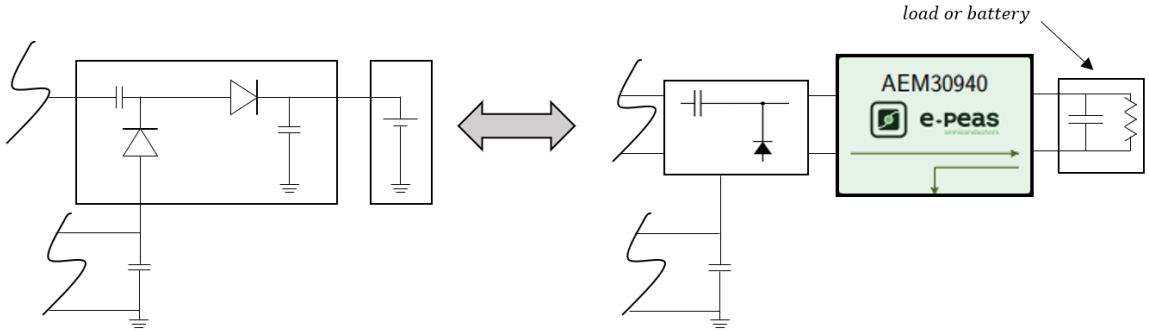


Figure 4.3: Representation of a part of the RFEH circuit and its equivalent circuit with the PMU and the load.

During the simulations, the voltage of the source that represent the PMU and the load can be fixed as the ratio of the open circuit votlage with the following expression:

$$V_{sc,DC} = 2\gamma V_{in.rec} + \gamma \left(V_{PV} - 2V_{TO}\right) \tag{4.2}$$

where $V_{in.rec}$ represent the maximum peak value of the AC input signal of the rectifier, V_{PV} the voltage of the solar cell and V_{TO} the turn on voltage of the Schokkty diodes inside the rectifier (150-250mV for the HSMS-286x serie).
The demonstration of expression (4.2) can be found in section 4.6 concerning the design of the rectifier with the incorpotation of the solac cell.

4.3 Antenna model

To perform transcient or AC analysis based on SPICE or ADS simulation, an equivalent model of the antenna is necessary. As explained in the state of art, the antenna converts the electromagnetic waves from the RF source into an electrical AC signal. So to represent the AC signal generated be the antenna, a AC source is used here to perform the simulations:

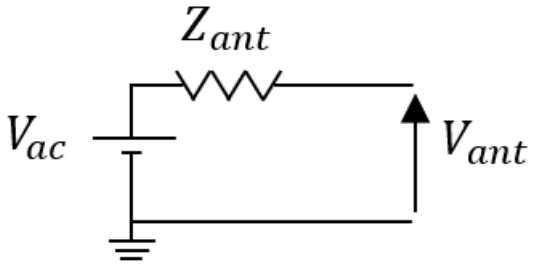


Figure 4.4: Representation of the equivalent model of the antenna used for ADS simulation.

Figure 4.4 represent the electrical equivalent model of the antenna used in the RFEH circuit design of this work. The AC signal generated by the AC source is equal to:

$$V_{ac} = (V_{in.RF})sin(\omega t) + V_{DC} \tag{4.3}$$

where $\omega = 2\pi f$ with $f = 2.45gHz$, $V_{in.RF}$ the maximum aplitude of the RF input signal and V_{DC} the DC component of the signal (equal to zero for the simulations).

When the Power Harvest Efficiency (PHE) of the RFEH circuit is computed through ADS simulation, this voltage source is replaced by a power source with the ADS software. In that case, the input variable is not the amplitude voltage $V_{in.RF}$ anymore but the input power of the RFEH circuit: $P_{in.RF}$.

4.4 Solar cell model

To perform simulation of a solar cell inside a circuit, a model need to be used. There a two popular model that use lumped element for representing a solar cell as an equivalent circuit: the single- and double-diode model. The model that is used here to design the solar cell is the single-diode model. This model consist of a current source that generates a photocurrent, a shunt diode and 2 resistors, see Figure 4.5:

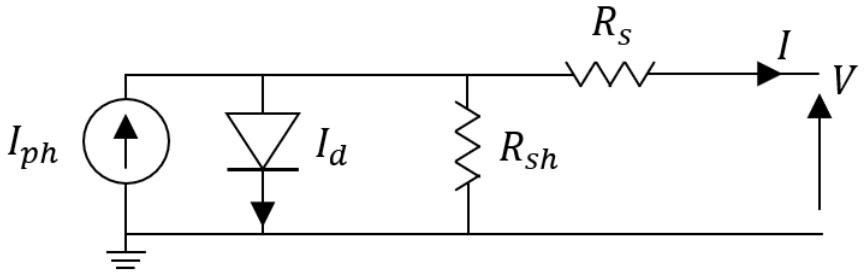


Figure 4.5: Representation of the single-diode model for the equivalent circuit of the solar cell.

The value of the lumped elements that compose the equivalent circuit of Figure 4.5 can be find either with the data from the I-V curve of the solar cell or with the electrical caracteristic from the data sheet. The lumped element of the equivalent circuit for the *3gsolar* cell are model here with the caracteristic of the solar cell that are resume in Table 4.1.

	50 lux	100 lux	200 lux	500 lux	1000 lux
Pmpp (uW)	17	41	93	257	564
Voc (mV)	439	479	504	542	564
Isc (uA)	59	128	263	662	1385
Vmpp (mV)	335	373	401	444	452
Impp (uA)	52	113	236	592	1249

Table 4.1: Elecrical specifications of the *3gsolar cell* from [1]

There are 4 parameters that need to be find with the data of table 4.1 to design the equivalent circuit of the solar cell: the value of the serie resistor R_s, the value of the shunt resistor R_{sh}, the saturation current of the shunt diode I_{sat} and the quality factor of the diode n. The method followed here to extract those parameters is the one from Wook Kim and Woojin Choi [18]. Their paper propose a method to extract those 4 coefficients with experimental measuerement of the I-V curve of the solar cell. Here, the parameters of table 4.1 are used.

Ideality factor: n

The ideality factor n of a diode, represent the degree of diavation from an ideal diode caracteristic. Its value lies between 1 and 2, $n = 1$ beeing the ideal case. To compute this factor with available data, the current expression of a forward biased diode is used. The current flowing through the diode from the equivalent circuit can be calculated with expression (4.4):

$$I_d = I_{sat}\left(exp\left(\frac{q(V + IR_s)}{N_s nkT}\right) - 1\right) = I_{sat}\left(exp\left(\frac{qV_D}{N_s nkT}\right) - 1\right) \tag{4.4}$$

where I_{sat} represent the reverse saturation current, V_D the voltage across the diode of the equivalent model, q the electron charge, N_s the number of cells in series that compose the overall solar cell, T the absolute temperature and k the Boltzmann's constant. The -1 inside equation (4.4) is neglected to compute the ideality factor to facilitate the calculation. By taking the natural logarithm of expression (4.4) (with the -1 simplification), the expression of the ideality factor can be computed:

$$ln(I_d) = ln(I_{sat}) + \frac{qV_D}{N_s nkT} \tag{4.5}$$

$$\Delta ln(I_d) = \frac{q\Delta V_D}{N_s nkT} \tag{4.6}$$

$$n = \frac{q}{kTN_s}\frac{\Delta V_D}{\Delta ln(I_d)} \tag{4.7}$$

The ideality factor can be computed with expression (4.7) by taking the maximum value of the slope $(\Delta V_D/\Delta ln(I_d))$ of the natural logarithm of the I-V curve. Figure 4.6 from [16] display an example of the maximum slope of typical $ln(I_d)$ curve available through measurement.

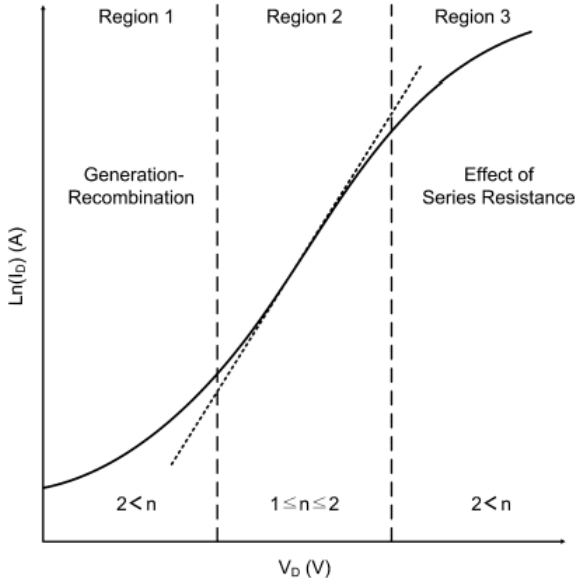


Figure 4.6: Evolution of the ideality factor in function of the voltage across the diode from the solar cell model[18].

Since the data of the I-V curve from the 3gsolar cell are not available for computations, the average ideality factor is computed here with equation (4.8) from [5], who uses the open circuit voltage of the solar cell and the short circuit current for different irradiances to estimate the factor:

$$n = \frac{q}{kTN_s}\left(\frac{V_{oc,1000lux} - V_{oc,50lux}}{ln(I_{sc,1000lux}) - ln(I_{sc,50lux})}\right) \tag{4.8}$$

With the data from table 4.1, the ideality factor is computed as follow, with $N_s = 1$ for the *3gsolar* cell:

$$n = \frac{1.602e^{-19}}{(1.381e^{-23})(298.15)}\left(\frac{0.564 - 0.439}{ln(1385e^{-6}) - ln(59e^{-6})}\right) = 1.31 \tag{4.9}$$

Simulations of an ideal equivalent model for the solar cell were made and it was found that the value $n = 1.31$ computed with expression (4.9) is overvalued. SPICE simulations show that an ideal factor of $n = 1$ presents better result in term of simulated I-V curve of the *3gsolar* cell. For the following computation of parameters, the value of $n = 1$ for the ideality factor is used.

Reverse saturation current: I_{sat}

The value of the reverse saturation current of a classical diode his fixed by the manufacturing condition. The diode inside the solar cell model has also a unique value of reverse saturation current that is not influence by the reverse bias voltage. This saturation current can be computed by performing a kirchhoff current analysis on the node at the input of the current source from the equivalent model of the solar cell:

$$I = I_{ph} - I_d - I_{sh} \tag{4.10}$$

where I represent the ouput current of the solar cell model, I_{ph} the photocurrent, I_d the diode current and I_{sh} the current flowing through the shunt resistor R_{sh}. Be isolating the diode current I_d and using expression (4.4) the saturation current can be computed:

$$I_{sat} = \frac{I_{ph} - I - \left(\frac{V + IR_s}{R_{sh}}\right)}{exp\left(\frac{q(V + IR_s)}{N_s nkT}\right) - 1} \tag{4.11}$$

Under open circuit condition, the ouput current of the solar cell model I is zero and the value of the shunt resistor R_{sh} can be considered infinit. With those consideration, expression (4.11) can be written as:

$$I_{sat} = \frac{I_{ph}}{exp\left(\frac{qV}{N_s nkT}\right) - 1} \tag{4.12}$$

The value of the saturation current for the equivalent circuit of the solar cell is computed with expression (4.12) and with the data from table 4.1 with a ideality factor $n = 1$:

$$I_{sat} = \frac{I_{sc}}{exp\left(\frac{qV_{oc}}{kT}\right) - 1} \tag{4.13}$$

Table 4.2 represent the value of the saturation current for the different value of open circuit voltage V_{oc} and short circuit current I_{sc} of the *3gsolar* cell:

	50 lux	100 lux	200 lux	500 lux	1000 lux
V_{oc}(mV)	439	479	504	542	564
I_{sc}(uA)	59	128	263	662	1385
I_{sat}(pA)	2.254	1.031	0.801	0.459	0.409

Table 4.2: Table that regroups the saturation current I_{sat} computed with expression (4.13) for different illuminatoions.

Since the saturation is a fixed value of the solar cell equivalent model, the value used inside the final equivalent circuit for the simulation of the RFEH circuit is the mean value of the saturation currents from table 4.2 for all illuminations:

$$I_{sat} = 0.9909pA \approx 1pA \tag{4.14}$$

Serie resistor: R_s

Once the ideality factor and the saturation current are knowed, the ideal I-V curves ($R_s = 0$ and $R_{sh} = \infty$) for different irradiances can be plot, see Figure 4.7. To plot the ideal curves, the equivalent model of the solar cell was simulated on SPICE with the parameters from table 4.11 and a voltage source was swept from 0 to 600mV for 4 different photocurrents: $662uA$, $263uA$, $128uA$ and $59uA$. The difference between the ideal I-V curves (Figure 4.7) and the measured I-V curves from *3gsolar* (Figure 4.8) for a fixed output current I is used to compute the serie resistor according to equation (4.15):

$$R_s = \frac{V_{ideal} - V_{data}}{I} \tag{4.15}$$

The current choose to extract the ideal voltage and the voltage from the *3gsolar* measurement is $I = 500uA$. From Figure 4.8, the voltage V_{data} corresponding to a current value of $500uA$ is extracted for an irradiance of $500lux$: $V_{data} \approx 500mV$. The same can be done with the I-V curves from the SPICE simulation: $V_{ideal} = 510mV$. The ratio between the diffence in voltages and the current give the value of the serie resistor:

$$R_s = \frac{(510e^{-3}) - (500e^{-3})}{500e^{-6}} = 10\Omega \tag{4.16}$$

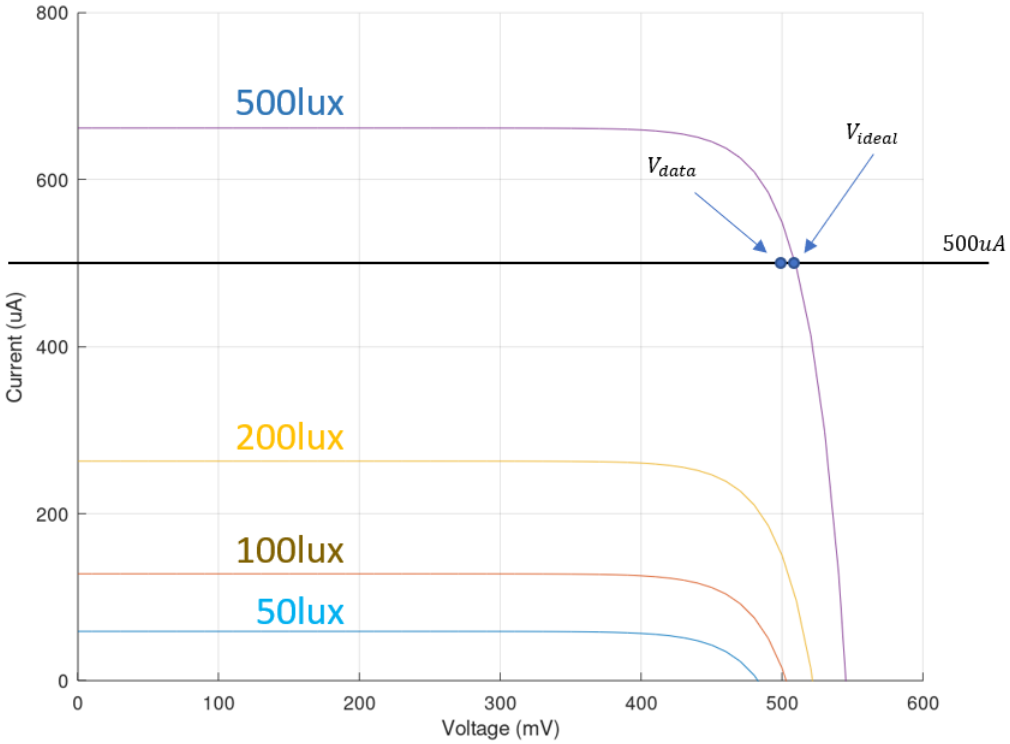


Figure 4.7: Ideal I-V curve simulated with SPICE of the *3gsolar* cell with highlighted voltage V_{data} from the real I-V of Figure 4.8.

In Figure 4.7, the difference between the ideal voltage V_{ideal} and the voltage extracted from the *3gsolar* curves V_{data} can be see for the selected current $I = 500uA$. The difference between the two voltages is due to the parasitic serie resistor R_s.

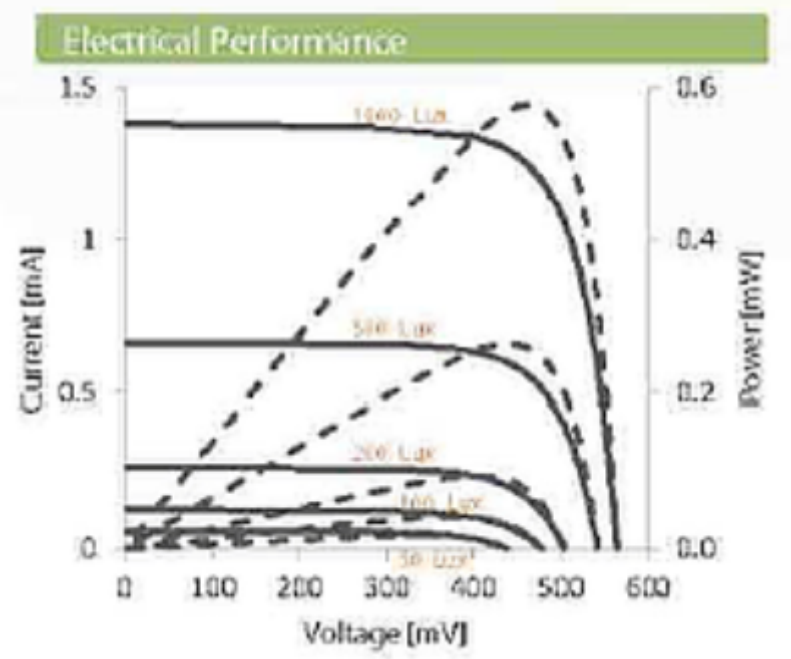


Figure 4.8: I-V curve of the *3gsolar* cell from the data sheet.

The procedure describe above for the compution of the serie resistor can be done for other level of irradiances (and thus other selected current). The irradiance of $500lux$ and the $500uA$ current were choose in order to get an accurate SPICE model of the *3gsolar* cell with the equivalent model.

Shunt resistor: R_{sh}

The shunt resistor of the equivalent model can be found with a procedure similar to the one used with the serie resistor R_s. This time, a fixed voltage is choose and the difference between the ideal current I_{ideal} (found with the fixed voltage and defined irradiance) and a current from the *3gsolar* curves I_{data} is done to compute the shunt resistor:

$$R_{sh} = \frac{V_{ideal}}{I_{ideal} - I_{data}} \tag{4.17}$$

However, SPICE simulations show that in order to achieve simulated I-V curves similar to the one from *3gsolar* (Figure 4.8) the shunt resistor need to be considered infinite:

$$R_{sh} = \infty \tag{4.18}$$

The final equivalent circuit of the solar cell does not have a shunt resistor.

Equivalent final model of the solar cell

The value of the 4 parameters needed to design the equivalent model of the solar cell based on the data of table 4.1 are summarize in table 4.3:

n	I_{sat}	R_s	R_{sh}
1	0.991pA	10Ω	∞

Table 4.3: Parameters of the equivalent single-diode model for the *3gsolar* cell.

Figure 4.9 and 4.10 represent repectively the SPICE simulation of the solar cell with the parameters of table 4.3 and the I-V curves extracted with that same model.

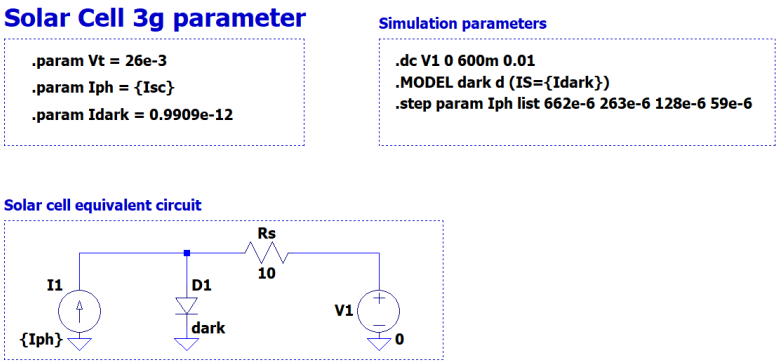


Figure 4.9: Equivalent circuit of the solar cell simulated on SPICE to plot the I-V curves of Figure 4.10.

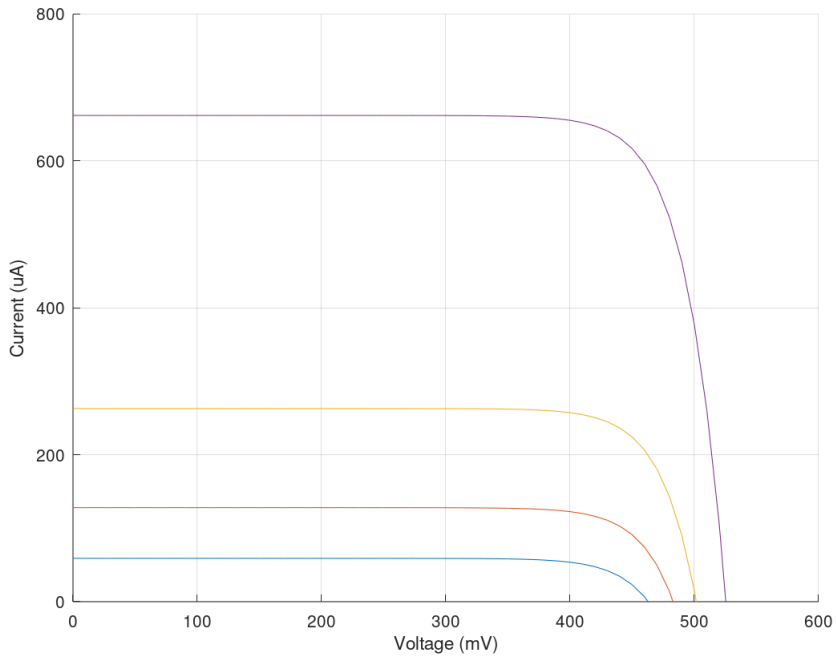


Figure 4.10: I-V curves simulated on SPICE with the single-diode model of the solar cell.

4.5 Matching Network design

The design of the π-type matching network is a crucial part of the RFEH circuit design to reduce the losses due to reflection. The procedure followed here to design the MN is the one useb by Pengcheng Xu in [46] which is a method inspired from [6] that uses a virtual resistor R_{vir} to design the MN. To compute the value of the lumped elements that compose the MN: L, C_1 and C_2, a equivalent circuit for the π-type MN is used with the presence of a virtual resistor R_{vir}, see Figure 4.11.

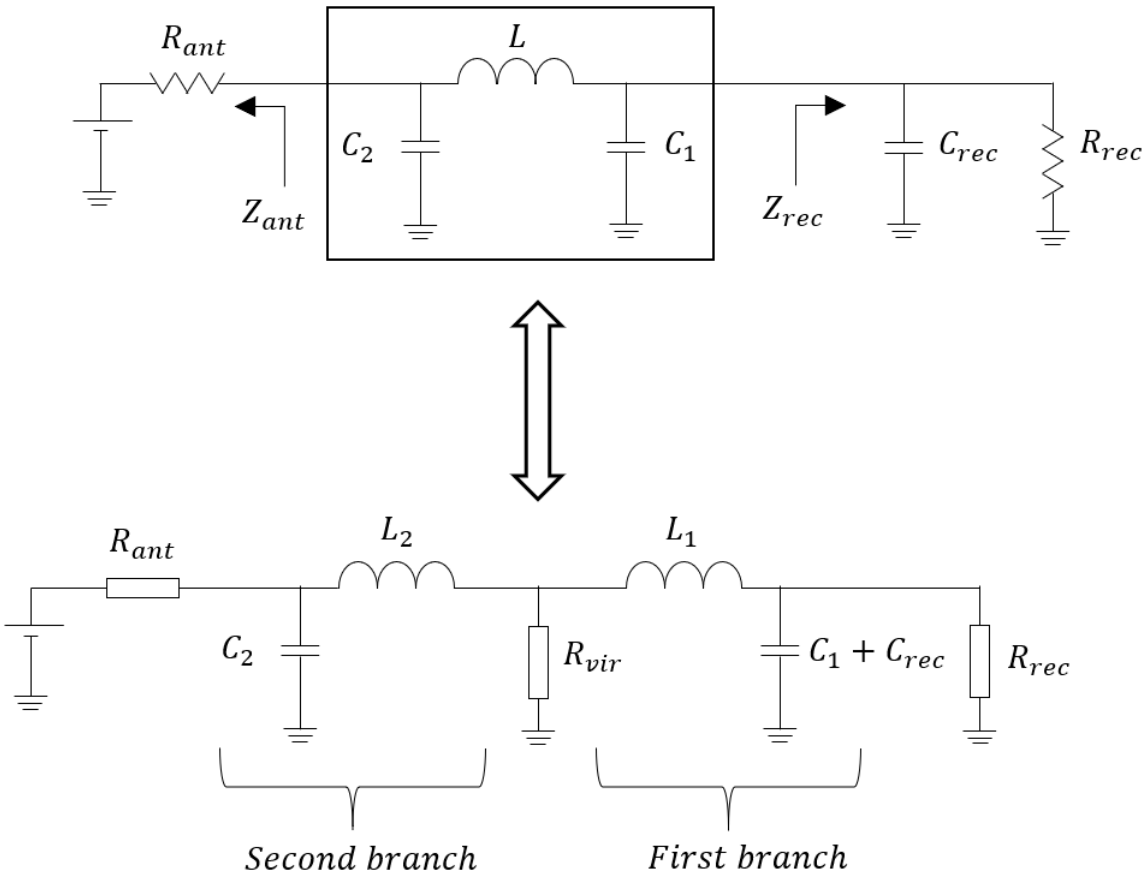


Figure 4.11: Schematic representation of the MN and the equivalent circuit with the virtual resistor R_{vir}.

The impedance seen at the input of the rectifier can be modeled by a resistor in parallel with a capacitor:

$$Z_{rec} = C_{rec}||R_{rec} \tag{4.19}$$

The purpose of the designed method based on the virtual resistor is to match both the antenna impedance and rectifier impedance to the virtual resistor at the center of the MN. To do that, the MN is divided into two "back-to-back" L networks labeled here as First branch and Second branch:

- First branch: R_{rec} is matched to the virtual resistor R_{vir} through the L network composed of $(C_1 + C_{rec})$ and L_1.

- Second branch: R_{ant} is matched to the virtual resistor R_{vir} through the L network composed of C_2 and L_2.

The value of the virtual resistor is usually choose as:

$$R_{vir} < min(R_{ant}, R_{rec}) \tag{4.20}$$

but here, the procedure from Pengcheng's paper is used, which is to leave the capacitor C_2 of the second branch as a design parameter and find a relation $R_{vir} = f(C_2)$ to design the remaning lumped elements of the MN based on the C_2 parameter and the virtual resistor.

4.5.1 Matching network design: second branch

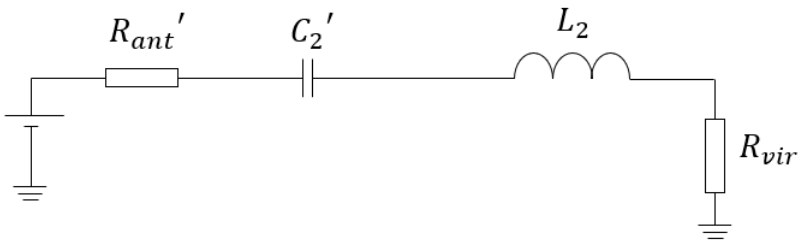


Figure 4.12: Equivalent serie representation of the second branch of the MN

To match the antenna impedance composed of the real resistor R_{ant} to the virtual resistor R_{vir} of the matching network, the second branch is tranformed into the serie equivalent model of the parallel impedance R_{ant} and $X_{C2} = 1/j\omega C_2$. This serie equivalent model can be see in Figure 4.12. From the virtual resistance R_{vir} and inductance L_2 point of view, the impedance composed of the new value for the antenna resistor and the capacitor does not change:

$$R'_{ant} - jX'_{C2} = \frac{R_{ant}}{1 + (\omega C_2 R_{ant})^2} - j\frac{\omega C_2 R_{ant}}{1 + (\omega C_2 R_{ant})^2} \tag{4.21}$$

To perform impedance matching between the new value of the antenna resistor R'_{ant} and the virtual resistor R_{vir}, the following equality is required to allow maximum power transfert from the AC source to the virtual resistor:

$$R'_{ant} - jX'_{C2} = R_{vir} + jX_{L2} \tag{4.22}$$

By identification of the real parts of expression (4.22), the relation between the virtual resistance and the input capacitor of the matching network (the parameter of the design methodology) can be found:

$$R_{vir} = \frac{R_{ant}}{1 + (\omega C_2 R_{ant})^2} \tag{4.23}$$

By identification of the imaginary part of expression (4.22), the relation between the inductance of the second branch L_2 and the antenna resistor R_{ant} can be found:

$$X_{L2} = \frac{\omega C_2 R_{ant}^2}{1 + (\omega C_2 R_{ant})^2} = R_{vir}\sqrt{\frac{R_{ant}}{R_{vir}} - 1} \tag{4.24}$$

the last part of equation (4.24) with only the resistors is obtained by injecting equation (4.23) into (4.24) though the capacitor C_2.

4.5.2 Matching network design: first branch

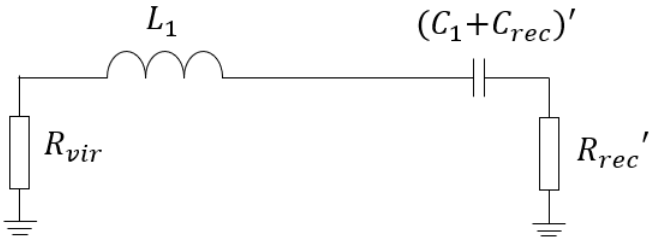


Figure 4.13: Equivalent serie representation of the first branch of the MN

To match the rectifier equivalent impedance R_{rec} to the virtual resistor R_{vir} of the matching network, the first branch of Figure 4.11 is tranformed into a serie equivalent equivalent model of the parallel impedances: R_{rec} and $X_{C_1+C_{rec}} = 1/j\omega(C_1 + C_{rec})$. This serie equivalent model can be see in Figure 4.13. From the virtual resistance R_{vir} and inductance L_1 point of view, the impedance composed of the new value for the rectifier equivalent resistor and the capacitor does not change:

$$R'_{rec} - jX'_{C_1+C_{rec}} = \frac{R_{rec}}{1 + (\omega(C_1 + C_{rec})R_{rec})^2} - j\frac{\omega(C_1 + C_{rec})R_{rec}}{1 + (\omega(C_1 + C_{rec})R_{rec})^2} \tag{4.25}$$

To perform impedance matching between the new value of the rectifier equivalent impedance R'_{rec} and the virtual resistor R_{vir}, the following equality is required:

$$R'_{rec} - jX'_{C_1+C_{rec}} = R_{vir} + jX_{L1} \tag{4.26}$$

By identification of the real parts of expression (4.26), the second relation that link the second capacitor of the network to the virtual resistor is found:

$$C_1 = \frac{\sqrt{\frac{R_{rec}}{R_{vir}} - 1}}{\omega R_{rec}} - C_{rec} \tag{4.27}$$

where C_{rec} is the value of the capacitor from the equivalent rectifier impedance seen at the ouput of the matching network. By identification of the imaginary parts of expression (4.26), the value of the inductance from the first branch is computed:

$$X_{L1} = \frac{\omega(C_1 + C_{rec})R_{rec}^2}{1 + (\omega(C_1 + C_{rec})R_{rec})^2} = R_{vir}\sqrt{\frac{R_{rec}}{R_{vir}} - 1} \tag{4.28}$$

4.5.3 Matching network design: inductor value

Onced each branch of the MN has been designed, the value of the final inductor L that compose the π-type MN can be computed. The virtual resistor of Figure 4.11 is not an actual component of the network. It is an imaginary resistor placed there to ease the design of the network. The real network only has the two capacitors C_1 and C_2 and the inductor that results from the merging of the two reactances X_{L1} and X_{L2} computed with the first and second branch:

$$\omega L = X_L = X_{L1} + X_{L2} \tag{4.29}$$

by using equation (4.28) and (4.24), the final inductor value of the MN is computed:

$$L = X_L/\omega = \frac{R_{vir}}{\omega}\left(\sqrt{\frac{R_{rec}}{R_{vir}} - 1} + \sqrt{\frac{R_{ant}}{R_{vir}} - 1}\right) \tag{4.30}$$

4.5.4 Matching network design: lumped element value

The final expressions for the value of the lumped elements that compose the π-type MN in function of the design parameter C_2 are:

$$R_{vir} = \frac{R_{ant}}{1 + (\omega C_2 R_{ant})^2} \tag{4.31}$$

for the virtual resistor,

$$C_1 = \frac{\sqrt{\frac{R_{load}}{R_{vir}} - 1}}{\omega R_{rec}} - C_{rec} \tag{4.32}$$

for the capacitor C_1 and

$$L = \frac{R_{vir}}{\omega}\left(\sqrt{\frac{R_{load}}{R_{vir}} - 1} + \sqrt{\frac{R_{ant}}{R_{vir}} - 1}\right) \tag{4.33}$$

for the inductor with $\omega = 2\pi f$ and $f = 2.45GHz$. Figure 4.14 and 4.15 represent respectivily the plot of expression (4.32) and (4.33) in function of the rectifier equivalent resistor R_{rec} for 3 different value of the design parameter C_2: 1pF, 2pF and 3pF and for an equivalent capacitor $C_{rec} = 0$pF.

In order to fixed the value of the lumped elements from the MN: L, C_1 and C_2, the rectifier and the PMU need to be simulated though ADS to extract the equivalent input impedance of the rectifier $Z_{rec} = C_{rec}||R_{rec}$. As explain in the state of art, at microwave frequencies the parasitic effect need to be taken into account when designing the MN, especially parasitic capacitor. For that reason, the required value C_1 is not fixed by the design parameter C_2 but rather by the value of the parasitic elements:

$$C_1 \triangleq C_{para} \tag{4.34}$$

Onced the value of C_1 is estimated, the value of the design parameter C_2 is choose in function of the estimated equivalent input resistor of the rectifier to perform impedance matching.

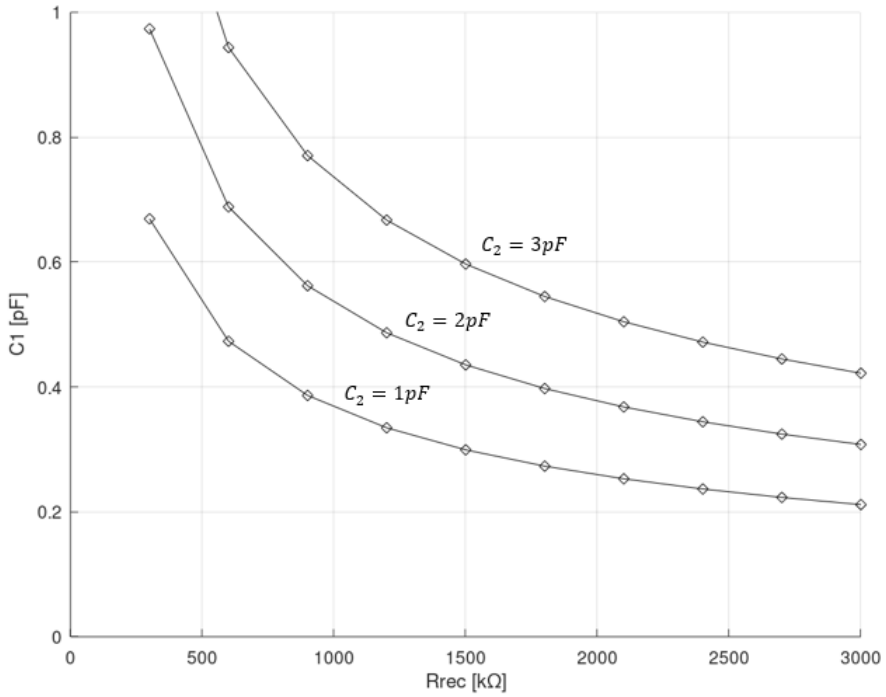


Figure 4.14: Representation of equation (4.32) in function of the rectifier equivalent resistor R_{rec} with $C_{rec} = 0$pF.

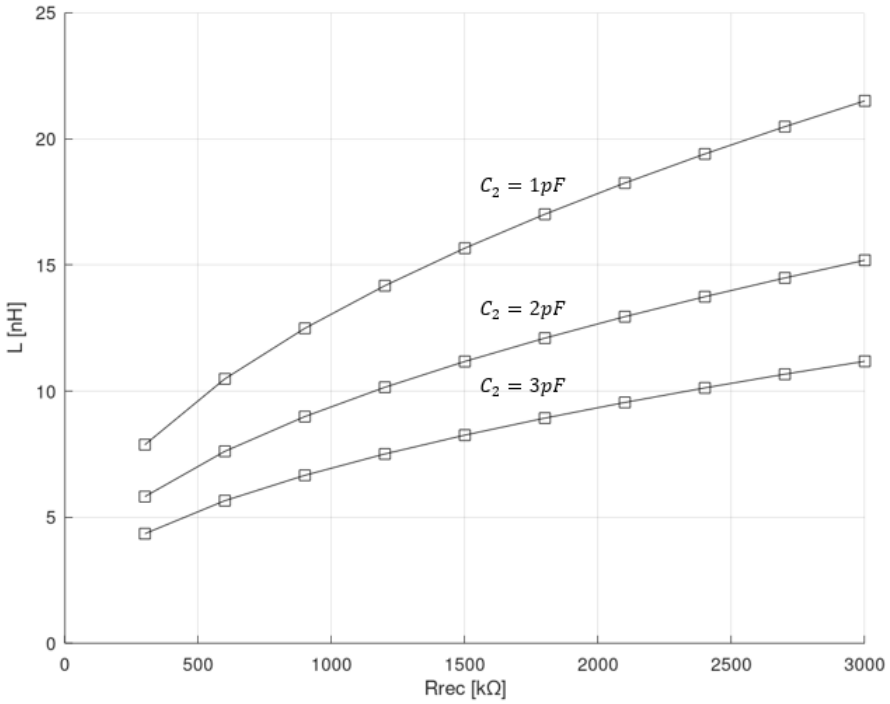


Figure 4.15: Representation of equation (4.33) in function of the rectifier equivalent resistor R_{rec}.

An estimation of the parasitic capacitor for a preliminary design can be used from [47]. If the PCB and package parasitic are taken into account then $C_{para} \approx 0.4$pF. The value of the equivalent capacitor of the rectifier doesn't vary as much as the resistor with the input power (see Section 4.6). For that reason, the equivalent capacitor can be considered to be fixed: $C_{rec} \approx 0.3$pF. By using the fixed value $C_1 = C_{para} \approx 0.4$pF, expression (4.32) gives the values of resistor R_{rec} needed to perform impedance matching. Figure 4.16 represents the values for R_{rec} needed to perform impedance matching if $C_1 = 0.4$pF and $C_{rec} = 0.3$pF. From Figure 4.16, we see that only 2 values of the design parameter C_2 can managed to tuned the matching network: $C_2 = 2$pF and $C_2 = 3$pF.

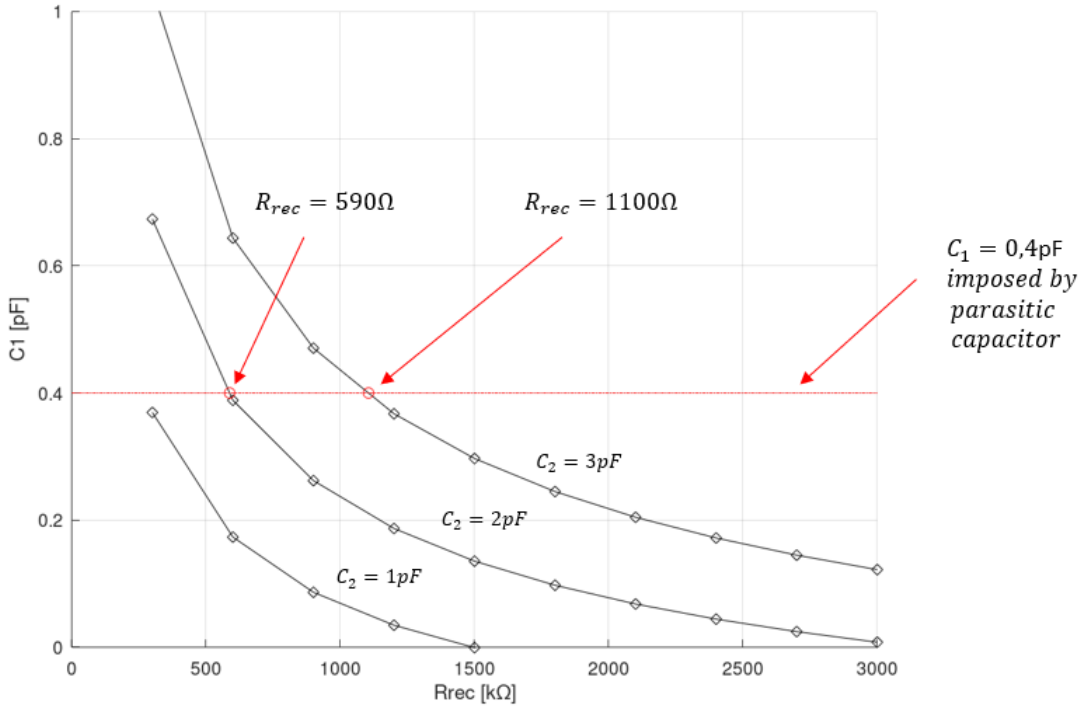


Figure 4.16: Representation of equation (4.32) in function of the rectifier equivalent resistor R_{rec} with $C_{rec} = 0.3$pF.

The value of the equivalent input resisistor R_{rec} of the rectifier tends to increase with decreasing RF input power. So to be able to design correctly the MN, $R_{rec} = 1100\Omega$ is choose as a target resistor. The analysis and design of the rectifier with the incorporated solar cell can identify the voltage requirement from the solar cell to reach that targeted value of equivalent resistor. Once C_1, C_2 and R_{rec} are identify, the value of the inductor can be found with expression (4.33), see Figure 4.15.

C_1	C_2	L
0.4pF	3pF	7.3nH

Table 4.4: π-type MN values of the lumped elements to perform impedance matching at $2.45GHz$ between the antenna impedance $R_{ant} = 50\Omega$ and the rectifier equivalent input impedance $R_{rec} = 1100\Omega$.

The final value of the lumped elements that compose the MN can be found in Table 4.4. One of the main challenge when designing a RFEH circuit is the high value of the equivalent resistor R_{rec} of the rectifier when the RFEH circuit is working at low level of input power. When the input power decrease, R_{rec} increases. This cause trouble for the design of the MN due to the effect of the parasitic elements on the value of C_1 from the MN and decreases the efficiency of the impedance matching.

4.6 Voltage rectifier design with incorporated solar cell

For the design of the rectifier, a one stage Greinacher topology is choose with Schokkty diode to perform the AC to DC convertion of the RF signal coming from the antenna. The solar cell from *3gsolar* is incorporated to the rectifier through the diode of the voltage doubler. A capacitor of 50pF is put in parallel with the solar cell to maintain a constant DC reference voltage V_{PV} at the bottom of the rectifier, see Figure 4.17.

4.6.1 Design justification

The incorporation of the solar inside the rectifier can be see as an addition of a DC voltage source at the diode that compose the voltage doubler, see Figure 4.17. There are two main reasons that justify the location of the solar cell inside the rectifier:

- The state of art show that in order to increase the ouput voltage of the rectifier, multiple stage can be used. However, at low input power condition, the increasing number of stages will decrease the PCE of the rectifier due to the losses inside the diodes. If the solar cell is incorporated inside the one stage rectifier, the ouput voltage can be boost without using additionnal Schokkty diode.
- The design of the matching network of section 4.5.4 shows that the equivalent input resistor of the rectifier needs to be low (under low input power condition) to perform the impedance matching due to the presence of the parasitic capacitor. So in order to decrease the equivalent input resistor R_{rec} an increase of power is needed at the input of the rectifier. The incorporation of the solar cell can be see as an additionnal input of power from a secondary energy source to decrease R_{rec}.

The second point of the justification for the addition of the solar is motivated by the following reasoning: the real part of the equivalent input impedance is inversly proportional to the input power of the rectifier according to equation (4.35):

$$R_{rec} \propto \frac{V_{in.rec}^2}{P_{in.rec}} \tag{4.35}$$

So by following expression (4.35), the additionnal power from the solar cell, can decrase the equivalent resistor R_{rec} for a fixed RF input power.

4.6.2 Output voltage of the rectifier

When the solar cell is incorporated inside the rectifier, the ouput voltage $V_{out.rec}$ increases. The expression of this ouput voltage can be found be following the analysis perform in section 3.5.2 for the simpple Greinacher topology.

If the input voltage of the rectifier is negative: $v_{in.rec} = -V_{DD}$, charges are flowing through the diode of the voltage doubler and are stored at the input capacitor, see Figure

4.17. When the input voltage becomes positive: $v_{in.rec} = +V_{DD}$ the charges previously accumulated go thougu the second diode of the rectifier and cause the apparition of a DC voltage at the capacitor from the peak detector, see Figure 4.18. The ouput voltage of the rectifier with the incorporated solar cell can be computed with expression (4.36):

$$V_{out.rec} = (2V_{DD} - 2V_{TO}) + V_{PV} \tag{4.36}$$

where V_{DD} represent the amplitude of the input signal, V_{TO} the voltage drop of the forward biases Schokkty diode and V_{PV} the voltage of the solar cell. Compare to expression (3.22) of the ouput voltage of a Greinacher topology without solar cell, expression (4.36) has the addition of the voltage coming from the solar cell. This mean that the ouput voltage of the rectifier is increased without using multiple stage.

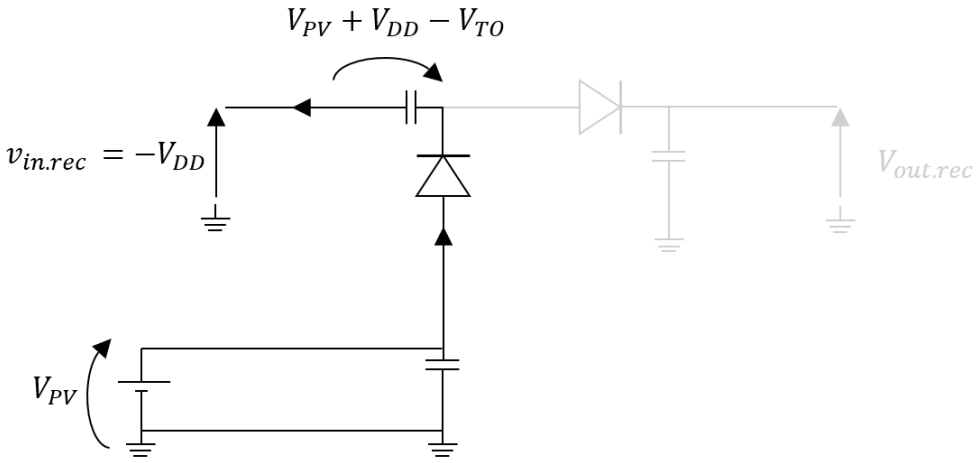


Figure 4.17: Representation of the Greinacher rectifier with incorporated solar cell when the input voltage is negative

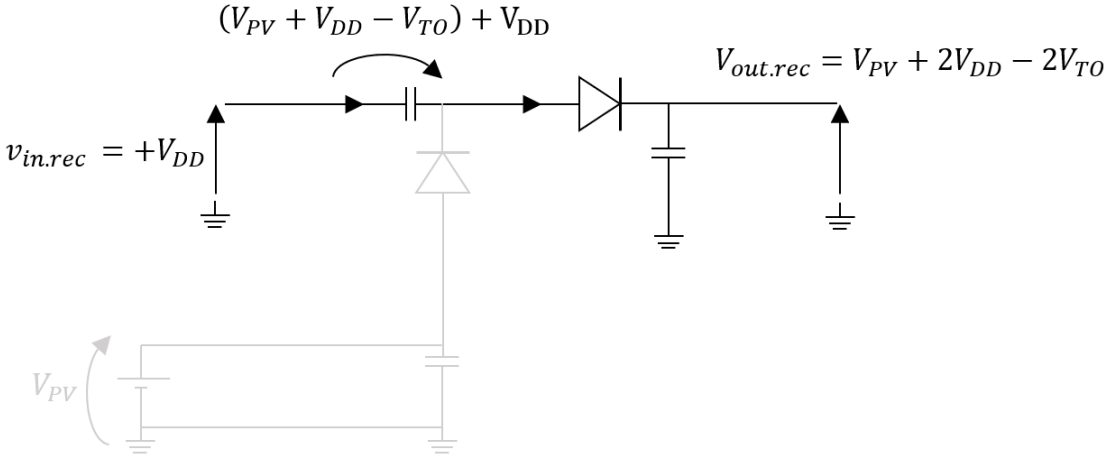
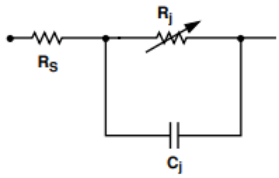


Figure 4.18: Representation of the Greinacher rectifier with incorporated solar cell when the input voltage is positive

4.6.3 Schokkty diode model and capacitor

To simulated the rectifier on ADS, 50pF capacitors are used for the voltage double and peak detector of the Greinacher topology. Concerning the capacitor at the ouput of the solar cell, see Figure 4.17, a 1nF capacitor is used to ensure a constant DC voltage reference at the bottom of the diode.
The SPICE parameters to model the Schokkty diode to perform ADS simulation can be obtain with the data sheet of the HSMS286x series, see Figure 4.19:

Equivalent Linear Circuit Model, Diode chip



R_S = series resistance (see Table of SPICE parameters)
C_j = junction capacitance (see Table of SPICE parameters)

$$R_j = \frac{8.33 \times 10^{-5}\ nT}{I_b + I_s}$$

where
I_b = externally applied bias current in amps
I_s = saturation current (see table of SPICE parameters)
T = temperature, °K
n = ideality factor (see table of SPICE parameters)

Note:
To effectively model the packaged HSMS-286x product, please refer to Application Note AN1124.

SPICE Parameters

Parameter	Units	Value
B_V	V	7.0
C_{J0}	pF	0.18
E_G	eV	0.69
I_{BV}	A	1 E - 5
I_S	A	5 E - 8
N		1.08
R_S	Ω	6.0
P_B (VJ)	V	0.65
P_T (XTI)		2
M		0.5

Figure 4.19: Equivalent model of the Schokkty HSMS286x diode and SPICE parameters from the data sheet of the component.

The parameters from Figure 4.19 are incorporated inside ADS with the diode model bloc, see Figure 4.20:

Figure 4.20: Diode model bloc from ADS to simulated the HSMS286x Schokkty diode.

Chapter 5

Simulation results

This rection gathers all the simulations of the RFEH circuit including simulations from the individual blocs that compose the circuit. Those simulations were perform using Advanced Design System (ADS).
First, the equivalent input impedance $Z_{rec} = C_{rec}||R_{rec}$ (see section 4.5) of the rectifier without the solar cell is extract with harmonic balance simulation at 2.45GHz. After that, the rectifier is simulated with the incorporation of the solar cell for different irradiances. To finish, the power harvest efficiency of the overall circuit is computed at 2.45GHz.

5.1 Output voltage of the rectifier with and without solar cell

The simulation perform in this section is to prove the influence of the solar cell on the ouput voltage of the rectifier. As state in the design justification, on way to increase the ouput voltage of the rectifier without using additional stages is to incorporate the solar cell.

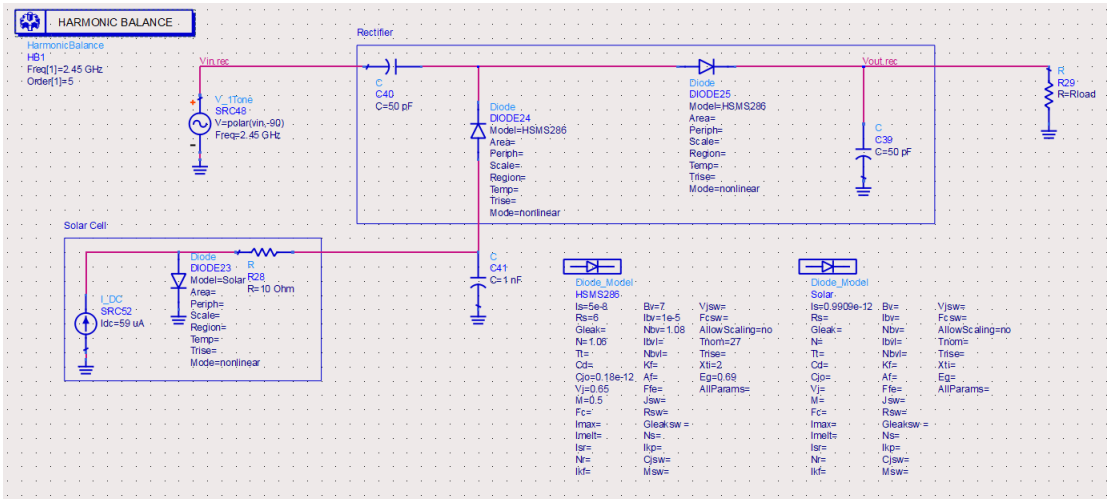


Figure 5.1: Representation of the circuit simulated on ADS with harmonic analysis to extract the output power of the rectifier.

Figure 5.4 represent the circuit simulated on ADS to perform the analysis of the output voltage at the load R_{load}. The AC source, represent the AC signal coming from the MN bloc. For the analysis, the resistor R_{load} is sweep from $10k\Omega$ to $10M\Omega$ for different illumination of the solar cell.

Figure 5.2 represent the ouput voltage of the rectifier in function of the load resistor for different illumination when the input AC voltage is equal to 0.1V. The ouput voltage of the rectifier when the solar cell is not incorporated is represented by the black curve of Figure 5.2. From that Figure, we can see that the ouput voltage is greatly increase by the solar cell even at $50lux$ compared to the ouput voltage without solar cell. Figure 5.3 represent the same analysis but with an input voltage of 1V at the rectifier.

The simulation of the ouput power of the rectifier shows that the ouput voltage of the recrifier can be increased by the solar cell without using a N-stage topology for the design of the rectifier.

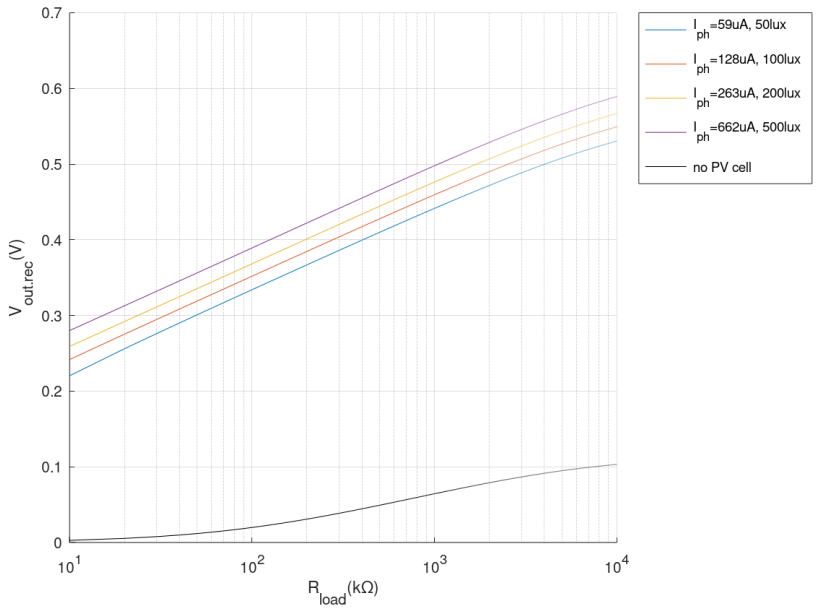


Figure 5.2: Simulation of the ouput voltage of the rectifier in function of the load R_{load} for different illumination of the solar cell and for a input voltage $V_{in.rec} = 0.1sin(\omega t)$ with $\omega = 2\pi f$ and $f = 2.45gHz$.

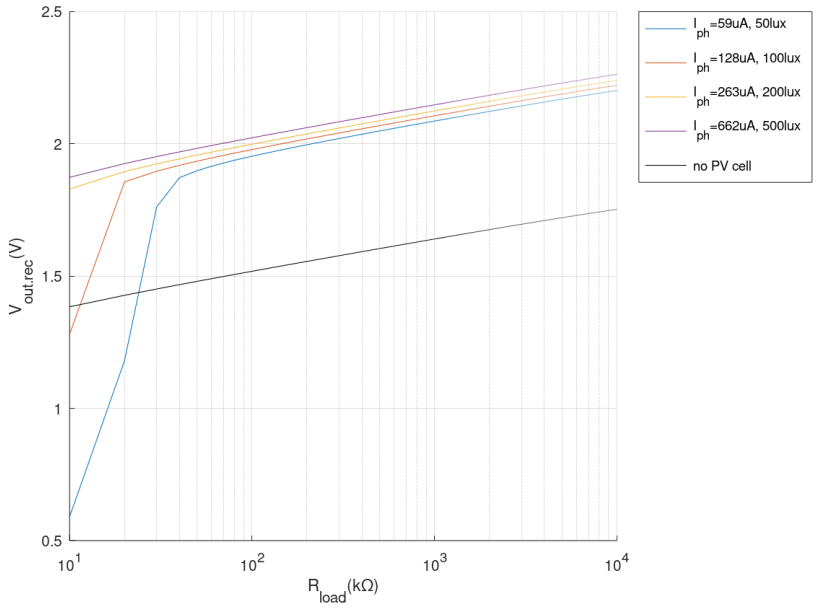


Figure 5.3: Simulation of the ouput voltage of the rectifier in function of the load R_{load} for different illumination of the solar cell and for a input voltage $V_{in.rec} = 1sin(\omega t)$ with $\omega = 2\pi f$ and $f = 2.45gHz$.

5.2 Equivalent input impedance of the rectifier with and without solar cell

As explain in the MN design section 4.5, the value of the equivalent input impedance of the rectifier needs to be know to perform the impedance matching based on the methodology describe in section 4.5.4. For that reason, onced the solar cell and rectifier are designed, the power magagement unit is incorporated at the ouput of the rectifier and the equivalent input impedance Z_{rec} can be computed through ADS simulation.

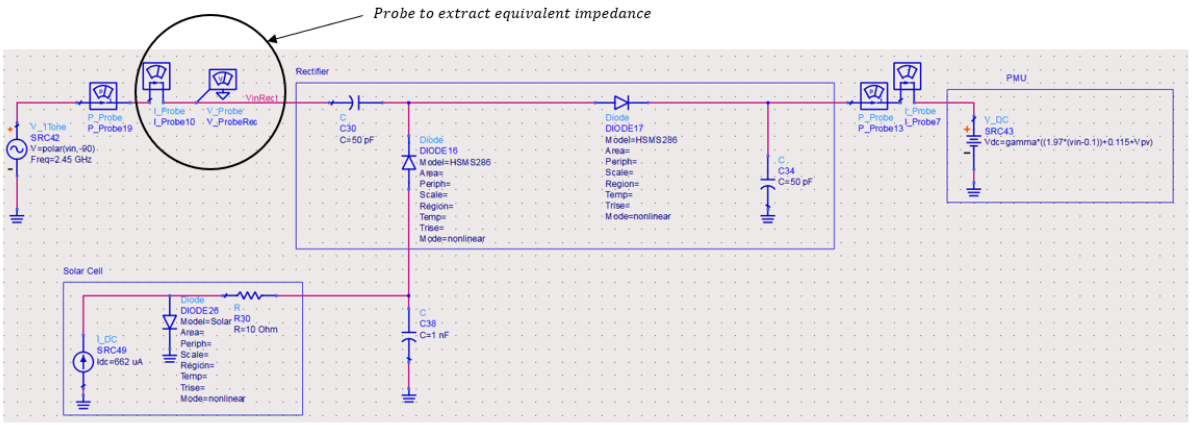


Figure 5.4: Representation of the circuit simulated on ADS with harmonic analysis to extract the equivalent imput impedance of the rectifier.

Figure 5.4 represent the circuit simulated on ADS with no solar cell to extract Z_{rec}. Figure 5.5 represent the evolution R_{rec} with the input voltage at the rectifier and for 3 different configurations of the PMU. A first conclusion can be draw from that simulation: The real part of the equivalent input impedance of the rectifier increase for an increasing output voltage for a fixed input voltage $V_{in.rec}$.

As state in the specification, we want the rectifier to have a high ouput voltage to perform the cold start of the PMU. On the other hand, if the ouput voltage increase, R_{rec} will also increase, thus making the design of the matching network more complicated. For that reason, $\gamma = 50\%$ is choose for the configuration of the PMU and for the following simulations.

Figure 5.6 represent the evolution of R_{rec} but this time with the incorporated solar cell and for 2 different irradiances. As predicted in the Design justification of section 4.6, the incorporation of the solar cell can decrease the equivalent input resistor of the rectifier. This decrase of Rrec can ease the design of the matching network and justify the value of $R_{rec} = 1300\Omega$ selected in section 4.5.4 for the design of the π-type MN. This value of $R_{rec} = 1300\Omega$ can be targeted if the irradiance of the solar cell is equal to 500lux (which corresponds to indoor conditions for the *3gsolar* cell).

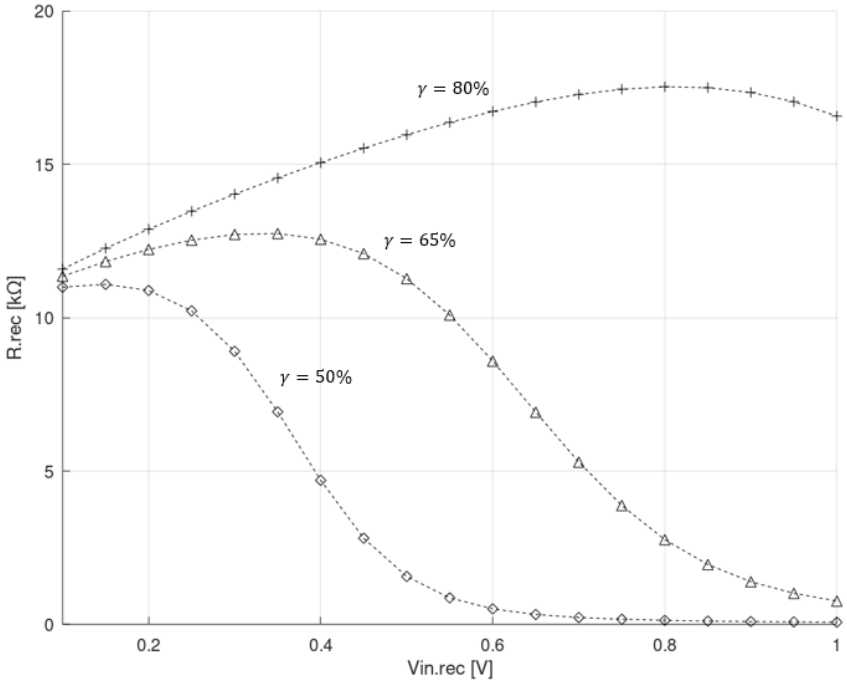


Figure 5.5: Simulation of the evolution of the equivalent input resistor R_{rec} with the input voltage $v_{in.rec}$ for different open voltage ratio γ of the PMU with no solar cell.

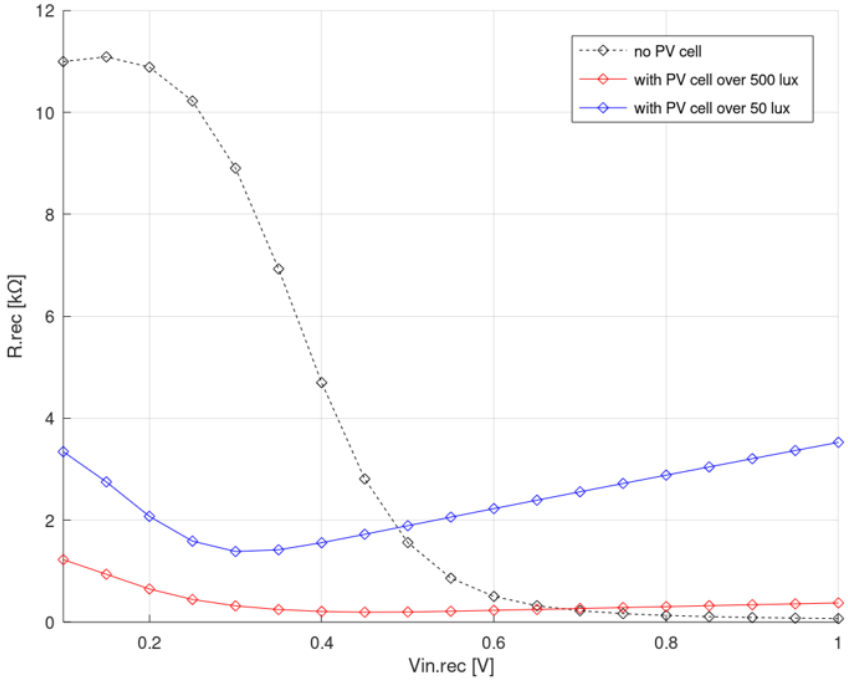


Figure 5.6: Simulation of the evolution of the equivalent input resistor R_{rec} with the input voltage $v_{in.rec}$ for different open voltage ratio γ of the PMU with the incorporated solar cell.

The evolution of the equivalent resistor C_{rec} of the rectifier with the input voltage can be see in Figure 5.7:

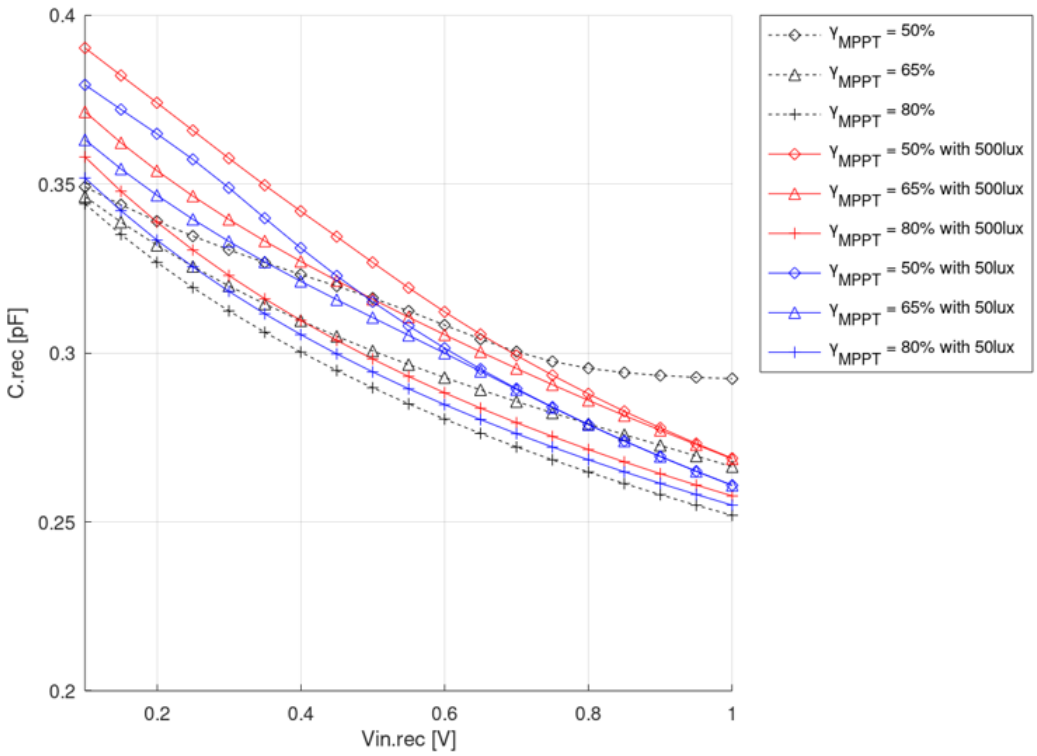


Figure 5.7: Simulation of the evolution of the equivalent input capacitor C_{rec} with the input voltage $v_{in.rec}$ for different open voltage ratio γ of the PMU with (blue and red curves) and without solar cell (black curves).

The approximation made in section 4.5.4 to keep a fixed value for C_{rec} is comfirmed by the simulations. For that reason, the value $C_{rec} \approx 0.3$pF is used for the design of the matching network.

5.3 Power harvest efficiency of the RFEH circuit

Onced the equivalent input impedance of the rectifier is extracted to design the MN, the complete RFEH circuit with the solar cell can be simulated. Figure 5.8 represent the proposed RFEH circuit with incorporated solar cell that was simulated on ADS to extract the Power Harvest Efficiency (PHE).

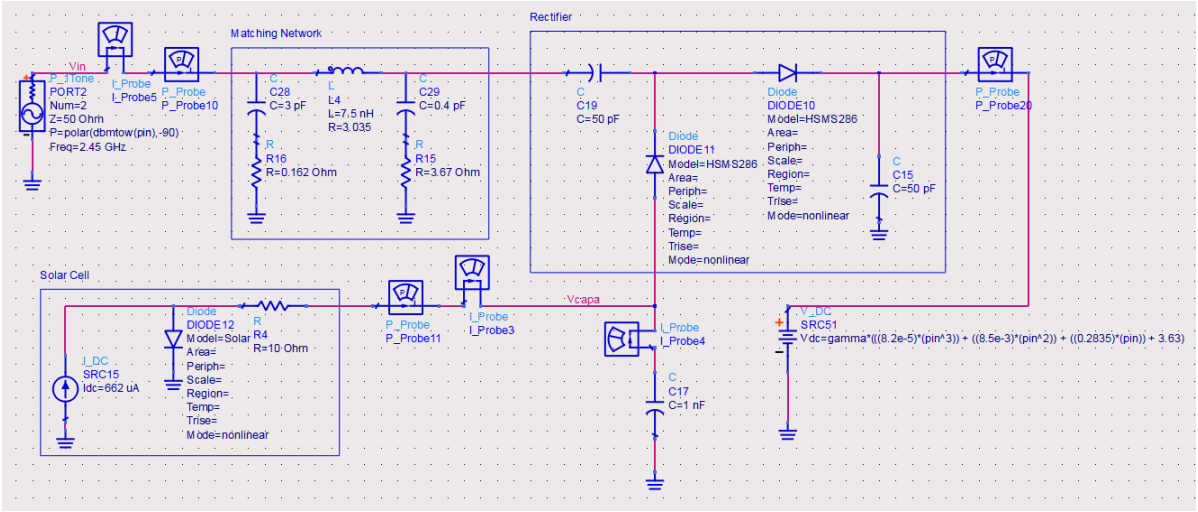


Figure 5.8: Representation of the circuit simulated on ADS with harmonic analysis at 2.45GHz to extract the PHE of the RFEH circuit with incorporated solar cell.

Since the PHE defined in section 3.1 only takes into account the RF energy and not the energy coming from the solar cell, a new PHE needs to be define. Expression (5.1) represent the new PHE used for the simulations:

$$PHE = \frac{P_{out.rec}}{P_{in.RF} + P_{in.PV}} \tag{5.1}$$

where $P_{in.RF}$ represent the RF input power, $P_{in.RV}$ the power coming from the ouput of the solar cell and $P_{out.rec}$ the power at the output of the rectifier.

Figure 5.9 represent the PHE from expression (5.1) simulated with ADS at 500lux and for different PMU configuration. The maximum efficiency is reached when $\gamma = 50\%$, this is because at that value for the configuration of the PMU, the equivalent resistor R_{rec} is close to the ideal value of $R_{rec} = 1300$ at which the matching network was designed.

Figure 5.10 represent the same analysis of expression (5.1) simulated with ADS but this time for an irradiance of 50lux. The maximum efficiency is still reached when $\gamma = 50\%$ but this time, the overall PHE curves are lower than the curves from Figure 5.9 because the input power coming from the solar cell is decreased.

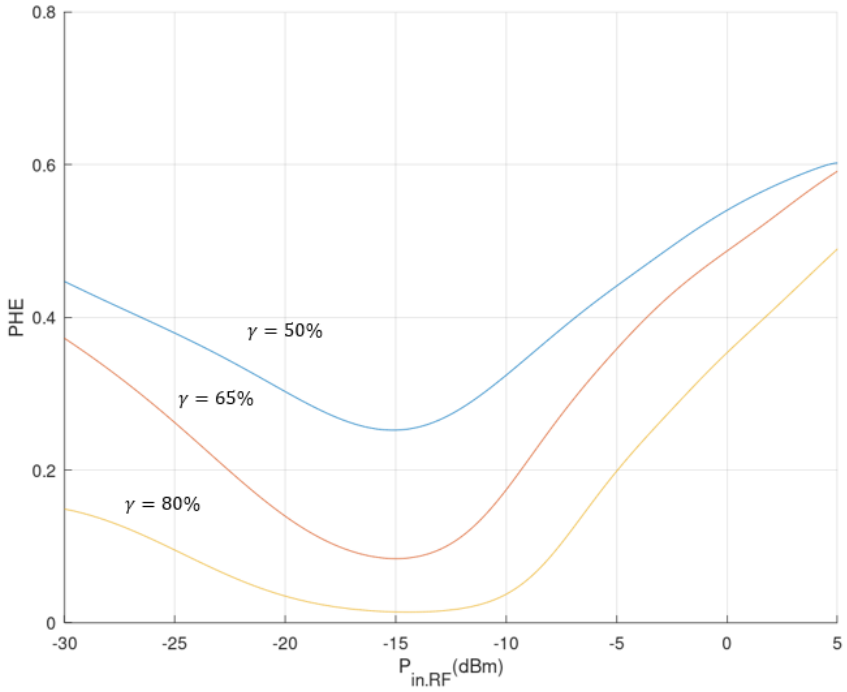


Figure 5.9: Simulation of the evolution of the PHE with the input power $P_{in.RF}$ for different open voltage ratio γ of the PMU with with a irradiance of $500lux$ at the solar cell.

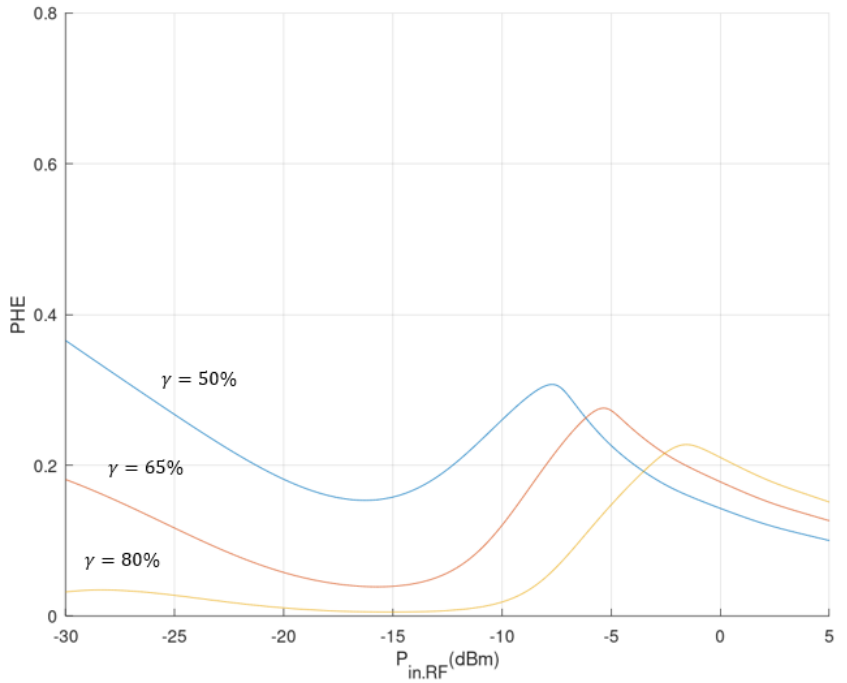


Figure 5.10: Simulation of the evolution of the PHE with the input power $P_{in.RF}$ for different open voltage ratio γ of the PMU with with a irradiance of $50lux$ at the solar cell.

Chapter 6

Conclusion and improvement clue for future works

This work presents the design of a Radio Frequency Energy Harvesting (RFEH) circuit with the addition of a solar cell. From the simulations results and the theory of impedance matching circuits, the incorporation of the solar cell can decrease the equivalent resistor of the rectifier resulting in an inprovement of impedance matching between the antenna and the rectifier. This improvement of impedance matching decreases the reflection losses. However, in order to decrease the equivalent resistor of the recrifier from the circuit, the open circuit ratio of the Power Management Unit (PMU) needs to be equal to 50% according to the simulation if the PMU from *epeas* is used for the final design. This means that there is a trade off to take into account between the ouput voltage of the rectifier and the efficiency of the matching network when designing the circuit.

The use of the solar cell inside the rectifier can also boost the ouput voltage to meet the requirement specifications. However, the main objective of the RFEH circuit is to supply power to the load (sensor, battery for WSN applications, etc). Simulations of the power extracted from the *3gsolar* cell alone (without the hybrid RF and solar energy harvesting) proved that the harvested power is greater if the solar cell is direclty connected to a PMU rather than through the AC to DC rectifier. Figure 6.1 displays the available power at the PMU if the solar cell is directly connected to it. The level of power reached is greater than the case where the solar cell is incorporated inside the proposed topology of this work.

The methotology presented in this work could be interesting if the solar cell used inside the rectifier was designed to provide voltage rather than high power. In that case, the PHE of the circuit could be increased while keeping the advantage of the solar cell inside the rectifier to decrease the impedance for the matching network design and increase the ouput voltage. However, the power at the ouput of the rectifier should be high enough to perform the cold start of the PMU.

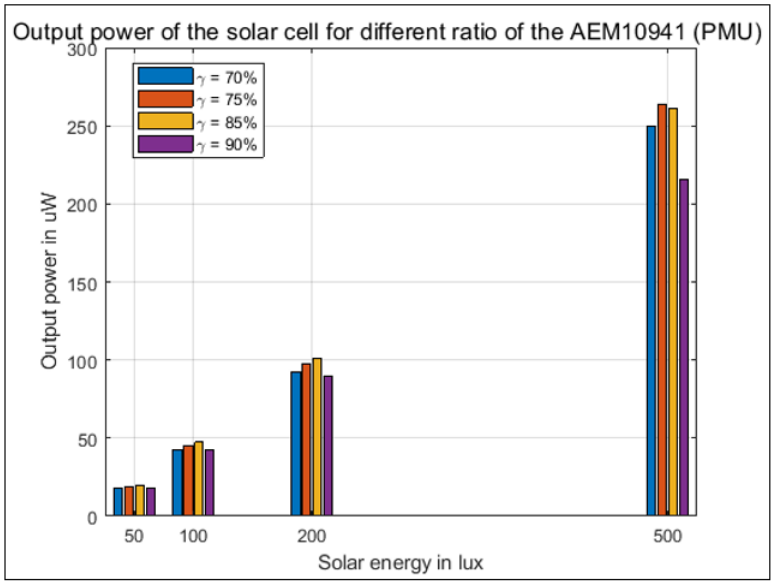


Figure 6.1: Simulation of the ouput power harvested from the *3gsolar* cell with the AEM10941 from *epeas*.

An other possibility could be to implement the Greinacher topology for the AC to DC conversion using MOSFET and solar cells. Rather than performong static V_{th} compensation, the solar cells inside the CMOS based rectifier could be used to generate a voltage at the gate of the MOSFETs to cancel out the effect of threshold voltage and increase the PCE. Recent paper from the litterature show that CMOS based rectifier can provide better PCE for RFEH circuit at very low input power condition.

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