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Comparative Study of MPPT Algorithms for Space Applications

Implementation on a Radiation Hardened Micro-Processor

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Academic year 2021–2022
Master [120] in Electro-mechanical Engineering

Abstract

This thesis aims at confronting several algorithms of maximum power point tracking and their digital implementation on a radiation hardened micro-processor. Extracting the maximum of the power received by the sun is essential during a satellite mission. This task was usually done in analog (with discrete electronic components), but in the last few years digital methods have been getting more and more popular.

A review of some of the most popular methods allowed to select three algorithms: Perturb and Observe, Incremental Conductance and Three Percent. These methods will be implemented on a radiation hardened micro-processor in order to study their behavior. Static tests identified their behaviour in regime while dynamic tests focused on their performance in a rapidly changing environment such that a satellite could experience during flight.

One of the key learning of this paper is that the digital implementation implies some constraints that were not present in an analog implementation. Among these, the discretization restricts the available power to be extracted.

Finally, some avenues for improvement and optimization are discussed. These can be used as a basis for future work.

Keywords – *Maximum Power Point Tracking, MPPT, algorithm, solar cell, radiation hardened micro-processor, digital implementation*

Acknowledgements

The write-up of this thesis would not have been possible without the help of several people whom I wish to acknowledge.

Firstly, I would like to thank my thesis supervisor, Pr. Marc Bekemans, for his continuous help, support and advice throughout this semester.

Then, I am particularly grateful to the people of Thales Alenia Space Belgium and more particularly, Benjamin Spitaels. I am thankful for his assistance on the technical points as well as his review of my work. In addition I would like to thank Gian Claudio de Lazzer for helping me in the lab.

Furthermore, I wish to thank Pr. Jean-Dider Legat and Guillaume Colinet for accepting being part of this master's thesis committee. I thank them for the time they spent reading this document.

Finally, I would like to thank my parents for helping me proofreading the English grammar of this document.

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List of Acronyms

3% Three Percent. 63

ADC Analog to Digital Converter. xi, 12, 23–27, 30, 36–40, 46, 47, 63

ASIC Application Specific Integrated Circuit. ix, 11

BCDR Battery Charge and Discharge Regulator. 4, 55

CAN Controller Area Network. 13

COM Communication Module. 12, 13, 39, 58

CPU Central Processing Unit. 12

CQFP Ceramic Quad Flat Pack. ix, 11

DAC Digital to Analog Converter. ix, 12, 13, 25–27, 30, 36–40, 46, 63

DEM Dynamic Element Matching. 26

DLK DPC Launch Kit. 36–39

DNL Differential Non-Linearity. 26

DPC Digital Programmable Controller. ix, 1, 11–13, 15, 23–25, 28–32, 36, 40, 60, 63

DPRAM Dual Port Random Access Memory. 29, 39

EMC Electromagnetic Compatibility. 64

FPGA Field Programmable Gate Array. 37

GEO Geostationary. 4

HWIL Hardware In the Loop. 35

IC Incremental Conductance. 17, 19, 48–50, 54, 63

INL Integral Non-Linearity. 26

IO Input Output. 12, 37

LEO Low Earth Orbit. 3, 10

LSB Least Significant Bit. 28

MACC Multiple and Accumulate. 12

MCU Micro-Controller Unit. 21, 63

MPP Maximum Power Point. x, 4, 10, 17–21, 32, 41, 43–45, 47–51, 53–57, 59, 60, 63, 64

MPPT Maximum Power Point Tracking. 1, 5, 15, 17, 23, 46, 63

MSB Most Significant Bit. 28

P&O Perturb and Observe. ix, 17, 31, 48–51, 54, 60, 63

PWM Pulse width Modulation. 12, 23

RAS Regulation Arithmetic Sequencer. xi, 1, 12, 13, 23–25, 27, 29, 39, 58, 60, 63

RCT RAS Cycle Timer. 23, 24, 27, 30, 63

RISC Reduced Instruction Set Computer. 12, 63

SA Solar Array. 4, 5, 10, 20, 46, 55

SDK Software Development Kit. 37

SSM Supervision & System Management Micro-Controller. 12, 13

TAS-B Thales Alenia Space Belgium. 1, 11, 20, 21, 36, 60, 63

UART Universal Asynchronous Receiver Transmitter. 13, 29, 39, 58

USI Universal Serial Interface. 13

Introduction

The use of renewable energies is one of the many measures set in place to reduce greenhouse gas emissions. Among these we can list : wind energy, solar energy, tidal energy, wave energy, ... In order to harvest these energies, a many converters already exist with great efficiency. However, renewable energies are intermittent: a wind turbine is useless if there is no wind, just as solar panels are useless at night. It is therefore essential to extract the maximum of power from these energies when they are available and to store the excess (if there is any) in order to redistribute it during the periods of null production.

It is exactly the same principle implemented in the power management of a satellite. In this case, the only source of energy is the sun and the periods of eclipse make it intermittent. The entity in charge of the power management must therefore ensure to extract a maximum of the available energy in order to cover the instantaneous needs but also to be able to provide for the needs of the mission during the eclipse phases.

This master thesis focuses on three maximum power point tracking algorithms and their implementation on a space hardened micro-processor. The paper is divided into five chapters.

The first chapter aims at providing the reader with some background on useful topics. First, satellites are briefly introduced : what are they ? In what environment do they evolve and how is the power distributed during the mission ? Then, the photo-electric effect is discussed. This phenomenon is at the basis of solar power generation. Finally, the micro-processor used for the implementation of the algorithms throughout this thesis dissertation is presented.

The second chapter introduces the Maximum Power Point Tracking (MPPT) concept with an analogy to other phenomenons. Then some popular MPPT methods are listed and finally three of them are selected to be implemented on the Digital Programmable Controller (DPC), a space hardened micro-processor developed by Thales Alenia Space Belgium (TAS-B).

The third chapter deals with the digital implementation of three selected MPPT algorithms: Perturb & Observe, Incremental Conductance and Three Percent. The algorithms are implemented on the Regulation Arithmetic Sequencer (RAS) core of the Digital Programmable Controller (DPC). This core is optimized for rapid regulations and is equipped with various features supporting this function. The peripherals used are presented with their configuration and the implementation of the three selected algorithms is further discussed.

The fourth chapter deals with the experiments conducted in order to characterize the behavior of the algorithms. First, the test bench is presented, qualified and validated. Then, the static and dynamic results are discussed. Finally, some of the issues encountered during the test campaign are listed.

Finally, the fifth chapter is giving suggestions on how to improve the implementation of the three algorithms studied so far. These are a few ideas among the many possibilities to improve the algorithms. They could serve as a basis for a future work.

Chapter 1

Background

This chapter is aiming at providing the reader with some background on useful concepts. First, satellites are briefly introduced : what are they ? In what environment do they evolve and how is the power distributed during the mission? Then, the photo-electric effect is discussed. This phenomenon is at the basis of solar array power generation. Finally, the micro-processor used in throughout this thesis dissertation is presented.

1.1 Artificial satellites

In the context of spaceflight, a satellite is an object that has been intentionally placed in orbit. These objects are called artificial satellites to distinguish them from natural satellites such as Earth's Moon [17]. The first ever man-made satellite launched to space is Sputnik 1. It was launched by the Soviet Union on October 4 1957. Since then, an estimate of around 9000 satellites were launched until 2019. Nevertheless this rate has rapidly been increasing in the recent years with the growth of small satellites constellations. Since 2018, Starlink[1] already launched around 1700 out of the 12000 planned satellites in Low Earth Orbit (LEO).

Satellites have a wide variety of applications including sciences, observation, defense, telecommunication, meteorology and many more.

1.1.1 Satellite environment

Satellites are evolving in the harsh environment of space. Space is enforcing constraints that need to be taken into consideration when designing and operating a satellite.

The lack of air (i.e. vacuum) makes thermal regulation extremely difficult. Indeed, convection is no longer possible. The only way to cool down the satellite is by conducting the heat between the pieces of equipment towards the cold part of the satellite and then radiating all the energy. This implies a huge temperature gradient and consequently stresses the mechanical structure of the satellite. Convection could be considered if air (or any other gas) was sealed in an equipment. However it is still not possible to use convection as the lack of

[1] A company founded by Elon Musk aiming to provide low latency internet anywhere in the world, including the most remote locations.

gravity does not make the warm air move.

Earth is protected by the atmosphere from space radiation, satellites are not. The materials used and the electronics must be robust and consequently designed. When charged particles strike the transistors of the memory banks (more details on storing digital data in Section 3.5), they interact with the electrons in the gate and can cause a unintended flow of electrons, resulting in the unintended loss or gain of electrons ultimately leading to a bit-flip. This can result to a crash of the application and ultimately the loss of the mission. Different hardware and software methods exist in order to overcome such situations.

Probably the most critical aspect of a satellite is the unavailability of maintenance operations. For example once a Geostationary (GEO) satellite is launched, it must be operational during at least 15 years. The system must be extremely robust and should be able to recover from a potential fault.

1.1.2 Power regulation in a satellite

Figure 1.1 is showing a simplified block diagram of the power regulation in a satellite. The power is usually distributed with a bus and the equipment are connected in parallel to that bus. A huge bank of capacitors is also connected in parallel to the bus. They aim at helping the battery for rapidly changing current consumption and stabilize the voltage bus.

The bus can be regulated or not. A regulated bus has a constant voltage. This voltage is kept at a reference value thanks to the Battery Charge and Discharge Regulator (BCDR). The reference value may vary over time in order to meet the demand of the payload or to maximize the power generation by the solar arrays. On the other hand, an unregulated bus operates at whatever the voltage of the batteries currently is. Each piece of equipment must therefore have a DC/DC converter in order to step up/down the bus voltage to meet its needs. In addition, the solar arrays will not operate at their highest capacity. Unregulated busses are now rarely used.

The BCDR is in charge of regulating the power flow from and to the batteries. It regulates the amount of current going to the payload and the amount of current going to the batteries. Multiple cases exist, for example:

- A high current transient occurs and the solar arrays are not able to react immediately. As a result, the BCDR increases the battery current to maintain the bus at the reference voltage while the solar array current is increased to match the load current.
- The demand in current is low and the batteries are fully charged. The BCDR will disconnect the one (or more) solar array section(s) in order to produce just the amount of current necessary. If the current demand is lower than what a single section is producing, then a duty cycle is applied to a single section.

Connecting and disconnecting solar arrays sections to meet the current needs is commonly called sequential shunt regulation. This not the most efficient method as the Solar Array (SA) are not operating at their Maximum Power Point (MPP). This is usually the case when the

satellite is in orbit and performing its routine mission and/or if the SA are oversized. Yet, during the stage of orbit raising, the payload is not active and all the power available is routed to the propulsion equipment. Therefore extracting the maximum power of the SA is key and can help to achieve the correct orbit faster. In addition, Maximum Power Point Tracking (MPPT) allows to decrease the size of the SA and therefore the cost of a mission. With MPPT the regulated bus voltage will be set at the voltage maximizing the power generation of the solar arrays.

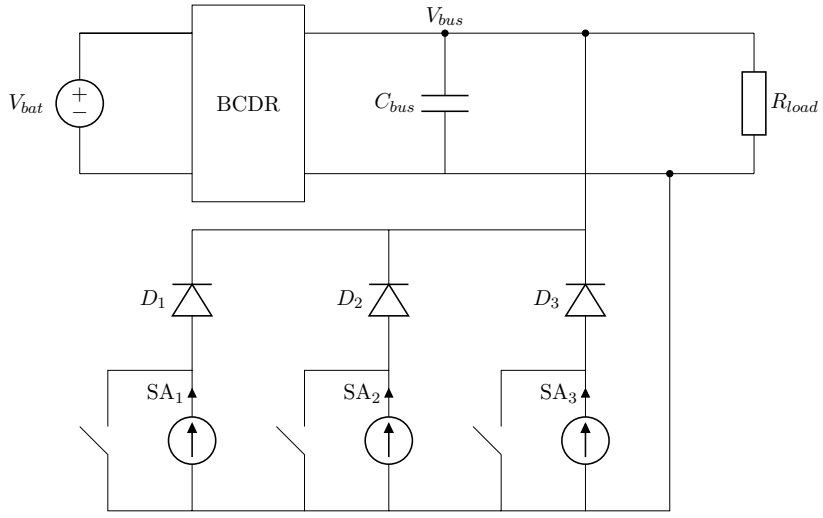


Figure 1.1: Simplified block diagram of a typical satellite power regulation. The diodes are protecting the pieces of equipment connected to the bus in the event of one (or more) solar array(s) failure.

1.2 Harvesting power from the sun

After being launched, the main source of energy available to the satellite is the sun. It is critical for the success of the mission to harvest that energy.

1.2.1 Black body radiation

The sun can be considered as a black body in thermal equilibrium at 5800 [K] which emits electromagnetic radiations. A black body is physical body that absorbs all incident radiation, regardless of their frequency or angle of incidence [16]. A black body in thermal equilibrium means its temperature is spatially and temporally uniform, as a consequence it is an ideal diffuse emitter: the black body emits at every frequencies a greater or equal amount of energy than any other body at the same temperature and this energy is radiated isotropically. In addition, the power spectral density of the radiations only depends on the temperature of the black body. The radiated intensity of a black body at a frequency ν and a temperature T is described by Planck's law:

$$I(\nu, T) = \frac{8\pi\nu^2}{c^2} \frac{h\nu}{\exp\left(\frac{h\nu}{kT}\right) - 1} \tag{1.1}$$

where $h = 6.626 \times 10^{-34}$ $\left[\mathrm{J\,Hz^{-1}}\right]$ is Planck's constant, $k = 1.38 \times 10^{-23}$ $\left[\mathrm{J\,K^{-1}}\right]$ is Boltzmann's constant and c is the speed of light. The irradiance spectrum of the sun is illustrated in Figure 1.2. The irradiance is defined as the flux of solar radiation on a given area $[\mathrm{W\,m^{-2}}]$.

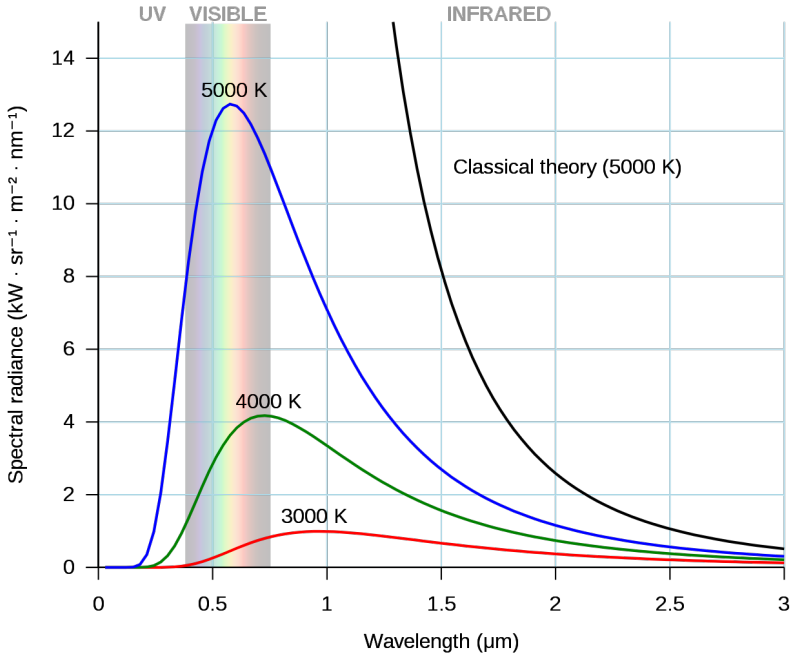


Figure 1.2: Sunlight spectrum in space as a function of wavelength

1.2.2 Photo-electric effect

Harvesting the solar energy is possible thanks to the photo-electric effect: transforming the energy carried by the photons into a flow of electrons. The energy of a photon is a function of the wave frequency and Planck's constant:

$$E = h\nu \tag{1.2}$$

Electrons of a material exposed to light are excited by the incoming photons and, as a consequence, are extracted from the material. The movement of these free extracted electrons are generating the photo-current. The minimum energy required to extract an electron from its band is the binding energy specific to each material. Nevertheless, according to (1.2), higher frequency photons are more energetic. If the photon has not enough energy (i.e. its frequency is to low) then it not capable of extracting the electron from the material. Figure 1.3 illustrates the threshold frequency for different materials and light frequency.

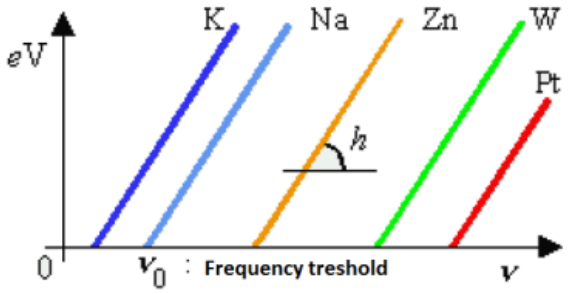


Figure 1.3: Energy of electrons extracted from different materials with respect to the frequency of the electromagnetic wave

1.2.3 PN junction

A PN junction is a semi-conducting device composed of two distinct regions: a P-region where the silicon is positively doped and a N-region where the silicon is negatively doped. In order to reach an equilibrium, a phenomenon of diffusion and recombination of carriers takes place.

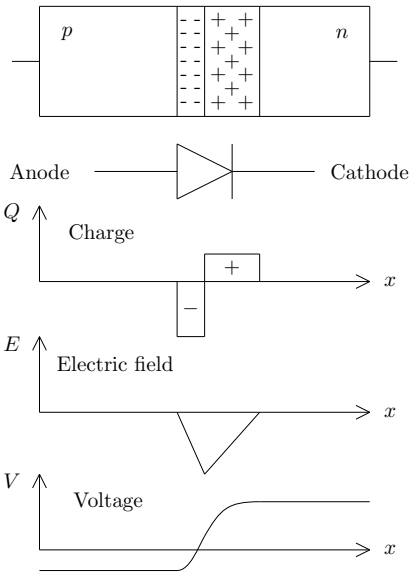


Figure 1.4: Classical PN junction with corresponding quantities

Holes (i.e. positive charges from the P-region) migrate to the N-region to recombine with electrons, while electrons from the N-region (i.e. negative charges) migrate to the P-region to recombine with holes. The introduction of positive ions in the N-region and negative ions in the P-region creates en electric field that is opposed to this diffusion. Once the equilibrium of these phenomenons is reached a depletion region (region free of carrier) is formed. A schematic of a PN junction is depicted in Figure 1.4 with a graph of the corresponding quantities.

1.2.4 Solar cell and solar array

Structure

A solar cell is a semiconductor diode (PN junction) that has been carefully designed and manufactured to efficiently absorb and convert light energy from the sun into electrical energy [5]. A conventional solar cell structure is depicted in Figure 1.5.

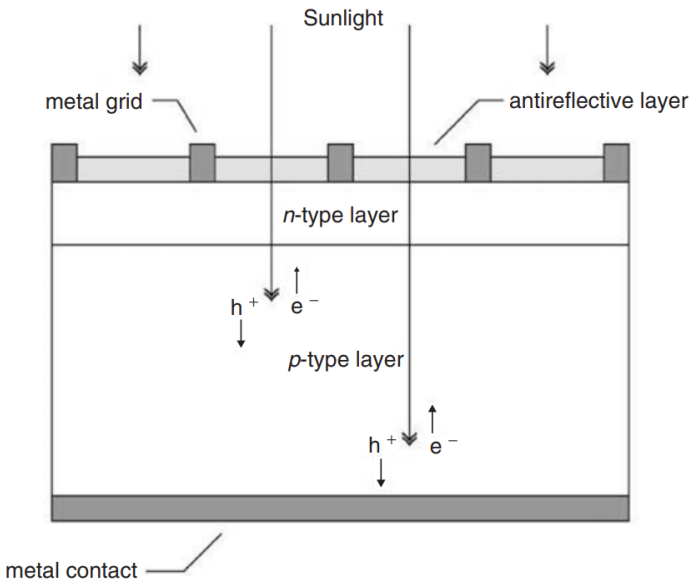


Figure 1.5: Schematic of a conventional solar cell. Creation of electron-hole pairs, e^- and h^+, respectively, is depicted. Courtesy of [5].

A metallic grid forms one of the electrical contacts of the diode and allows light to fall on the semiconductor between the grid lines and thus be absorbed and converted into electrical energy. An antireflective layer between the grid lines increases the amount of light transmitted to the semiconductor.

Equivalent circuit

The equivalent circuit of a single solar cell is illustrated in Figure 1.6. It is made of an ideal current source, a diode and two resistors. The shunt resistor represents the current path through the semiconductor along mechanical defects and material dislocation. The value of R_{sh} is usually very high. The series resistor embodies the series resistance in the outer semiconductor regions such as metals contacts. The value of R_s is usually very low. The current source represents the charge generation in the semiconductor layer of the cell caused by the incident radiation. The diode models the recombination of these charge carriers [6].

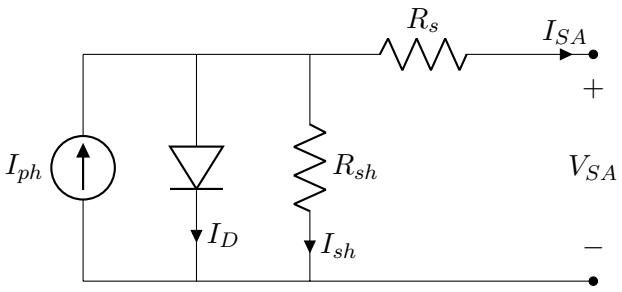


Figure 1.6: Equivalent circuit of a solar cell.

Using Kirchhoff's current law the following relation can be written:

$$I_{SA} = I_{ph} - I_D - I_{sh} \tag{1.3}$$

The current in the diode can be expressed using Schockley's diode equation:

$$I_D = I_0 \left[\exp\left(\frac{q(V_{SA} + I_{SA}R_s)}{nkT} \right) - 1 \right] \tag{1.4}$$

The current I_{sh} is determined using Ohm's law:

$$I_{sh} = \frac{V_{SA} + I_{SA}R_s}{R_{sh}} \tag{1.5}$$

Injecting equations (1.4) and (1.5) in (1.3) yields:

$$I_{SA} = I_{ph} - I_0 \left[\exp\left(\frac{q(V_{SA} + I_{SA}R_s)}{nkT} \right) - 1 \right] - \frac{V_{SA} + I_{SA}R_s}{R_{sh}} \tag{1.6}$$

Under normal circumstances the value of the leakage resistance R_{sh} is very large and the value of the series resistance R_s is very small [11]. From these assumptions, (1.6) is simplified to:

$$I_{SA}(V_{SA}) = I_{ph} - I_0 \left[\exp\left(\frac{V_{SA}}{V_T} \right) - 1 \right] \tag{1.7}$$

where $V_T = \frac{kT}{q}$ is the thermal voltage, I_0 is the saturation current of the diode and n is the ideality factor of the diode and is supposed to be equal to 1. This relation is fundamental and is illustrated in Figure 1.7.

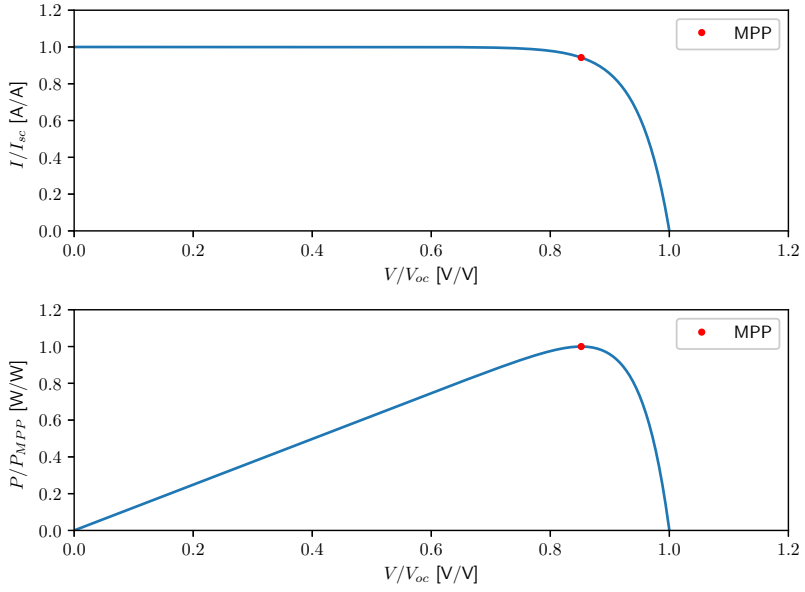


Figure 1.7: Normalized IV and PV curves with its corresponding MPP

Solar array

A solar array is made by the series (resp. parallel) connection of multiple solar cells together increasing the output voltage (resp. current) while keeping the output current (resp. voltage) constant. This is depicted in Figure 1.8.

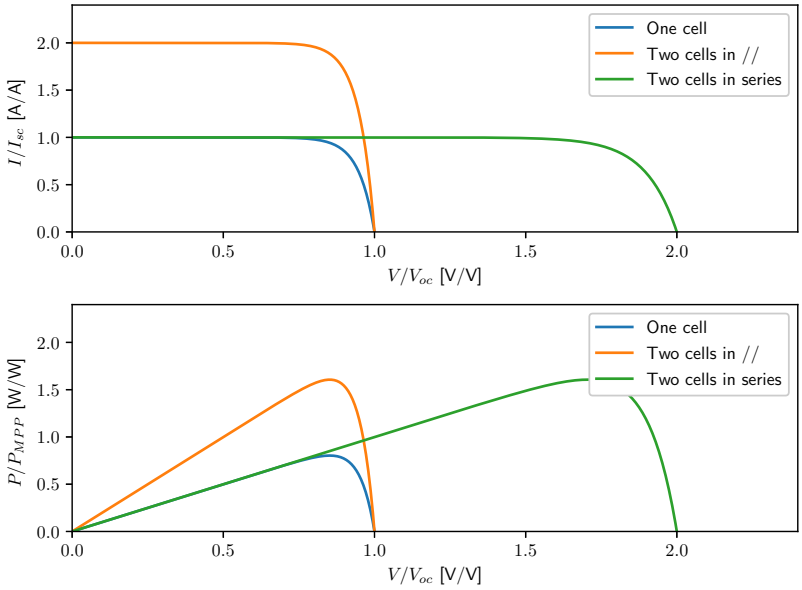


Figure 1.8: Series and parallel connection of two solar cells

Maximum Power Point

Operating the solar array at the voltage V_{MPP} and current I_{MPP} where the power generation is maximal is commonly named the MPP (Figure 1.7). Tracking this point is critical in space mission. In orbit a satellite can experience temperatures from -85°C to 125°C (in LEO) and periods of eclipse where the SA are not exposed to light. These variations are moving the MPP throughout the mission.

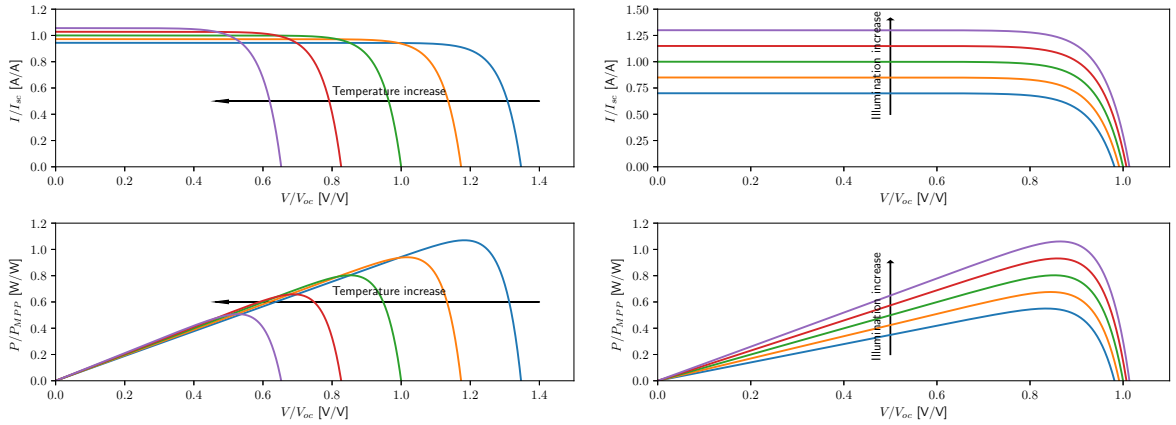
The concept of maximum power point is not specific to solar arrays. Indeed it is greatly used in the wind turbines industry as well as a lot of other applications. This notion is developed in Chapter 2.

Effect of temperature

Temperature has an influence on the IV characteristic. Increasing the operating temperature of the PN junction decreases the performances of the solar array. The open-circuit voltage of a cell decreases on average by 0.35%/°C and the short-circuit current increases on average by 0.056%/°C. This thermal dependence is shown in Figure 1.9a.

Effect of irradiance

Irradiance has an influence on the IV characteristic. An increase of illumination increases the incident power on the solar cell. As a consequence the short-circuit current of a cell linearly increases with illumination but the open-circuit voltage remains almost constant (Figure 1.9b).



(a) Effect of temperature **(b)** Effect of illumination

Figure 1.9: Normalized IV and PV curves under different operating conditions

1.3 Digital Programmable Controller (DPC)

This thesis is aiming at confronting the implementation of MPPT algorithms on a specific micro-processor. This section briefly presents the Digital Programmable Controller (DPC), the micro-processor used in this application.

The Digital Programmable Controller (DPC) (cf. Figure 1.10) is a radiation hardened quad-core micro-processor developed by Thales Alenia Space Belgium (TAS-B). Each core is based on the MSP430 architecture. The DPC was developed in order to replace the controlling analog circuits with their software equivalent. Software solutions are more flexible than hardware which need to be redesigned at every design iteration. In addition, it makes over the air firmware update possible. Typical applications of the DPC range from power conversion control, motor control, intelligent remote sensing and many more.

Figure 1.10: The digital programmable controller ASIC in its CQFP package. Courtesy of [15]

1.3.1 MSP430 CPU

Each core has its own CPU based on the openMSP430 architecture, an opened implementation of the TI MSP430 processor. The MSP430 architecture is a 16-bits RISC CPU based on a von Neumann machine in which an instruction fetch and a data operation cannot occur at the same time as they share the same memory bus. Each core is running at the same frequency (15, 30 or 40 MHz). This clock is known as the system clock and is generated from the 120 MHz master clock.

In addition they are equipped with a watchdog, a least one timer, a long term counter, a barrel shifter and many other peripherals. The watchdog is a timer that should be periodically triggered. If the CPU cannot trigger the watchdog then it means it is stuck in an infinite loop or has encountered a fault. The watchdog emits a signal connected to the reset of the CPU to recover from the fault.

1.3.2 Multi-core segregation

An effort was made in the design of the DPC to avoid fault propagation by isolating critical functions such that each of them can proceed with normal/degraded operation even in case of failure of a neighboring process. As the applications (sensors monitoring, power conditioning, ...) are considered as mission critical, a failure of the DPC might result in a complete loss of the mission.

Here the multi-core term is referring to the fact that each core has its own speciality rather than duplicating multiple instance of the same core as in personal computers. Figure 1.11 is a schematic of the DPC segregation of the three main cores used in flight: SSM, RAS and COM.

1.3.3 Regulation Arithmetic Sequencer

The Regulation Arithmetic Sequencer (RAS) core is responsible for rapid and time critical process control. The main input sources are the Analog to Digital Converter (ADC) allowing massive data acquisition from multiple sensors. Some digital inputs may as well be fed if needed. To process data fast and efficiently, the RAS is equipped with one hardware Multiple and Accumulate (MACC) (16 by 16-bit multiply and 32-bit accumulate) and one hardware 32-bit divide by 16-bit.

The memory resource is limited: 4kB for firmware and 2kB for data. This is made on purpose as the aim of this core is to execute a fast sequence of code repetitively such as a regulation loop. The result of the fast calculation may be output to one of the 6 PWM generators, 3 DAC or any of the 46 IOs.

1.3.4 SPY

The SPY core is aimed at supporting the engineers during the design phase. It offers a non intrusive overview of the registers states of the other cores. This core is not meant to be used in flight.

1.3.5 Communication Module

The Communication Module (COM) core is used for serial data exchange (synchronous or asynchronous). It has two built-in Controller Area Network (CAN) bus and three Universal Asynchronous Receiver Transmitter (UART). Some basic "on-off" commands will be more efficiently managed within the COM module without involving the other cores. This is why it is equipped with the same amount of digital IOs as the RAS. Nevertheless its first task is to be the interface between its environment the DPC itself therefore it embeds a large memory for data buffering (8kB) and for firmware (16kB).

1.3.6 Supervision & System Management

The Supervision & System Management Micro-Controller (SSM) is dedicated to controlling and managing the other cores (e.g. realizing the system state-machine or dynamically update the regulation loop frequency of the RAS). It can also be used for slow regulation loops. As a result it is equipped with a Universal Serial Interface (USI) and four DACs.

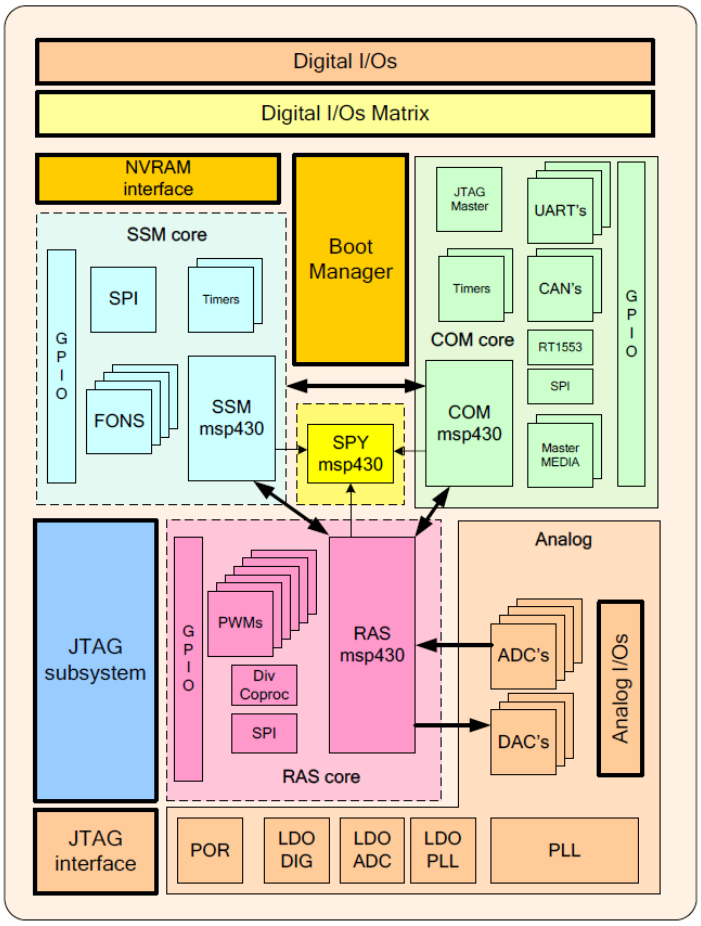


Figure 1.11: Top level block diagram of the DPC showing the core segregation. Courtesy of [15]

Chapter 2

Maximum power point tracking

This chapter is introducing the Maximum Power Point Tracking (MPPT) concept with an analogy to other phenomenons. Then some popular MPPT methods are listed and finally three of them are selected to be implemented on the DPC.

2.1 Universality of energy and power

Regardless of the considered domain, the exchanged power between two systems can be expressed as the product of two quantities:

- Effort, commonly noted e, needed to displace a certain quantity of matter against some resistance of the system.
- Flux, commonly noted f, which characterize the displacement of the matter with a specific flow.

$$P = Effort \times Flux \tag{2.1}$$

Some examples illustrating this concept are summarized in Table 2.1.

Domain	Effort e	Flux f
Electrical	Voltage u	Current i
Mechanical (rotation)	Torque C	Velocity ω
Mechanical (translation)	Force F	Velocity v
Hydraulic, pneumatic	Pressure p	Flow Q
Thermal	Temperature T	Derivative of entropy S

Table 2.1: Universality of power : regardless of the domain, the exchange power is the product of the effort by the flux

Taking the ratio of the effort by the flux denotes the impedance of the system, commonly noted Z. In other words, it characterizes the response of the system to an excitation.

$$Z = \frac{Effort}{Flux} \tag{2.2}$$

In a system when a source is exchanging power with a load, matching the impedances of both the source and the load allow an optimal power transfer. Let us take a simple example. A battery is connected to a resistance. The battery is represented by a voltage source V_{bat} and an internal resistance R_i. The load is modelled by R_L. This circuit is illustrated in Figure 2.1.

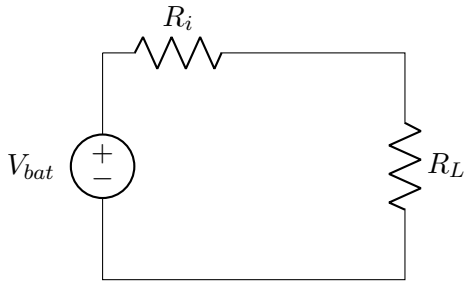


Figure 2.1: A source-load system represented by a battery, its internal resistance and a load resistance

Using Ohm's law, the IV characteristics are represented in Figure 4.11. The intersection of the characteristics is dictating the operating point of the system and the area of the rectangle represents the power. Yet, this point is probably not extracting the maximum power available of the source.

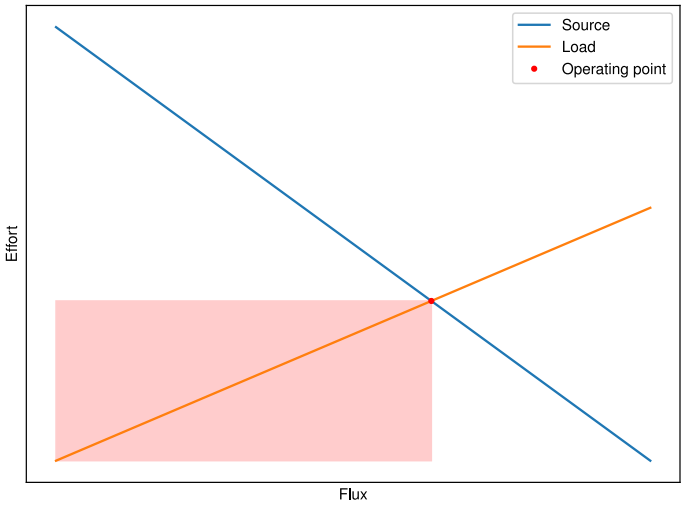


Figure 2.2: The operating point of the source-load system is given by the intersection of the characteristics

The power in the load can be expressed as:

$$P_L = V_L I_L = V_L \frac{V_L}{R_L} = \frac{V_L^2}{R_L} \tag{2.3}$$

The amount of power extracted from the source depends on the load. Taking the derivative of the power with respect to the load resistance yields:

$$\frac{dP_L}{dR_L} = \frac{R_i^2 - R_L^2}{(R_i + R_L)^4} V_{bat}^2 \tag{2.4}$$

This relation is equal to zero if $R_i = R_L$. Consequently the maximum power is extracted when the impedance of the source is equal to the impedance of the load. This is commonly called impedance matching. Depending on the type of application, it can be the source or the load that can be modified in order to extract the maximum power given the specifications. For example, a human driving a car. The motor is the source and the load is the steepness of the road. When the road is becoming steeper, the driver shift gear so that the impedance of the motor seen by the road is matching the impedance of the road.

In the case of a solar cell supplying power to a load, the same reasoning can be applied. Nevertheless, as the environment is impacting the IV characteristic, the MPP is continuously changed. Tracking this maximum power point is fundamental in order to be as efficient as possible.

2.2 Algorithms

Many algorithms have been developed throughout the years: [2] states that at least 19 distinct methods have been introduced in the literature, with many variations on implementation. This section is presenting some popular MPPT techniques used for solar arrays systems. Their major advantages and drawbacks are also listed.

Continuing the analogy with the driver shifting gear to match the steepness of the road, here the gearbox is represented by a DC/DC converter. The goal of the MPPT algorithms is to compute the new operating point of the system. The output is usually a reference voltage or a duty cycle directly fed to the DC/DC converter.

2.2.1 Constant voltage

Working principle

This method keeps the voltage close to the MPP voltage by matching it to a fixed reference. This is based on the assumption that temperature and irradiance variations are not significant enough to move the operating point. This method performs better under low insulation conditions than the Perturb and Observe (P&O) or Incremental Conductance (IC) methods (see sections 2.2.4 and 2.2.5) making it a good candidate when combined with other techniques [3].

Measurement

This method requires a voltage measurement.

Limitations

The major drawback of this technique is the lack of feedback action, therefore there is no real tracking of the MPP. This technique is thus not efficient in changing environments such as a space mission where temperature and irradiance are varying but rather suited for ground-level use such as in a domestic installation.

2.2.2 Fractional open-circuit voltage

Working principle

This method is based on empirical observations stating that the MPP voltage V_{MPP} is always close to a fraction of the open-circuit voltage V_{oc}:

$$V_{\mathrm{MPP}} = kV_{oc} \tag{2.5}$$

where k is a proportional constant depending on the type of solar cells used (usually $k \approx 0.7 \ldots 0.8$).

Measurement

This method requires a voltage measurement.

Limitations

It is necessary to periodically disconnect the cells in order to perform the short circuit voltage measurement causing a non continuous power generation which can be an issue for some applications. A possible workaround is to use a dedicated cell for measurements which is not participating in the power generation. However adding extra hardware can be expensive and add unnecessary weight to the satellite.

2.2.3 Fractional short-circuit current

Working principle

This method is similar to the previous one except that in this case it is the short-circuit current that is used as reference. Empirical data shows that the optimal current I_{MPP} is equal to a fraction of the short-circuit current I_{sc}:

$$I_{\mathrm{MPP}} = kI_{sc} \tag{2.6}$$

where k is a proportional constant depending on the type of solar cells used (usually $k \approx 0.78 \ldots 0.92$).

Measurement

This method requires a current measurement.

Limitations

It is necessary to use a switch capable of putting the system periodically in short circuit in order to perform the measurement. Again, the power generation is not continuous. A similar approach as in the previous method can be used in order to avoid this issue.

2.2.4 Perturb and Observe

Working principle

The perturb and observe method takes advantage of the sign of the slope of the PV curve (see Figure 1.7). On the left of the MPP, the slope is positive and flips to negative on the right of the MPP. The MPP is tracked by comparing the instantaneous power delivered by the solar array with the power delivered during the previous iteration. If the power P_t is higher (resp. lower) than the power at the previous iteration, P_{t-1}, then the operating voltage of the solar array is increased (resp. decreased). The power is computed from the readings of the instantaneous current and voltage which require dedicated sensors.

Measurements

This method requires a voltage and a current measurement.

Limitations

The major drawback of this technique is the constant oscillation around the MPP in steady state as the algorithm doesn't know when the optimum is achieved. This voltage (and current) ripple introduce power losses. Theses oscillations can be reduced (but cannot be cancelled) by decreasing the amplitude of the perturbation applied at every step at the cost of time to achieve the MPP [7]. In addition, rapidly changing conditions of irradiance may lead to never converge towards the optimal point. Despite that, the perturb and observe method remains one of the most popular because of its simplicity and low-cost of implementation. The optimization of the amplitude of the perturbation and the sampling frequency can lead to an increased efficiency as discussed in [1].

2.2.5 Incremental Conductance

Working principle

The Incremental Conductance (IC) is based on the fact that the generated power is $P = VI$ and the maximum value is reached when $dP = 0$. Therefore

$$\begin{aligned} \frac{dP}{dV} &= \frac{d(IV)}{dV} = 0 \\ &= \frac{dI}{dV}V + \frac{dV}{dV}I \\ \Rightarrow \frac{I}{V} &= -\frac{dI}{dV} \end{aligned} \tag{2.7}$$

In other words, it means that the maximum power is generated when the instantaneous conductance is matching the incremental conductance (in absolute value). The major advantage

of this technique is that the algorithm knows when the MPP is reached and therefore there is no steady state oscillation.

The technique is a direct application of the impedance matching method introduced at the beginning of this chapter.

Measurements

This method requires a voltage and a current measurement.

Limitations

Computing the derivatives require more computational power than previous methods.

2.2.6 Three Percent

Working principle

The 3% method is the "go to" method at Thales Alenia Space Belgium (TAS-B). This technique is also based on the incremental conductance. However instead of tracking the null slope of the PV curve, it is the unitary slope of the IV curve that is tracked (see Figure 1.7).

$$\frac{dI}{I} = -\frac{dV}{V} \tag{2.8}$$

The successive decreases of 3% of the current and of the voltage lead to a stabilization around the MPP. Indeed at the unitary slope, decreasing the voltage by 3% leads to an increase of the current by the same amount. Then a decrease of 3% of the current leads to an increase of the voltage by 3%. The value of 3% was kept as it is a good trade-off between convergence speed and power accuracy [13]. Still, any value could be used depending on the specifications of the application.

Measurements

This method requires a voltage and a current measurement.

Limitations

The parasitic capacitance of the SA and the parasitic inductance of the wires are moving the unitary slope and the true MPP is thus not achieved. This effect is further discussed in [12].

2.2.7 Other techniques

Many other techniques exist including variant or optimized versions of the ones presented above. New methods are emerging using more recent technologies such as machine learning and artificial intelligence to achieve similar or better performances [4][14]. Nevertheless these methods are not yet mature enough to be used in flight and will not be discussed in this document.

2.3 Selection

It has been decided to select three algorithms to further continue with this work:

- Perturb & Observe: it is one of the most popular algorithms currently in use due its simplicity, still it comes with great performances.
- Incremental Conductance: this method is very similar to the previous one. Nevertheless it is based on the conductance rather than the power and has no oscillating behavior around the MPP.
- Three Percent : this method is very popular within TAS-B.

The rest of this document will focus on these three methods and their implementation on a space hardened micro-processor. The peripherals and features of the MCU used will be presented as well as how they are configured.

This work is aiming at highlighting the challenges of their digital implementation on that a space hardened micro-processor. The three methods will be tested in order to characterize their static and dynamic behavior.

Chapter 3

MPPT implementation on the DPC

This chapter deals with the digital implementation of the three selected MPPT algorithms: Perturb & Observe, Incremental Conductance and Three Percent. The algorithms are implemented on the Regulation Arithmetic Sequencer (RAS) core of the Digital Programmable Controller (DPC). This core is optimized for rapid regulations and is equipped with various features supporting this function.

First, the peripherals used are presented with their configuration. Then the implementation of the three selected algorithms is further discussed.

3.1 RAS cycle timer

The RAS Cycle Timer (RCT) is an internal peripheral of the RAS core used to sequence the regulation loop by generating a periodic interrupt signal. This signal is used as a time reference to synchronize multiple regulation events such triggering an ADC reading or generating a PWM signal for example.

The RCT is a 16-bit counter clocked at 120 MHz divided by a prescaler. This prescaler generates the signal `Cycle_Tick` which is the minimum time unit of the PWM controllers and the ADC controllers. The prescaler is programmed by writing a 16-bit value in the register `RCT-PRESC`. It can take any value between 0 and 65535 allowing a `Cycle_Tick` frequency of 120 MHz down to 1.8 kHZ.

Additionally, the RCT has also a programmable maximum value `RCT-PER` and can further divide the prescaler cycle tick. Writing a value between 0 and 65535 in the register `RCT-PER` allow to reach a RAS cycle period anywhere between 8.33 ns up to 35.79 s.

$$\texttt{Cycle\_Tick} = \frac{\texttt{RCT-PRESC} + 1}{120\ [\text{MHz}]} \tag{3.1}$$

$$\texttt{RAS\_Cycle} = (\texttt{RCT-PER} + 1)\texttt{Cycle\_Tick} = \frac{(\texttt{RCT-PRESC} + 1)(\texttt{RCT-PER} + 1)}{120\ [\text{MHz}]} \tag{3.2}$$

These parameters are used to set the iteration frequency of the MPPT algorithms. They are summarized in Table 3.1.

Desired frequency	Parameter	Value
1 [Hz]	RCT-PRESC	12000
	RCT-PER	10000
10 [Hz]	RCT-PRESC	12000
	RCT-PER	1000
100 [Hz]	RCT-PRESC	12000
	RCT-PER	100

Table 3.1: RAS cycle timer configuration

3.2 Analog to digital converter

The DPC is equipped with four 13-bit differential signed ADCs with a differential input voltage range between -1.25 [V] and 1.25 [V]. Two ADCs are optimized for small signal differential measurements with good common mode rejection. They cannot be used in single-ended mode. The two others can either be used in single-ended mode or for differential measurements. Moreover, they are equipped with an internal multiplexer allowing to connect and sample up to 14 pins.

3.2.1 Configuration

The ADCs are intrinsically linked to the RCT which synchronizes the PWM and ADC controllers to the firmware. During a `RAS_Cycle`, each ADC can be configured to automatically perform three measurements without firmware action required. For each of the measurements, three registers must be configured.

The configuration multiplexer, `ADCx_MUXy`, which defines the input to be sampled. It allows to select the positive and negative voltages to use for the sampling.

The start instant of the sampling, `ADCx_Ty`, which defines when the sample & hold circuit is connected to the input pin. It is the time (in `Cycle_Tick` units) with respect to the beginning of the RAS cycle marking the start of the acquisition.

Finally the latency, `ADCx_Ly`, which defines the sampling duration. It is the delay (in `Cycle_Tick` units) from the start instant `ADCx_Ty` during which the voltage is applied to the sample & hold capacitors. This delay must be long enough to charge the 2.2 [pF] capacitors. After this delay, the digital conversion begins. This delay is equal to:

$$\frac{3 + 64(\texttt{ADCx\_Ly} + 1)}{120\ [\text{MHz}]}\ [\text{s}] \tag{3.3}$$

The timing diagram of an ADC reading is presented in Figure 3.1. Note that one ADC cannot perform two measurements in parallel. The necessary delay between two start instants is equal to the sum of the hold delay and the conversion delay.

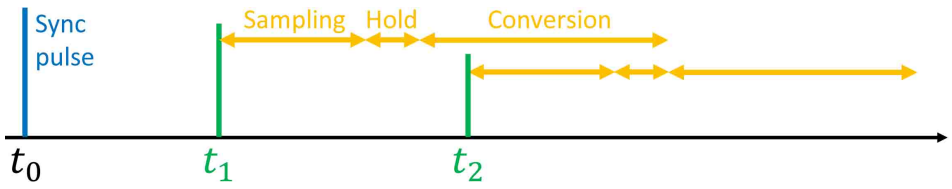


Figure 3.1: ADC measurement timing. Courtesy of [15]

Moreover, the DPC is optimized for a two-period control where the measurements are performed during RAS cycle $n-1$ and the regulation based on these measurements happens in RAS cycle n. This is illustrated in Figure 3.2.

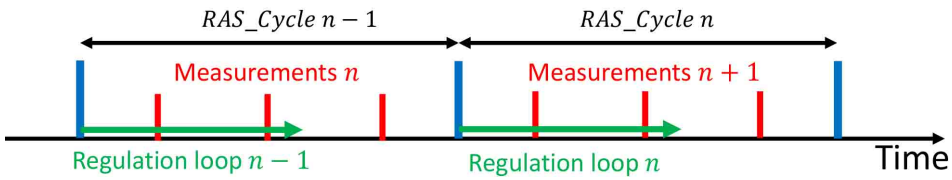


Figure 3.2: Two-periods regulation timing. Courtesy of [10]

3.2.2 Measurements

In the scope of this thesis, the ADCs are configured in single-ended mode to measure a positive pin. As the input voltage of the ADC must be kept between -1.25 [V] and 1.25 [V], the measurement of V_P (the analog voltage to be sampled) must be done between the input positive voltage and the internal mid-rail voltage V_{CM}. Then to obtain a positive digital value between 0 and $2^{13}-1$ for V_P, the digital value of the mid-rail voltage V_{CM} must be added to the measurement. As a result, it is necessary to perform two measurements.

$$meas_D(V_P, V_{CM}) = G \cdot (V_P - V_{CM}) + Off_{ADC} \tag{3.4}$$

$$meas_D(V_{SS}, V_{CM}) = G \cdot (V_{SS} - V_{CM}) + Off_{ADC} \tag{3.5}$$

Then to obtain the single-ended measurement, the difference between the two measurements must be carried out in software.

$$D_{meas} = meas_P(V_P) = meas_D(V_P, V_{CM}) - meas_D(V_{SS}, V_{CM}) = G \cdot (V_P - V_{SS}) \tag{3.6}$$

The nominal gain is $G = 2962.923$ LSB_{13}/V. Note that by subtracting the two measurements cancels the offset of the readings.

The ADC configuration used in this work is described in Table 3.2a for the signals measurements and in Table 3.2b for the mid-rails measurements.

3.3 Digital to analog converter

The RAS core is equipped with three p-type current steering DACs with open drain output. Each DAC is identical and has a 12-bit resolution. The current is fed to an accurate resistor

Input	Parameter	Value
Voltage signal	Instance	`ADC3_MUX1`
	`ADC3_T1`	`RCT-PER/4`
	`ADC3_L1`	1
Current signal	Instance	`ADC4_MUX1`
	`ADC4_T1`	`RCT-PER/4`
	`ADC4_L1`	1

(a) Voltage signals

Input	Parameter	Value
Voltage V_{CM}	Instance	`ADC3_MUX2`
	`ADC3_T2`	`RCT-PER/2`
	`ADC3_L2`	1
Current V_{CM}	Instance	`ADC4_MUX2`
	`ADC4_T2`	`RCT-PER/2`
	`ADC4_L2`	1

(b) Mid-rail signals

Table 3.2: ADC configuration registers

to provide a voltage to the client circuitry and a parallel capacitor for filtering purposes. The circuitry of one DAC is depicted in Figure 3.3.

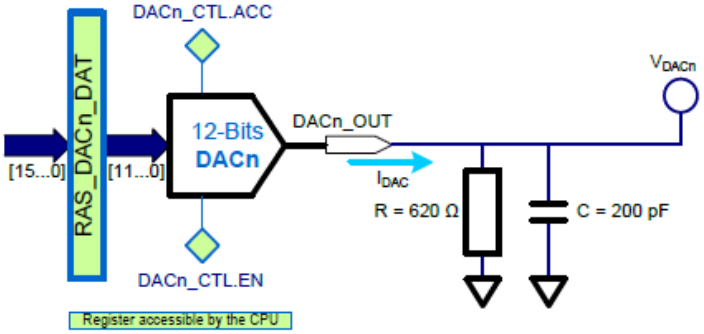


Figure 3.3: DAC circuitry. Courtesy of [15]

3.3.1 Configuration

Two registers are controlling each DAC instance. The `DACx_CTL` register enables the DAC and defines the mode of operation. Two modes are available : normal mode for fast conversion or Dynamic Element Matching (DEM) mode (high accuracy mode). The latter improves its INL/DNL by continuously toggling the transistors combinations used to generate the output.

The `DACx_DAT` register defines the desired output current (and voltage as a consequence). The output current follows this relation:

$$I_{DAC} = G \cdot \texttt{DACx\_DAT} \tag{3.7}$$

with the nominal gain $G = 0.9766$ [µA/LSB$_{12}$]. Assuming an ideal resistor value $R = 620$ [Ω], the voltage is:

$$V_{DAC} = 620 \cdot I_{DAC} \tag{3.8}$$

Using the nominal gain, the ranges of the DACs are $[0 \cdots 4095]$ LSB$_{12}$ $= [0 \cdots 3.9992]$ mA which converted in volts equals to $[0 \cdots 2.4795]$ V.

The DAC used in this application is configured in dynamic element matching mode as fast conversions are not required. In opposition to the ADC, the DAC is not linked to the RCT. Once an instruction loads a new value in the `DACx_DAT` register, the output is instantaneously updated regardless of the RCT timing.

3.4 Hardware multiplier

The RAS core is equipped with a multiply and accumulate co-processor which is physically outside the CPU. The supported operations are: (un-)signed multiply, (un-)signed multiply and accumulate with 16 × 16-bit, 16 × 8-bit, 8 × 16-bit and 8 × 8-bit. A block diagram is depicted in Figure 3.4.

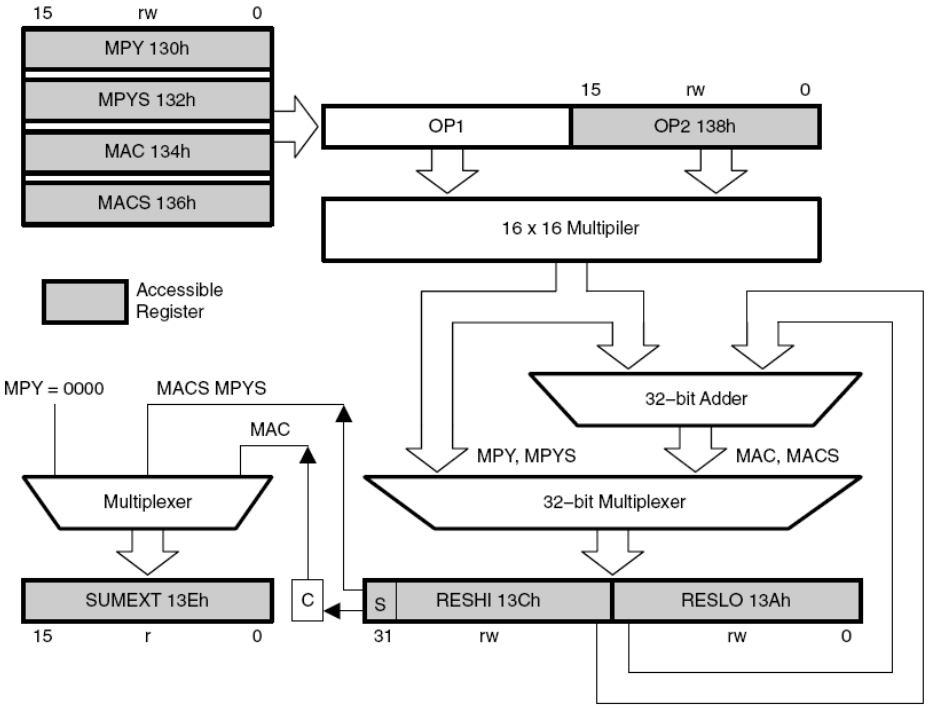


Figure 3.4: Hardware multiplier block diagram. With courtesy of [8]

The hardware multiplier has two 16-bit operand registers: `OP1` and `OP2`, and three result registers: `RESLO` for the low word of the result, `RESHI` for the high word of the result and `SUMEXT` that stores information about the result. The latter is not used in this application.

The operand `OP1` has four addresses, one for each type of operation. Writing the first operand to one of them selects the desired multiplication but does not start any operation. Writing the second operand to the `OP2` registers initiates the selected operation. The result can be read with the next instruction.

The three selected algorithms are using multiplications. It is always the same type of operation used: signed multiplication with 16×16-bit. For the Perturb and Observe method, a multiplication is required for the power. For the Incremental Conductance method, multiplications are required to compute the terms idv and vdi. Finally, for the Three Percent method, a multiplication is required when checking if the decrease of the parameter has reached 3% of the control value. This last case is dealing with decimals values which requires a specific attention. This is further discussed in the next section.

3.5 Fixed point representation

It is common to represent number using a base 10 representation. This means we have ten different numerals (symbols), $0, 1, \cdots, 9$, and a combination of these can represent any number. Counting with a base ten representation works by increasing the least significant digit (rightmost number) until all the symbols are used, then it overflows to 0, the next digit of higher significance is incremented and the incremental substitution of the low-digits resumes.

However, digital electronics is using a base two numeral system commonly known as binary representation. The binary representation uses two numerals, 0 and 1, known as bit. This system was chosen as it is easily transportable to digital electronics circuits where a high voltage level represents a 1 and a low voltage level represents a 0. This is one of the fundamental concepts in computer engineering. Nevertheless, this is only representing positive integers. Representing negative numbers is implemented following the two's complement principle.

The P&O and IC methods do not require floating point nor negative representation but the 3% method does requires both. The DPC is capable of dealing with floating point numbers but not in an efficient manner as is it optimized to perform operations on 16-bit integers data words. Still it possible to perform efficient operations on decimal numbers using the fixed point representation. Usually the Least Significant Bit (LSB) has a weight of $2^0 = 1$, but with the fixed point representation, it can take a weight lower than 1. Depending on the level of precision required by the application, the user can virtually place a comma where he wants.

- Integer representation, 8-bit word with 0-bit of decimal

$$1101\,0110 = 2^7 + 2^6 + 2^4 + 2^2 + 2^1 = 214 \tag{3.9}$$

- Fixed point representation, 8-bit word with 4-bits of decimals :

$$1101.0110 = 2^3 + 2^2 + 2^0 + 2^{-2} + 2^{-3} = 13.375 \tag{3.10}$$

To represent the decimal number 0.97 (used in the 3% method) in a 16-bit two's complement fixed point representation, it has been chosen to assign all bits as decimals with the Most Significant Bit (MSB) used for the sign. The convention for the format is thus one bit for the sign, zero bit for the integer and 15 bits for the decimals.

$$0.97 * 2^{15} = 31784 = 0111\,1100\,0010\,1000 \tag{3.11}$$

where $*$ is the integer product operator.

To perform a signed multiplication on such a number, some rules must be followed. Defining D_1 and D_2 as the number of decimals bits of both operands and considering the operands are 16-bits words, the 32-bits result will have the following format: 1 bit for the sign, $31 - (D_1 + D_2)$ bits for the integers and $D_1 + D_2$ bits for the decimals.

Let us take an example where the operation in base 10 representation is $0.97 \times 123 = 119.31$. The operand 123 will be represented with 1 bit for the sign, 15 bits for the integers and zero bits for the decimal. Following this convention, $123 = 0000\,0000\,0111\,1011$ and using the result of equation (3.11):

$$0000\,0000\,0111\,1011 \times 0111\,1100\,0010\,1000 = 0000\,0000\,0011\,1011\,1010\,0111\,0011\,1000 \quad (3.12)$$

Starting from the MSB, the sign bit is 0 so the result is positive, then the $31 - 0 - 15 = 16$ following bits are the integers bits : $0000\,0000\,0111\,0111 = 119$. The remaining bits are the decimals: $0011\,1010\,0111\,0011\,1000 = 0.2283248901$, giving a final result of 119.2283248901. The result is not exactly correct as there is a loss of precision when converting 0.97 to a binary format. Although this is not an issue as the aim of the 3% method is to decrease successively the current and the voltage by the same amount : in this case it won't be 3% but 3.0664%.

3.6 Inter-cores communication

In order to plot and analyze the experimental results *a posteriori* it is necessary to have a way to record the data. The data acquisition methods are discussed in details in section 4.1.4. One of them makes extensive use of the inter-cores communication, which is a feature of the DPC.

Each one of the three cores used in flight is connected to the other cores using a Dual Port Random Access Memory (DPRAM). This memory is 'write-only' for the transmitting core but read only for the receiving core. This communication structure is illustrated in Figure 3.5. The DPRAM can be interpreted as a mailbox where the emitter drops a letter (i.e. the data to transmit) in the mailbox and the receiver can read that letter.

In this application, the RAS core is the transmitting entity and the COM core is the receiving entity. Once the RAS is done with computing the new voltage reference, it writes the result, as well as some intermediate results for debugging purposes, to the DPRAM connected to the COM core. Then it triggers an interrupt of the COM core in order to signal that new data is available. A dedicated routine of the COM core handles this interrupt and fetches the data. The data is then sent over UART to the main computer[1].

[1]The experimental setup used is detailed in Section 4.1

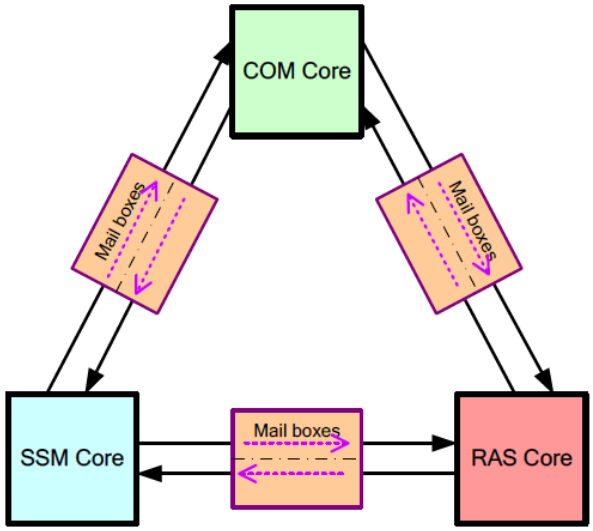


Figure 3.5: Block diagram of the inter-cores communication using mailboxes. Courtesy of [15]

3.7 Algorithms implementation

The selected methods are implemented following the same structure. First the peripherals (RCT, ADC, DAC, ...) are initialized and configured. Then the regulation is taking place during the interrupt routine of the RCT. The full codes are available in Appendix A.

3.7.1 Perturb & observe

The flowchart of the perturb and observe method implemented in the DPC is depicted in Figure 3.6. When the RCT interrupt is raised, the first instruction executed is to read the registers of the ADCs and fetch the current (in this case represented by a voltage, more details in Section 4.1) and voltage measurements as well as the mid-rails voltages. Theses values are stored in `T_INT16` variables[2]. Then, according to equation (3.6), the instantaneous current and voltage are computed. Again, the results are stored in `T_INT16` variables.

[2] `T_INT16` variables can hold a signed 16-bit data word. The sign is handled with the two's complement convention.

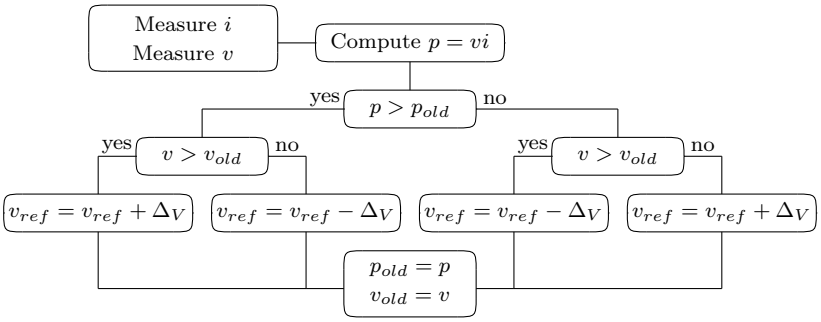


Figure 3.6: Flow chart of the Perturb and Observe (P&O) method implemented in the DPC

The next step is to compute the instantaneous power. This is done using the hardware multiplier. The two operands are the current and voltage and the operation is a signed multiplication (`MSYS`). Multiplying two 16-bit values yields a 32-bit result. In order to make the code more readable, a dedicated structure was created in order to store the 16-bit high word and 16-bit low word of the result. The access of the 32-bit value is then much more easier.

```
typedef union {
  T_INT32 int32;
  struct {
    T_UINT16 int16_lo;
    T_INT16 int16_hi;
  } WORDS_HILO;
}T_INT_32_16HI_16LO;
```

In order to know if the reference voltage should be in-/decreased, the values of the power and voltage of the previous iteration are compared. The new reference voltage is then written in the `DAC1_DAT` register. Once a new value is written, the analog output voltage is instantaneously updated.

Finally the current values of the power and voltage are stored for the next iteration.

3.7.2 Incremental conductance

The flowchart of the incremental conductance method implemented in the DPC is depicted in Figure 3.7. The first few instructions that compute the instantaneous current and voltage are similar as the perturb and observe method.

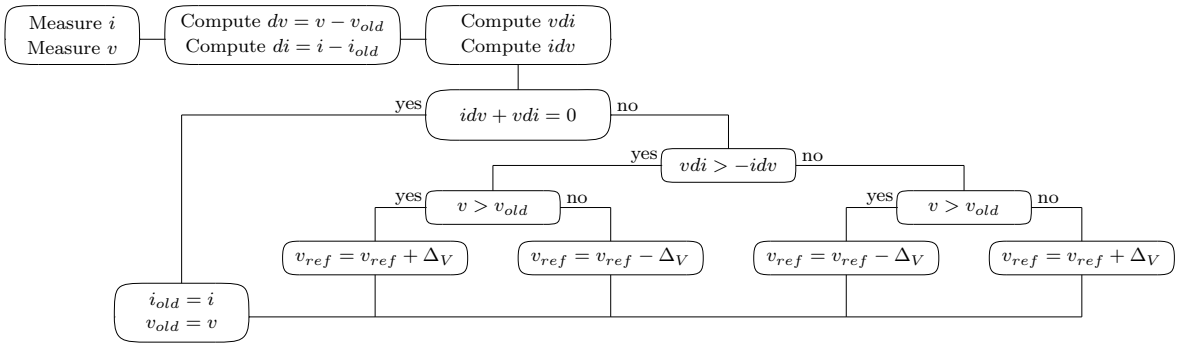


Figure 3.7: Flow chart of the incremental conductance method implemented in the DPC

The variations of current and voltage are then computed using the values from the previous iteration. The results are stored in `T_INT16` variables. At this stage, all the values necessary to evaluate the relation (2.7) are available. However, the hardware multiplier does not support divisions. Consequently, it has been decided to rearrange the terms to avoid divisions in favor of multiplications. The new relation to evaluate if the MPP is reached is therefore:

$$idv + vdi = 0 \tag{3.13}$$

This relation is only using multiplications which can be easily computed using the hardware multiplier. Again the type of operation is a signed multiplication and the results are stored in a structure allowing an easy access to the 32-bit value.

The next instructions are determining if the new reference voltage should be in-/decreased. Finally the current and voltage are stored for the next iteration.

3.7.3 3% method

The flowchart of the three percent method implemented in the DPC is depicted in Figure 3.8. The first few instructions in order to compute the instantaneous current and voltage are similar as the two previous methods.

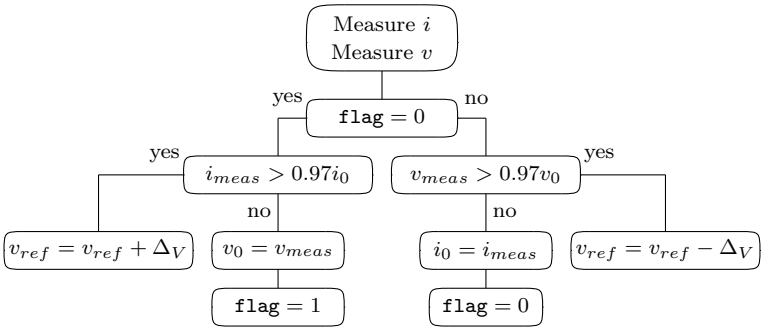


Figure 3.8: Flow chart of the three percent method implemented in the DPC

A flag is used in order to keep track if the current state is to decrease the current or to decrease the voltage. The two phases are pretty similar, which explains the symmetry within the flowchart. Let us take the example with the right side of the flowchart.

The flag is set to 1, therefore the current phase is to decrease the voltage. The first step is to check if the three percent decrease is achieved. To this end, the instantaneous voltage is compared to the value $0.97 \times i_0$. This term is computed as usual using the hardware multiplier. Yet this time, one of the operand is a decimal number. The 0.97 operand is converted to a fixed point binary notation as explained in Section 3.5. Then the multiplication can be performed and the results stored in the same structure as the two previous methods.

If the 3% are not achieved, the reference voltage keeps being decreased. On the other hand, if the condition is met, the new reference parameter is measured (i.e. the current) and the flag is set to 0 for the next iteration. The same logic is used to determine if the 3% are reached, however instead of actually decreasing the current, it is the voltage that is increased.

Chapter 4

Experimental results

This chapter is dealing with the experiments performed to characterize the behavior of the algorithms. First, the setup is presented and qualified. Then, the static and dynamic results are discussed. Finally, some of the issues encountered during the test campaign are listed.

4.1 Experimental setup

The experimental setup used to perform the tests is based on the concept of Hardware In the Loop (HWIL). This testing technique allows to avoid unnecessary complexity by modelling complex systems with a mathematical representation. In the case of this thesis, it would have been difficult to use a real solar array in order to perform the tests. One could think of the size of the installation to be the issue but it is rather the ability to recreate the exact same environment (temperature and illumination) for each experiment. Therefore it was chosen to model the solar array with its equivalent model. Figure 4.2 illustrates the blocks used in the setup while Figure 4.1 shows the test bench used in the lab. The following sections are further describing each block individually. Finally the results of the validation of the setup are discussed.

Figure 4.1: Test bench used in the lab

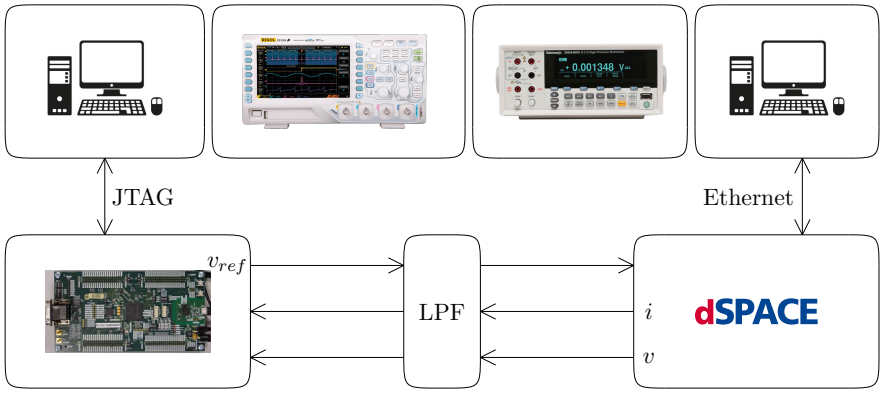


Figure 4.2: Block diagram of the experimental setup

4.1.1 DPC launch kit (DLK)

A test platform was developed by TAS-B in order to help engineers in the development of a space application with the DPC. This platform allows the following activities : demonstrations, applications firmware development, firmware unit tests and firmware integration test at instance, board or equipment software level.

The DLK provides access to the DPC signals and has ready-to-use transceivers, indicators and stimulators. The board also has connectors allowing the user to easily plug its application hardware that has to cooperate with the DPC, in this case, the dSPACE.

This block is the core of the experimental setup. Two ADCs are used to measure the operating conditions of the (model of the) solar array i.e the voltage and current. From the readings a new reference voltage is computed and output on one of the DAC.

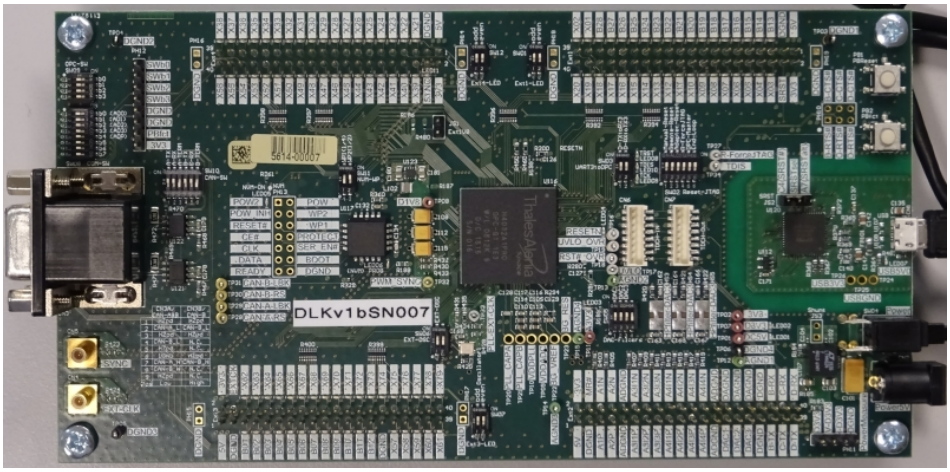


Figure 4.3: Digital Programmable Controller Launch Kit (DLK)

4.1.2 dSPACE

The dSPACE (Figure 4.4) embeds a powerful IBM processor and a Xilinx FPGA as well as many IOs, DACs, ADCs and communication peripherals. The processor is programmed using Simulink (Matlab) with blocks from the SDK. The Simulink diagram is transformed in C language and then compiled to run on the processor. The FPGA is not used in this application. The dSPACE is widely used in the automotive industry for testing purposes.

Figure 4.4: MicroAutoBox, dSPACE

The block diagram embedded in the dSPACE is shown in Figure 4.5. An ADC reads the reference voltage output from the DLK and outputs the same voltage as the operating voltage of the solar array. The reference voltage is also fed into the IV block which models the solar array (developed in the next section). The output of this block is the current of the solar array.

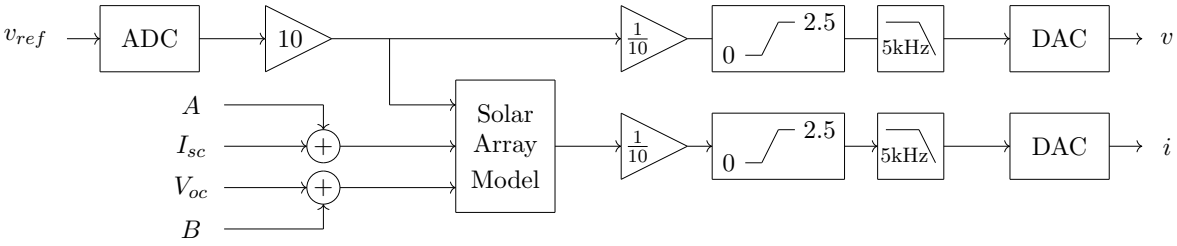


Figure 4.5: Block diagram embedded in the dSPACE

The gain blocks after the ADC (10) and before the DAC (1/10) are scale factors to match the electrical specifications of both the DLK and the dSPACE. A saturation block is also used on signals going to the DLK. It limits the voltage between 0 and 2.5 V to avoid damaging the DLK in case of an issue. Finally a bandwidth of 5 kHz is used to represent the very large capacitor bank placed on the voltage bus of a satellite. It models the inertia of the system when changing the operating voltage of the bus.

4.1.3 Solar array model

The solar array block presented in the previous section is representing a simplified mathematical model of the equivalent circuit of a solar array. Starting from equation (1.7), the following relation was derived. This relation is used to facilitate the changes in temperature and illumination during the test campaign.

$$I(V) = (I_{sc} + A) - \exp\left(\frac{V - (V_{oc} + B)}{V_T}\right) \tag{4.1}$$

Table 4.1 summarizes the parameters and the values of this model. The value of I_{sc} and V_{oc} are purposely chosen to be in the middle of the range of the DAC and ADC. This makes it possible to perturb those values by ± 1 V (i.e up to 80% in both directions) without violating the electrical specifications of the DLK. The parameter A offsets the short circuit current. This perturbation models changes in the illumination of the solar array while parameter B offsets the open circuit voltage which represents a change in temperature of the solar array.

Parameter	Typical value	Description
I_{sc}	1.25 [V]	Short circuit current
V_{oc}	1.25 [V]	Open circuit voltage
V_T	0.0259 [V]	Thermal voltage
A	$-1, \cdots, 1$ [V]	Illumination perturbation model
B	$-1, \cdots, 1$ [V]	Temperature perturbation model

Table 4.1: Parameters of the mathematical model of the IV curve in the dSPACE

Figure 4.6 illustrates the nominal curve (i.e. A and $B = 0$). For the sake of simplicity the current of the solar cell is modelled by a voltage. In a real application, the current measurement should be first converted to a voltage.

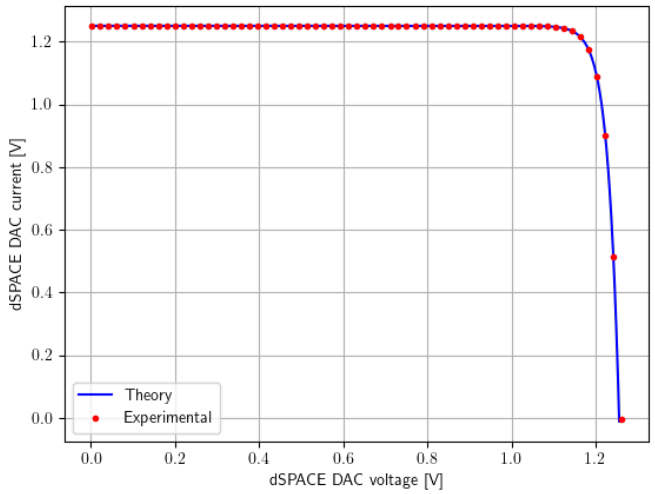


Figure 4.6: Nominal IV curve embedded in the dSPACE

4.1.4 Data acquisition

To analyze the experimental results, multiple data acquisition methods are used. Oscilloscope probes are measuring the three main signals: v_{ref}, v and i. This method is very helpful for rapid and visual checks of the waveforms but not very precise in the measured quantities. A 6 1/2 digits multimeter was used during the setup validation tests for precise and accurate voltage measurements.

In order to gather the values of the DAC and ADC registers, the Dual Port Random Access Memory (DPRAM) between the RAS core and the COM core is used. At each iteration of the algorithm, the RAS core stores these values in the DPRAM and then triggers an interrupt of the COM core. The COM core then fetches the data from the DPRAM and sends them over UART. A python script running on the main computer reads the serial port and prints the data in a terminal and a to a `csv` file for post experiment data analysis.

In addition, to limit noise on the readings, a low pass filter is placed on each of the three signals. This low pass filter has a time constant of $\tau = 2\pi \times 680\ [\Omega] \times 1\ [\mu F] = 4.275\ [ms]$ which gives a cutoff frequency of 234.051 [Hz]. This low pass filter is soldered on a prototype perf-board and plugged directly on the connectors of the DLK.

4.1.5 Setup validation

In order to validate the experimental setup, a test campaign was performed aiming at retrieving the gains and offsets of the DAC and ADC of the DLK and the gain and offset of the DLK-dSPACE-DLK loop. These tests consisted in incrementing the DAC value by 32 LSB_{12} every 10 seconds and measuring the voltages at the different stages of the loop. In addition the digital values are stored in a file at each time step. The results are illustrated in Figures 4.7, 4.8 and summarized in Table 4.2.

	Expected gain	Experimental gain	Offset	Units
dSPACE	1	1.001065	0.000569	V/V
DAC DLK	0.000605	0.000614	0.002405	LSB_{12}/V
ADC DLK	2962.962	2961.756	59.35372	V/LSB_{13}
Loop	2	1.820943	68.16496	V/V

Table 4.2: Results of the validation tests

The first three lines of Table 4.2 are consistent with what was expected. Indeed the dSPACE is simply outputing the same value as its input and the DAC/ADC of the DLK have a gain close to what is stated in the datasheet. However the gain of the loop DLK-dSPACE-DLK was predicted to be 2. As mentioned in Section 1.3, the DAC of has a 12 bits resolution while the ADC has 13 bits, hence the factor 2. Nevertheless, the experimental results suggest a gain of 1.82.

To better understand this result, it is useful to manually compute the values at each step of the loop:

- Let us assume the DPC has the value 1234 [LSB_{12}] in its `DACn_VAL` register. Using the theoretical gain (c.f. Table 4.2), the analog output value is $0.000605 \times 1234 = 0.746\,57$ [V].
- The dSPACE output value is $0.74657 \times 1.001065 + 0.000569 = 0.747\,93$ [V].
- The DAC of the DPC reads the analog value and stores the result it its `ADCn_VAL` as $0.74793 \times 2962.962 = 2215$ [LSB_{13}].

Computing the ratio `ADCn_VAL/DACn_VAL` yields the value 1.79 which is close to the experimental gain of 1.82. This can be explained as the digital full scale range of the DAC and the ADC are different.

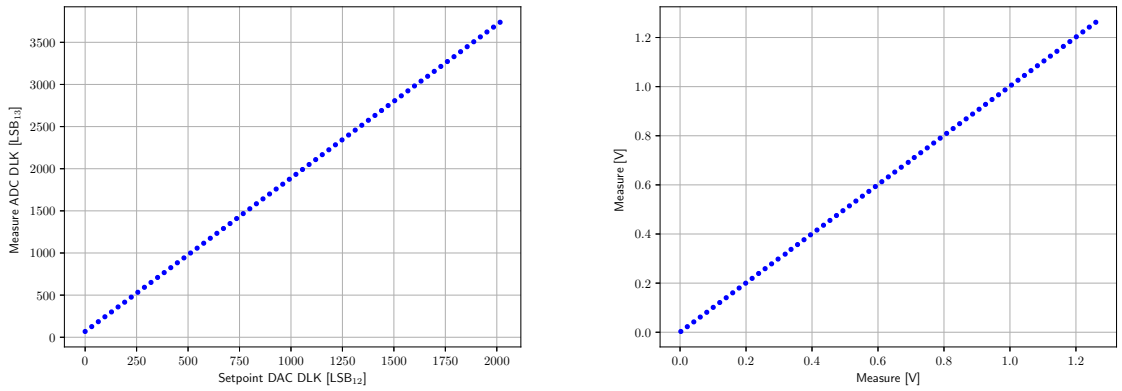
The dynamic of the DAC is 2.478 08 [V]. While the ADC has a theoretical range of

$$\frac{2^{13}}{2962.962} = 2.7648 \text{ [V]} \tag{4.2}$$

However the DAC is limited to 2.5 [V] which is equivalent to (using experimental results):

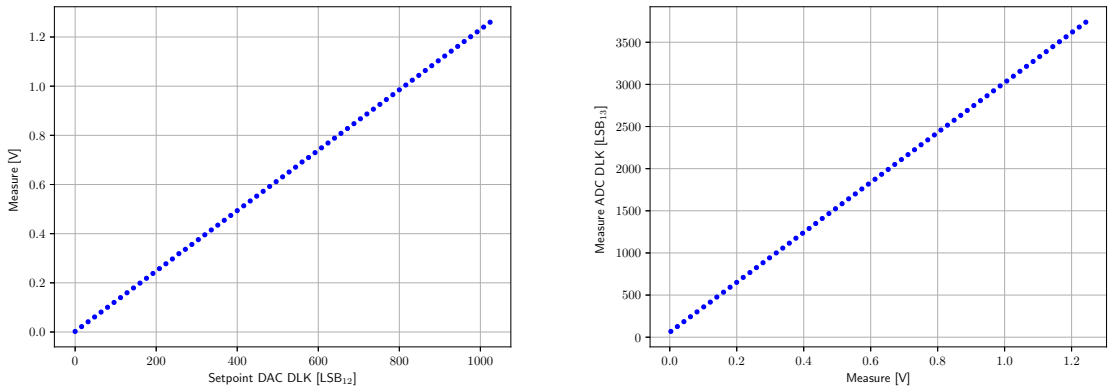
$$2.5 \times 2961.756 + 59.35371 = 7463 \text{ [LSB}_{13}\text{]} \tag{4.3}$$

This is the reason why the experimental results suggest a ratio of $7463/4096 = 1.82$.



(a) Loop DLK-dSPACE-DLK **(b)** dSPACE

Figure 4.7: Results of the experimental setup validation



(a) DAC DLK **(b)** ADC DLK

Figure 4.8: Results of the experimental setup validation

4.2 Static tests

4.2.1 Tests description

Static test means that the IV characteristic of the solar panel is static. There is no perturbation of temperature nor illumination (all parameters are nominal) as the aim is to evaluate the performance of the algorithms in steady state.

Each algorithm will be tested with three different frequencies of iteration: 1, 10 and 100 Hz with a voltage increment on the reference voltage of 32 LSB_{12}. Another test will be performed at 10 Hz but with a voltage increment of 16 instead 32 LSB_{12}. The metrics recorded are the current i, the voltage v (thus the power $p = iv$ as well), the number of iterations to converge to the MPP and the time required for one iteration.

The parameters of the solar panel characteristic used for theses tests are shown in Table 4.3.

I_{sc}	V_{oc}	V_T	A	B	I_{MPP}	V_{MPP}	P_{MPP}
1.25 [V]	1.25 [V]	0.0259 [V]	0	0	1.222 62 [V]	1.156 81 [V]	1.414 34 [V]

Table 4.3: Parameters of the static IV characteristic (i.e. nominal curve)

4.2.2 Results

For each recorded metric, the average value, minimum value, maximum value and ripple were computed as well as the ratio between the average value and the theoretical MPP. The results are summarized in Tables 4.4, 4.5 and 4.6. An attentive reader will spot some unexpected results. These are discussed in the following section.

		i					v				p				Iterations	
		avg LSB13	MPP %	min LSB13	max LSB13	ripple LSB13	ripple %	avg LSB13	MPP %	min LSB13	max LSB13	ripple LSB13	ripple %	avg LSB13	MPP %	min $LSB13^2$	max $LSB13^2$	ripple $LSB13^2$	ripple %	#	t [us]
16 [LSB12]	10 [Hz]	3580.51	98.84	3560	3601	41	1.15	3460.54	100.96	3447	3474	27	0.78	12390306.13	99.79	12356760	12420000	63240	0.51	120	3.10
32 [LSB12]	1 [Hz]	3543.37	97.81	3479	3604	125	3.53	3475.02	101.38	3445	3507	62	1.78	12313282.77	99.17	12197374	12423144	225770	1.83	61	3.08
32 [LSB12]	10 [Hz]	3541.83	97.77	3479	3603	124	3.50	3475.79	101.41	3446	3505	59	1.70	12308973.17	99.13	12190416	12423144	232728	1.89	61	3.08
32 [LSB12]	100 [Hz]	3452.34	95.30	3230	3607	377	10.92	3504.04	102.23	3444	3564	120	3.42	12091771.53	97.38	11505260	12433329	928069	7.68	60	3.10

Table 4.4: Perturb & Observe : static results

		i					v				p				Iterations	
		avg LSB13	MPP %	min LSB13	max LSB13	ripple LSB13	ripple %	avg LSB13	MPP %	min LSB13	max LSB13	ripple LSB13	ripple %	avg LSB13	MPP %	min $LSB13^2$	max $LSB13^2$	ripple $LSB13^2$	ripple %	#	t [us]
16 [LSB12]	10 [Hz]	3580.09	98.82	3553	3636	83	2.31	3459.30	100.92	3414	3476	62	1.79	12384298.74	99.73	12346596	12422988	76392	0.61	121	3.52
32 [LSB12]	1 [Hz]	3544.91	97.85	3481	3606	125	3.52	3474.29	101.36	3444	3507	63	1.81	12311467.92	99.15	12190482	12430040	239558	1.94	60	3.6
32 [LSB12]	10 [Hz]	3541.43	97.76	3482	3604	122	3.44	3476.70	101.43	3446	3506	60	1.72	12313290.12	99.16	12200928	12426747	225819	1.83	61	3.6
32 [LSB12]	100 [Hz]	3453.36	95.32	3236	3607	371	10.74	3504.88	102.25	3444	3564	120	3.42	12098324.23	97.43	11526632	12433645	907013	7.49	63	3.54

Table 4.5: Incremental Conductance : static results

		i					v				p				Iterations	
		avg LSB13	MPP %	min LSB13	max LSB13	ripple LSB13	ripple %	avg LSB13	MPP %	min LSB13	max LSB13	ripple LSB13	ripple %	avg LSB13	MPP %	min $LSB13^2$	max $LSB13^2$	ripple $LSB13^2$	ripple %	#	t [us]
16 [LSB12]	10 [Hz]	3624	100.06	3555	3676	121	3.33	3416.15	99.66	3355	3476	121	3.54	12381591.38	99.71	12322915	12427629	104714	0.84	121	2.97
32 [LSB12]	1 [Hz]	3578	98.76	3481	3661	180	5.03	3448	100.59	3385	3505	120	3.48	12333470.98	99.32	12197446	12423144	225698	1.82	61	2.94
32 [LSB12]	10 [Hz]	3579	98.79	3480	3660	180	5.02	3446.76	100.55	3384	3505	121	3.51	12332496.12	99.32	12193964	12422988	229024	1.85	61	2.94
32 [LSB12]	100 [Hz]	3530	97.45	3228	3687	459	13.00	3447.78	100.58	3327	3565	238	6.90	12159115.52	97.92	11501364	12437250	935886	7.69	60	2.98

Table 4.6: Three Percent : static results

4.2.3 Discussion

Globally, the three algorithms are performing very well with an average extracted power of more than 99% of the maximum available power and with a ripple smaller than 2%. The average current and voltage have less than 2.5% deviation from the theoretical values MPP values.

The same amount of iterations is required by each method, 60 with $\Delta_V = 32$ LSB_{12} and 120 with $\Delta_V = 16$ LSB_{12} which is expected as they all use the same voltage increment. In addition, with an increment two times smaller (16 instead of 32 $_{12}$) it is expected to converge in twice as many iterations and it is the case. The time required for each iteration is roughly the same (≈ 3 [µs]). Let us note that all multiplications are performed with the hardware multiplier which accelerates the computations of these operations.

The voltage ripple is smaller than the current ripple

With a voltage increment of 32 LSB_{12}, both at 1 and 10 Hz, the ripple on the current is higher than the ripple of the voltage. Theoretically, these values should be equal as the MPP is located at the unitary slope of the IV characteristic. Therefore the amplitude of the oscillations should be similar for both the current and voltage.

To justify this inconsistency, it is interesting to look at the slope of the discretized curve around the MPP. Indeed, since the operation points are by definition multiples of the voltage increment, the curve is no longer continuous but discrete. Figure 4.9 illustrates the value of the slope around the MPP as a function of the value of the voltage increment Δ_V.

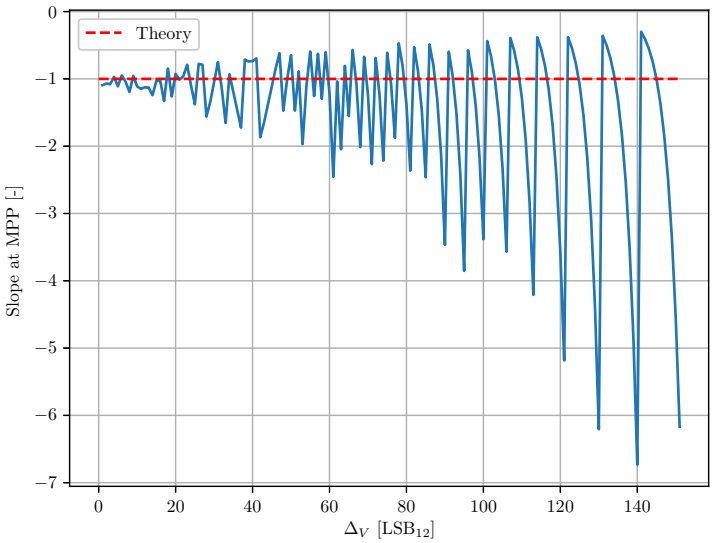


Figure 4.9: Evolution of the slope at MPP in function of the voltage increment Δ_V

The slope is generally more negative than the theoretical slope of -1 (red dashed line). This figure also highlights the fact that the slope has a strong dependence on the value of the voltage increment.

Intuitively, one could say that it is enough to choose the smallest possible voltage increment in order to be as close as possible to the theoretical curve. Following this logic, the slope should tend towards -1 by making Δ_V tend to 0. Although the general trend confirms this hypothesis, still some points do not obey this rule. In addition, there is a periodic pattern increasingly amplified as the voltage increment gets larger. This can be explained quite easily. When the algorithm is in steady state, it oscillates between two points. One to the left of the MPP and the other to the right. These two points are spaced horizontally by Δ_V and the slope can be computed as:

$$m = \frac{i_{right} - i_{left}}{\Delta_V} = \frac{i_{right} - i_{left}}{v_{right} - v_{left}} \tag{4.4}$$

However, the true MPP is initially closer to the left point and by increasing Δ_V, both points (left and right) move to the right. The slope becomes more and more negative. However, as the left point passes the true MPP, it becomes the right point (and therefore the previous point becomes the left point). The slope becomes shallow again and the process continues. This phenomenon is illustrated in Figure 4.10 where a zoom is made around the MPP and the slopes with several successive Δ_V values are represented.

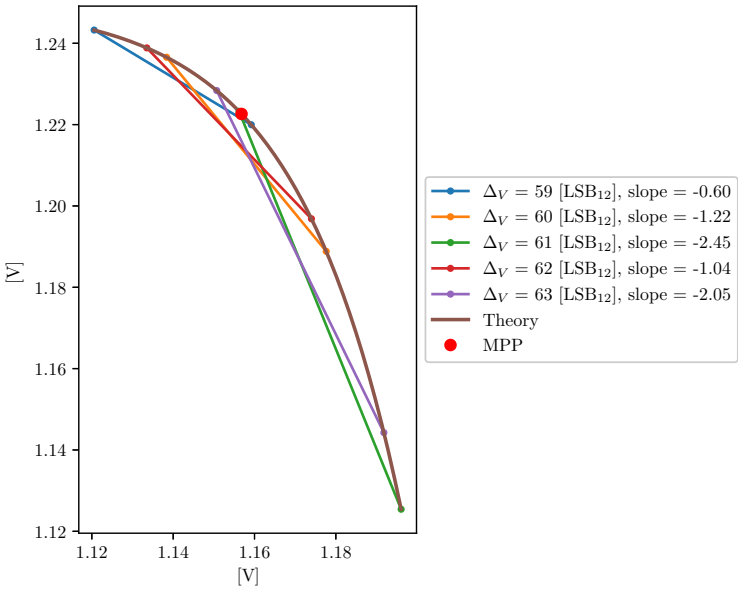


Figure 4.10: Zoom on the slope at MPP to highlight the periodic pattern

Another intriguing aspect in Figure 4.9 is that with a Δ_V of 145 LSB_{12}, the slope happens to be perfectly -1 as indicated by the theory. Careful, this does not mean that the curve is the same as in theory. On the contrary, this is a pure coincidence ! Given that in regime, the algorithm oscillates between the left and right points, the average is:

$$(v_{avg}, i_{avg}) = \left(\frac{v_{right} - v_{left}}{2}, \frac{i_{right} - i_{left}}{2} \right) \tag{4.5}$$

Over a long time interval, the operating point can be considered to be at the average point. Therefore, it is possible to compare the average extracted power (red rectangle, Figure 4.11) with respect to the maximum available power (blue rectangle). Once again, the discretization plays against us because it does not allow to operate at the true MPP.

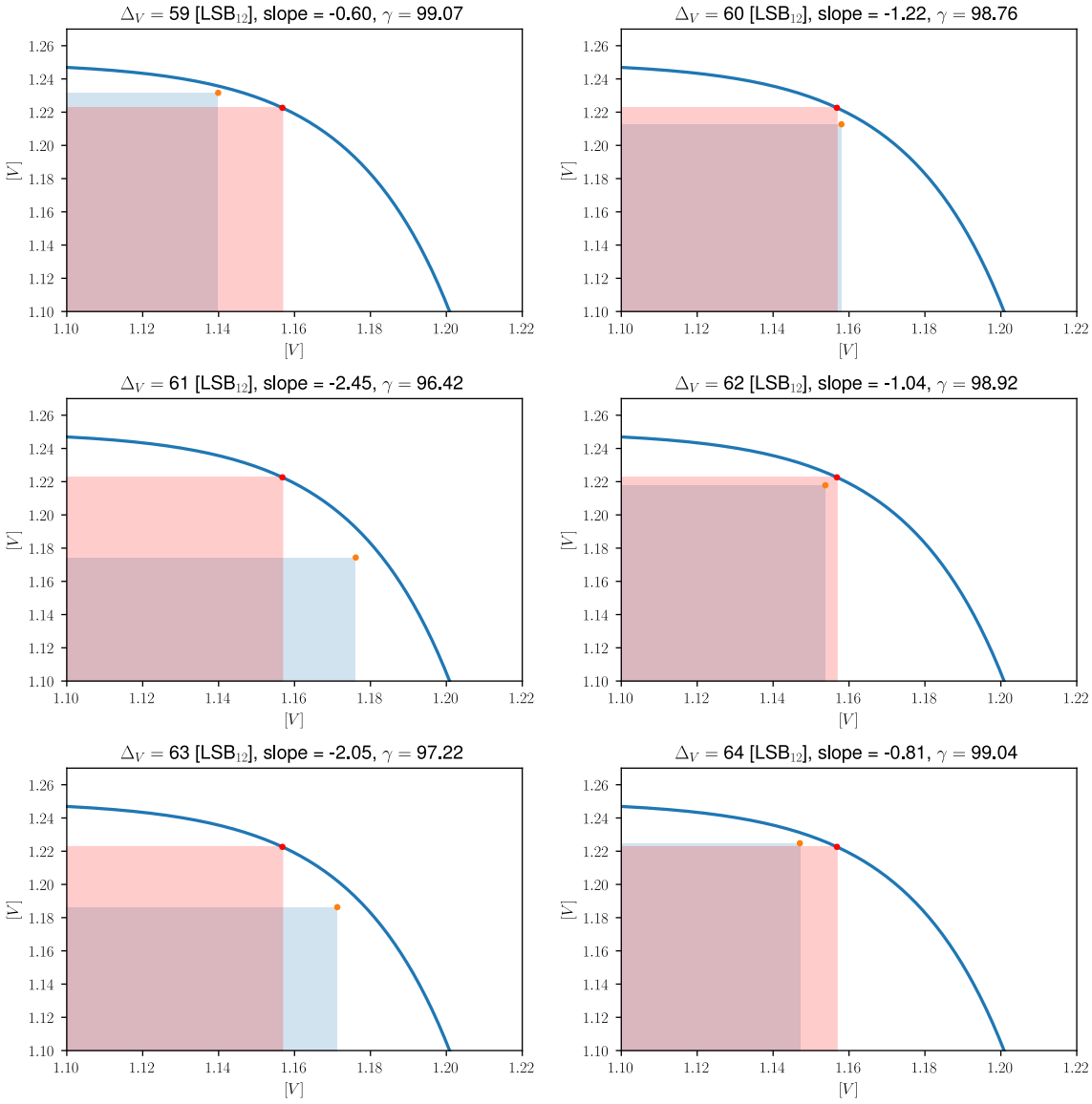


Figure 4.11: The discretization does not allow to operate at the true MPP

The parameter γ is defined as the ratio of the average extracted power with respect to the

maximum power of the SA:

$$\gamma = 100\frac{P_{avg}}{P_{max}}\% \tag{4.6}$$

Its value as a function of the voltage increment Δ_V is depicted in Figure 4.12. This also highlights another aspect to consider when choosing a suitable value of Δ_V, such that while the majority of the experimental tests were performed with a value of 32 LSB_{12} and some tests with 16 LSB_{12}, the average power extracted is 0.1% better with 16 LSB_{12} at the cost of a large loss in robustness. Indeed, the lower the value of Δ_V, the closer it gets to the noise level of the ADC/DAC.

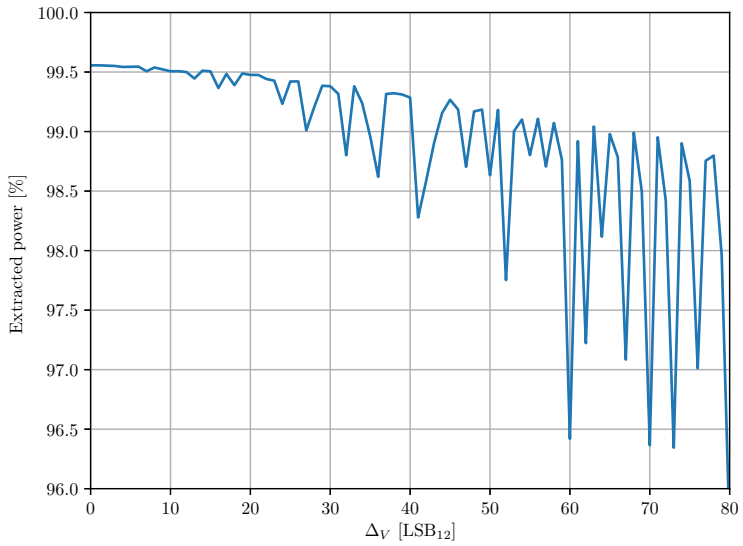


Figure 4.12: Evolution of the parameter γ in function of the voltage increment Δ_V

Poor performances at 100 Hz

The tests performed at 1 and 10 Hz are showing similar results however at 100 Hz, the performance is significantly degraded for the three methods. The average extracted power decreased to 97%. This is unexpected as the bandwidth modelling the inertia of the solar array is set at 5 kHz which is more than a decade above the operating frequency. In addition, this phenomenon happened with each of the three algorithms.

This is the consequence of the low pass filter used to smooth the signals. As a reminder the cutoff frequency of this filter is 234 Hz, which is very close to the 100 Hz at which the algorithms poorly performs. Consequently, it has been decided not to further test/discuss the algorithms at 100 Hz for the static/dynamic tests since their poor performance is caused by an external block which is not part of the Maximum Power Point Tracking (MPPT) methods themselves.

Oscillations around MPP with incremental conductance method

The major benefit of the incremental conductance algorithm, compared to the two others, is that it knows when the MPP is reached because the derivative of the power is null. As a consequence the voltage reference should not be updated as the MPP voltage is achieved. Yet the static results show an oscillation when it has converged to the MPP.

The condition used to detect the MPP is :

$$-idv = vdi \tag{4.7}$$

This condition is never exactly met due to the noise in the ADC readings. A possible workaround would be to set a threshold at which the condition is supposed true but the condition is based on derivatives that can take very high values. Indeed when performing the multiplications, the high values of the derivatives are amplifying the readings and their noise.

4.3 Dynamic tests

4.3.1 Tests description

In order to characterize the dynamic behavior and analyze the stability of the algorithms under rapidly changing conditions, four types of tests were performed.

- Temperature perturbation
  - Step on the open-circuit voltage V_{oc}
  - Ramp on the open-circuit voltage V_{oc}
- Illumination perturbation
  - Step on the short-circuit current I_{sc}
  - Ramp on the short-circuit current I_{sc}

These perturbations were achieved using the parameters A and B from equation (4.1). The time evolution of a ramp perturbation and a step perturbation are respectively depicted in Figures 4.13. These perturbations are modifying the IV characteristic of the solar array and consequently the maximum power point is now a function of time.

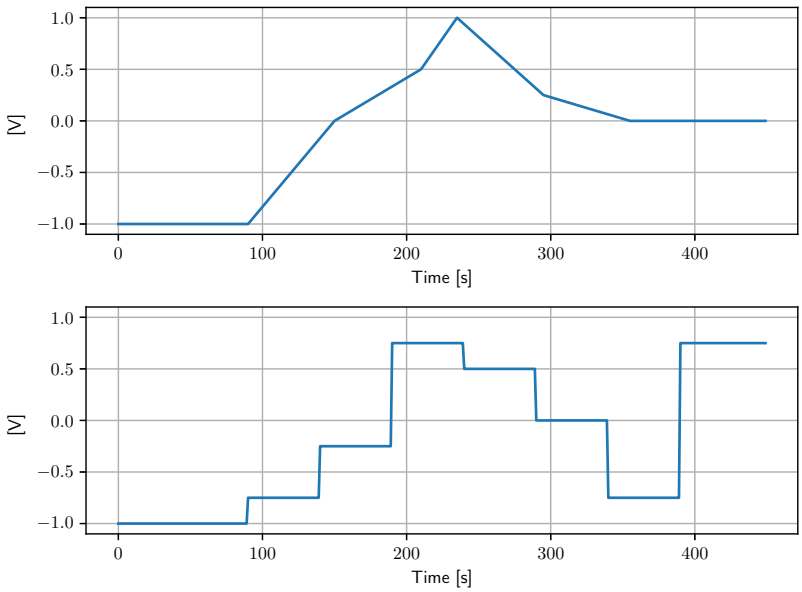


Figure 4.13: Time evolution of a ramp perturbation and a step perturbation

The three algorithms will undergo the four dynamic tests mentioned here above and each individual dynamic test will be tested with two different frequencies of iteration: 1 and 10 Hz[1] with a voltage increment on the reference voltage of 32 LSB_{12}. Another test will be performed at 10 Hz but with a voltage increment of 16 instead 32 LSB_{12}. In total 36 different tests were performed. The metrics recorded are the current i and the voltage v, thus the power $p = iv$ as well.

4.3.2 Results

Overall, the three algorithms handled the dynamic tests relatively well even though they are more robust against illumination perturbations than against temperature perturbation. This section highlights the most relevant results and illustrates some of them in figures. Nevertheless, for the sake of clarity, all the figures of the dynamic tests performed are depicted in Appendix B.

Illumination step : P&O and IC

Figure 4.14 illustrates one of the test performed. In this case the P&O method is operating at 10 Hz with a voltage increment of 16 LSB_{12}. The time evolution of the theoretical MPP operating points (current and voltage) are computed taking into consideration the perturbation at each time instant. This is also depicted in the figure.

[1]Taking into account that 100 Hz was to close to the low pass cut-off frequency, it has been decided not to go further with the testing at this frequency (cf. Section 4.2.3).

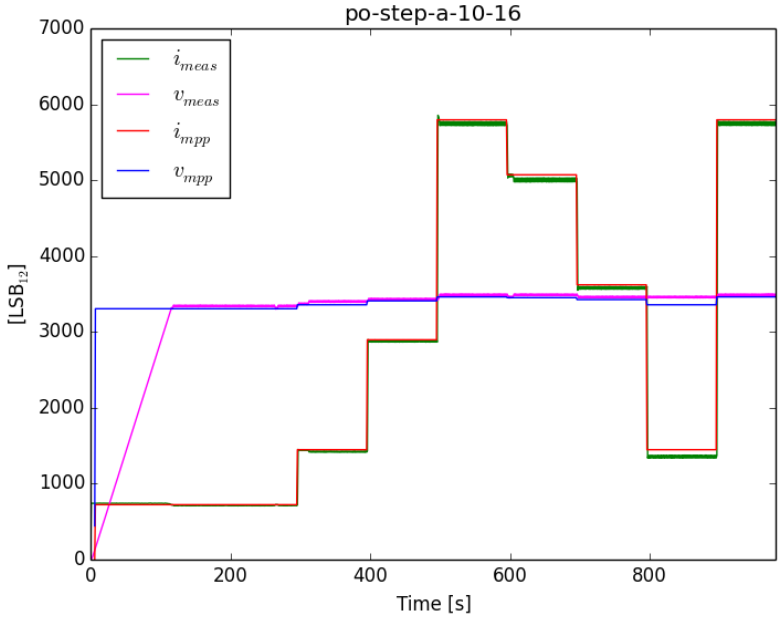


Figure 4.14: Perturb & Observe operating at 10 Hz with a voltage increment of 16 LSB_{12} during step perturbation on illumination

Current and voltage are precisely following the theoretical MPP values. The frequency of iteration has no impact on the perturbation rejection. This is mainly due to the fact that the perturbation is targeting the current ratter than the voltage. Let us remind ourselves that the three selected methods are changing the operating point by playing on the voltage across the solar cells. Therefore perturbing the current has no significant impact on the algorithm's performances.

The amplitude of the voltage increment Δ_V has no effect except reducing the ripple around the operating point, however this is a static feature and not a dynamic one.

With both IC and P&O methods, at the third negative step on A (see Figure 4.14 at $t = 790$ s), the voltage does not follow the theoretical MPP. The perturbation does not seem to have an impact and as a consequence the operating current is to low. The phenomenon is observed with all the tested frequencies and voltage increments.

Illumination step : 3%

Contrary to the other two techniques, the 3% approach does not have the issue at the third negative step discussed in previous paragraph. The voltage follows closely the theoretical operating point which forces to sink the correct amount of current for a maximum power extraction.

Yet, another phenomenon is happening. With a positive edge of the illumination step perturbation, a transient phase where the current does not follow the ideal curve appears.

This can be observed in Figure 4.15.

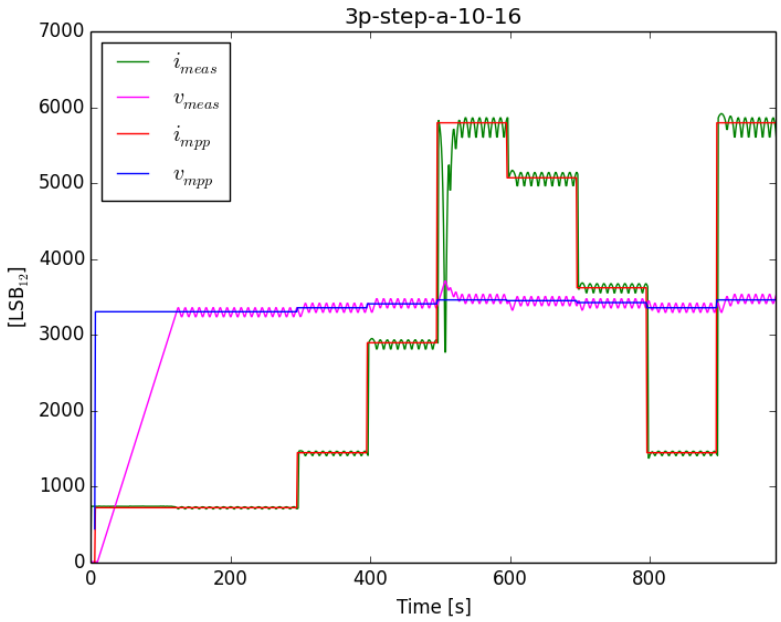


Figure 4.15: Three Percent operating at 10 Hz with a voltage increment of 16 LSB_{12} during step perturbation on illumination

The reason behind this transient phase lies in the definition of the algorithm. The Three Percent method is successively increasing (resp. decreasing) the operating voltage until achieving a decrease of 3% of the current (resp. the voltage). Hence, a perturbation is very likely to happen during one of the two states and not perfectly when the 3% are achieved. Consequently, the decrease keeps going until the condition is met. Then, and only then, a new reference is measured. This transient phase is easily observable in Figure 4.15. After a positive step, the current spikes (due to the perturbation) but then decreases until reaching 97% of the previous value. Then it gradually reaches the correct operating point thanks to the voltage decrease phase.

This phenomenon is not visible for negative steps. Indeed a negative illumination step means shifting the IV curve down. As a consequence, if the current phase was a decrease of voltage then the decrease happens regularly until 3% are achieved. On the other hand, if the current phase was a decrease of current, the perturbation is playing in our favor as the negative step is already decreasing the current by more than 3%.

Illumination ramp : P&O, IC and 3%

The three methods performed similarly and follow the theoretical MPP curves. The frequency does not seem to have an impact, as well as the voltage increment is only dictating the ripple amplitude (again, this is a static feature).

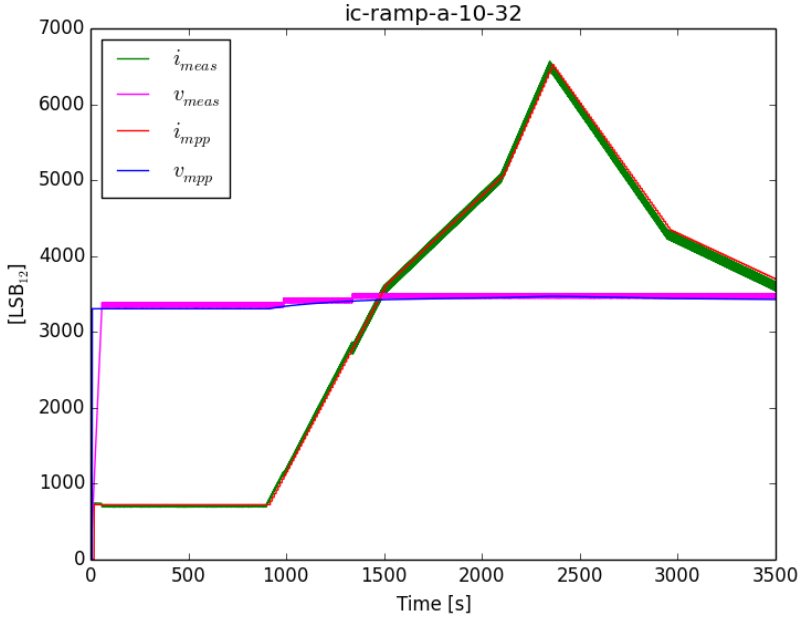


Figure 4.16: Incremental Conductance operating at 10 Hz with a voltage increment of 32 LSB_{12} during a ramp perturbation on illumination

Temperature step : P&O

Temperature perturbations have an impact on the voltage of the IV curve. In this case, the iteration frequency and the voltage increment both play a large role. These parameters are enforcing the rate of change of the voltage reference (i.e. the slope of the time evolution of the new voltage reference). Indeed the higher the frequency and the voltage increment, the faster the algorithm can converge to the new MPP. This is confirmed by the test performed at 1 Hz (cf. Figure 4.17), as the voltage cannot keep up with the positive steps.

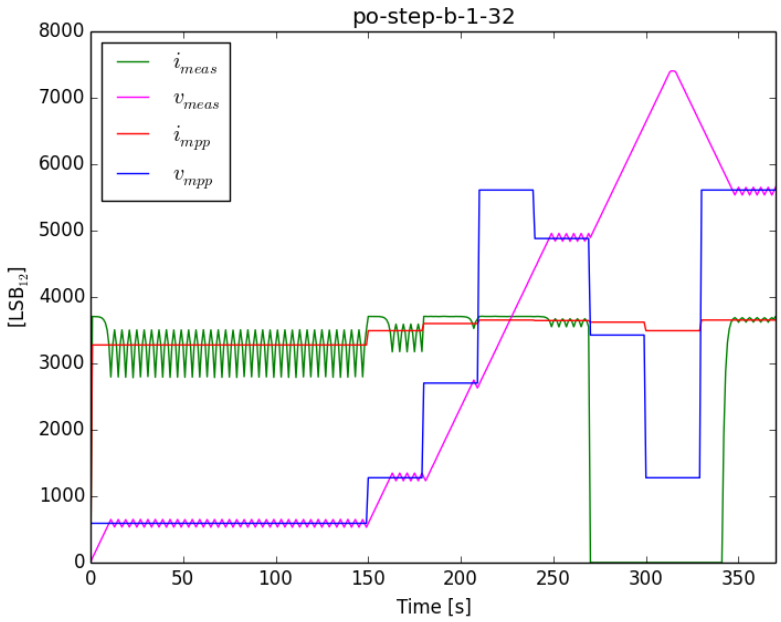


Figure 4.17: Perturb & Observe operating at 1 Hz with a voltage increment of 32 LSB_{12} during step perturbations on temperature

Yet, if the steps where temporally more spaced then the algorithm would have converged. Increasing the frequency by an order of magnitude shows much better performances as the algorithm is able to respond quicker to fast changing conditions. This is shown in Figure 4.18. Nevertheless, in the case of negative steps, the algorithm is completely lost. A negative step is shifting the IV curve, and consequently the PV curve, instantaneously to the left. As a result the current collapses to zero and the voltage saturates.

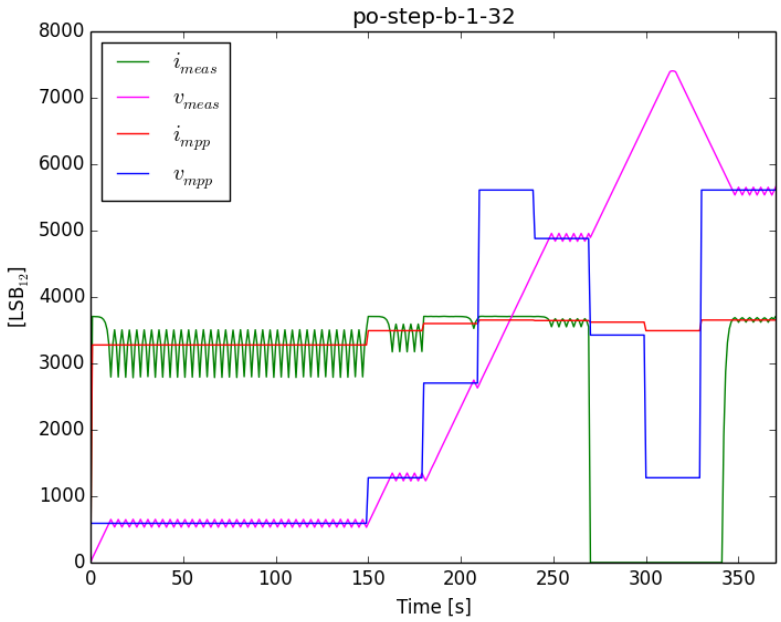


Figure 4.18: Perturb & Observe operating at 10 Hz with a voltage increment of 16 LSB_{12} during step perturbations on temperature

The avoid such a behavior, the open-circuit voltage after the perturbation must be greater than the MPP voltage before the perturbation:

$$V_{oc}^{n} > V_{\text{MPP}}^{n-1} \tag{4.8}$$

In this way, the operating point drops but is "caught" by the new PV curve (see Figure 4.19). The algorithm then re-converges towards the new MPP. If the condition (4.8) is not met, then the voltage drops to zero and the voltage increases until it reaches is maximal value. Then it starts decreasing until an equilibrium point is found.

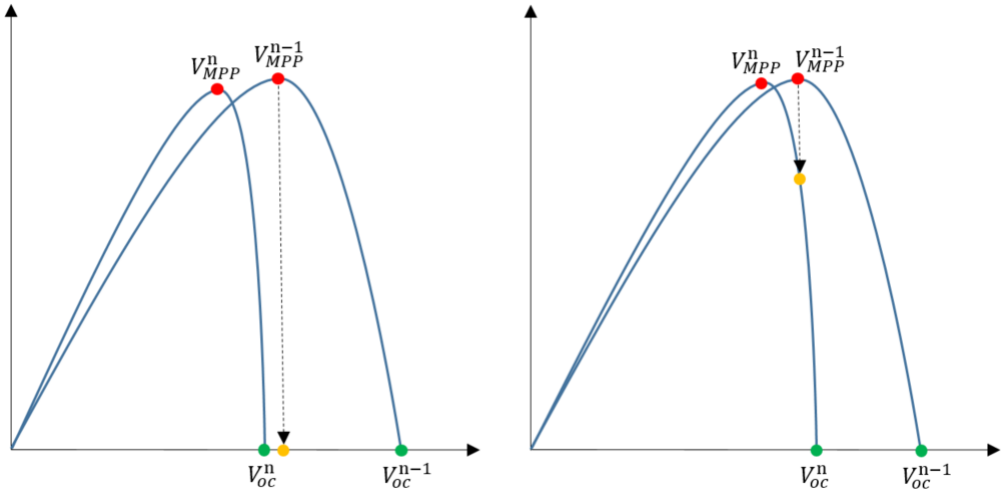


Figure 4.19: A high amplitude negative step on temperature stalls the algorithm.

Temperature step : IC and 3%

The observations are similar than P&O. However, for negative steps with the Incremental Conductance method, it is stuck once the voltage saturates. The algorithm no longer converges, however this is expected. The incremental conductance method is trying match the dynamic impedance with the instantaneous impedance.

$$idv + vdi = 0 \tag{4.9}$$

If by any chance after a perturbation the condition (4.8) presented in the previous paragraph is not met, then the IV curve is a horizontal line with zero current. Therefore both the incremental and instantaneous conductance are equal (to zero). This means the algorithm thinks it has reached the MPP. As a consequence the reference voltage is no longer updated and the algorithm is stuck.

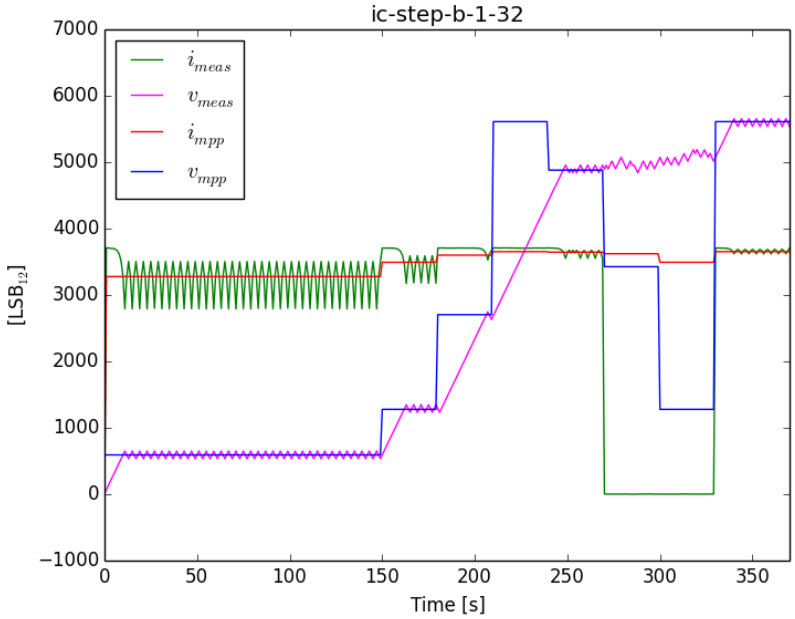


Figure 4.20: Incremental Conductance operating at 10 Hz with a voltage increment of 32 LSB_{12} during step perturbations on temperature

Again, for positive steps, similar conclusions can be drawn for 3% as for IC and P&O.

Temperature ramp : P&O, IC and 3%

The tree methods performed similarly. Te current and the voltage follow the theoretical curves as well in the case of positive ramps as in the case of negative ramps.

4.3.3 Discussion

Overall the dynamic tests performed are extreme and do not represent real temperature and illumination variations a satellite will undergo during a mission. These tests were purposely

made difficult in order to detect and observe their behavior under such hard conditions. Indeed during each test the parameters were shifting the MPP more than 80% in every direction.

The major issue observed during the dynamic tests is when the operating point collapses when a high amplitude negative step is applied on the open circuit voltage. If this situation would happen during flight it would be critical as the output power of the SA would suddenly drop to zero. However, these conditions fall outside of the normal satellite environmental envelope and will not be faced in reality for at least two reasons.

The first reason is the fact that the thermal inertia of the satellite and the solar arrays makes temperature steps almost impossible as it takes time to heat up and cool down the material. Furthermore, the amplitude of the variations during testing are much greater than in reality[2]. For reference, a low Earth orbit satellite experience temperatures from -65 to +125°C. Nevertheless, the solar array temperature usually varies between -25 and +85°C (see Figure 4.21). This variation results in a change of V_{oc} by $(85 - (-25)) \times 0.35\% = 38.5\%$ (cf. Section 1.2.4). In addition this variation is happening during an entire orbit which lasts 45 minutes while the tests performed for this work lasted just for a few minutes with multiples perturbations.

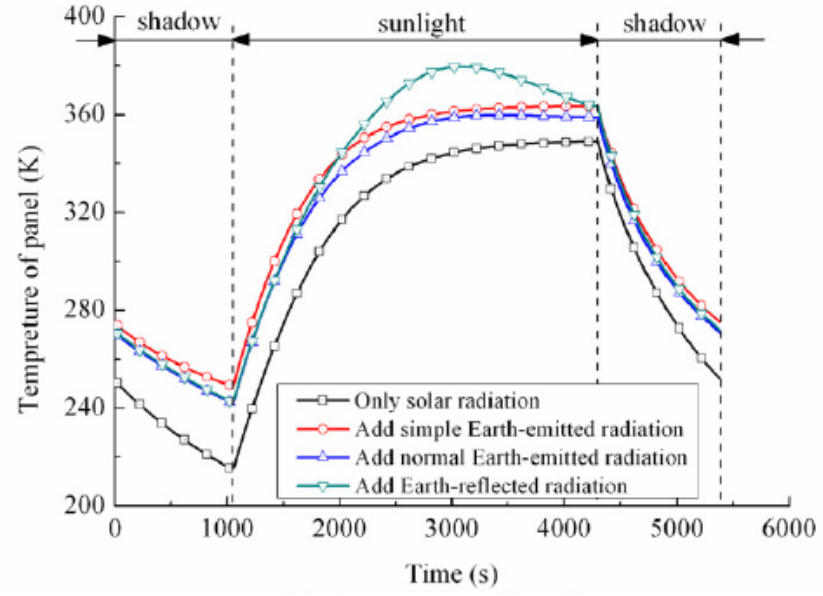


Figure 4.21: Evolution of the temperature of a solar array in low Earth orbit. With the courtesy of [9]

The second reason lies in the fact that there is a higher level regulator (such as the BCDR module, see Section 1.1.2) that is preventing events that would make the power drop to zero. Therefore, even if by any means a sudden decrease in temperature of the solar arrays would

[2]The variation of the open-circuit voltage by 80% in both directions would theoretically be the consequence of a temperature variation of 457°C.

occur and violate the condition $V_{oc}^{n} > V_{\text{MPP}}^{n-1}$, the higher level controller has built-in safety measures in order to avoid it.

4.4 Key learnings

The test campaign has identified some important aspects. Among these, it is interesting to note that for the three selected algorithms, 99% of the available power is extracted. Moreover, when the algorithms converged to the MPP, the largest deviation observed from the theoretically calculated values is limited to 2.5%.

As it relates to the time needed to perform an iteration loop, it is similar for the three methods: about 3 [us]. Indeed, each algorithm performs two measurements and then one or two multiplications. After that, the result of the multiplication follows a decision tree in order to determine the action to be taken on the reference voltage. Multiplications should be the most time consuming, however they are carried out with the help of a co-processor which makes these operations very fast.

Dynamic tests have shown that the algorithms are very robust against illumination perturbations but less to temperature perturbations. Indeed, the illumination has an impact on the short-circuit current which results in the IV curve shifting vertically. Therefore, the MPP voltage (almost) does not vary while it is actually on the voltage that the algorithm is acting. In the case of temperature perturbations, it is the open-circuit voltage that is modified and consequently the curve is shifted horizontally. The condition $V_{oc}^{n} > V_{MPP}^{n-1}$ should be respected in order to avoid the stall of the algorithm.

The main point to remember from these tests is the impact of the discretization that a digital solution imposes contrary to an analog implementation. Indeed, the three algorithms use the voltage to regulate the operating point of the solar panels by increasing or decreasing the reference voltage by a fixed value. Therefore, it is only possible to operate at voltages that are multiples of the voltage increment. Consequently, it has an impact on the slope around the MPP point perceived by the algorithm. In contrast, moving the voltage increment towards zero only slightly increases the amount of power extracted at the expense of a big loss in robustness.

Table 4.7 gives a qualitative assessment of the different algorithms tested.

	P&O	IC	3%
Ease of implementation	★ ★ ★ ★	★ ★	★ ★ ★
Speed of convergence	=	=	=
Single iteration time	=	=	=
Tracking accuracy	=	=	=
# measurements	=	=	=
Oscillations amplitude in regime	★ ★ ★ ★	★ ★ ★	★ ★
Robustness against noise	★ ★	★	★ ★ ★
Robustness against temperature variations	★ ★ ★	★ ★ ★	★ ★ ★
Robustness against illumination variations	★ ★ ★ ★ ★	★ ★ ★ ★ ★	★ ★ ★ ★ ★

Table 4.7: Qualitative assessment of the selected methods

4.5 Encountered issues

4.5.1 High frequency noise

As mentioned in section 4.1.4, a low pass filter was added to reduce the noise in the signal. This was added after some preliminary tests yielded poor results and the algorithms where not always converging. This was caused by another team of engineers testing a 40 amperes DC/DC converter equipment right next to my experimental setup. The 50 kHz switching frequency of the buck converter was interfering with the signals of my setup.

To solve this issue it has been decided to shield the wires between the DLK and dSPACE, to reference all the grounds to a copper plate placed under the whole setup and connect that plate to the ground of the building. This avoid loops by giving a short path to ground. In addition a RC filter was also added. With these measures in place, the unpredictable behavior of the algorithms when the buck converter was switching were no longer experienced.

4.5.2 SW vs HW multiplication

During the static test campaign of the Three Percent method, each iteration was taking 76 [µs]. This delay is more than 25 times longer than the 3 [µs] average of the other methods. After timing each instruction executed during the interrupt routine, a multiplication was spotted that was performed in software however not with the hardware multiplier. Correcting this issue led to a 3 [µs] iteration similar to the other methods. This situation highlights the efficiency of the hardware multiplier.

4.5.3 Incomplete algorithms

During the dynamic tests and more particularly when testing the temperature parameter B, the current was collapsing when a negative step or ramp was applied to B. This is the consequence of the open circuit voltage V_{oc} after the perturbation being smaller than the MPP voltage v_{MPP} before the perturbation. The steepness of the ramp perturbation was therefore adjusted such that it no longer was violating the condition $V_{oc}^{n} > v_{\text{MPP}}^{n-1}$. Yet the current was still collapsing.

After thoroughly inspecting all the edges cases of the algorithms, it was identified that the P&O and IC methods were not taking into account all the possible cases. Up until then, in all static tests (and positive ramp/step dynamic tests), the algorithm was always starting with $v_{ref} = 0$ and then gradually increasing until v_{MPP} was achieved. Therefore the IV curve was always "travelled from left to right". Yet in the case of a temperature perturbation where the MPP is slightly shifted to the left with respect to the current MPP, the algorithm needs to decrease the voltage in order to get back to the new MPP. In this case, the IV curve is "travelled from right to left". The direction has therefore to be taken into account as the conditions to increase/decrease the reference voltage are reversed. Taking the direction of the IV into consideration the algorithms are now successfully tracking negative perturbations on the temperature parameter B.

4.5.4 Sampling frequency

This is not a real issue but rather an area that can be improved. For all tests performed, the signals are sampled at the same rate as the rate of iteration. Actually, it is during each iteration that the RAS core is storing the ADC readings which are then fetched by the COM core and sent over UART to the main computer where they are written and saved in a file.

The Nyquist-Shannon sampling theorem establishes a sufficient condition for a sample rate that permits a discrete sequence of samples to capture all the information from a continuous-time signal of finite bandwidth. This is a fundamental theorem in signal processing. It states that sampling a signal requires a number of samples per unit of time greater than twice the difference between the minimum and maximum frequencies it contains. In general, the minimum frequency is negligible with respect to the maximum frequency and the theorem simplifies to :

Theorem *The discrete representation of a signal requires regularly spaced samples at a sampling frequency greater than twice the maximum frequency present in that signal.*

Chapter 5

To go further

This chapter is providing suggestions on how to improve the implementation of the three algorithms studied so far. These are a few ideas among the many possibilities to improve the algorithms. These suggestions were not implemented due to timing constraints.

5.1 Perturb & Observe

The Perturb & Observe method is very popular and widely used. This is mainly due to its simplicity and good performances. Nevertheless, the major drawback lies in the oscillations around the MPP. These oscillations make it impossible to extract the maximum power available. In addition, the capacitor bank should be sized accordingly as the photo-generated current will oscillate as well.

In an effort to remove this oscillating behavior, we suggest a simple technique. Indeed, when the MPP is reached, the algorithm successively increases then decreases the reference voltage. This pattern can be detected in software. A possible improved implementation could take advantage of this pattern and use a variable holding in memory the amount of successive positive voltage increments. Similarly, a variable would be storing the amount of successive negative voltage increments. In the case where these two variables are equal, the MPP is reached. Once this condition is met, the reference voltage is set to a fixed value (for example, the middle of the high and low peak) and is no longer updated until a perturbation occurs.

The reference voltage is no longer updated but the power is still monitored. In the case where the power is significantly different than the previous iteration (a threshold could be experimentally determined), then the tracking is re-activated.

This improvement helps to remove the oscillating behavior and reduces the stress on the capacitors. Yet, the maximum power is still not extracted as the algorithm will set the voltage to the average value.

5.2 Incremental Conductance

This method is slightly more complex and requires a bit of computational resources however it was selected for its ability to detect when the MPP is reached by checking if the following condition is met:

$$\frac{i}{v} = -\frac{di}{dv} \tag{5.1}$$

Once this condition is achieved, the incremental conductance is equal to the instantaneous conductance and the power transfer is optimal. In order to take advantage of the hardware multiplier, this condition was rearranged to:

$$idv = -vdi \tag{5.2}$$

As already stated in the previous chapter, this condition is never exactly met due to the intrinsic noise generated by the setup. The values of the derivative terms become very significant compared to the measured terms. As a result, when executing the multiplication instructions, the noise is amplified by the very high value of the derivative. Determining a relevant threshold to validate the condition is not easy. Consequently, the condition is never *exactly* met and the oscillating behavior similar to the P&O method is observed.

A first possible workaround is to apply the suggested improvement for the P&O method. A second possibility is to use the condition with divisions instead of multiplications. The advantage is that the noise in the readings won't be amplified. Furthermore, the division acts as a "normalization" and therefore the result is not a very high value anymore. This can help finding a relevant threshold in order to validate the condition.

The division can be executed in software, at the expense of execution time. During this time the RAS core is busy and cannot perform any other instructions. This solution is not viable as a single DPC is usually performing multiple regulations processes.

5.3 Three Percent

As a reminder this method is tracking the unitary slope of the IV curve by successively decreasing the current and voltage by a constant fraction, in this case 3%. This value (let us denote it by α) was found by TAS-B engineers to be a good trade-off between speed and accuracy. Indeed, decreasing α leads to a more accurate tracking but at the cost of a higher converging time. On the other hand, increasing α makes the algorithm converge faster but at the cost of high oscillations around the MPP resulting in an inaccurate tracking.

Finding a trade-off between speed and accuracy is not always easy, therefore one could suggest to take advantage of the versatility of the DPC by dynamically changing the value of α depending on the current state of the algorithm. In other words, in the case where the algorithm is in a search phase, we are looking for speed and consequently a high α value. As soon as the reference voltage is getting closer to the MPP, then α decreases for accuracy.

Again an oscillating behavior is observed but the amplitude of the oscillation is lower as α is smaller. Yet if the oscillations are an issue, the same workaround can be used by detecting the oscillating pattern in software and fixing the reference voltage to its average value.

Conclusion

The first chapter provided the reader with some background on useful concepts. First, satellites were briefly introduced. The difference between natural and artificial satellites was explained and the environment in which they evolve was presented as well as the constraints it implies when designing spacecrafts. Then, the photo-electric effect was discussed. The phenomenon is at the basis of solar energy harvesting. The equivalent model of a solar cell was detailed. Finally, the micro-processor used throughout this work, the Digital Programmable Controller (DPC), was presented. This MCU has been developed by Thales Alenia Space Belgium (TAS-B). It is a 16-bit RISC machine based on the MSP430 architecture. Its main missions range from power regulation, motor control, sensor interface and many more.

The second chapter discussed the universality of energy and in particular that the power, regardless of the domain, is the product of two quantities : effort and flux. From there, the Maximum Power Point Tracking (MPPT) concept was introduced. Then some popular algorithms were presented. Finally, three algorithms were selected in order to be implemented: Perturb and Observe (P&O), Incremental Conductance (IC) and Three Percent (3%).

The Perturb & Observe, as the name suggests, perturbs the operating voltage and then observes the power evolution in order to determine the direction of the next perturbation. This method eventually converges towards the point where the slope of the PV curve is null which is the optimum point.

The Incremental Conductance is based on impedance matching. In a source-load system, impedance matching leads to an optimal power transfer. In this case, the MPP criterion is when the incremental conductance is matching the instantaneous conductance.

The Three Percent method successively decreases the current and the voltage by 3% and naturally converges towards the unitary slope of the IV curve which is where the maximum power point is located.

The third chapter was dedicated to the digital implementation of the three algorithms in the DPC. The MPPT methods are programmed in the RAS core. This choice is motivated as this core is optimized to execute fast regulations loops. In addition, it is equipped with many features supporting this function: ADCs, DACs, hardware multiplier, RAS Cycle Timer (RCT), ... The peripherals used are first presented as well as their configurations. Finally, the implementation of each algorithm was described.

The fourth chapter focused on the test campaign carried out in order to characterize the behavior of the algorithms under different conditions. Several test benches allowed to

identify how the algorithms reacted to illumination and temperature perturbations but also the performance in regime.

Some key figures can be retained: the three methods allow to extract on average more than 99% of the available power, the currents and voltages deviate maximum of 2.5% from theoretical values and an iteration lasts about 3 µs (independently of the method). On the other hand, it has also been shown that discretization implies that the slope at MPP is not equal to -1 as in theory. Therefore the power extraction is not optimal. Decreasing the voltage increment only slightly increases the amount of power extracted but makes the algorithm less robust.

Dynamic tests have shown that temperature perturbations have a greater impact than illumination. It was also shown that to avoid stalling, the condition $V_{oc}^{n} > V_{MPP}^{n-1}$ must be respected between successive iterations.

Finally, the fifth chapter gave some suggestions for improving and/or optimizing the selected methods. One of the improvements aims for example at suppressing the oscillatory behavior around the MPP. This would result in a lower stress on the components and a better power extraction. Another discusses a real time adaptation of the tracking criterion in order to converge faster and track with high accuracy the maximum power point. These are some tracks that could be at the basis of a future work.

As is relates to my experience, I had the chance to conduct this master's thesis at Thales Alenia Space. This experience was extremely rewarding. I was able to learn a great deal about real life engineering. During my curriculum I had been accustomed to the academic side of problem solving. This internship allowed me to capitalize on my formal education and bridge it with the professional world that I will be entering into next September. It also has been an opportunity to interact with seasoned professionals in the aerospace industry.

During this internship I was able to apply the skills I have acquired throughout my studies. Indeed, beyond the EPL theoretical cursus, I was happy to have been trained to conduct projects in teams. The numerous group works proved to be formative and allowed me to appreciate the value of leveraging the team members individual synergies.

On the technical side, I was confronted with different obstacles that reflect the reality of the job of an engineer. For example, during the test campaign in the lab, I learned a lot about Electromagnetic Compatibility (EMC) by being directly confronted with this situation myself on my test bench.

On a personal note, this document marks the end of my academic journey at the École Polytechnique de Louvain. While these past five years have been challenging at times, I have had the opportunity to grow not only as an engineer but also as a person.

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Appendix A

Sample codes

A.1 Peripherals initialization

Peripherals are initialized in a similar fashion for each algorithm.

```
/* Stop watchdog timer */
R_WDTCTL = C_WDTPW + C_WDTHOLD;

/* Init ADC */
R_ADC3MUX1 = C_ADC_MUX_IN1_P_SINGLE_CFG;
R_ADC3T1 = CK_K/4;
R_ADC3L1 = 1;
R_ADC3MUX2 = C_ADC_MUX_OFFSET_IN_P_SINGLE_CFG;
R_ADC3T2 = CK_K/2;
R_ADC3L2 = 1;
R_ADC3_CFG |= C_DEFAULT_ADC_CFG_ENA;

R_ADC4MUX1 = C_ADC_MUX_IN4_P_SINGLE_CFG;
R_ADC4T1 = CK_K/4;
R_ADC4L1 = 1;
R_ADC4MUX2 = C_ADC_MUX_OFFSET_IN_P_SINGLE_CFG;
R_ADC4T2 = CK_K/2;
R_ADC4L2 = 1;
R_ADC4_CFG |= C_DEFAULT_ADC_CFG_ENA;

/* Init DAC */
R_DAC1_CTL = C_DAC_CFG_DEM_MODE | C_DAC_CFG_ENA;
R_DAC1_VAL = 0x0000; // not necessary but good practice

/* Init RCT */
R_CKDIV_PRESC = 12000-1;
R_CKDIV_RAS_PER = 1000-1;

/* Enable RCT interrupt */
R_CKDIV_CFG_ST = C_RAS_PER_IRQ_ENA;

/* Init IO */
R_IO_DIR_0 = 0x8005; /* BIO01 and BIO03 output and BIO04 input */
R_IO_ALT_0 = 0x8000;
R_IO_ALT_1 = 0x0000; /* GPIO bank 1: no alternate used */
R_IO_DIR_1 = 0x0800; /* GPIO bank 1: bit 11 as output (pin X73 on DLK)*/
```

```

  /* Trigger for COM core communication */
  R_IO_ALT_2 = 0x0000;
  R_IO_DIR_2 = 0x4000;
  R_IO_O_2 = 0x0000;

  /* Enable global interrupts */
  C_EINT;
```

A.2 Perturb & Observe

```
/**
 * @brief the RAS cycle interrupt routine, called at each start of a new RAS cycle
 * @details
 */
C_INTERRUPT(C_IRQ12)  ckDivInterrupt(void)
{
  static T_UINT16 counter = 1;
  // Set pin B01 HIGH to be checked on scope as an entry point
  R_IO_O_0 |= 0x0001;

  /* Measure voltage
   * We need to perform 2 measurements
   *    1 from 2.5V to 1.25V
   *    1 from 0V to -1.25V
   * Then subtract them to get the correct value which is a 2.5V on ((2^13bit) -1)
   * Note :  ADC measurements are signed*/
  v_meas = (T_INT16) (R_ADC3MEAS1) - (T_INT16) (R_ADC3MEAS2);

  // Measure current
  i_meas = (T_INT16) (R_ADC4MEAS1) - (T_INT16) (R_ADC4MEAS2);
  if(i_meas<20) i_meas = 0;
  // Compute instantaneous power using multiplier hardware
  R_MPYS = v_meas;
  R_OP2  = i_meas;

  // Get result of multiplication
  p_meas.WORDS_HILO.int16_lo = (T_UINT16) R_RESLO;
  p_meas.WORDS_HILO.int16_hi = (T_INT16)  R_RESHI;

  // Pointer to the inter-core communication structure
  T_RAS_TO_COM_DPRAM_CONTENT *g_ptr_to_com_dpram = ((
    T_RAS_TO_COM_DPRAM_CONTENT *)&R_DPRAM_TO_COM);
  g_ptr_to_com_dpram->current = (T_INT16) i_meas;
  g_ptr_to_com_dpram->voltage = (T_INT16) v_meas;
  g_ptr_to_com_dpram->power = p_meas.int32;
  g_ptr_to_com_dpram->power_old =  p_old.int32;
  g_ptr_to_com_dpram->counter = counter;

  // Compare instantaneous power to previous iteration
  if(p_meas.int32 >= p_old.int32)
  {
```

```
    if(v_meas > v_old)
    {
      v_ref += (T_INT16) DELTA_V;
    }
    else
    {
      v_ref -= (T_INT16) DELTA_V;
    }
  }
  else
  {
    if(v_meas > v_old)
    {
      v_ref -= (T_INT16) DELTA_V;
    }
    else
    {
      v_ref += (T_INT16) DELTA_V;
    }
  }

  // Saturation
  if(v_ref>4095) v_ref = 4095;
  // Saturation
  if(v_ref<0) v_ref = 0;

  // Output new operating voltage on DAC
  R_DAC1_VAL = v_ref;

  // Save current power value for next iteration
  p_old.int32 = p_meas.int32;

  i_old = i_meas;
  v_old = v_meas;

  // Set pin B01 LOW to be checked on scope as final point
  R_IO_0_0 &= ~0x0001;

  // Trigger COM core to fetch data from DPRAM
  trigger_com_int();

  // Increment counter
  counter += 1;
}
```

A.3 Incremental Conductance

```

/**
 * @brief the RAS cycle interrupt routine, called at each start of a new RAS
    cycle
 * @details
 */
C_INTERRUPT(C_IRQ12)  ckDivInterrupt(void)
```

```
{
  static T_UINT16 counter = 1;
  /* Set pin HIGH to be checked on scope as an entry point */
  R_IO_O_0 |= 0x0001;

  /* Measure voltage */
  v_meas = (T_INT16) (R_ADC3MEAS1) - (T_INT16) (R_ADC3MEAS2);

  /* Measure current */
  i_meas = (T_INT16) (R_ADC4MEAS1) - (T_INT16) (R_ADC4MEAS2);

  /* Compute dI and dV */
  dV = v_meas-v_old;
  dI = i_meas-i_old;

  /* Compute idV using MAC */
  R_MPYS = i_meas;
  R_OP2  = dV;

  /* Get result of multiplication */
  idV.WORDS_HILO.int16_lo = (T_UINT16) R_RESLO;
  idV.WORDS_HILO.int16_hi = (T_INT16)  R_RESHI;

  /* Compute vdI using MAC */
  R_MPYS = v_meas;
  R_OP2  = dI;

  /* Get result of multiplication */
  vdI.WORDS_HILO.int16_lo = (T_UINT16) R_RESLO;
  vdI.WORDS_HILO.int16_hi = (T_INT16)  R_RESHI;

  if(vdI.int32 == - idV.int32)
  {
    // MPP, keep the same voltage
  }
  else
  {
    if(-vdI.int32 <= idV.int32)
    {
      if(dV<0)
      {
        v_ref = v_ref - DELTA_V;
      }
      else
      {
        v_ref = v_ref + DELTA_V;
      }
    }
    else
    {
      if(dV<0)
      {
        v_ref = v_ref + DELTA_V;
      }
      else
      {
```

```
63          v_ref = v_ref - DELTA_V;
64        }
65      }
66    }
67
68    /* Saturation v_ref */
69    if(v_ref>4095) v_ref = 4095;
70    if(v_ref<0) v_ref = 0;
71
72    /* Assign new reference voltage */
73    R_DAC1_VAL = v_ref;
74
75    /* Store values for next iteration */
76    i_old = i_meas;
77    v_old = v_meas;
78
79    /* Set pin LOW to be checked on scope as an exit point */
80    R_IO_0_0 &= ~0x0001;
81
82    // Send data to COM core
83    /* Pointer to the inter-core communication structure */
84    T_RAS_TO_COM_DPRAM_CONTENT *g_ptr_to_com_dpram = ((
        T_RAS_TO_COM_DPRAM_CONTENT *)&R_DPRAM_TO_COM);
85    g_ptr_to_com_dpram->idV = idV.int32;     /*pass data to COM core */
86    g_ptr_to_com_dpram->vdI = vdI.int32;     /*pass data to COM core */
87    g_ptr_to_com_dpram->i = i_meas;        /*pass data to COM core */
88    g_ptr_to_com_dpram->v = v_meas;        /*pass data to COM core */
89    g_ptr_to_com_dpram->di = dI;         /*pass data to COM core */
90    g_ptr_to_com_dpram->dv = dV ;          /*pass data to COM core */
91    g_ptr_to_com_dpram->counter = counter ;    /*pass data to COM core */
92    g_ptr_to_com_dpram->v_ref = v_ref;       /*pass data to COM core */
93
94    // Send interrupt to COM core
95    trigger_com_int();
96
97    counter += 1;
98  }
```

A.4 3% method

```
1
2  /**
3   * @brief the RAS cycle interrupt routine, called at each start of a new RAS
        cycle
4   * @details
5   */
6  C_INTERRUPT(C_IRQ12)  ckDivInterrupt(void)
7  {
8    static T_UINT16 counter = 1;
9    static T_INT8 first = 1;
10
11   R_IO_0_0 |= 0x0001;
12
13   /* Measure voltage */
```

```
14  v_meas = (T_INT16) (R_ADC3MEAS1) - (T_INT16) (R_ADC3MEAS2);
15
16  /* Measure current */
17  i_meas = (T_INT16) (R_ADC4MEAS1) - (T_INT16) (R_ADC4MEAS2);
18
19
20  /* Assign the correct values in function of the flag */
21  control_param  = (flag==1) ? i_0 : v_0;
22  measured_param = (flag==1) ? i_meas : v_meas;
23
24  // Compute condition using MAC
25  R_MPYS = ALPHA;
26  R_OP2  = control_param;
27
28  /* Get result of multiplication */
29  condition.WORDS_HILO.int16_lo = (T_UINT16) R_RESLO;
30  condition.WORDS_HILO.int16_hi = (T_INT16)  R_RESHI;
31
32  // Back to non fixed point representation
33  T_INT16 cond = (T_INT16) (condition.int32 >> 15);
34
35  /* Check if 3% are achieved */
36  if(measured_param <= cond)
37  {
38    // 3% achieved, switch flag value and get the new reference
39    if(flag==0)
40    {
41      // switch flag for next time
42      flag = 1;
43      // Get new reference
44      i_0 = (first==1) ? 3700 : i_meas;//i_meas;
45      if(i_0<0) i_0 = 0;
46      first = 0;
47    }
48    else if(flag==1)
49    {
50      // switch flag for next time
51      flag = 0;
52      // Get new reference;
53      v_0 = v_meas;
54      if(v_0<0) v_0 = 0;
55    }
56  }
57  else
58  {
59    // Keep on updating the voltage
60    v_ref = (flag==1) ? v_ref+DELTA_V : v_ref-DELTA_V;
61    // Saturation
62    if(v_ref<0) v_ref = 0;
63    if(v_ref>4095) v_ref = 4095;
64  }
65
66  /* Send new reference voltage on DAC */
67  R_DAC1_VAL = v_ref;
68
69  // Toggle for scope measurement
```

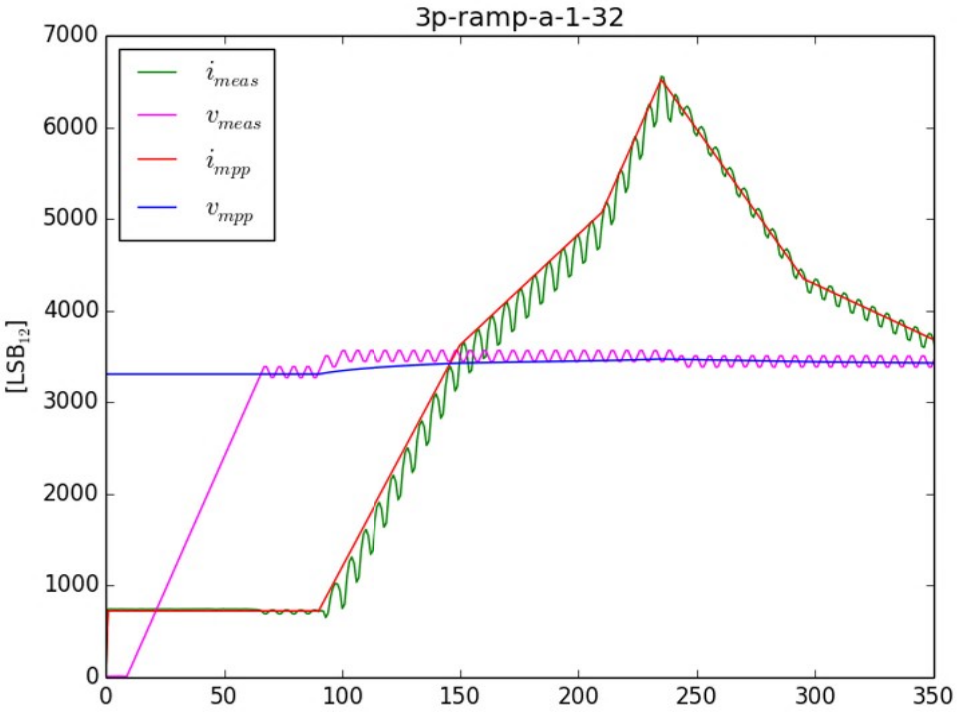
```
70   R_IO_O_0 &= ~0x0001;
71
72   // Send data to COM core
73   /* Pointer to the inter-core communication structure */
74   T_RAS_TO_COM_DPRAM_CONTENT *g_ptr_to_com_dpram = ((
       T_RAS_TO_COM_DPRAM_CONTENT *)&R_DPRAM_TO_COM);
75   g_ptr_to_com_dpram->measured_param = measured_param;  /*pass data to COM
       core */
76   g_ptr_to_com_dpram->control_param = cond;       /*pass data to COM core */
77   g_ptr_to_com_dpram->v_ref = v_ref;            /*pass data to COM core */
78   g_ptr_to_com_dpram->flag = flag;            /*pass data to COM core */
79   g_ptr_to_com_dpram->imeas = i_meas;           /*pass data to COM core */
80   g_ptr_to_com_dpram->vmeas = v_meas;           /*pass data to COM core */
81   g_ptr_to_com_dpram->counter = counter;          /*pass data to COM core */
82
83
84   // Send interrupt to COM core
85   trigger_com_int();
86
87   counter += 1;
88 }
```

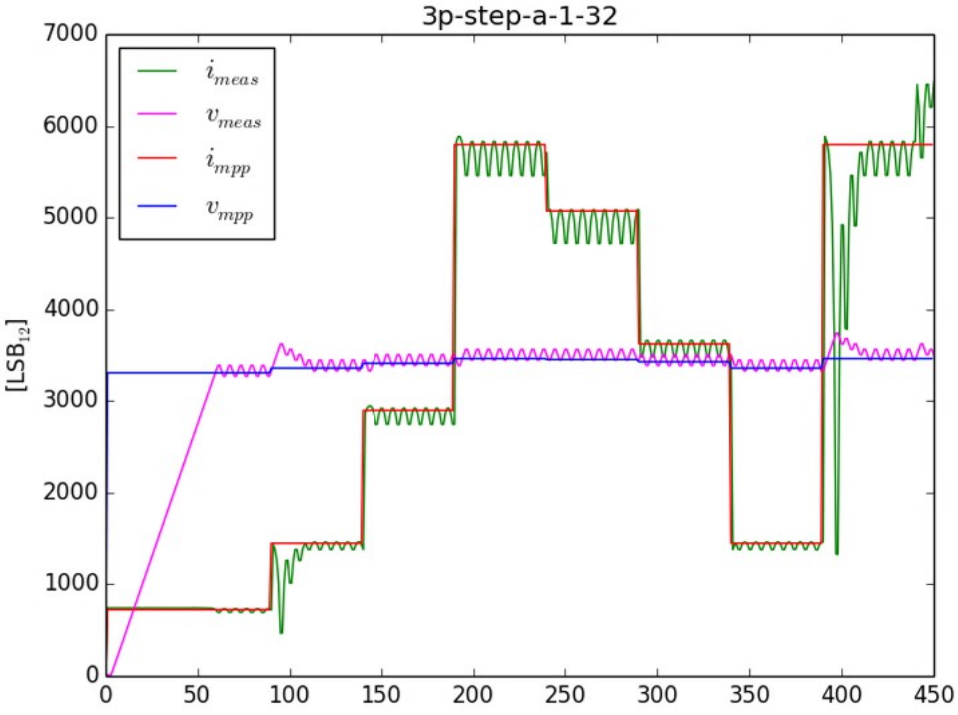
Appendix B

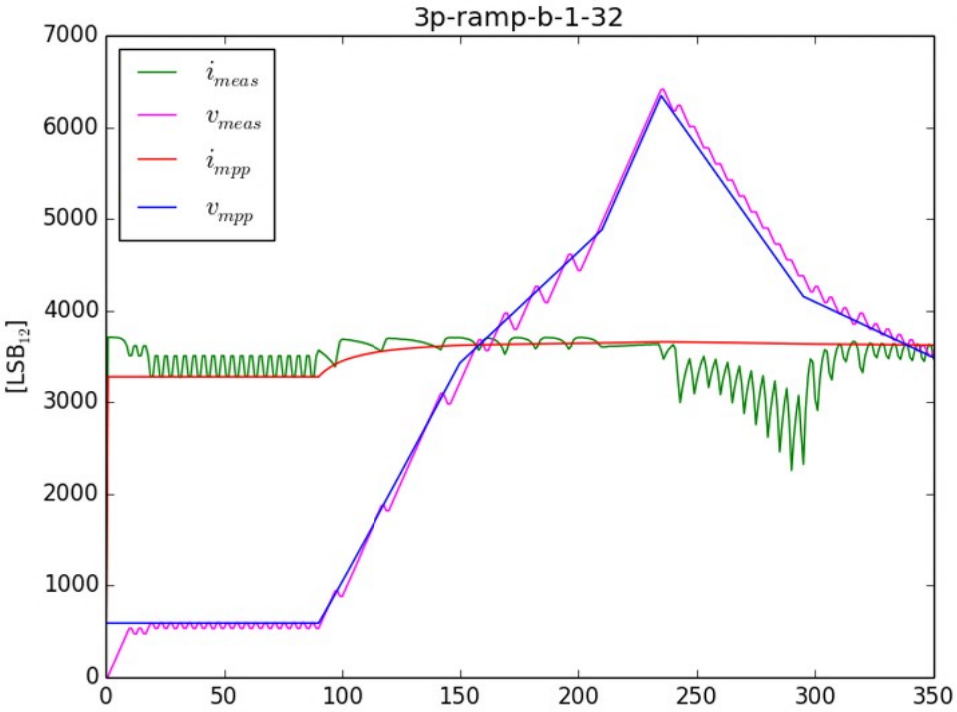
Complete dynamic test results

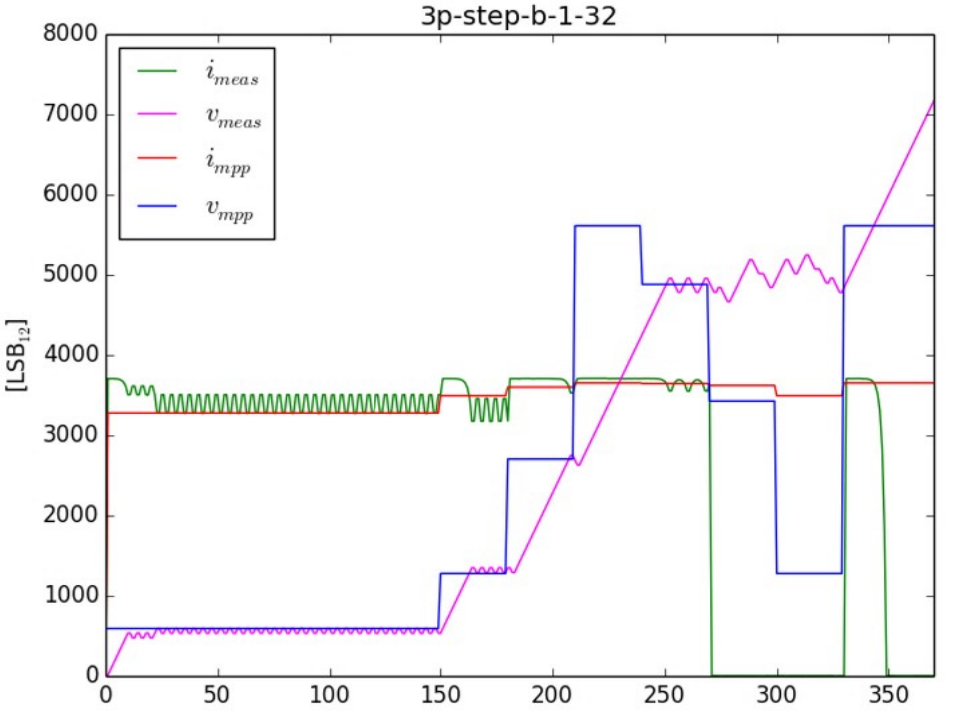
In order to differentiate the tests, a nomenclature has been set up. All the following figures are titled **aa-bbbb-c-x-yy** and can be deciphered as:

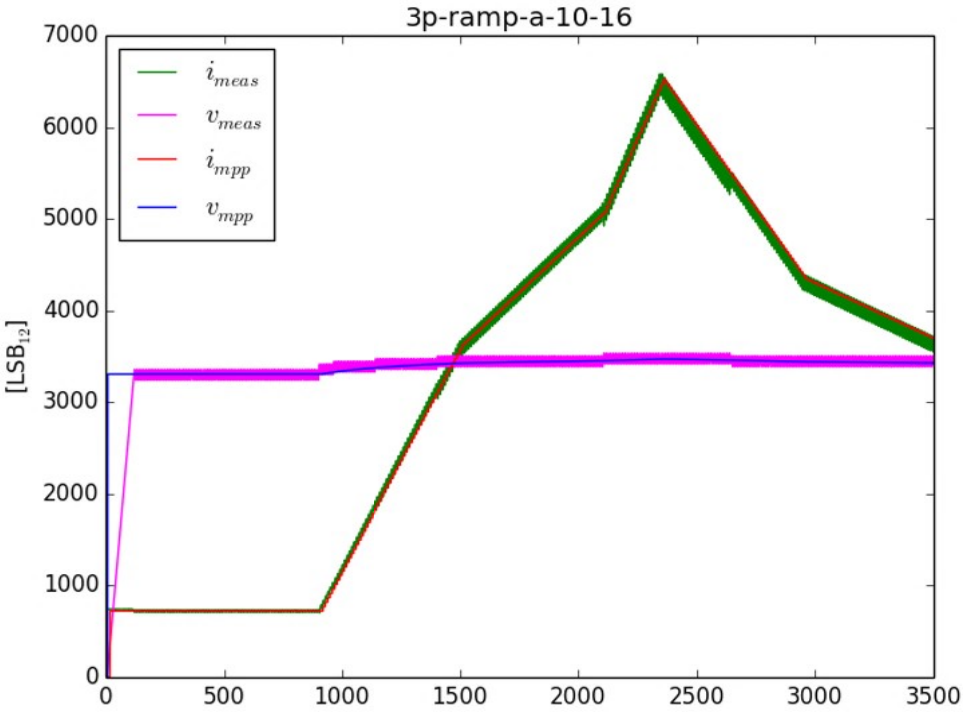
- **aa** – The algorithm under test. It can take the following values: **po**, **ic** or **3p** and respectively represent Perturb & Observe, Incremental Conductance or Three Percent.
- **bbbb** – The type of test. It can take the following values: **ramp** or **step**.
- **c** – The parameter being perturbed. It can take the following values: **a** or **b** and represents the parameter of equation (4.1).
- **x** – The frequency of iteration in Hertz. It can take the following values: **1** or **10**.
- **yy** – The amplitude in LSB_{12} of the voltage increment. It can take the following values: **16** or **32**.


3p-ramp-a-1-32
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
0
1000
2000
3000
4000
5000
6000
7000
0
50
100
150
200
250
300
350


3p-step-a-1-32
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
0
1000
2000
3000
4000
5000
6000
7000
0
50
100
150
200
250
300
350
400
450


3p-ramp-b-1-32
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
0
1000
2000
3000
4000
5000
6000
7000
0
50
100
150
200
250
300
350


3p-step-b-1-32
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
0
1000
2000
3000
4000
5000
6000
7000
8000
0
50
100
150
200
250
300
350


3p-ramp-a-10-16
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
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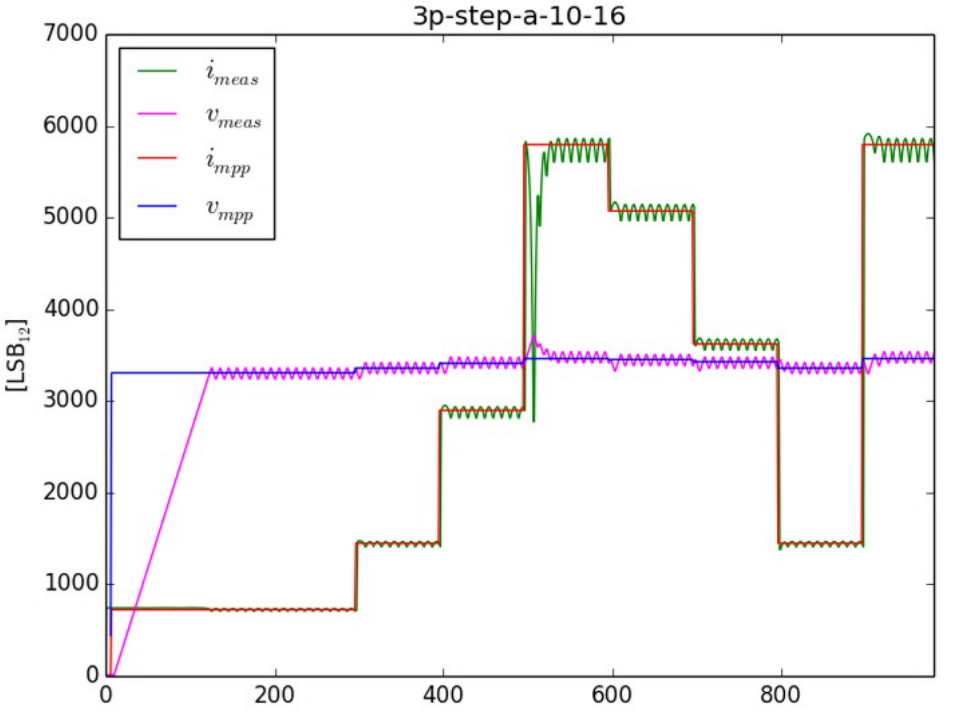
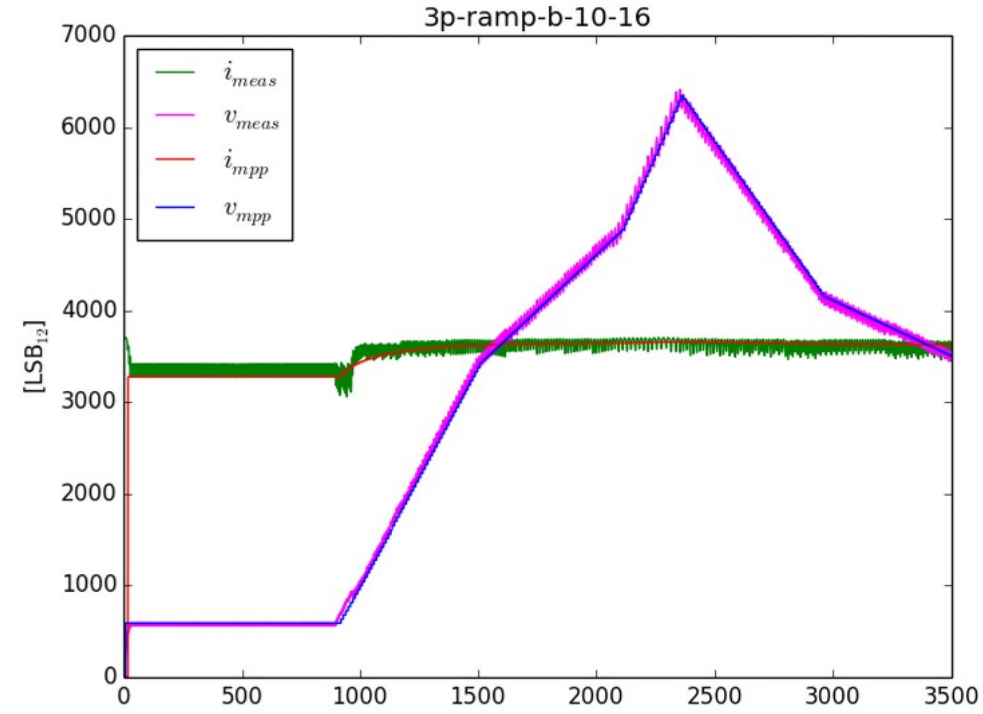
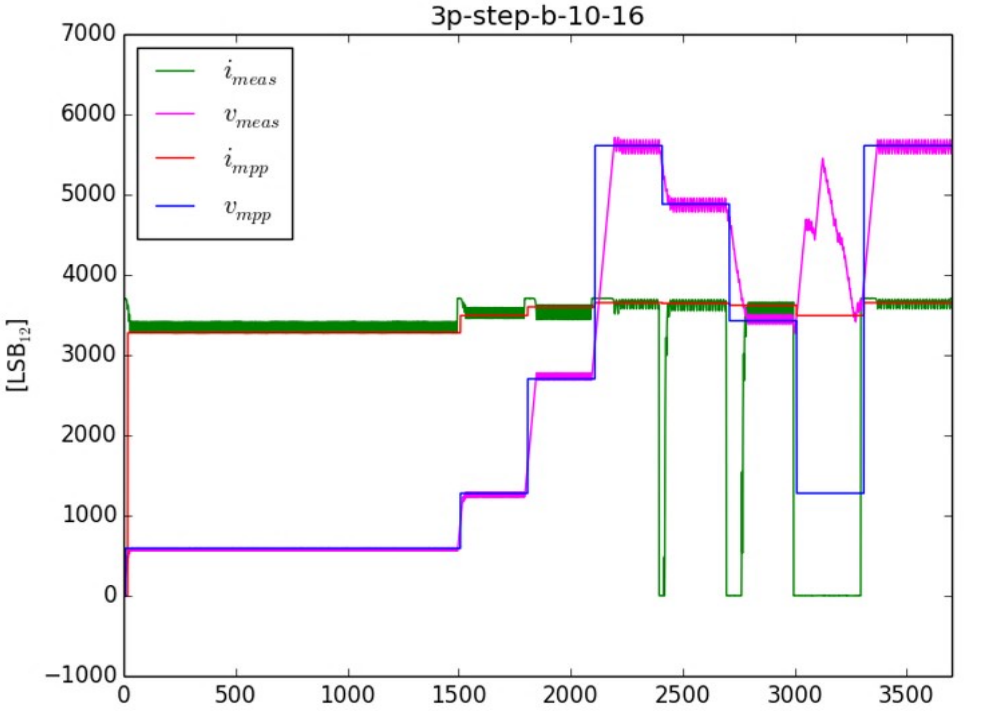
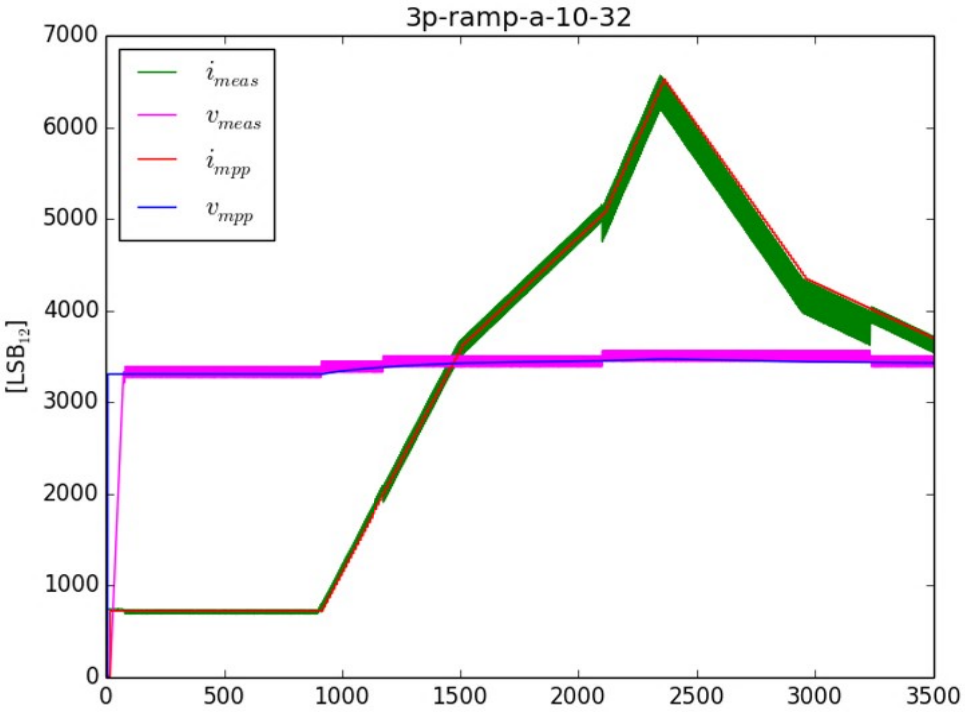
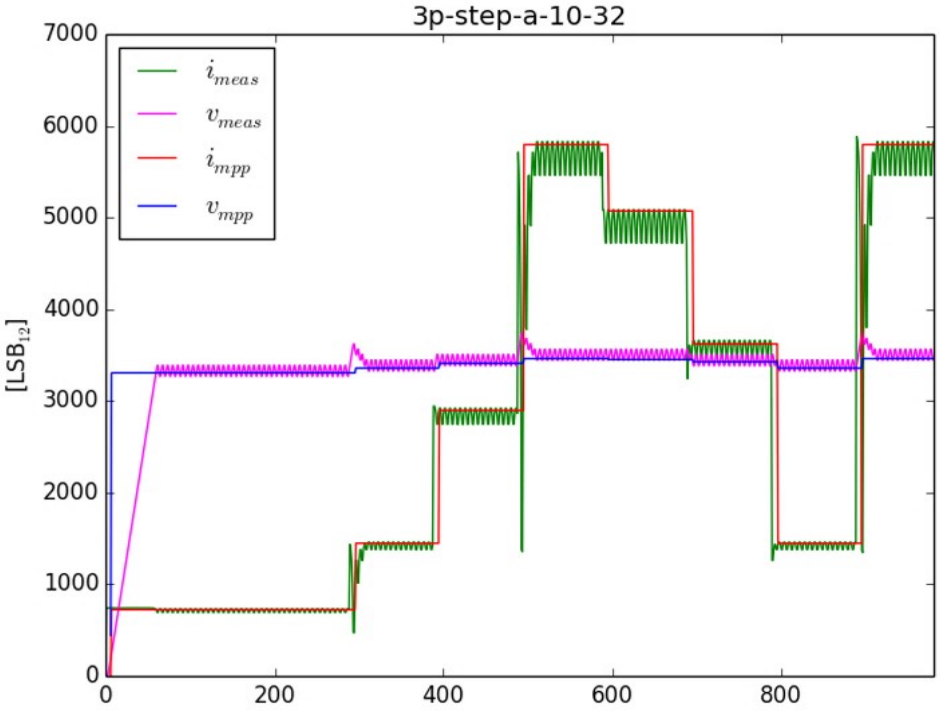
2000
3000
4000
5000
6000
7000
0
500
1000
1500
2000
2500
3000
3500

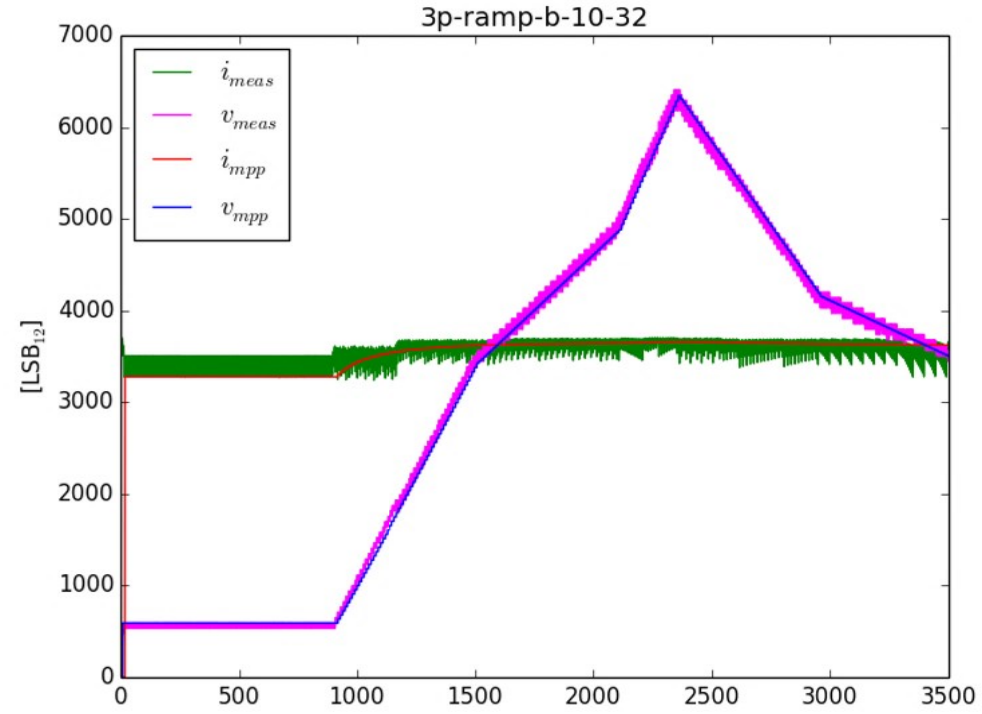

3p-step-a-10-16
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
0
1000
2000
3000
4000
5000
6000
7000
0
200
400
600
800

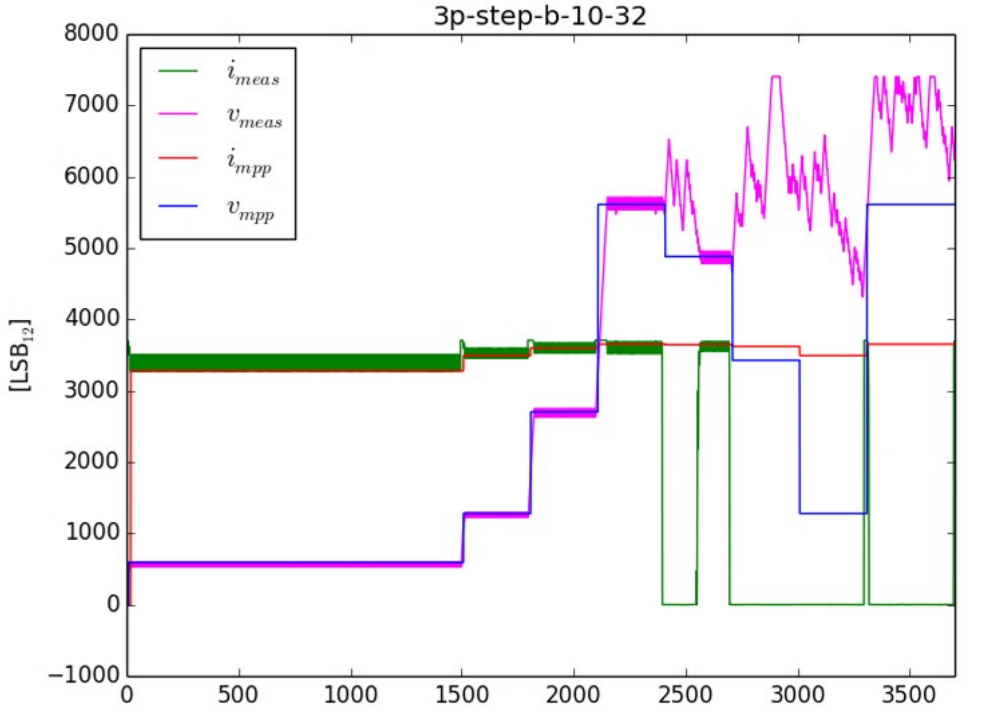

3p-ramp-b-10-16
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
0
1000
2000
3000
4000
5000
6000
7000
0
500
1000
1500
2000
2500
3000
3500


3p-step-b-10-16
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
−1000
0
1000
2000
3000
4000
5000
6000
7000
0
500
1000
1500
2000
2500
3000
3500


3p-ramp-a-10-32
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
0
1000
2000
3000
4000
5000
6000
7000
0
500
1000
1500
2000
2500
3000
3500


3p-step-a-10-32
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
0
1000
2000
3000
4000
5000
6000
7000
0
200
400
600
800


3p-ramp-b-10-32
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
0
1000
2000
3000
4000
5000
6000
7000
0
500
1000
1500
2000
2500
3000
3500


3p-step-b-10-32
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
−1000
0
1000
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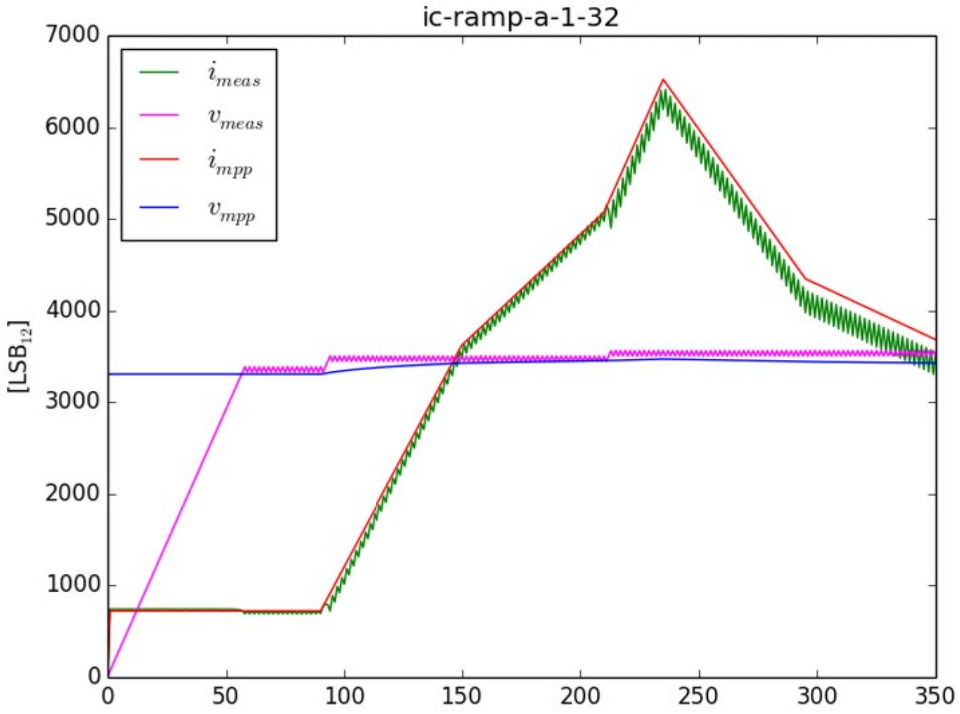
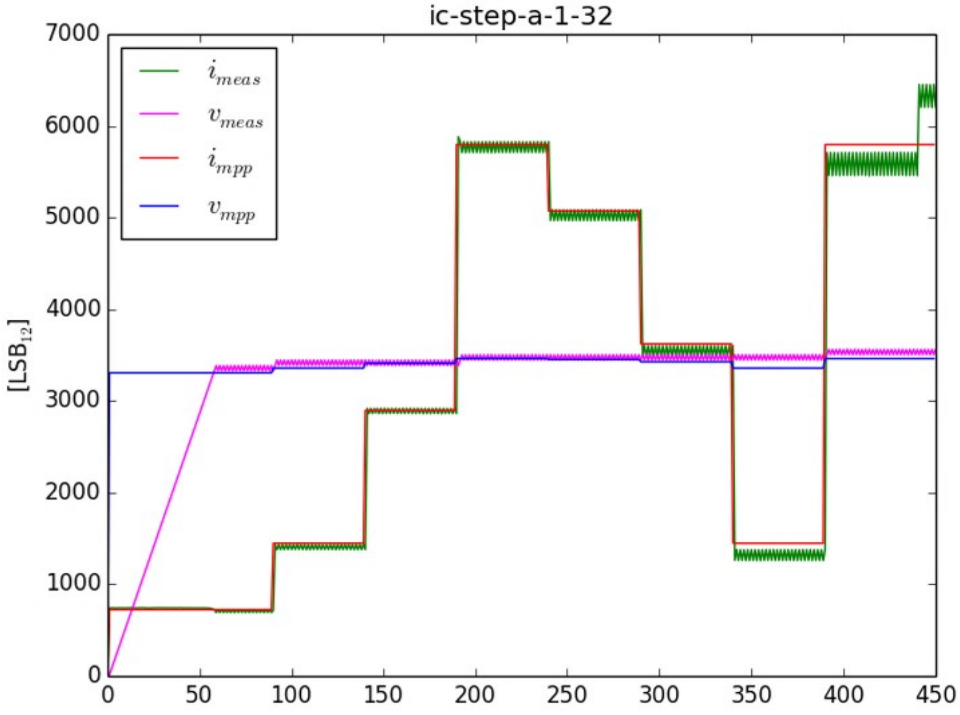
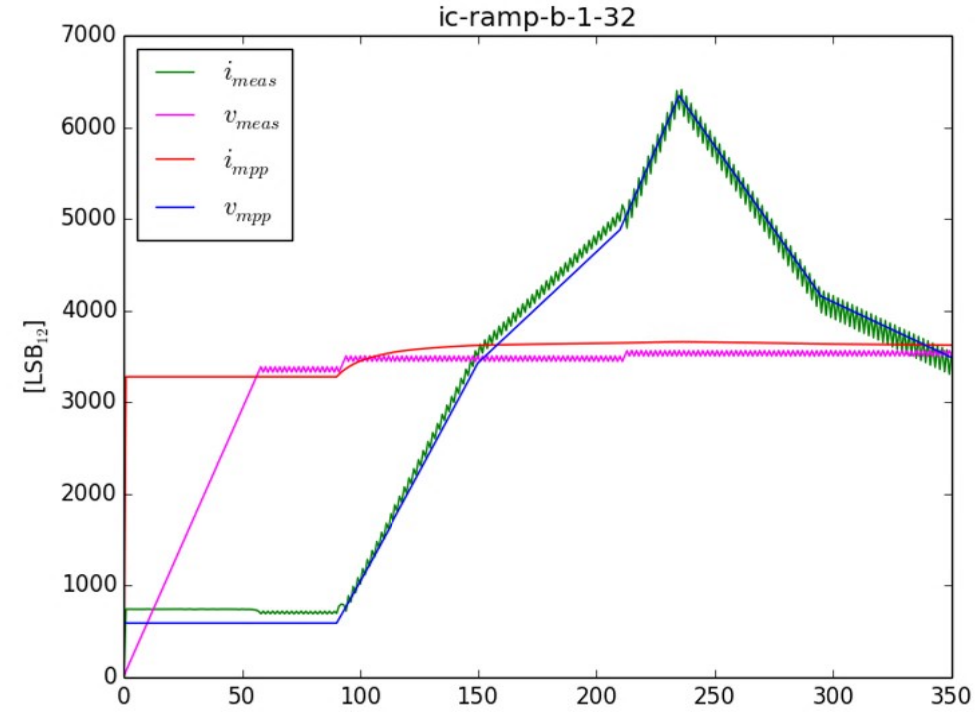
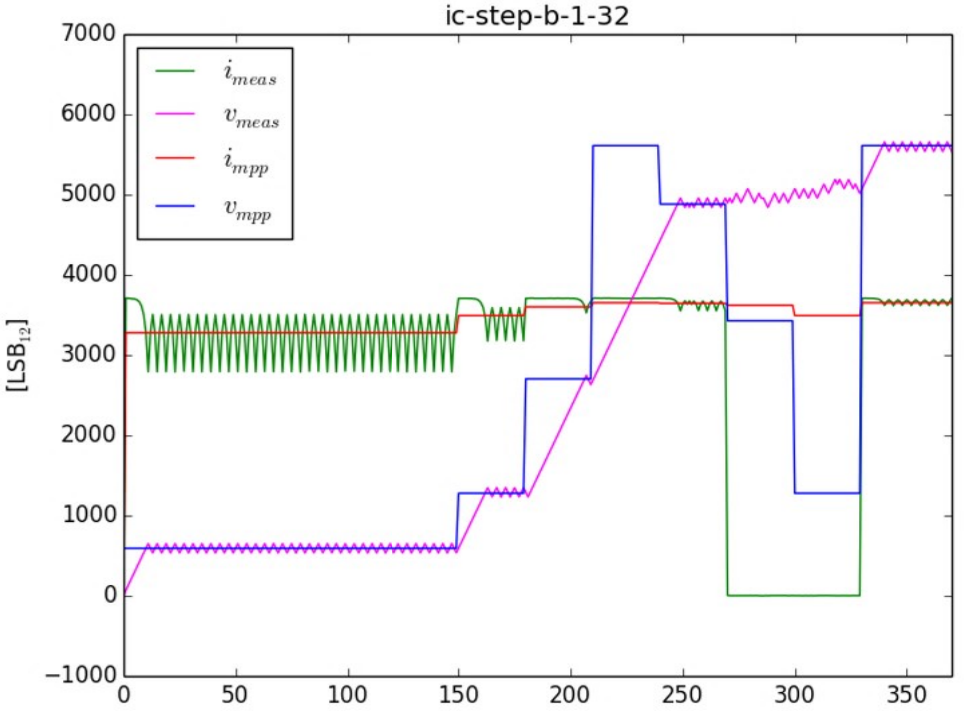
8000
0
500
1000
1500
2000
2500
3000
3500


ic-ramp-a-1-32
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
0
1000
2000
3000
4000
5000
6000
7000
0
50
100
150
200
250
300
350


ic-step-a-1-32
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
0
1000
2000
3000
4000
5000
6000
7000
0
50
100
150
200
250
300
350
400
450


ic-ramp-b-1-32
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
7000
6000
5000
4000
3000
2000
1000
0
0
50
100
150
200
250
300
350


ic-step-b-1-32
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
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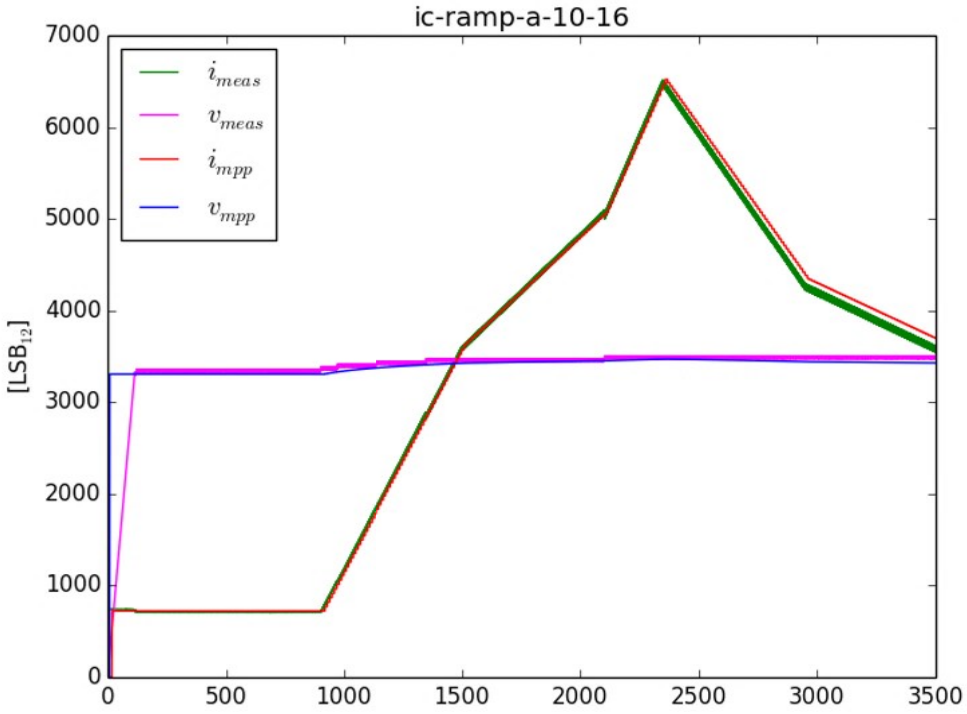
6000
5000
4000
3000
2000
1000
0
−1000
0
50
100
150
200
250
300
350


ic-ramp-a-10-16
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
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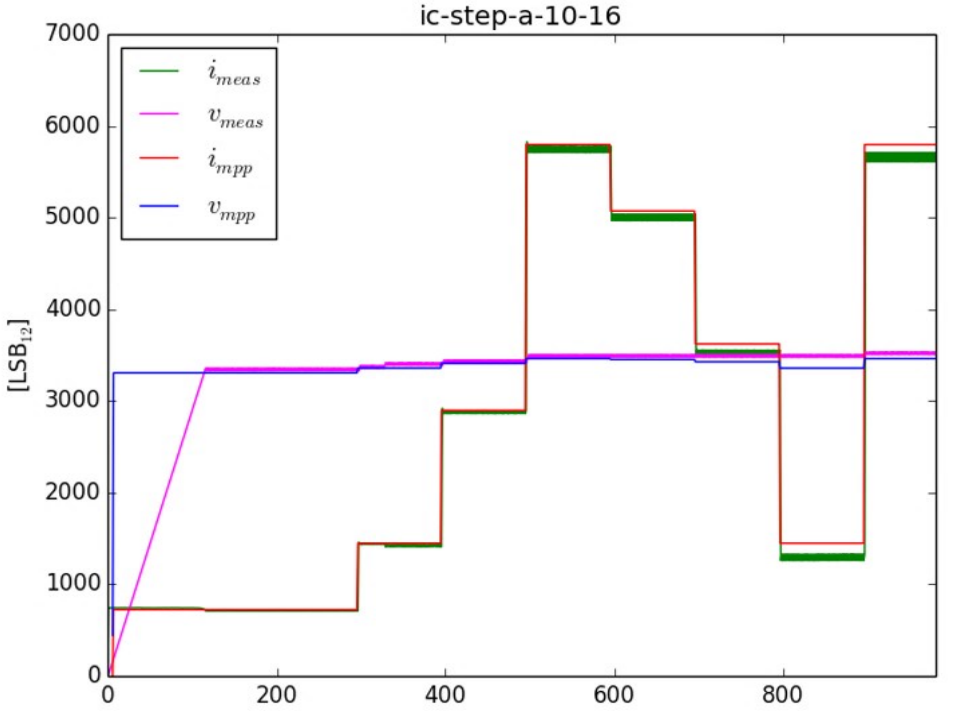
2000
3000
4000
5000
6000
7000
0
500
1000
1500
2000
2500
3000
3500


ic-step-a-10-16
i_{meas}
v_{meas}
i_{mpp}
v_{mpp}
[LSB$_{12}$]
0
1000
2000
3000
4000
5000
6000
7000
0
200
400
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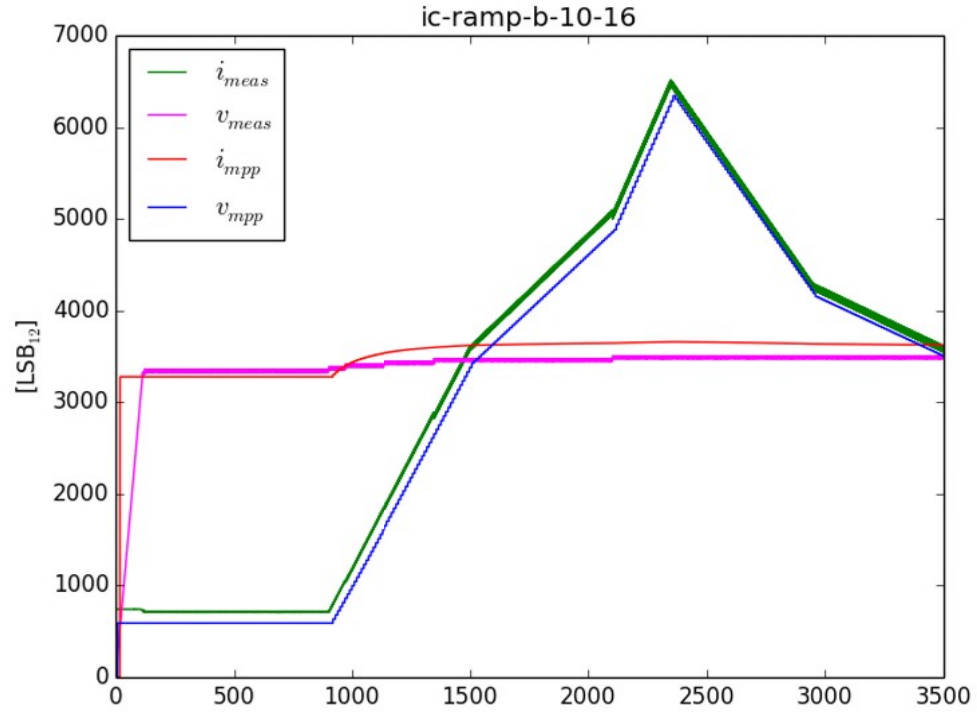
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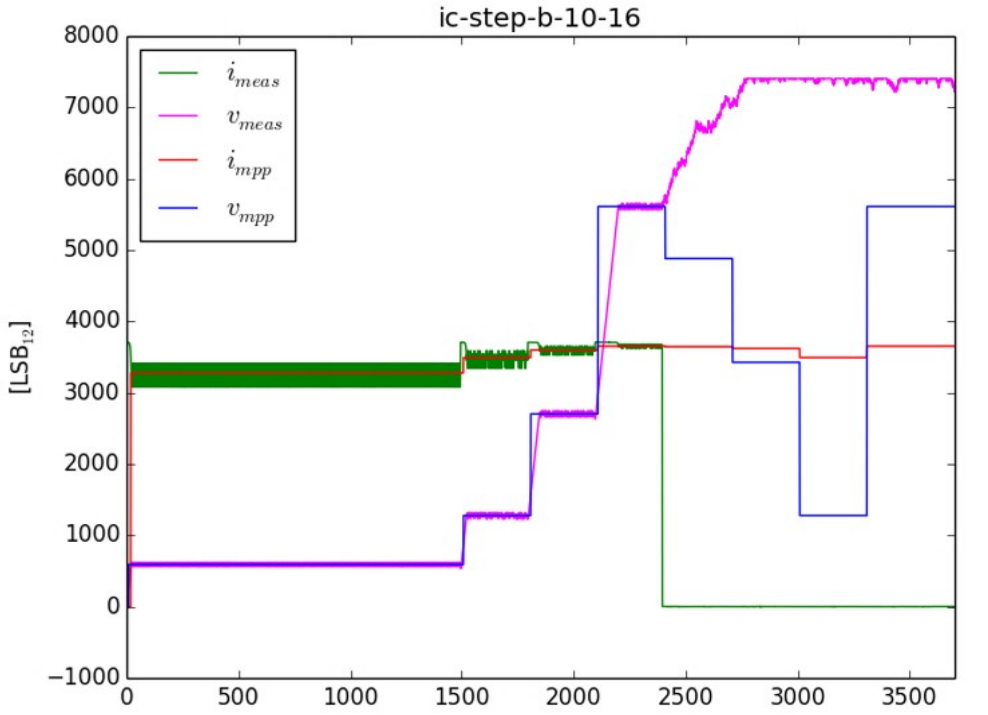
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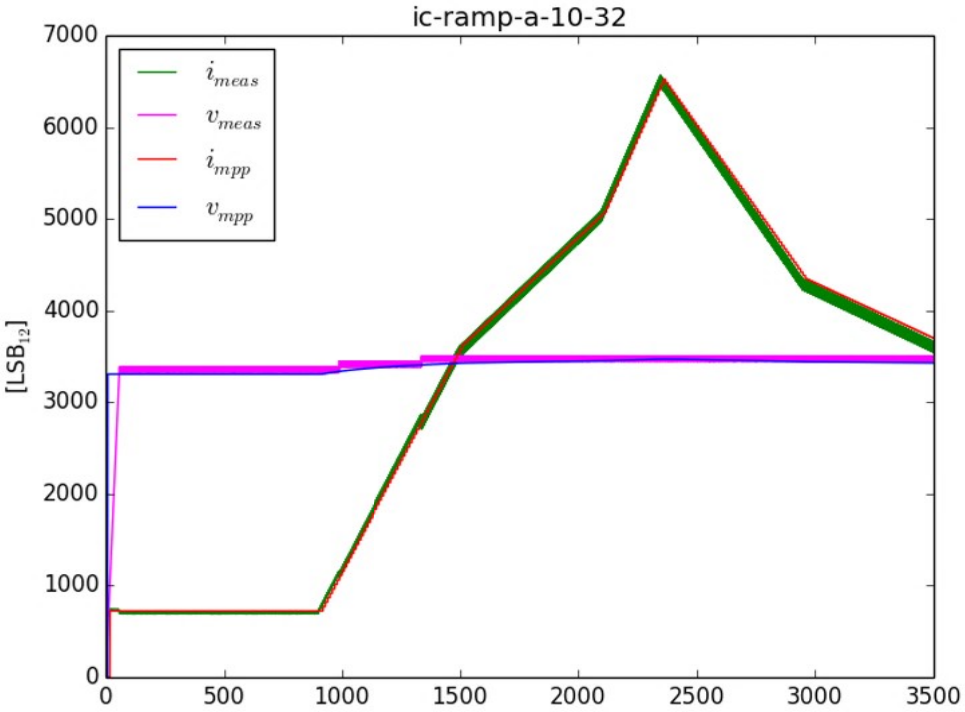
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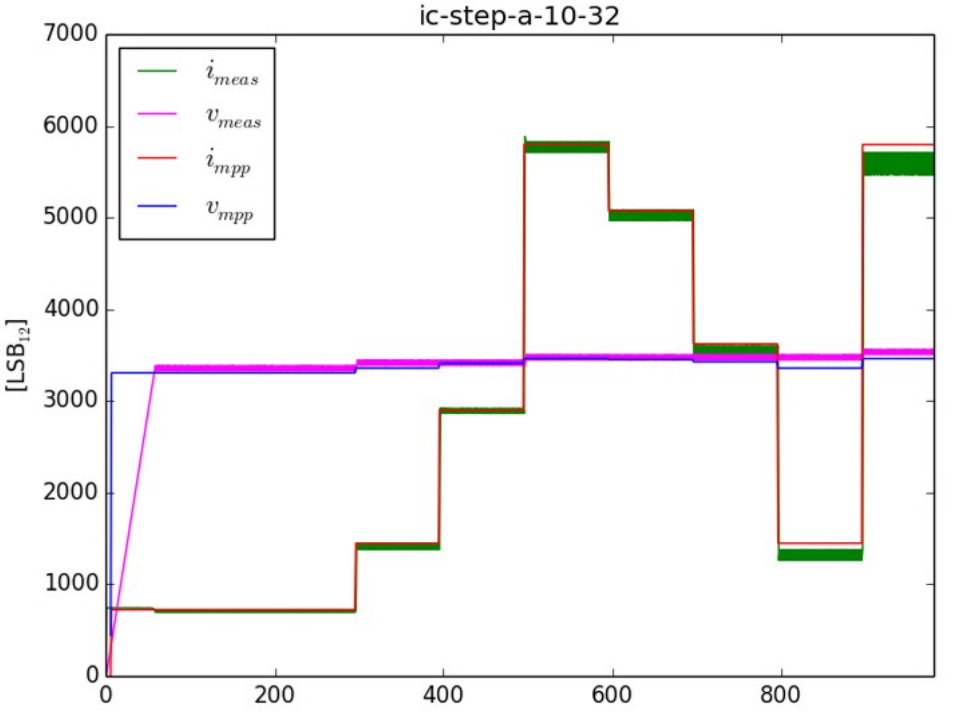
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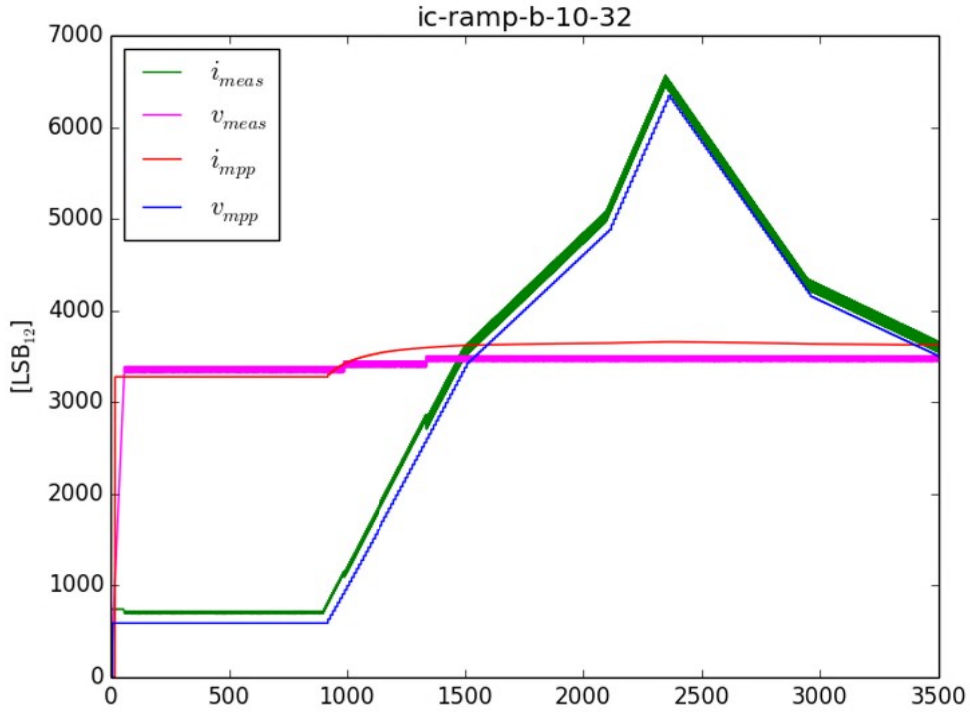
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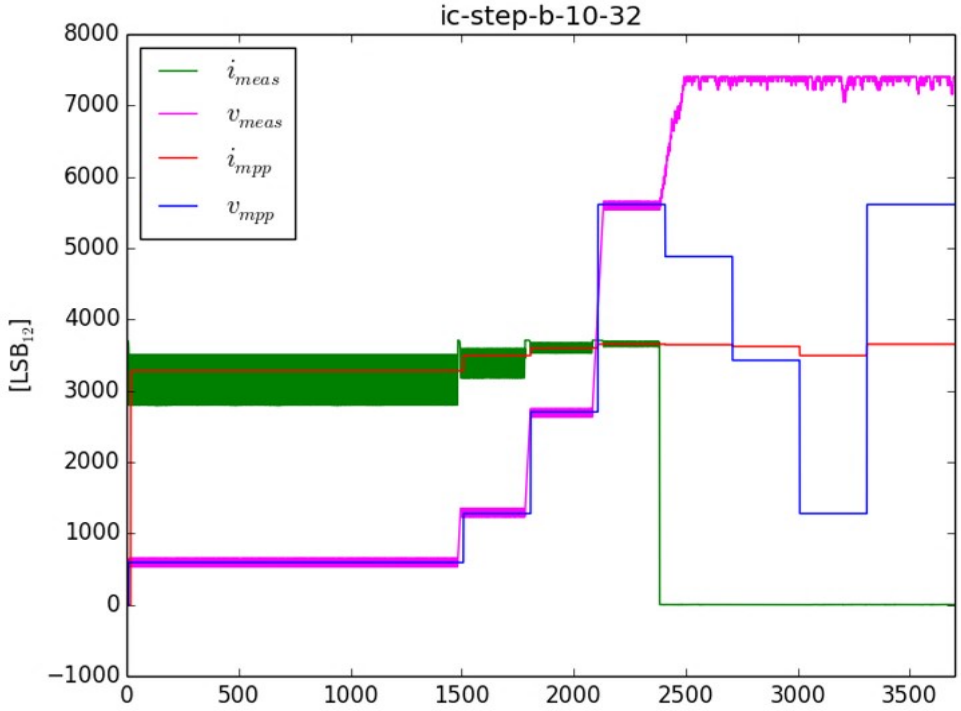
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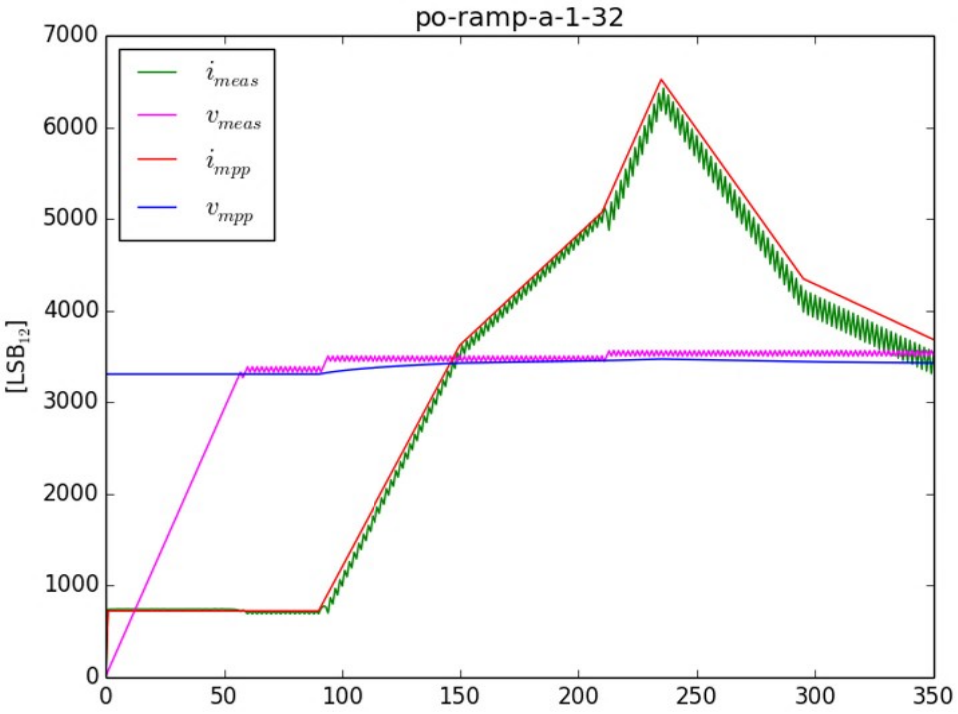
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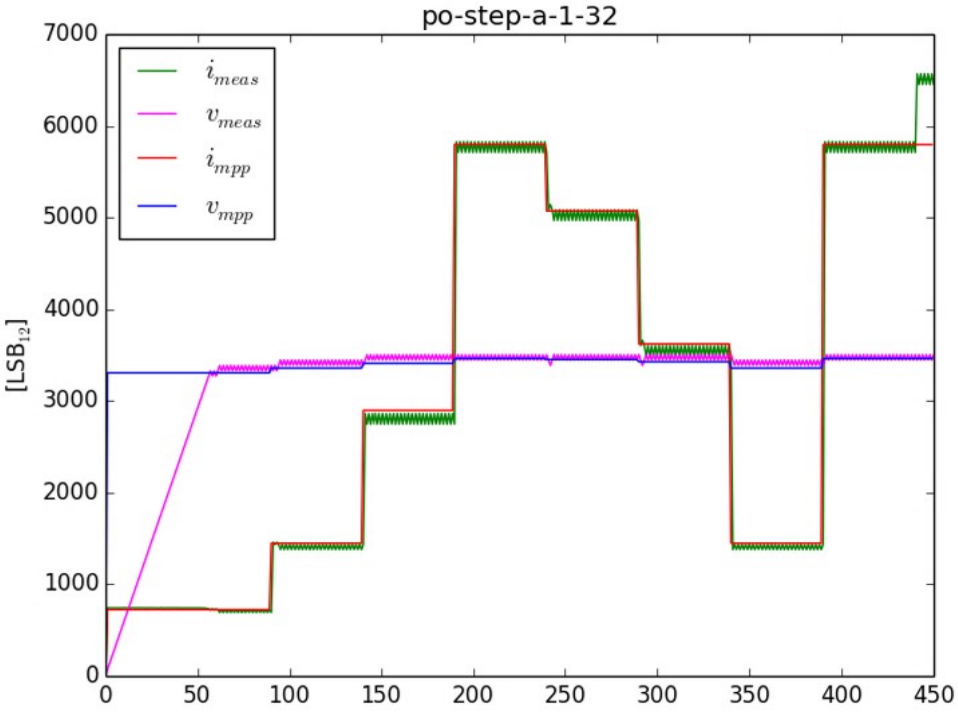
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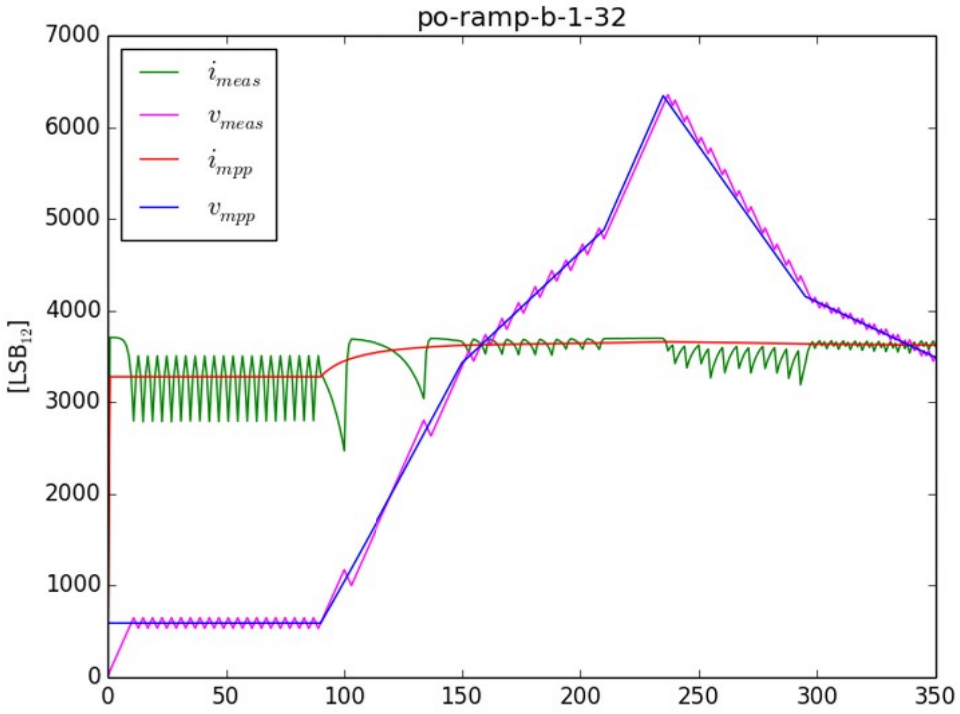
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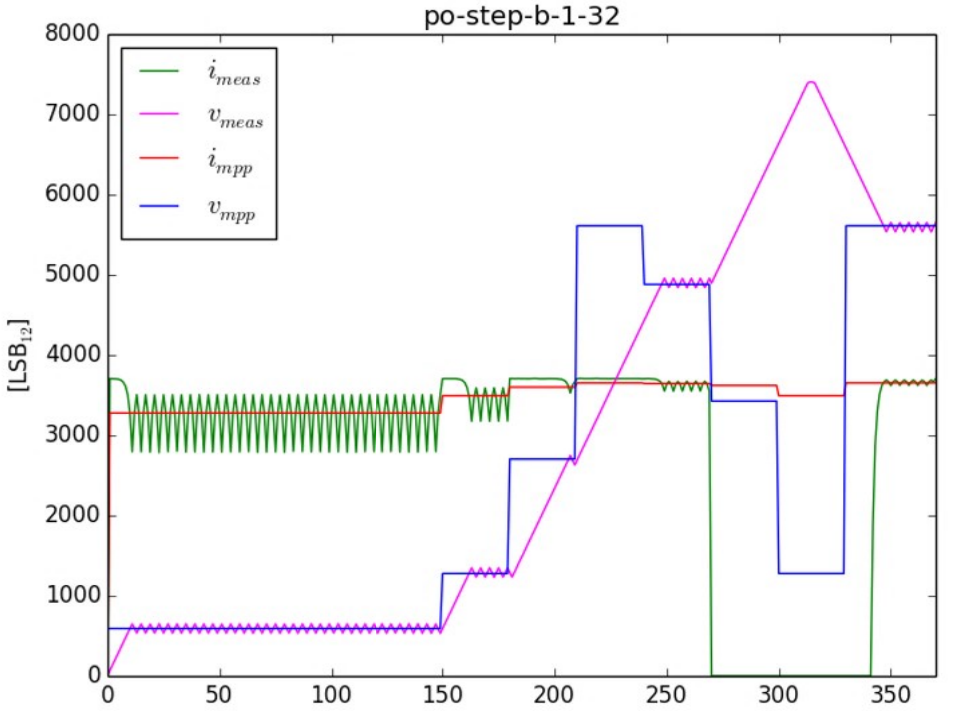
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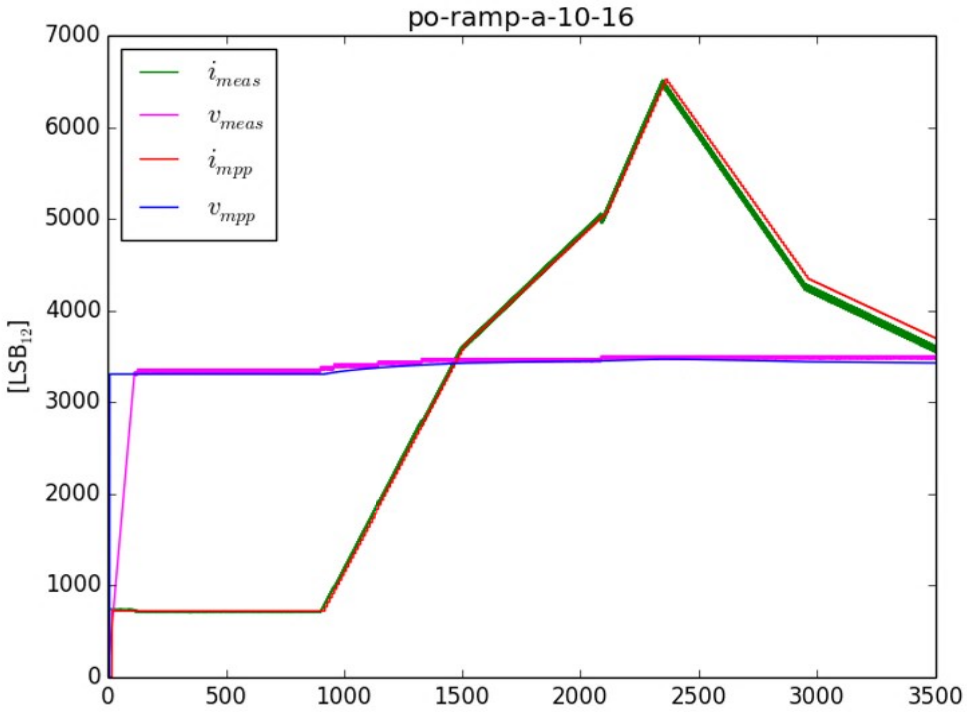
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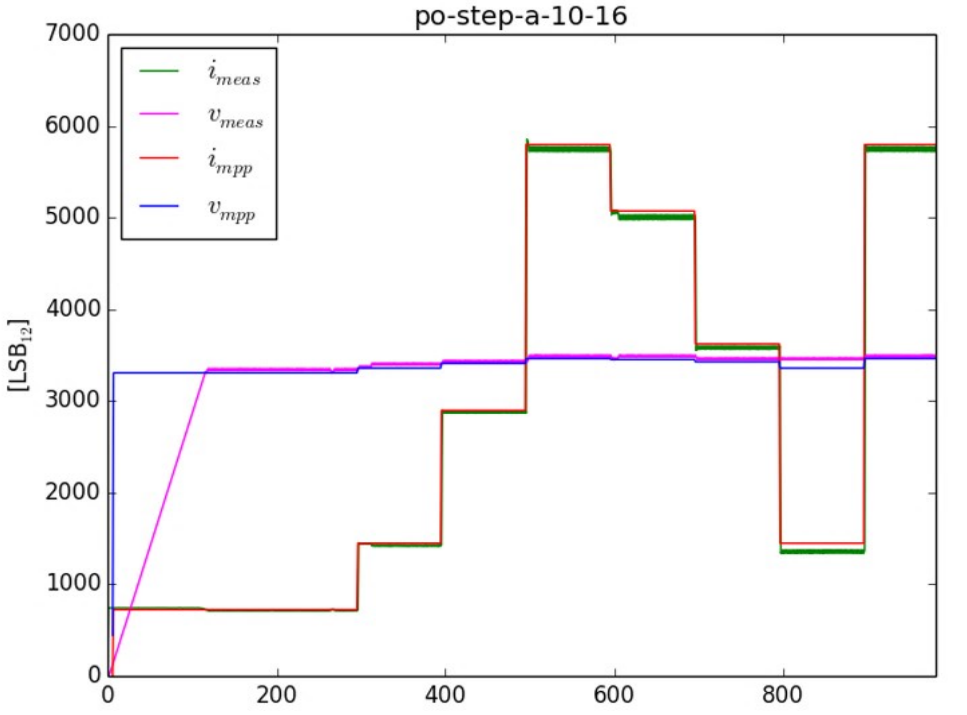
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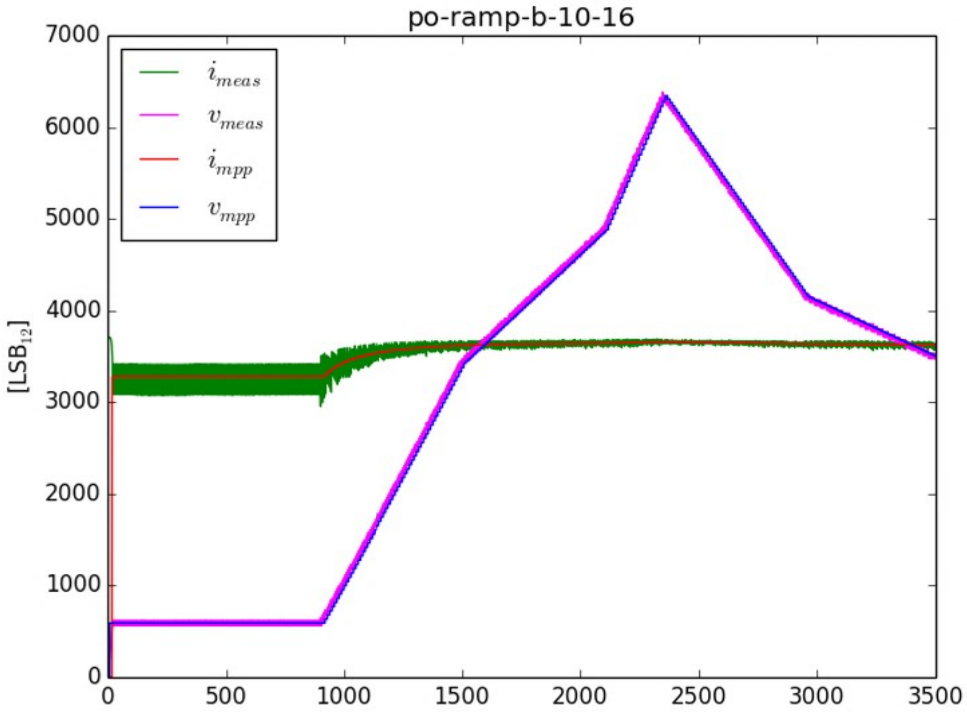
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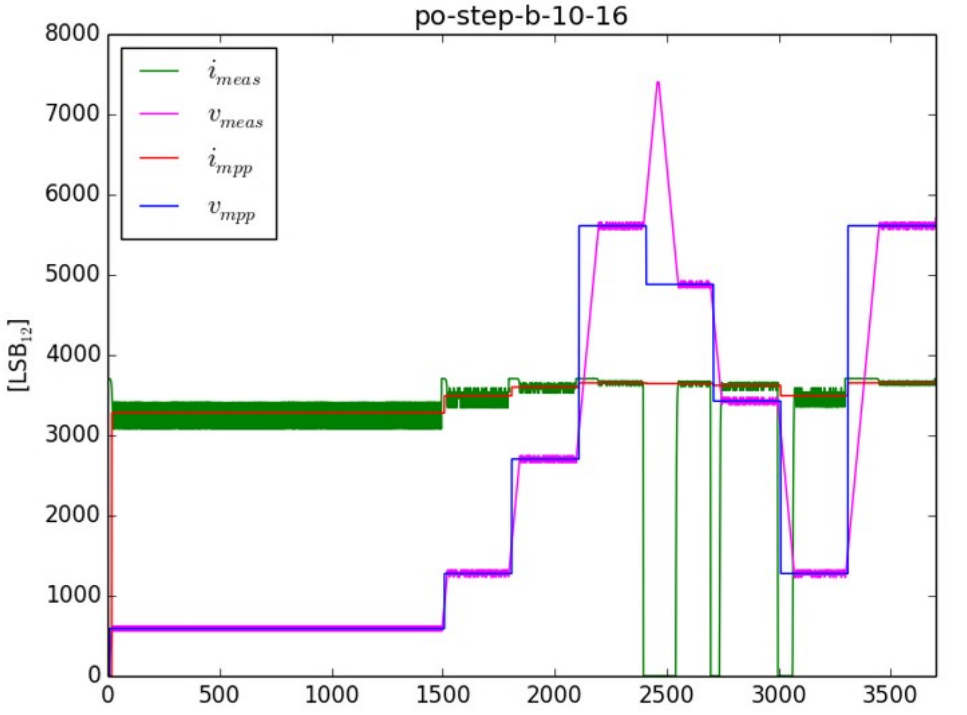
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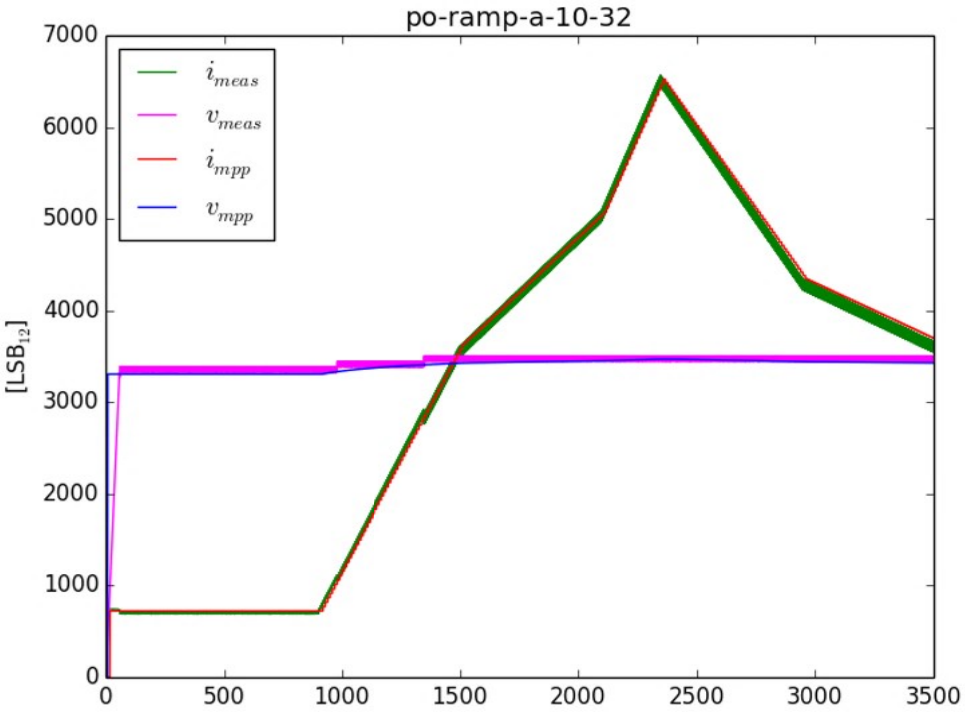
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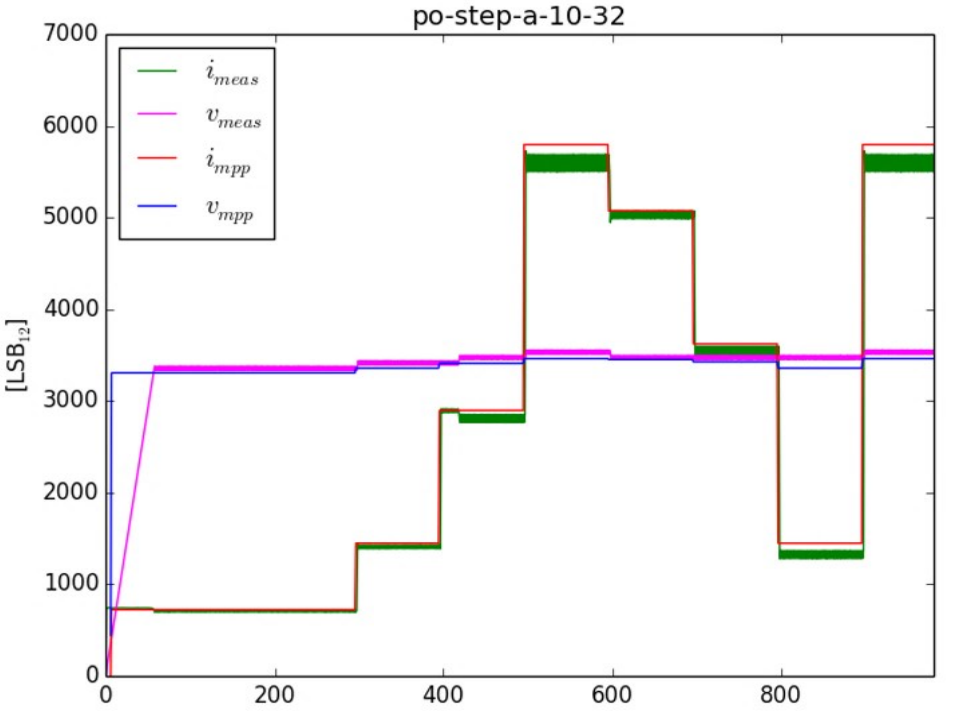
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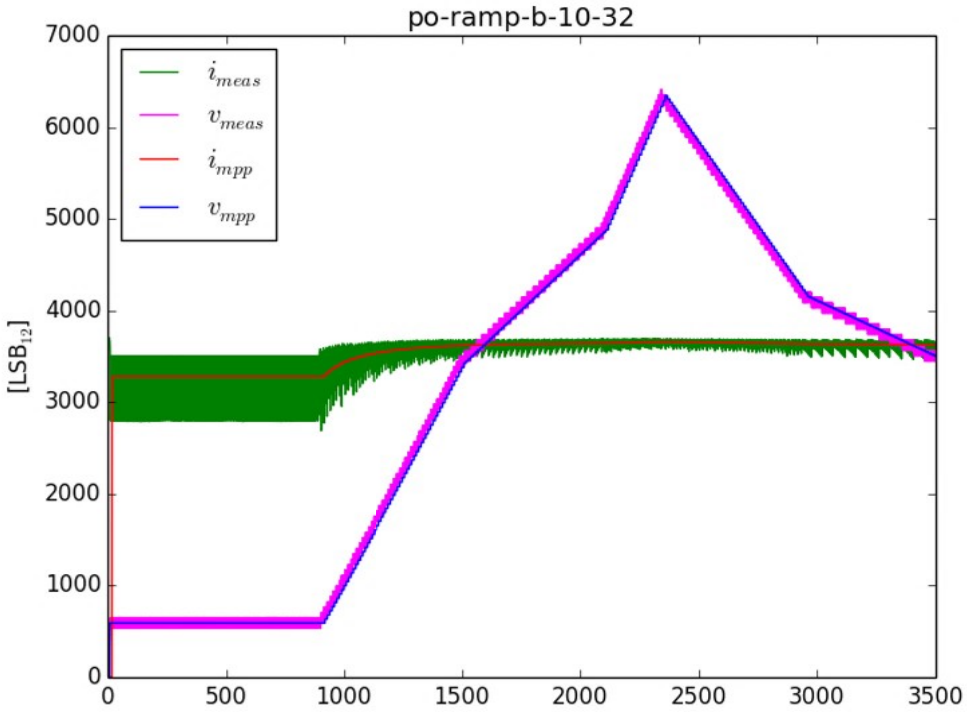
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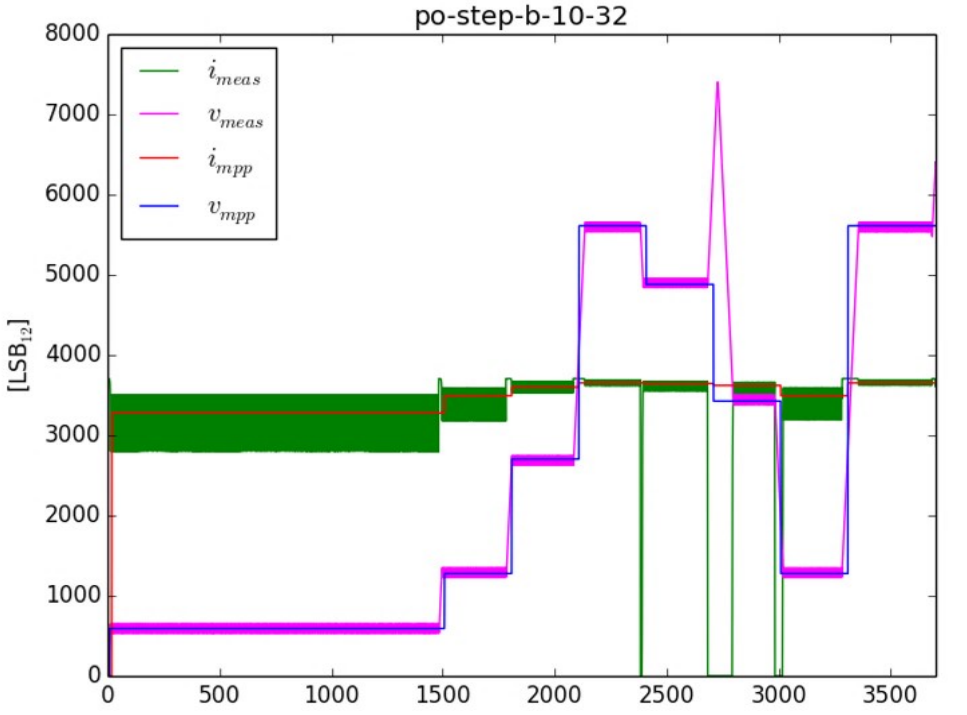
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Appendix C

Thales Group

C.1 Thales Group

Thales Group is a French industrial group that provides solutions to various industries. It is present in the aerospace industry, the space industry, the ground transportation industry, the defense industry and finally the cyber-security industry. The group has 81,000 employees in 70 countries. It spends more than €1 billion a year on research and development.

In Belgium, Thales is present on six different sites and employs approximately 1000 people. All of the Thales Group's areas of expertise are represented in Belgium.

C.2 Thales Alenia Space

Thales Alenia Space is a joint venture between Thales (67%) and Leonardo (33%). Active in satellite manufacturing, it designs and builds state-of-the-art solutions in telecommunications, satellite navigation, Earth observation, environmental monitoring, science, space exploration and orbital infrastructure. It employs 8,000 people in 9 European countries.

The main market for Thales Alenia Space (TAS) is satellites. TAS can either build complete satellites or provide pieces of equipment for satellites. The main activity in which TAS satellites or payloads are involved is telecommunications (40% of total activity). The remaining 60% is shared between earth observation, earth exploration, earth navigation, orbital infrastructure and equipment.

Within the framework of their achievements, we can mention that TAS is the prime contractor of the European meteorological satellites. Indeed, all European Meteosat meteorological satellites have been built by TAS since 1977. TAS was also the prime contractor for the Iridium NEXT satellite constellation, producing 81 satellites for the new constellation. Iridium NEXT provides global coverage of telecommunications capabilities.

C.3 Thales Alenia Space Belgium

Thales Alenia Space has 3 sites in Belgium :

- Charleroi is the "nerve center" of TAS in Belgium. The entire equipment production chain is located here, as well as the engineers in each field (chemistry, electronics, mechanics, thermal, software, etc.) and finally the general management, human resources, etc.
- Hasselt is a solar panel factory.
- Louvain is a design office.

Thales Alenia Space Belgium is one of the world's leading suppliers of power conditioning and distribution systems for European satellites and launchers such as Ariane, Soyuz and Vega. In fact, TAS-B supplies more than half of the electronics for the Ariane 5 launcher, as well as certain modules for Ariane 6 (still under development). The Russian Soyuz launchers taking off from the launch pad in Kourou (French Guiana) are equipped with the flight termination system supplied by TAS-B. Figure C.1 illustrates the different modules produced by TAS-B on three different launchers.

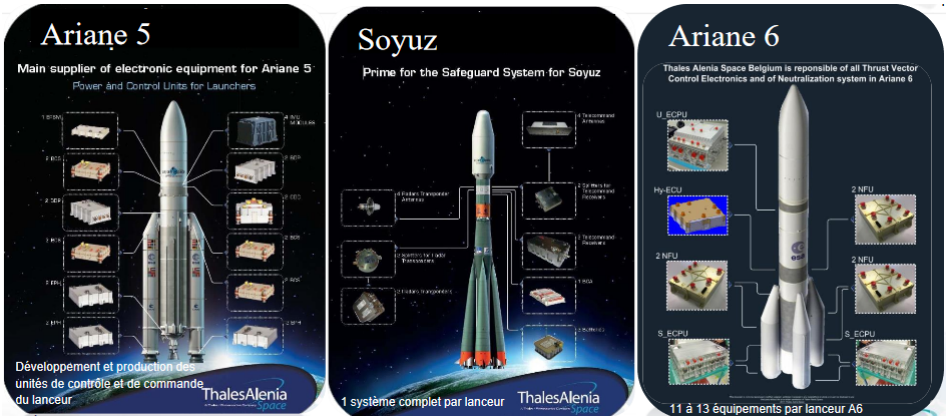

Figure C.1: Thales Alenia Space is the world leader in onboard power conditioning and distribution for European satellites and launchers

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