

École polytechnique de Louvain

Study of a dual polarity output voltage DC-DC converter for leakage current cancelling in space electrical propulsion

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Abstract

In satellites, the propulsion engines play a crucial role in changing orbits efficiently and controlling the attitude of the satellite. The current technology used in spacecraft propulsion is the use of a plasma thruster, which is connected to the power bus by means of a transformer. Thales Alenia Space has been working on a new technology called the Direct-Drive architecture, but as it remains a project for now, the need of a new kind of power supply has been identified in order to cancel leakage current.

The aim of this master thesis is to find a suitable solution that addresses the needs of the Direct-Drive architecture. A Watkins-Johnson converter will be designed, in order to deliver a dual polarity output voltage to the thruster's cathode. The theoretical design will first be explained. Then, a physical circuit will be constructed and tests will be performed in order to show the good working of this prototype.

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List of Abbreviations

AC	Alternating Current
BJT	Bipolar Junction Transistor
CCM	Continuous Conduction Mode
CRP	Cathode Reference Potential
DC	Direct Current
DCM	Discontinuous Conduction Mode
ECSS	European Cooperation for Space Standardization
EDDA	European Direct-Drive Architecture
EU	European Union
GEO	Geosynchronous Orbit
HEO	High Earth Orbit
HET	Hall Effect Thruster
IC	Integrated Circuit
IGBT	Insulated-Gate Bipolar Transistor
LEO	Low Earth Orbit
MEO	Middle Earth Orbit
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PCDU	Power Conditionning and Distribution Unit
PI	Proportional Integral (controller)
PPU	Power Processing Unit
PWM	Pulse Width Modulation
TAS	Thales Alenia Space
WJC	Watkins-Johnson converter

Introduction

Space has always fascinated people, whether it was to conquer it or for more advanced scientific research such as understanding the creation of the Earth. In order to observe Earth, to improve communication systems, or to realize scientific measurements, satellites have become a necessary tool in today's industry. Building and launching satellites is an advanced technological challenge, and Thales Alenia Space (TAS) is working on constantly improving them.

In the quest of lighter and more efficient satellites, TAS has been working on improving and creating new technologies. Among those new innovations, the so-called Direct-Drive architecture was a project done in partnership with the European Union [1]. This new architecture aims at lightening the satellite by changing its propulsion system architecture, and connecting the electrical thruster directly to the solar arrays, without using a step-up transformer. While this technology would improve the overall efficiency, it is still under development before satellites can actually work with this architecture.

Through some previously conducted research, TAS and its partners have found some shortcomings to the Direct-Drive architecture. Among those, the absence of galvanic isolation allows leakage current to flow out of the thruster. The aim of this master thesis is to overcome this already identified obstacle by designing, implementing, and testing an innovative power supply that can achieve dual polarity output voltage conversion : the output voltage of the supply must be both positive and negative, independently of the input voltage nor the current. Additionally, the input and output of the converter must share a common ground reference. The Watkins-Johnson converter stands as the ideal candidate for this application and will therefore be studied.

This thesis will be divided in eight chapters. Chapter 1 will give context to the propulsion systems of satellites, why it is necessary, how it is currently implemented and why the Direct-Drive architecture would be beneficial. It will also explain the technological challenges of this emerging technology and why a new type of power supply is needed.

Chapter 2 will review the main existing power converter for single and dual voltage quadrants converter. Then, it will analyse the Watkins-Johnson converter, a state-of-the-art converter suitable for this application.

In Chapter 3, the controllability aspects of the chosen topology will be addressed. The state-space model and the transfer functions of the converter will be derived. Then, the AC model of the converter will be studied and finally, a theoretical controller scheme will also be designed.

Chapter 4 will dive into the specific requirements of the power supply, which the design will have to be adapted to.

In Chapter 5, the design of the converter will be addressed. First, the passive components of the circuit will be designed in order to meet the constraints given in Chapter 4. Then, the choice of the active components will be detailed, including the switches selection and the design of a gate driver. Finally, computer simulations will be performed.

Chapter 6 will dive into the practical realization of the converter, by designing a printed circuit board of the converter. This chapter will show the design schematics and the assembled circuit board.

In Chapter 7, the lab measurements will be addressed. First, a test bench that best reproduces the expected behaviour of the converter will be designed and the lab set-up will be detailed. Then various measurements will be completed in order to measure the performances of the converter. An analytical loss model will be established based on a least-square approximation of the measurements. This chapter will conclude by providing further possible improvements.

Finally, Chapter 8 will conclude this thesis and will briefly summarize the performances achieved by the converter.

1 | Satellite propulsion systems

This chapter aims at giving an overview of the satellite propulsion system, and why a new type of power supply has to be designed in order for the new satellite architecture to properly function.

It will first go through the spatial context, explaining what are the different types of satellites, how they orbit and why they require propulsion systems. Then, the current propulsion architecture will be explained and compared to the emerging architecture. The challenges of the new architecture will be explained in the last part of this chapter.

1.1 Spatial context

Satellites orbit around Earth at different altitudes depending of the mission they are engaged in. They all operate in space and are therefore subject to vacuum, radiations, and extreme changes of temperatures. The four types of orbit are listed below and shown in Figure 1.1. These orbit are crucial for the satellite design, as two satellites orbiting on different orbits will not have the same requirements, in term of power, cost, equipment and lifetime.

Low Earth Orbit (LEO) Satellites in LEO have an altitude that can range from 160 km to 2000 km above Earth. These satellites are less subject to radiations than higher orbit satellites but they experience more atmospheric drag. They are widely used for Earth observation or for all kinds of satellite constellation such as Starlink [2][3][4].

Middle Earth Orbit (MEO) Extending from LEO, this orbit goes up to GEO. It can therefore range from 2000 km to 35 000 km. Satellites in this orbit are used for navigation purposes such as GPS, Galileo, etc. These satellites are subject to higher radiation than in LEO [3][4].

Geosynchronous Orbit (GEO) Satellites orbiting exactly 35 786 km above Earth, at the latitude of the equator are said to be in GEO. They orbit around Earth at the same speed than Earth's rotational speed, and they appear to constantly stay above one particular place on Earth. This orbit is primary used for telecommunications [3][4].

High Earth Orbit (HEO) With an apogee that is at least 200 km higher than GEO, these orbits are often highly elliptical, and subject to high radiation because they cross high radiation belts during their orbit. Satellites on these orbits can be used for telecommunication also, especially for high latitude places, where GEO satellites do not offer a good coverage [3][4].

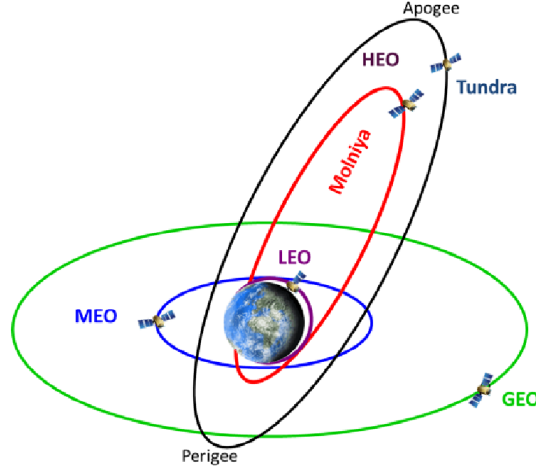


Figure 1.1: Satellites orbits [5].

Whatever the orbit, satellites are always launched by a rocket, that uses fuel in order to elevate in the sky. However, in order to be more efficient and consume less fuel, the satellites are not always placed directly on their orbit by the rocket, but they are disconnected from the rocket earlier in the process, and use their own propulsion system in order to reach their final orbit. This is particularly the case for GEO satellites, as they have to go further into space. Such a process is called transferring orbits, where the satellite elevates from a lower orbit to a higher orbit. The most effective transfer orbit is called a Hohmann transfer (represented in Figure 1.2), requiring minimal change of velocity for the satellite to change orbits.

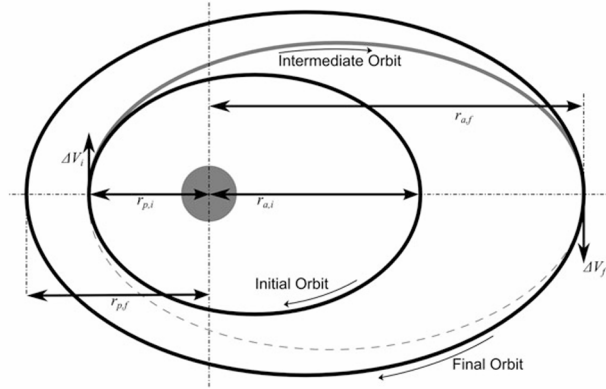


Figure 1.2: Hohmann transfer orbits [4].

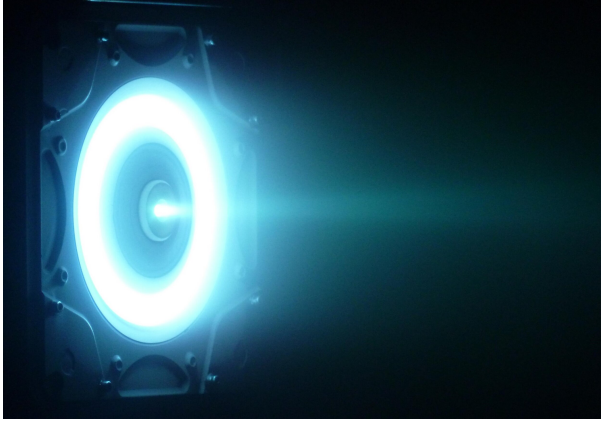
Chemical propulsion engines can exert a large change of velocity in order to reach a higher orbit. Electrical engines such as plasma thruster, however, are unable to give such a large difference of velocity. Instead, they reach their final orbit through a long and repetitive change of orbits, which can take up to a few months. Nowadays, plasma thruster is the most common type of propulsion system for satellites, as it is more efficient than chemical thrusters.

This type of thruster is also a good candidate for on-orbit service and interplanetary space vehicles, as these vehicles also operate in space for a long period of time, with maximal efficiency.

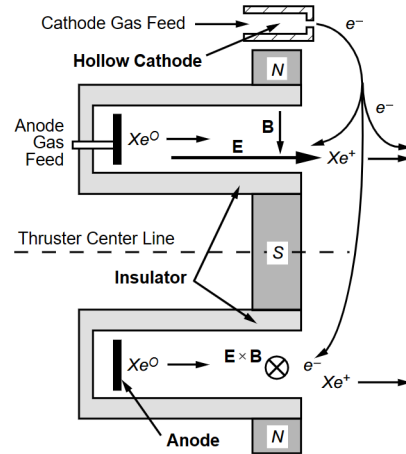
1.2 Plasma thruster

The electrical propulsion is usually achieved through ionisation of a gas. The ions of the gas are accelerated to reach a large exhaust velocity, and create thrust. A commonly used electrical thruster is the Hall Effect Thruster (HET). Its working principle is simpler than other types of ion thruster, and it requires few power supplies to operate [6].

HET operates as follow: inside a chamber, a radial magnetic field is created by permanent magnets or electromagnets. A perpendicular, axial electric field is created between the anode and the cathode of the thruster. These perpendicular fields trap some electrons and create a current by hall effect. At the anode, a gas is released, and is ionized because of the interaction of the atoms with the hall current. The positive charges are accelerated with the applied electric field and reach a large exhaust velocity. Upon exiting, they pull an equal number of electrons, and create a plasma plume with no net charges. An HET during firing test and its schematic cross section are shown in Figure 1.3. The blue color in the circular part of the HET is the Xenon ions (Xe^+) expelled by the anode, while the color of the central part is due to the electrons produced at the anode. Together, they will form a neutrally charged plume.



(a) During firing tests [7].



(b) Cross section schematic. [6].

Figure 1.3: Hall Effect Thruster.

The efficiency of the HET is limited by the hall current, because 20 % to 30 % of the discharge current is an electron current responsible for the hall effect in the chamber, which does not produce thrust. The remaining 70 % to 80 % is the ion current creating thrust [8]. The discharge current is therefore proportional to the volume of gas required to produce thrust.

In a satellite, the electrical thruster is linked to the remaining of the satellite through the Power Processing Unit (PPU), which is itself linked to the main power bus of the satellite. This bus and its associated electronic is called the Power Conditioning and Distribution Unit (PCDU). On one side of the PCDU, the solar array feeds power when the sun illuminates the solar array. The PCDU stores the energy in batteries and feeds it to the loads and the PPU. At times in the orbit, the satellite enters Earth's shadow and the energy is directly fed from the batteries, because the solar arrays are not illuminated. A simplified schematic of this architecture is shown in Figure 1.4

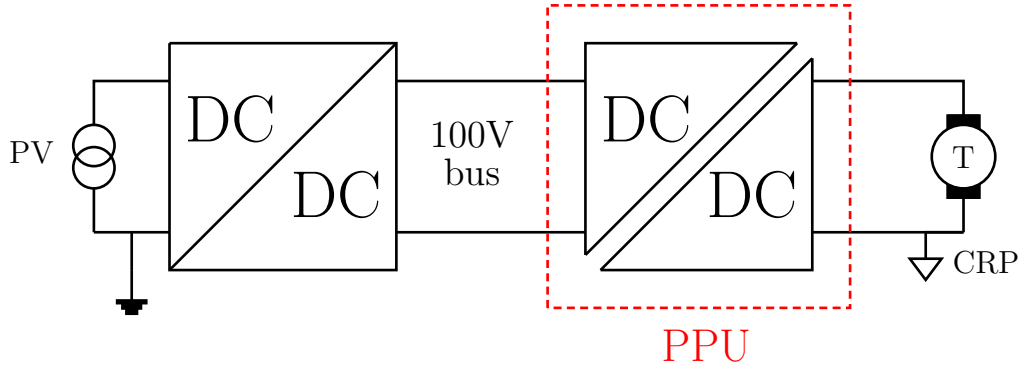


Figure 1.4: Current satellite propulsion system architecture. On the right, a DC-DC converter with galvanic isolation is represented.

Currently, the solar array and the main power bus are usually limited to 100 V in order to reduce the risk of arcing (i.e. creating an electric arc)[9]. The electrical thruster, however, requires a larger input voltage, of around 300 V. In order to reach this voltage, the PPU is responsible for stepping up the voltage of the main power bus. This is currently done through a transformer, which also provides galvanic isolation.

The usage of a step-up transformer has advantages but also drawbacks. Its main advantage is that it eliminates leakage current. This current can come from many different sources as the structure of a satellite is quite complex. Since the transformer provides galvanic isolation, its output voltage is floating and the cathode of the thruster is at a floating voltage reference called the Cathode Reference Potential (CRP). In practice, this floating end is connected to the ground potential of the satellite through a RC network, since nothing can be left at a floating potential in space, in order to avoid charge accumulation and arcing. As a result, if leakage current was to flow, the floating voltage of the transformer (and of the thruster) would change, in the direction opposing the leakage current to flow [10]. The propulsion system with this transformer is shown in Figure 1.5. Additionally, the usage of a transformer allows to keep the main power bus at a lower voltage, thus reducing the risk of arcing. However, this transformer makes the PPU quite heavy, and decreases its total efficiency. As a result, improving the PPU by connecting the thruster directly to the PCDU by removing the transformer would increase the overall efficiency of the satellite, and decrease the cost at launch, since the satellite would be lighter.

With this objective in mind, the European Union (EU) funded a project called European Direct-Drive Architecture (EDDA), which had to investigate the possibility of connecting the electrical thruster directly to the main power bus, therefore removing the currently needed transformer.

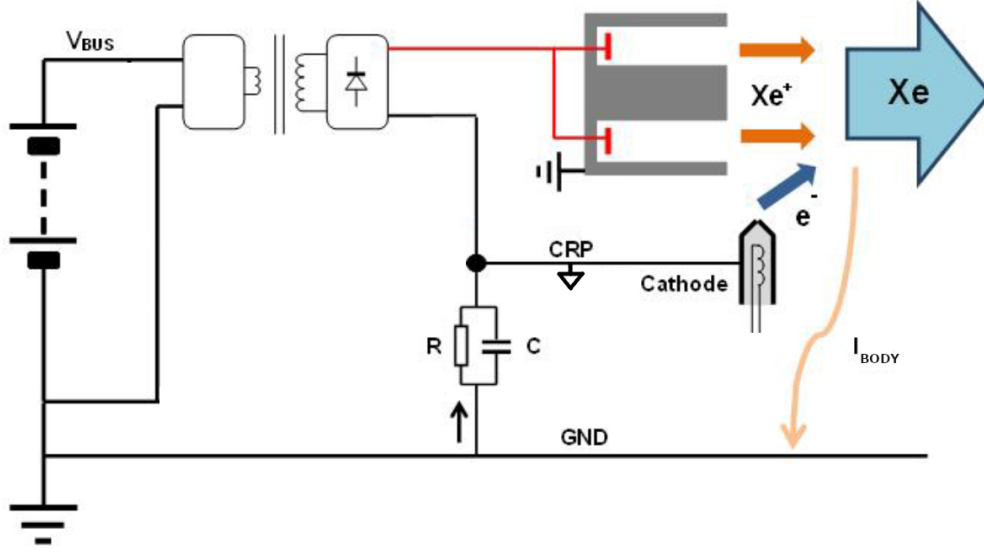


Figure 1.5: PPU and thruster with the current architecture. I_{body} represents the leakage current [10].

1.3 Direct-Drive

The Direct-Drive architecture is thus another architecture for spacecraft propulsion, where the electrical thruster would be directly connected to the main power bus of the PCDU.

This new architecture has been developed by TAS and different partners for the EDDA project and the propulsion system's architecture is shown in Figure 1.6. According to them, the Direct-Drive would significantly improve the spacecraft's propulsion performances. Table 1.1 summarizes the expected improvements of this new architecture compared to the standard one [11].

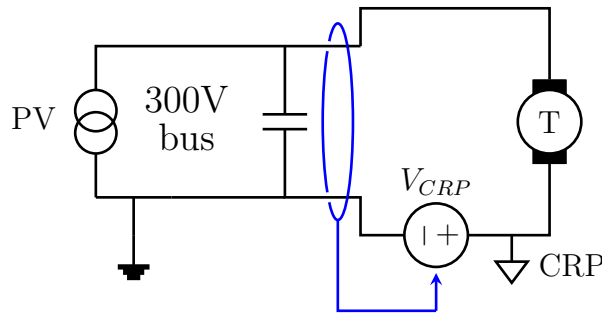


Figure 1.6: Direct-Drive satellite propulsion system architecture .

Although it would permit major improvements in spacecraft propulsion, it also holds notable challenges. First, the main power bus voltage must increase, as the thrusters have a nominal voltage of around 300 V [9] [12][13]. Secondly, common mode leakage current could flow more easily as the thruster's voltage is not floating. This could be mitigated by the means of a converter that would change the Cathode Reference Potential (CRP) in order to oppose the leakage current, therefore artificially creating a floating CRP.

Performances	Standard architecture	Direct-Drive architecture
PPU efficiency	95%	> 99%
Thermal losses	10%	< 2%
PPU Mass saving	/	−50%

Table 1.1: Direct-Drive architecture expected benefits [11].

1.3.1 Bus voltage increase

The main risk of increasing the bus voltage is arcing. Arcing (creating an electrical arc between two conductors) is due to a combination of high voltage and low pressure. The breakdown voltage (voltage at which an arc can be produced) can be characterized as a function of the distance between the conductors and the pressure using the Paschen curve. Paschen curves for different gas are shown in Figure 1.7. At low pressure-distance gap, the mean free path of electrons becomes significant and the breakdown voltage is high. The breakdown voltage decreases as the quantum effects become negligible, but as the distance increases drastically, the breakdown voltage increases again [14]. Space standards make sure that the bus voltages in a spacecraft remain below the minimal breakdown voltage.

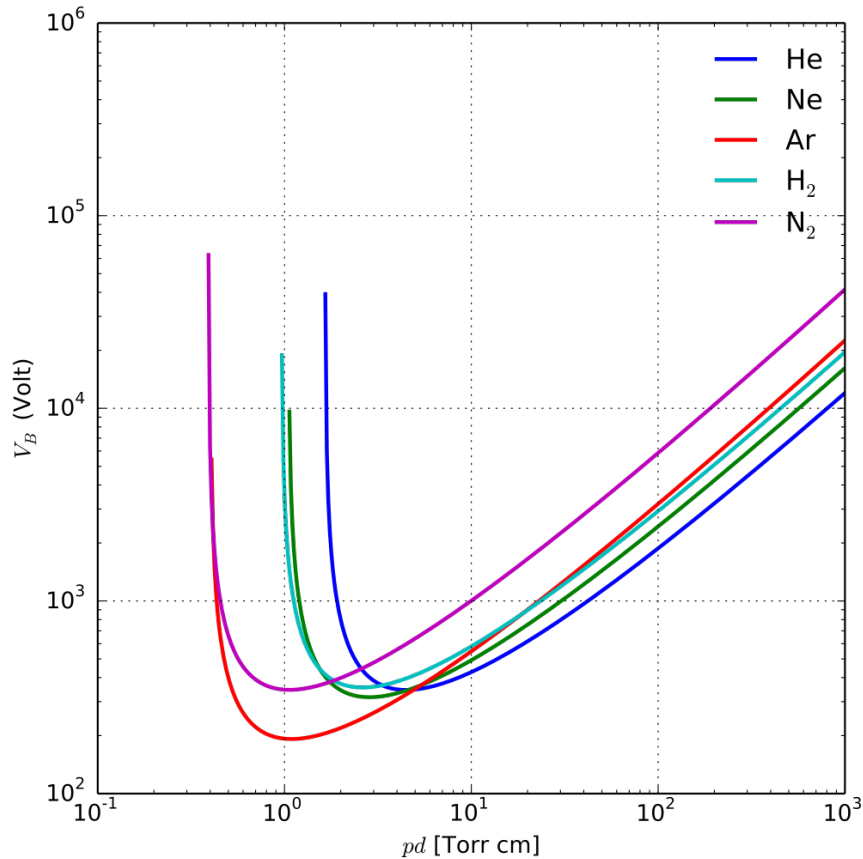


Figure 1.7: Breakdown voltage versus pressure-distance product for different gas [14].

In space, arcing may occur in different phases:

- during launch at the minimum Paschen pressure (1 mbar) above 100 km altitude),

- during outgasing (in early phase after launch or if any material degradation occurred),
- outside the spacecraft due to environment, mainly on the solar array [13].

For the Direct-Drive architecture, the voltage requirements had already been studied in a previous EU project (HV-EPISA). Those results gave confidence in mitigating the arcing risk for the solar arrays and the main bus at 300 V [13].

1.3.2 Leakage current cancellation

The second challenge of the Direct-Drive architecture was to minimize the common mode leakage current flowing through the structure. Since the thruster's voltage is not floating any more, a new power supply was added between the ground and the cathode, to bias the Cathode Reference Potential (CRP), called the CRP supply. The new propulsion system with the CRP supply is shown in Figure 1.8.

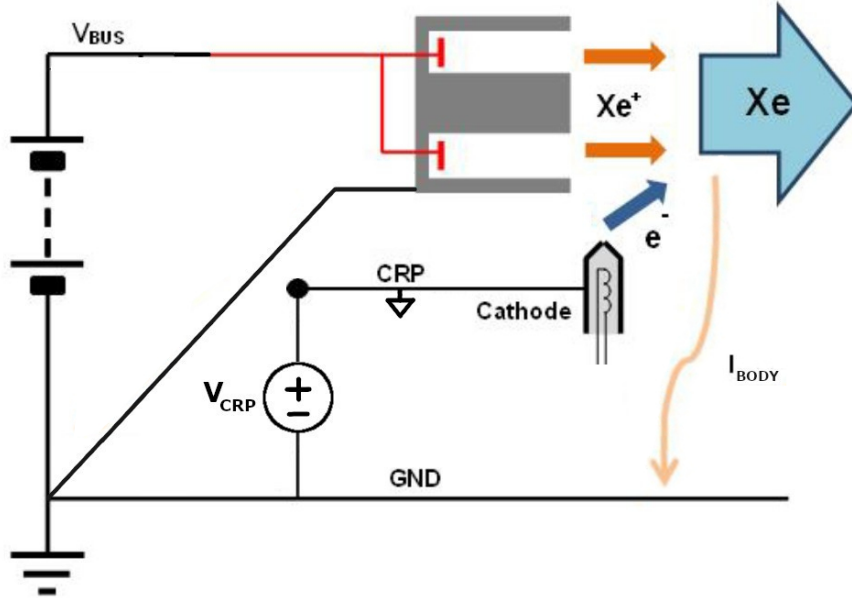


Figure 1.8: PPU and thruster with the Direct-Drive architecture. I_{body} represents the leakage current [15].

Initially, the CRP supply was an unidirectional voltage supply, as it was only expected to bias the cathode with negative voltage in order to suppress the common mode current of the thruster [10]. However, during testing, TAS and its partners discovered that the CRP voltage could be both positive or negative depending on the situation. An active load was added in series with the unidirectional CRP supply in order to perform the test [9].

Figure 1.9 shows the common mode current characteristic as a function of the applied CRP voltage, measured during the EDDA test campaign. It can be seen that in order to limit the leakage current ($I_{body} = 0$), the CRP voltage (V_{CRP}) can be both positive or negative depending on the situation or the power of the thruster.

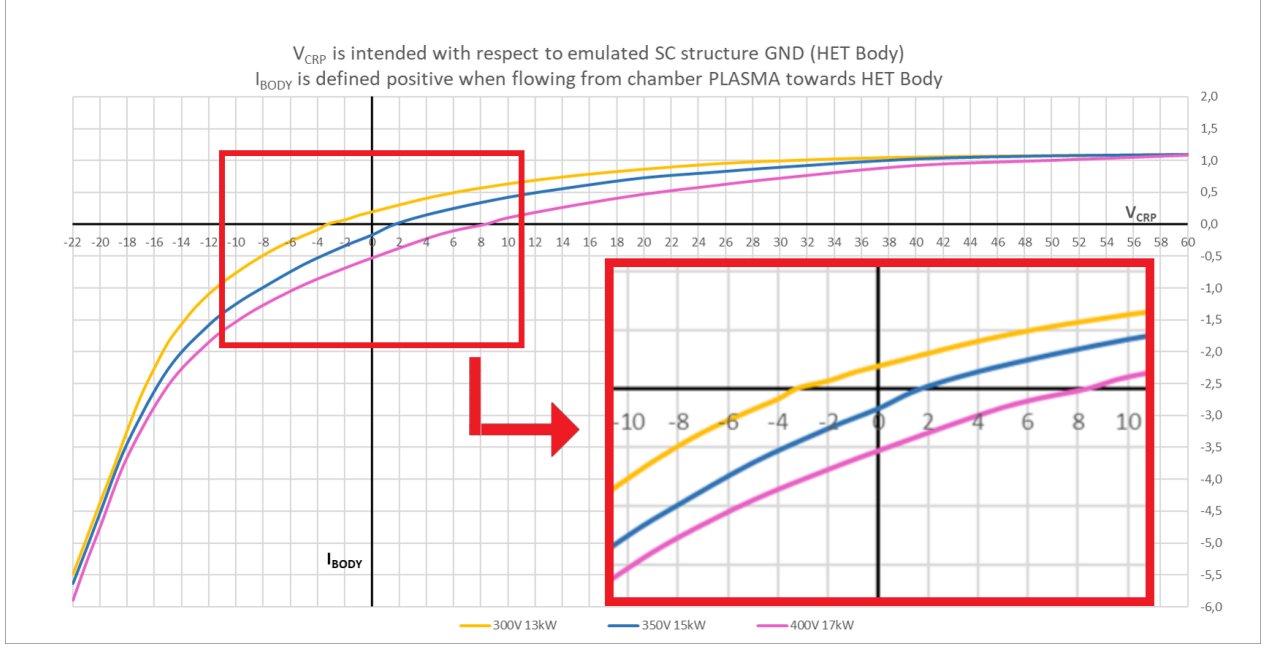


Figure 1.9: Leakage current characteristic measured by SITAEL during EDDA test campaign [15].

Although EDDA project showed promising results and a good alternative to the current spacecraft propulsion architecture, its executive summary mentioned : *"The cathode potential may be positive or negative depending on configuration and environment. This requires a two-quadrant cathode supply. Further investigations shall be done based on theory as well as already experimented situations"* [13].

The aim of this thesis is to find a suitable topology that can achieve this dual polarity voltage for the CRP supply, to implement it and to test it. The particularity of this power supply is that it must provide this positive and negative voltage, while being connected to the ground reference of the satellite.

2 | Review of topologies

In order to minimize the common mode leakage current in the propulsion architecture, tests have shown that the CRP supply had to be bipolar in output voltage (positive and negative). A new converter with a suitable topology has to be designed in order to do so, while having the output voltage connected to the ground of the satellite.

This chapter will review state of the art converters. Single voltage quadrant and two voltage quadrants converters will be reviewed. Later, it will also review a converter that can achieve this two quadrant power transfer while having the load connected to the ground, as required for the CRP supply.

2.1 Single voltage quadrant converter

The most basic converter to step-down a voltage is the Buck converter. It is composed of two switches, which operate in a complementary manner : when S_1 is ON, S_2 is OFF and vice-versa. The output voltage oscillates between V_{in} and 0, and the transfer function of this converter is

$$\frac{V_{out}}{V_{in}} = D, \quad (2.1)$$

where $D = \frac{t_{on}}{t_{on}+t_{off}}$ is the duty cycle, the ratio of on-time of S_1 over the full wave period. Its topology and associated output voltage are shown in Figure 2.1.

This topology is also close to a half bridge converter, where capacitors would be placed between the load and the input voltage, and between the load and the ground.

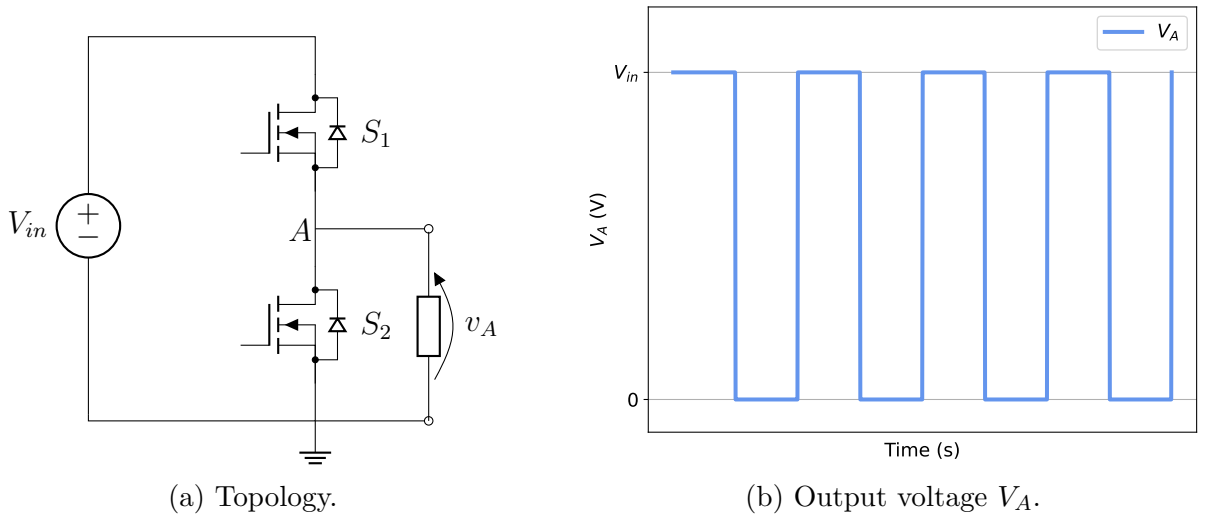


Figure 2.1: Single quadrant converter.

2.2 Two voltage quadrant converter

In order to obtain two voltage quadrants, another converter has to be considered. A commonly used converter to achieve bipolar power transfer is the full bridge converter. The full bridge converter is composed of two half bridge legs, with the load connected between the two legs. Figure 2.2a shows the topology of the full bridge converter. Both legs of the converter are controlled in a complementary manner, while in each leg, each switch operates sequentially.

Switches S_1 and S_3 operate simultaneously and switches S_2 and S_4 as well : while S_1 and S_3 are ON, S_2 and S_4 are OFF and vice-versa. This allows for both positive and negative output voltage, while the direction of the current is determined by the load. The output voltage V_{AB} is shown in Figure 2.2b. This converter is said to operate in four quadrants, which are shown in Figure 2.3.

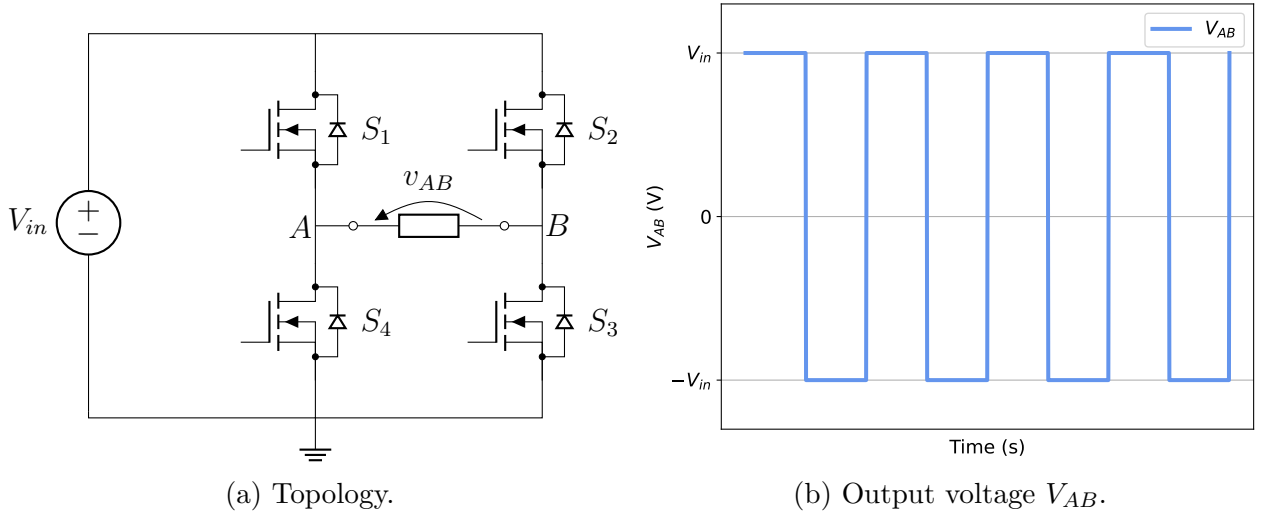


Figure 2.2: Full Bridge converter.

The input-output transfer function is given by

$$\frac{V_{out}}{V_{in}} = 2D - 1, \quad (2.2)$$

with D the duty cycle. From Equation 2.2, one can see that the output voltage V_{out} is stepped down, and can be both positive and negative.

With regards to the specification of the CRP power supply needed in the PPU, this topology fulfils some criterion but not all. The CRP bias needs to source current and supply voltage that can range from negative to positive values. It must therefore operate in quadrant 1 and quadrant 4. The full bridge converter meets (and exceeds) this requirement since it can operate in all quadrants.

However, the voltage applied on the load must have a common ground reference with the input power supply, which is not the case here. Indeed, the voltage at node B V_B is constantly changing, or is said to be floating.

In order to overcome this major drawback, another converter has to be implemented, such that is still operates at least in quadrant 1 and 4, but has a common reference point for the load and the input power supply. This new converter will be analysed in the next section.

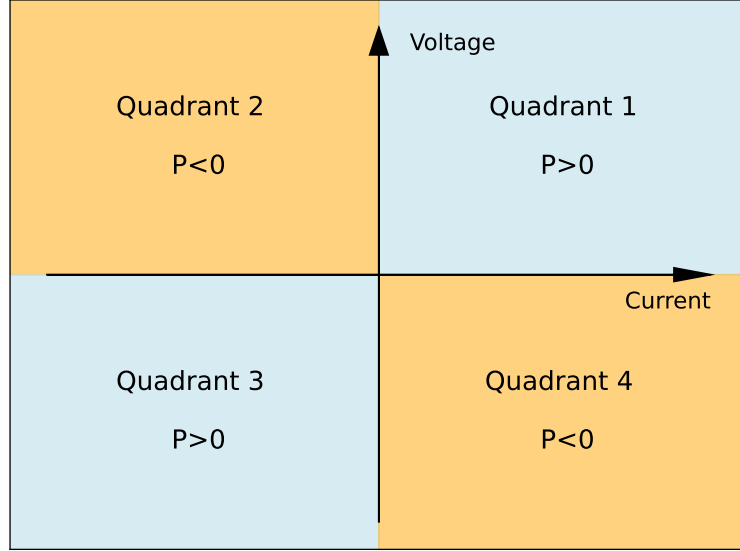


Figure 2.3: Four quadrants representation. $P > 0$ is defined as sourced by the input and $P < 0$ as consumed by the input.

2.3 Watkins-Johnson converter

In order to meet the specification, a possible solution is based on the topology of the full bridge converter. Instead of having the load connected between the two legs of the full bridge, an inductor can be placed there, and the load and its filtering capacitor are connected between S_3 and the ground. This converter, also known as Watkins-Johnson converter (WJC), was proposed in [16] to achieve a four quadrant DC-AC conversion. Figure 2.4 shows the topology of this proposed converter. While the application, control and sizing of the converter presented in [16] differ from the specification of the CRP supply, the topology remains of great interest.

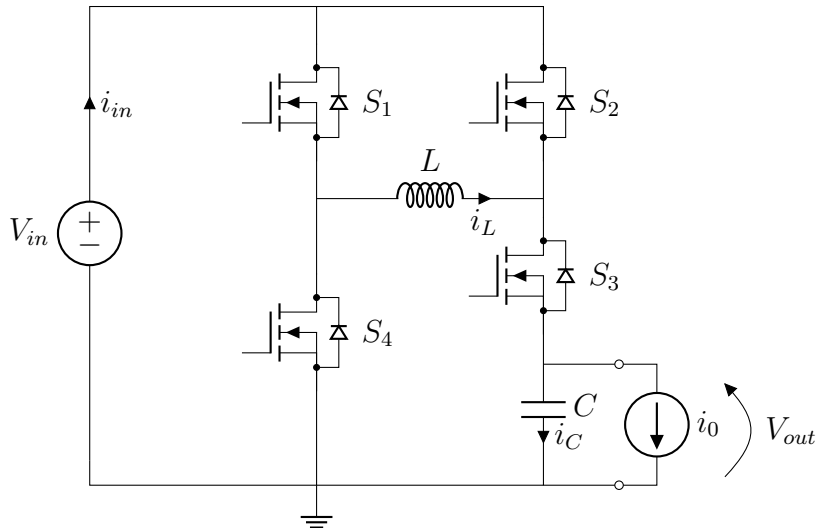


Figure 2.4: Watkins-Johnson converter proposed in [16].

Assuming that the converter is operated in Continuous Conduction Mode (CCM), meaning that the current in the inductor never decreases beyond 0 A, and keeps flowing in the same direction, the switches S_2 and S_4 could be replaced by diodes, making the driving stage

of the switch easier since there are less active switches. This other possible topology (with diodes) is shown in Figure 2.5. In Chapter 5, the losses of the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) and the diodes will be compared, to see which topology is more efficient. But for now, it will be assumed that the converter is constituted of four MOSFET, though it does not have an impact on the principle of operation. Finally, the load of the converter is represented as a constant current load. As it was explained in Chapter 1, the power supply is placed in series with the electrical thruster, which requires a constant current proportional to the flow of injected gas, that can be represented as a current load.

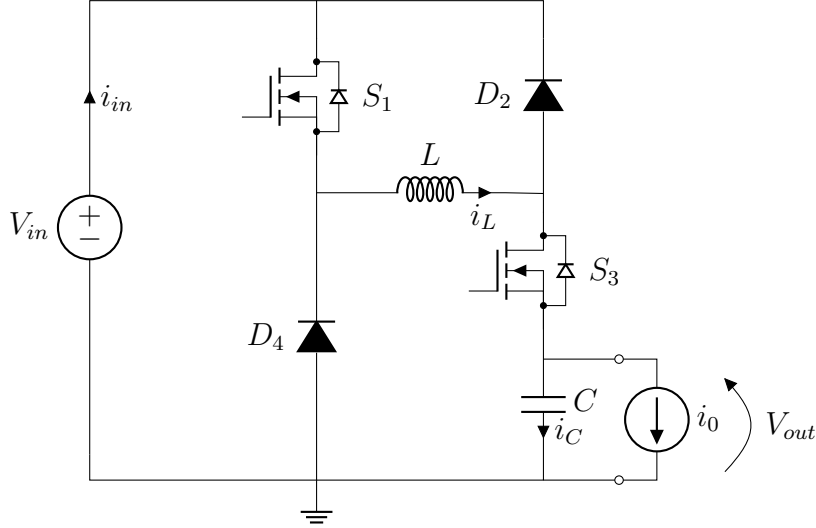


Figure 2.5: Watkins-Johnson converter with two active switches and two diodes.

2.3.1 Principle of operation

The Watkins-Johnson converter operates as follow : S_1 and S_3 are ON and conduct current. The voltage applied on the inductor is positive and current builds up in the inductor according to

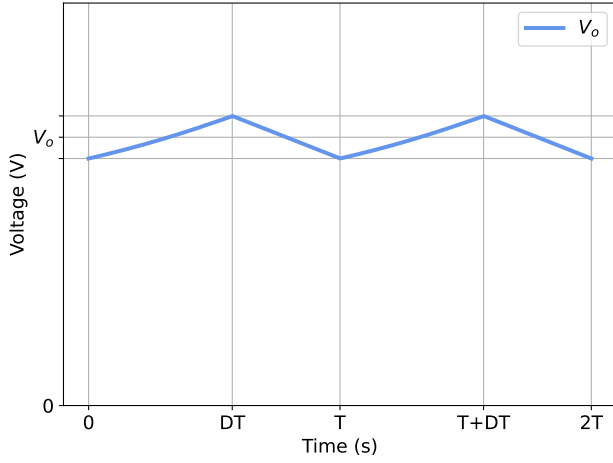
$$V_L = L \frac{di_L}{dt}. \quad (2.3)$$

The inductor current flows through S_3 , feeds the load and charges the capacitor.

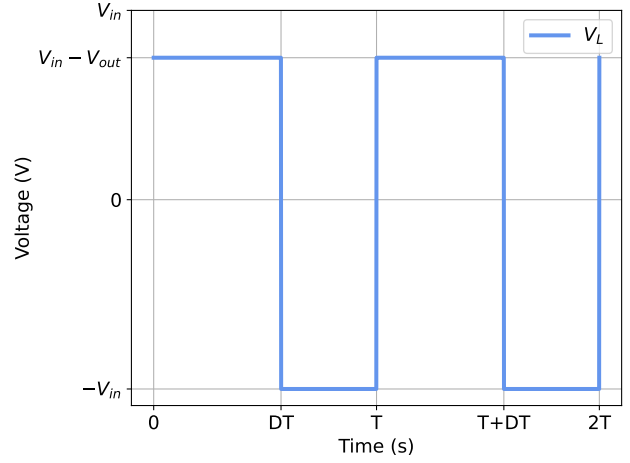
When S_1 and S_3 are OFF, S_2 and S_4 are ON simultaneously. The current in the inductor keeps flowing in the same direction, but decreases since the voltage applied on the inductor is negative. The voltage source sinks the current and absorbs power. Since S_3 is not conducting, the capacitor discharges and feeds current to the load. The current in the load is constant, and assuming that the capacitor is large enough, the output voltage remains constant. Figure 2.6 shows the waveforms of the WJC.

The input-output transfer function can be found by computing the volt-second balance on the inductor : since the converter operates in steady state, the current in the inductor must be the same at the start of each period, so that the inductor does not saturate. In steady-state, the average voltage applied on the inductor is 0 V:

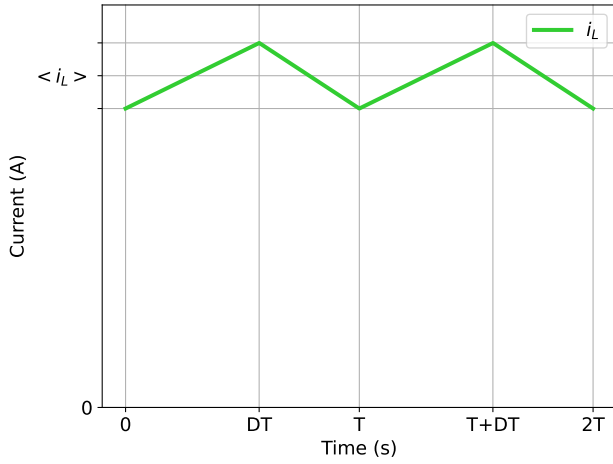
$$\frac{1}{T} \int_0^T V_L dt = \frac{1}{T} \left(\int_0^{DT} V_L dt + \int_{DT}^T V_L dt \right) = 0. \quad (2.4)$$



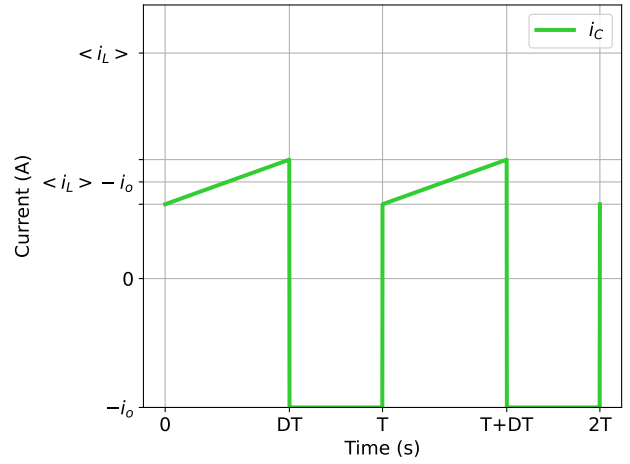
(a) Output voltage.



(b) Voltage across the inductor.



(c) Inductor current.



(d) Capacitor current.

Figure 2.6: Theoretical waveforms across the main components of the WJC.

From 0 to DT , S_1 and S_3 are ON thus $V_L = V_{in} - V_{out}$, and from DT to T , S_2 and S_4 are ON thus $V_L = -V_{in}$. Equation 2.4 can be rewritten as

$$\frac{1}{T} \left(\int_0^{DT} (V_{in} - V_{out}) dt + \int_{DT}^T -V_{in} dt \right) = D(V_{in} - V_{out}) - (1 - D)V_{in} = 0. \quad (2.5)$$

The transfer function can then be computed and is given by

$$\frac{V_{out}}{V_{in}} = \frac{2D - 1}{D}. \quad (2.6)$$

Figure 2.7 shows this transfer function and its difference with the transfer function of the full bridge converter. Key values of duty cycle and transfer function are given in Table 2.1.

It is important to note that the transfer function is continuous around $D = 0.5$. Indeed, since the output voltage will be controlled such that it cancels the common mode current, it will vary between positive and negative values around 0 V. Having a discontinuity around the point of operation, i.e. the value of D that makes $V_{out} = 0$, would have been problematic, in terms of power dissipation, control, etc.

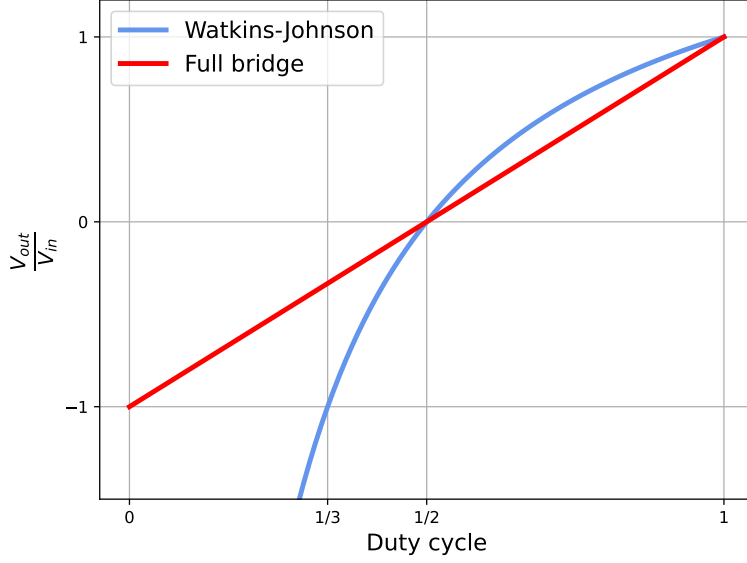


Figure 2.7: Transfer functions for Watkins-Johnson (WJC) and full bridge (FBC) converters.

D	$\frac{V_{out}}{V_{in}}$ WJC	$\frac{V_{out}}{V_{in}}$ FBC
0	$-\infty$	-1
$\frac{1}{3}$	-1	$-\frac{1}{3}$
$\frac{1}{2}$	0	0
1	1	1

Table 2.1: Key duty cycle values for Watkins-Johnson (WJC) and full bridge (FBC) converters.

2.3.2 Alternative topology

Another way of designing a Watkins-Johnson converter with coupled inductors is shown in Figure 2.8 [17] [18] [19] .

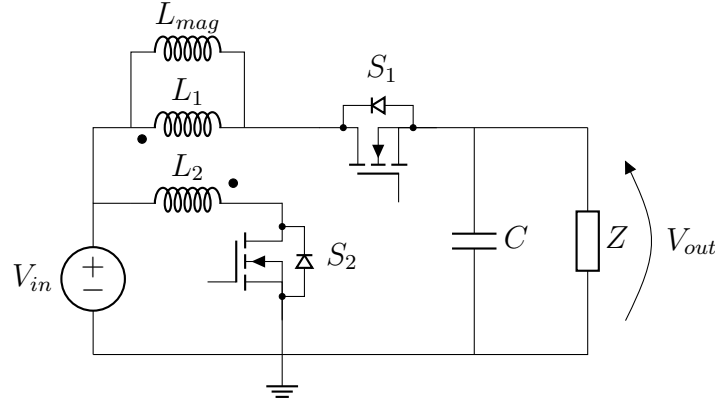


Figure 2.8: Watkins-Johnson converter with coupled inductors.

The working principle remains quite similar to that of the topology presented previously. When switch S_1 conducts, current builds up in the core of the inductor and switch S_2 is OFF. When S_1 is turned-off, S_2 turns-on and the current is fed back to the voltage source. During this process, the load current is supplied by the capacitor.

The transfer function of this converter remains the same than Equation 2.6. Though it may look less complex, this topology has advantages and drawbacks. As for the other topology of the WJC, the switch S_2 could be replaced by a diode (whose anode is connected to the ground). But for the same reasons explained previously, and in order to compare similar solutions, this topology with diode will not be explored. However, it would again be easier to control the converter with a diode instead of S_2 , but would also imply Discontinuous Conduction Mode (DCM) problems if the load current is too low.

2.3.3 Choice of the topology

The four-switches version of the WJC has the disadvantage of having twice as many switches than the coupled inductors version of the WJC, requiring more driving units, thus more space on the Printed Circuit Board (PCB). However, the stress is much lower on each switch, since the switches must block a voltage of either V_{in} or $V_{in} - V_{out}$, depending on the switch. On the other hand, the alternative topology has switches that are more stressed, because they must block $(1 + \frac{n_1}{n_2})V_{in} - V_{out}$ for the switch S_1 and $(1 + \frac{n_2}{n_1})V_{in} - V_{out}$ for the switch S_2 . n_1 and n_2 represent the number of turns for each coil of the coupled inductor.

Assuming $n_1 = n_2$ for the sake of simplicity, the switches of the alternative topology must block approximately twice as much voltage than the four-switches topology, but for twice less switches. The switching losses on one single component will increase since the voltage is higher when switching. Moreover, switches with a higher voltage rating also have larger $R_{ds,on}$, thus leading to increased losses. Doubling the blocking voltage capability of a switch does not effectively double its on state resistance, but could increase it even further depending on the component. Also, with higher losses on a single component comes the fact that more heat has to be extracted, increasing the complexity of the thermal management. Table 2.2 summarises the advantage and drawbacks of both topologies.

Though both topologies offer different advantages and drawbacks, it has been decided to work with the initial topology of the WJC, using four switches and no coupled inductors.

	4-switches WJC	Coupled inductors WJC
Switches	4	2
Stress per switch	Low	High
Thermal management	Easier	Harder
Overall losses	Similar	Similar
PCB area	Larger	Smaller

Table 2.2: Comparison of the four-switches WJC and coupled inductors WJC.

3 | Controllability and small signal model

Independently of the sizing of the converter, its controller must also be designed with care.

The objective of the controller is that the converter's output matches a reference point. This can be done through a feedback loop and a variation of parameters, such as the duty cycle.

This chapter will first establish the state-space model of the Watkins-Johnson converter, in order to find its different voltage gains, current gains, input and output impedances. Then, its AC equivalent model (which can be represented in the same form for any converter) will be established. The derivation of the state-space model and the small signal equivalent circuit follows the steps presented in [20]. Finally, this chapter will go over the controller design.

3.1 State-space model

An important aspect of the control of the converter is its state-space model. It allows to study transient phenomena happening through a change of state (change in voltage/current/duty cycle) around an operating point. In this section, variables will be defined as the sum of their steady-state value at the point of operation and their small variations around that point. For example, $i_L = I_L + \hat{i}_L$, or $d = D + \hat{d}$. Finally, all parasitic behaviour (parasitic capacitances, inductances and resistances) will be neglected as they can hardly be identified and they would complicate the model.

The state variables are i_L and v_{out} , and the inputs are v_{in} and i_o . When S_1 and S_3 are ON, the state equations are

$$\begin{cases} \frac{di_L}{dt} = \frac{v_{in} - v_o}{L} \\ \frac{dv_{out}}{dt} = \frac{i_L - i_o}{C} \end{cases} \quad (3.1)$$

and when they are OFF,

$$\begin{cases} \frac{di_L}{dt} = \frac{-v_{in}}{L} \\ \frac{dv_{out}}{dt} = \frac{-i_o}{C} \end{cases} \quad (3.2)$$

Since S_1 and S_3 are ON during dT and OFF during $(1-d)T$, state averaging can be performed to combine the two set of equations. Written in vector form, it gives

$$\frac{d}{dt} \begin{bmatrix} i_L \\ v_{out} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-d}{L} \\ \frac{d}{C} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_{out} \end{bmatrix} + \begin{bmatrix} 0 & \frac{2d-1}{L} \\ \frac{-1}{C} & 0 \end{bmatrix} \begin{bmatrix} i_o \\ v_{in} \end{bmatrix}, \quad (3.3)$$

which can also be written as

$$\frac{d}{dt}\mathbf{x} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}, \quad (3.4)$$

with $\mathbf{x}$ the state vector and $\mathbf{u}$ the input vector. An output vector can also be computed :

$$i_{in} = \begin{bmatrix} 2d - 1 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_{out} \end{bmatrix} \quad (3.5)$$

or more generally,

$$\mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u}. \quad (3.6)$$

In this case, the matrix $\mathbf{D}$ is $\mathbf{0}$.

In steady-state, or at equilibrium, there are no small variations: $\frac{d}{dt}\mathbf{x} = 0$ and

$$\begin{bmatrix} I_L \\ V_{out} \end{bmatrix} = \begin{bmatrix} \frac{1}{D} & 0 \\ 0 & \frac{2D-1}{D} \end{bmatrix} \begin{bmatrix} I_o \\ V_{in} \end{bmatrix}. \quad (3.7)$$

Small AC variation can be introduced in the model, such that $\mathbf{x} = \mathbf{X} + \hat{\mathbf{x}}$, $\mathbf{u} = \mathbf{U} + \hat{\mathbf{u}}$ and $d = D + \hat{d}$, where the small variation is considered much smaller than the steady state value:

$$\hat{\mathbf{x}} \ll \mathbf{X}. \quad (3.8)$$

The small signal state-space model can be rewritten as

$$\frac{d}{dt}\hat{\mathbf{x}} = \mathbf{A}(D, \hat{d})\hat{\mathbf{x}} + \mathbf{B}(D, \hat{d})\hat{\mathbf{u}}, \quad (3.9)$$

where $\mathbf{A}$ and $\mathbf{B}$ still depends on d . The same can be done for Equation 3.6. These equations contain some second order AC terms, which can be neglected. As detailed in Appendix A the small signal model is expressed by

$$\begin{aligned} \frac{d}{dt}\hat{\mathbf{x}} &= \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\hat{\mathbf{u}} + ((\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U})\hat{d} \\ \hat{\mathbf{y}} &= \mathbf{C}\hat{\mathbf{x}} + ((\mathbf{C}_1 - \mathbf{C}_2)\mathbf{X}), \end{aligned} \quad (3.10)$$

where

$$(\mathbf{A}_1 - \mathbf{A}_2) = \begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & 0 \end{bmatrix}, \quad (3.11)$$

$$(\mathbf{B}_1 - \mathbf{B}_2) = \begin{bmatrix} 0 & \frac{2}{L} \\ 0 & 0 \end{bmatrix}, \quad (3.12)$$

and

$$(\mathbf{C}_1 - \mathbf{C}_2) = \begin{bmatrix} 2 & 0 \end{bmatrix}. \quad (3.13)$$

Introducing Laplace variable $s = \frac{d}{dt}$, Equation 3.10 rewrites as

$$\begin{aligned}
s \begin{bmatrix} \hat{i}_L \\ \hat{v}_{out} \end{bmatrix} &= \begin{bmatrix} 0 & \frac{-D}{L} \\ \frac{D}{C} & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_{out} \end{bmatrix} + \begin{bmatrix} 0 & \frac{2D-1}{L} \\ \frac{-1}{C} & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_o \\ \hat{v}_{in} \end{bmatrix} + \begin{bmatrix} \frac{2V_{in}-V_{out}}{L} \\ \frac{I_L}{C} \end{bmatrix} \hat{d} \\
\hat{i}_{in} &= \begin{bmatrix} 2D-1 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_{out} \end{bmatrix} + 2i_L \hat{d}
\end{aligned} \tag{3.14}$$

Finally, it gives

$$\begin{aligned}
\begin{bmatrix} \hat{i}_L \\ \hat{v}_{out} \end{bmatrix} &= \frac{1}{s^2 + \frac{D^2}{LC}} \left(\begin{bmatrix} \frac{D}{LC} & s \frac{2D-1}{L} \\ \frac{-s}{C} & \frac{D(2D-1)}{LC} \end{bmatrix} \begin{bmatrix} \hat{i}_o \\ \hat{v}_{in} \end{bmatrix} + \begin{bmatrix} \frac{s(2V_{in}-V_{out})}{L} - \frac{DI_L}{LC} \\ \frac{D(2V_{in}-V_{out})}{LC} + \frac{sI_L}{C} \end{bmatrix} \hat{d} \right) \\
\hat{i}_{in} &= \begin{bmatrix} 2D-1 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_{out} \end{bmatrix} + 2i_L \hat{d},
\end{aligned} \tag{3.15}$$

which can be compared to

$$\begin{bmatrix} \hat{i}_L \\ \hat{v}_{out} \end{bmatrix} = \begin{bmatrix} G_I & Z_{in}^{-1} \\ Z_{out} & G_V \end{bmatrix} \begin{bmatrix} \hat{i}_o \\ \hat{v}_{in} \end{bmatrix} + \begin{bmatrix} G_{ID} \\ G_{VD} \end{bmatrix} \hat{d} \tag{3.16}$$

where G_I is the current gain, G_V the voltage gain, Z_{in} the input impedance and Z_{out} the output impedance. G_1 and G_2 represent voltage and current variations due to the variation of the duty cycle. Mapping Equation 3.15 to Equation 3.16, one finds

$$\left\{ \begin{aligned} G_I(s) &= \frac{1}{s^2 + \frac{D^2}{LC}} \frac{D}{LC} \\ G_V(s) &= \frac{1}{s^2 + \frac{D^2}{LC}} \frac{D(2D-1)}{LC} \\ Z_{in}^{-1}(s) &= \frac{1}{s^2 + \frac{D^2}{LC}} s \frac{2D-1}{L} \\ Z_{out}(s) &= \frac{1}{s^2 + \frac{D^2}{LC}} \frac{-s}{C} \\ G_{ID}(s) &= \frac{1}{s^2 + \frac{D^2}{LC}} \left(s - \frac{D^2 I_L}{C V_{in}} \right) \frac{V_{in}}{LD} \\ G_{VD}(s) &= \frac{1}{s^2 + \frac{D^2}{LC}} \left(s + \frac{V_{in}}{L I_L} \right) \frac{I_L}{C} \end{aligned} \right. \tag{3.17}$$

Though all of those parameters are important, $G_{VD}(s)$ will be of great interest for the design of the controller, as it is the transient output voltage gain for a variation of the duty cycle.

3.2 AC canonical model

Another important model of the converter is the canonical model, which can be found for any converter. The derivation of this canonical model follows the steps described in [20].

Stating from Equation 3.14, one can rewrite it as a system of three equations :

$$\begin{cases} L \frac{d\hat{i}_L}{dt} = \hat{d}(2V_{in} - V_{out}) + (2D - 1)\hat{v}_{in} - D\hat{v}_{out} \\ C \frac{d\hat{v}_{out}}{dt} = \hat{d}I_L + D\hat{i}_L + \hat{i}_o \\ \hat{i}_{in} = (2D - 1)\hat{i}_L + 2\hat{d}I_L. \end{cases} \quad (3.18)$$

These equations can be described in an equivalent circuit presented in Figure 3.1. Each equation corresponds to a part of the circuit, where the duty cycle D can be interpreted as a transformer ratio.

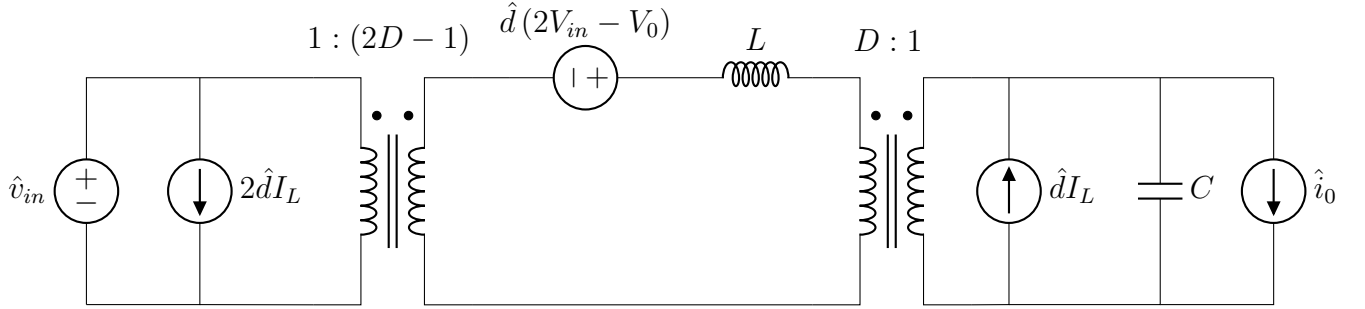


Figure 3.1: Equivalent AC model of Equation 3.18.

This model can be simplified in order to get the canonical form of the AC model: by moving the inductor to the other side of the transformer and having all voltage and current sources on the left side of the transformer, one finds the canonical model presented in Figure 3.2.

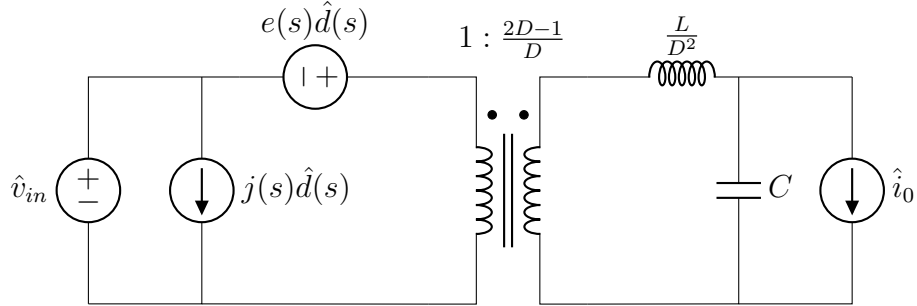


Figure 3.2: Canonical AC model of the Watkins-Johnson converter.

The values for the current source $j(s)$ and the voltage source $e(s)$ are given in Table 3.1.

Parameter	Value
$j(s)$	$\frac{I_0}{D^2}$
$e(s)$	$\frac{1}{(2D-1)^2} \cdot \left(V_0 + \frac{sLI_0(2D-1)}{D^2} \right)$

Table 3.1: Canonical model parameters.

3.3 Controller

All converters require to be controlled in order to reach the desired output. Whether the converter needs to be regulated to maintain a constant output voltage, output current, or to regulate their output to match a reference, controlling them is key to achieving the desired goal of the product.

In the case of the Direct-Drive architecture, the CRP supply must adapt its output voltage such that it suppresses the common mode current flowing through the thruster. The controller must therefore measure the common mode current by probing the current flowing in and out of the thruster. This current is then compared to the desired reference (in this case, the desired reference is 0 A, as the goal is to minimize it). The error is then integrated in a PI controller, which will set the duration of the Pulse Width Modulation (PWM) signal. The converter will then adapt to the change in duty cycle and produce a different output voltage. This feedback loop is represented in Figure 3.3, where e represent the error, $\hat{d}$ the variation of duty cycle, V_{CRP} the output voltage, i_{CM} the measured common mode current and $H(s)$ the gain of the sensor.

The implementation of the controller has not been done in practice for multiple reasons. First, doing such measurements (for probing the common mode current) would require a complex setup. Then, the design of the PI controller is out of the scope for this thesis.

For the experimental validation of the converter, basic, unregulated PWM signals will drive the converter. However, the analysis of the controllability of the WJC will be of interest for Thales Alenia Space in the case of further study of the converter, which goes beyond the scope of this thesis.

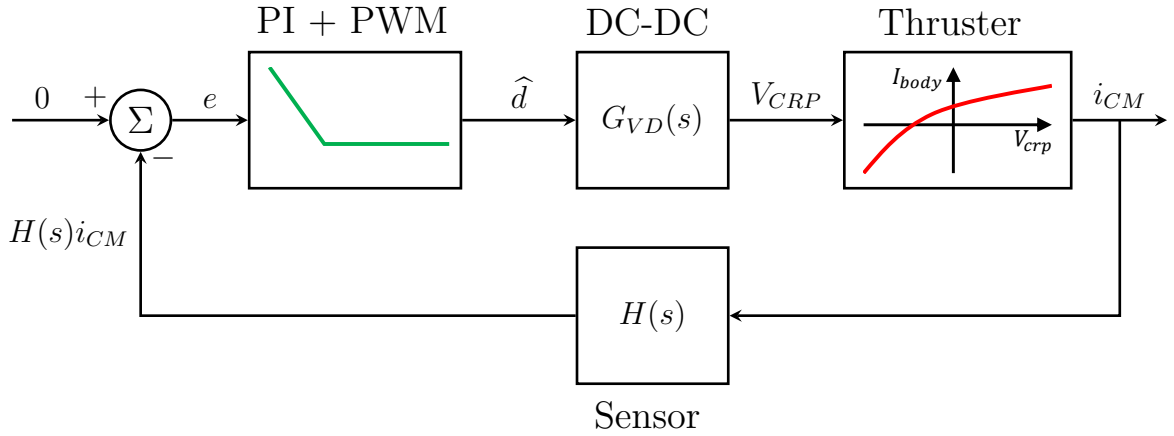


Figure 3.3: Control scheme for common mode current (i_{CM}) cancellation.

4 | Design requirements

Now that the topology has been found, the design of each components has to be done. In order to do so, the requirements have to be specified, since values of capacitors, inductors, MOSFET selection, etc. will be done accordingly.

Ideally, in the satellite, the input voltage of the converter would match the one of the battery, or of a low voltage bus connected to the battery, but different than the main 300 V power bus. This bus would have a nominal voltage of 100 V. The output would have to be large enough to make sure that it can cancel the common mode current, whatever the mode of operation of the satellite. From the measurements done by TAS and its partners shown in Figure 1.9, an output voltage varying between -20 V and 20 V is considered.

However, for safety reasons in the lab, I was not allowed to work with voltage sources that supplied more than 40 V. It has therefore been decided to use $V_{in} = 40$ V and an output voltage varying between -10 V and 10 V, such that the duty cycle remains close to what it would be expected in the satellite. The allowed ripple on the output voltage, ΔV_{out} should not exceed 0.1 V : a lower value of voltage ripple would be much smaller than all the voltage variation produced by the remaining of the PPU, while a much larger ripple would be too imprecise. Since this CRP voltage supply remains a proof of concept, having a ripple somewhat larger would still be acceptable.

The load current is purely inductive since it is the current feeding the thruster, and can vary from around 5 A to around 10 A. The ripple on the inductor should not exceed approximately 10 % of the average current at full load, so that it can be approximated as constant. The input current also has to be filtered in order to respect the current space standards for electromagnetic emissions. Finally, the switching frequency can be chosen: a large switching frequency will reduce the size of the components, but increase the switching losses, whereas a small switching frequency will do the opposite. It has been decided to operate the switches at $f_{sw} = 150$ kHz. Table 4.1 summarizes the requirements of the CRP voltage supply.

Parameter	Symbol	Value
Input voltage	V_{in}	40 V
Output voltage	V_{out}	$\in [-10 \text{ V}, 10 \text{ V}]$
Output current	i_o	10 A
Switching frequency	f_{sw}	150 kHz
Maximal allowed output voltage ripple	ΔV_{out}	0.1 V
Maximal allowed inductor current ripple	Δi_L	10 % of i_L at full load
Maximal allowed input current ripple	Δi_{in}	In accordance with ECSS-E-ST-20-07C [21]

Table 4.1: Requirements for the voltage supply.

5 | Design of the converter

Chapter 2 introduced the Watkins-Johnson converter and its principle of operation. This chapter will dig deeper into that topology, and design the inductor, output capacitors, input filter, etc. Finally, this chapter will show some simulations done with LTSpice to validate the design.

5.1 Inductor design

Given the requirements of Table 4.1, the design can start with the sizing of the inductor. The voltage drop across an inductor is given by

$$V_L = L \frac{di_L}{dt}. \quad (5.1)$$

The current ripple can be expressed as

$$\Delta i_L = \frac{1}{L} \int V_L dt. \quad (5.2)$$

In order for the inductor not to saturate, the average voltage across it over one period must be 0 V. This means that when S_1 and S_3 are conducting, V_L is positive and the current increases, and when S_2 and S_4 conduct, the voltage across the inductor is negative and the current decreases. Defining the ripple Δi_L as the maximum value above $\langle i_L \rangle$, the average current in the inductor, Equation 5.2 can be rewritten as

$$2\Delta i_L = \left| \frac{1}{L} \int_{DT}^T -V_{in} dt \right|. \quad (5.3)$$

The absolute value means that the sign is not important, what is important is the magnitude of the ripple. Therefore,

$$\Delta i_L = \frac{V_{in}(1-D)}{2Lf_{sw}}. \quad (5.4)$$

The average current in the inductor can be found with the ampere-second balance over one period on the capacitor. When S_1 and S_3 are ON, $i_C = i_L - i_o$, and when they are OFF, $i_C = -i_o$. Since the average current flowing through the capacitor is 0 A, it gives

$$\int_0^T i_C dt = \int_0^{DT} (i_L - i_o) dt + \int_{DT}^T -i_o dt = 0. \quad (5.5)$$

This simplifies as

$$\langle i_L \rangle = \frac{i_o}{D}, \quad (5.6)$$

where i_o is the load current. Using Equation 5.4 and Equation 5.6, the requirement $\Delta i_L \leq 0.1 < i_L >$ rewrites as

$$0.1 \frac{i_o}{D} \geq \frac{V_{in}(1-D)}{2Lf_{sw}}, \quad (5.7)$$

and the expression of the inductor is

$$L \geq \frac{D(1-D)V_{in}}{2 \cdot 0.1 i_o f_{sw}}. \quad (5.8)$$

The maximal value is obtained when $D = 0.5$ and gives $L \geq 33.3 \mu\text{H}$. Finally, in order to operate in CCM, the ripple must be smaller than the average current :

$$\Delta i_L \leq < i_L > = \frac{i_o}{D}. \quad (5.9)$$

Using the inductance value found with Equation 5.8, the minimal load current required to operate in CCM is

$$i_o \geq \frac{D(1-D)V_{in}}{2Lf_{sw}} = 1 \text{ A}, \quad (5.10)$$

whose minimum is found at $D = 0.5$.

5.2 Capacitor design

The design of the output capacitor can be done following the same approach as for the inductor, starting with the fundamental equations of the capacitor.

The current in a capacitor is given by

$$i_C = C \frac{dv_C}{dt}. \quad (5.11)$$

The voltage ripple can therefore be expressed as

$$\Delta v_C = \frac{1}{C} \int i_C dt. \quad (5.12)$$

For the average voltage to remain constant, the voltage ripple over one period must be 0 V, which means that the average current over one period in the capacitor is 0 A. When switches S_1 and S_3 are ON (during DT), the current on the capacitor is

$$i_C = i_L - i_o, \quad (5.13)$$

and when S_1 and S_3 are OFF (during $(1-D)T$),

$$i_C = -i_o. \quad (5.14)$$

Defining Δv_C as the maximum value above $< v_C >$ the average output voltage, Equation 5.12 can be rewritten as

$$2\Delta v_C = \left| \frac{1}{C} \int_{DT}^T -i_o dt \right|, \quad (5.15)$$

which gives

$$\Delta v_C = \frac{(1-D)i_o}{2Cf_{sw}}. \quad (5.16)$$

In order to match the requirements of Table 4.1,

$$\Delta v_C = \frac{(1-D)i_o}{2Cf_{sw}} \leq 0.1 \text{ V.} \quad (5.17)$$

The expression of the output capacitor is therefore

$$C \geq \frac{(1-D)i_o}{2 \cdot 0.1 f_{sw}}, \quad (5.18)$$

whose maximal value is found at the minimal duty cycle.

Recall that the transfer function of the WJC was given by

$$\frac{V_{out}}{V_{in}} = \frac{2D-1}{D}. \quad (5.19)$$

The expression of the duty cycle with respect to the output voltage is therefore

$$D = \frac{V_{in}}{2V_{in} - V_{out}}. \quad (5.20)$$

Important values of duty cycle are given in Table

$V_{out}[\text{V}]$	D
-10	0.44
0	0.5
10	0.57

Table 5.1: Output voltage vs duty cycle.

Finally, the minimal capacitor value can be computed and gives $C \geq 185 \mu\text{F}$.

5.3 Expected waveforms

As it was shown with the design of the inductor, the voltage across its terminals will rise during the conduction of S_1 and S_3 , and fall during the rest of the period. The expected inductor current and its ripple can therefore be computed with Equation 5.2. From $t = 0$ to $t = DT$,

$$i_L(t) = \frac{1}{L} \int_0^{DT} (V_{in} - V_{out}) dt, \quad (5.21)$$

and from DT to T , it is

$$i_L(t) = \frac{1}{L} \int_0^{DT} -V_{out} dt. \quad (5.22)$$

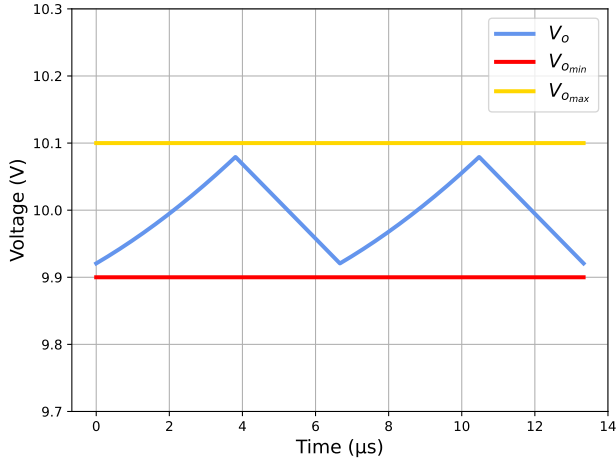
The voltage ripple can also be computed, thanks to Equation 5.16. From $t = 0$ to $t = DT$,

$$v_o(t) = \frac{1}{C} \int_0^{DT} (i_L(t) - i_o) dt, \quad (5.23)$$

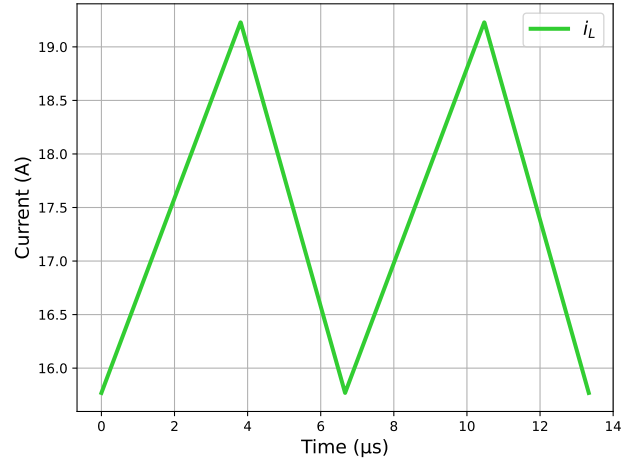
and from DT to T , it is

$$v_o(t) = \frac{1}{C} \int_0^{DT} -i_o dt. \quad (5.24)$$

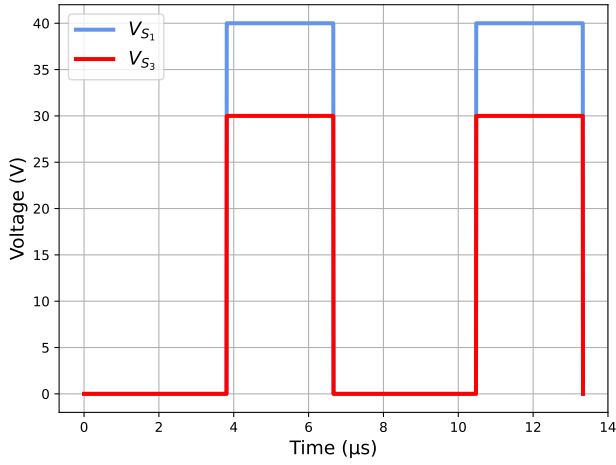
Those waveforms, along with the voltages and currents across the switches are shown in Figure 5.1 and Figure 5.2, for both the minimal duty cycle and the maximal duty cycle.



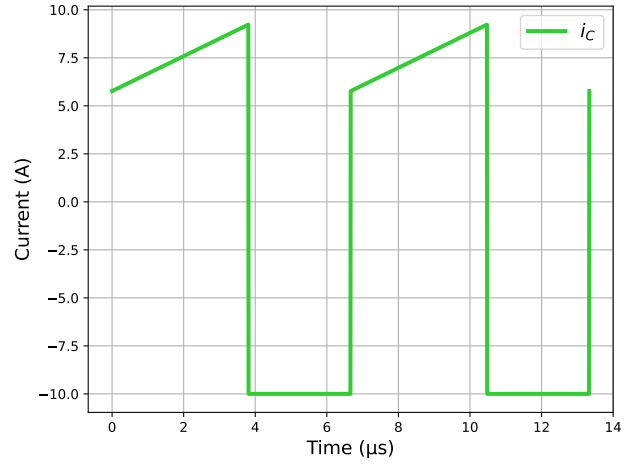
(a) Output voltage.



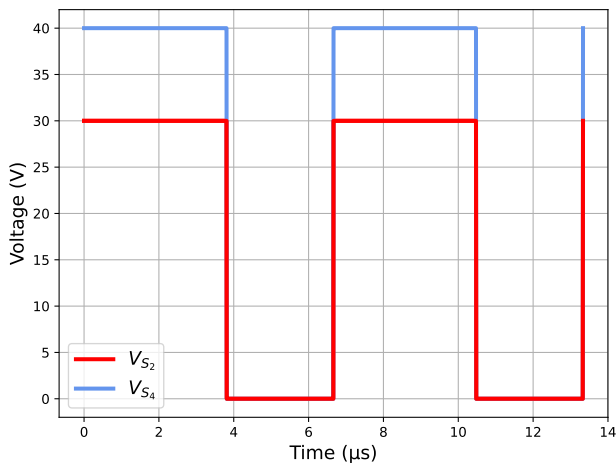
(b) Inductor current.



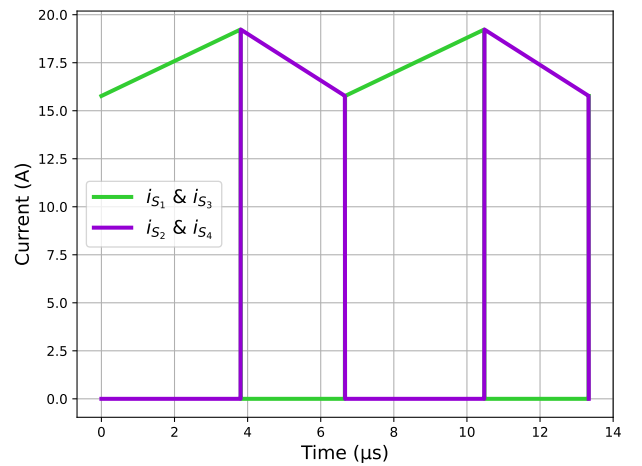
(c) Voltage across S_1 and S_3 .



(d) Capacitor current.

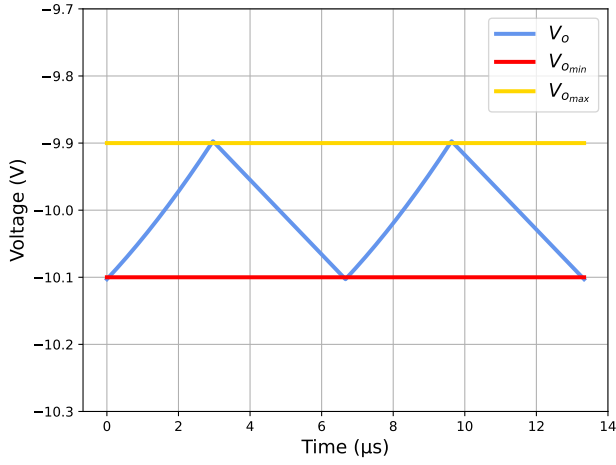


(e) Voltage across S_2 and S_4 .

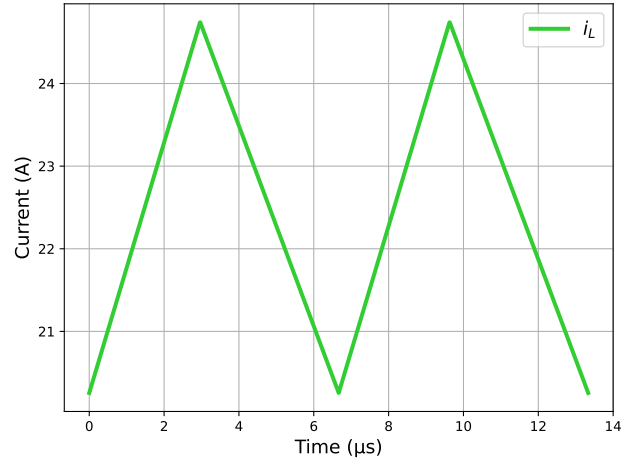


(f) Current through each switch.

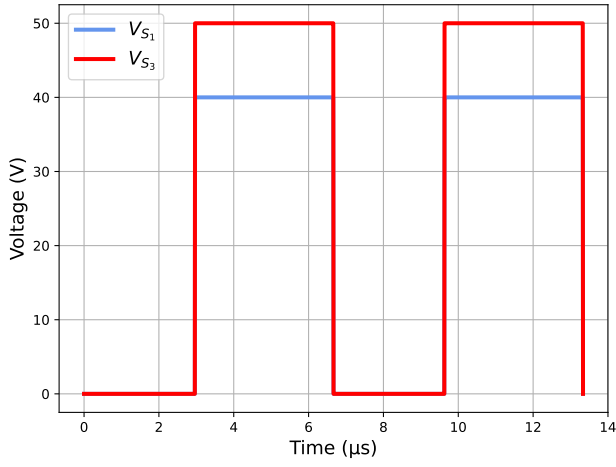
Figure 5.1: Expected waveforms for $D = D_{max}$.



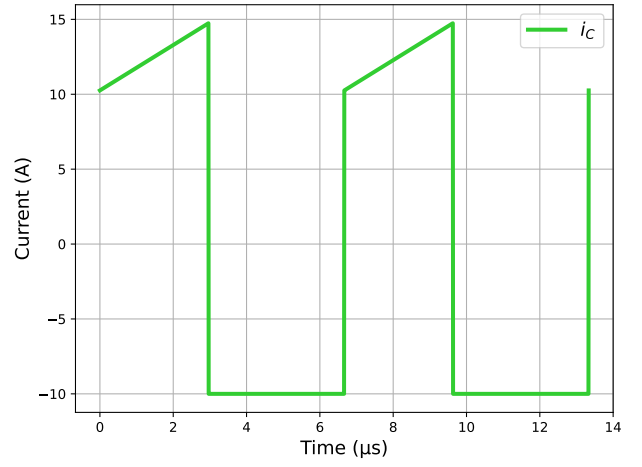
(a) Output voltage.



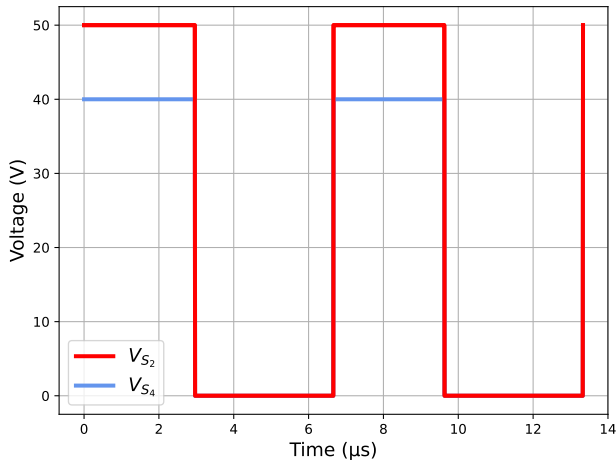
(b) Inductor current.



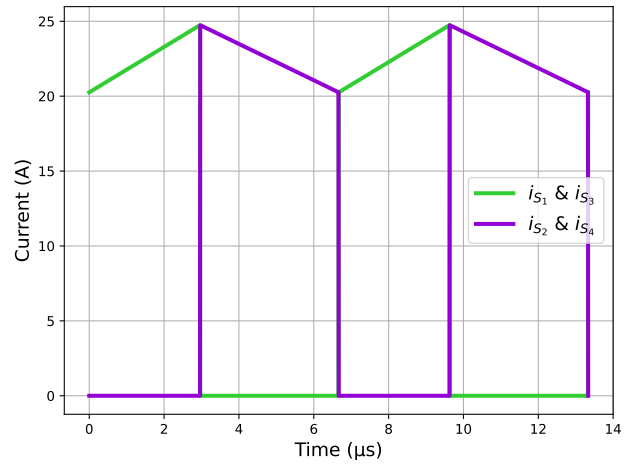
(c) Voltage across S_1 and S_3 .



(d) Capacitor current.



(e) Voltage across S_2 and S_4 .



(f) Current through each switch.

Figure 5.2: Expected waveforms for $D = D_{min}$.

5.4 Input filter

If the input current is not filtered, its waveform is shown in Figure 5.3.

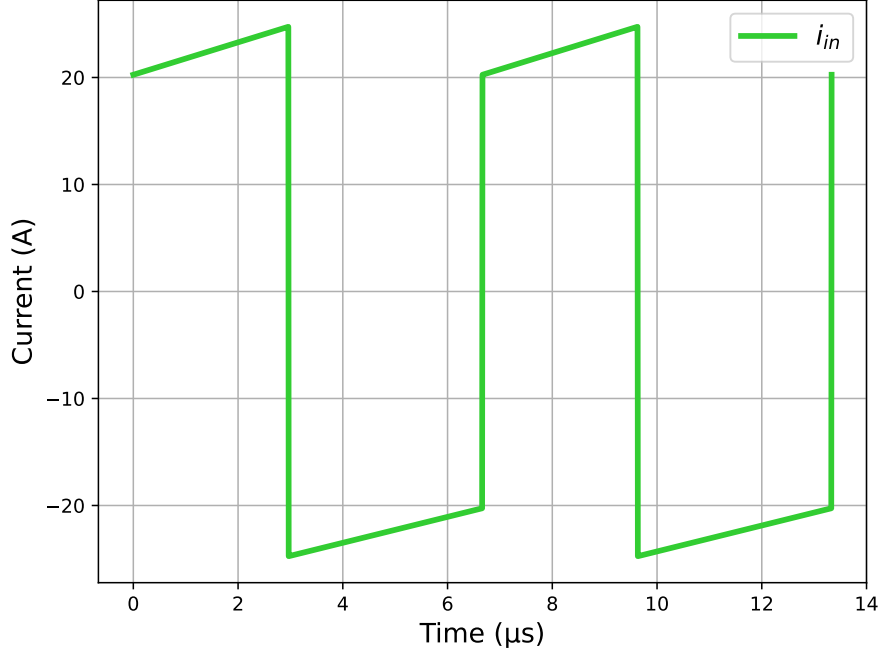


Figure 5.3: Input current without filter, for $D = 0.44$.

This waveform contains high frequency harmonics, predominantly at the switching frequency, and has an RMS value :

$$i_{in,RMS} = \sqrt{\frac{1}{T} \left(\int_0^{DT} i_L^2 dt + \int_{DT}^T (-i_L)^2 dt \right)} = i_L = \frac{i_{out}}{D} \quad (5.25)$$

where the assumption was made that i_L remains constant during one period. Its average value is given by

$$i_{in,avg} = \frac{2D - 1}{D} i_o. \quad (5.26)$$

However, space applications must follow very strict standards that are dictated by the European Cooperation for Space Standardization (ECSS). According to these standards [21], the conducted emissions induced by the load must remain below certain threshold depending on the frequency of the conducted emission. Figure 5.4 shows the current limit, which depends on the DC value at low frequencies. At the switching frequency of 150 kHz, that dependency disappears, and the current limit is roughly 75 dB μ A.

The RMS value of the input current at 150 kHz is largest at the minimal duty cycle, which was given in Table 5.1, $D = 0.44$. This gives

$$i_{in,RMS} = 22.5 \text{ A} = 147 \text{ dB } \mu\text{A}. \quad (5.27)$$

In order to fulfil the requirement of the ECSS, the filter must be designed such that it attenuates the current harmonic of 72 dB μ A. Common input filter for power supplies are LC filters, thus second order filters, that have a gain of -40 dB/dec . This means that the cut-off frequency of the filter must be 1.8 decades lower, around 2.3 kHz.

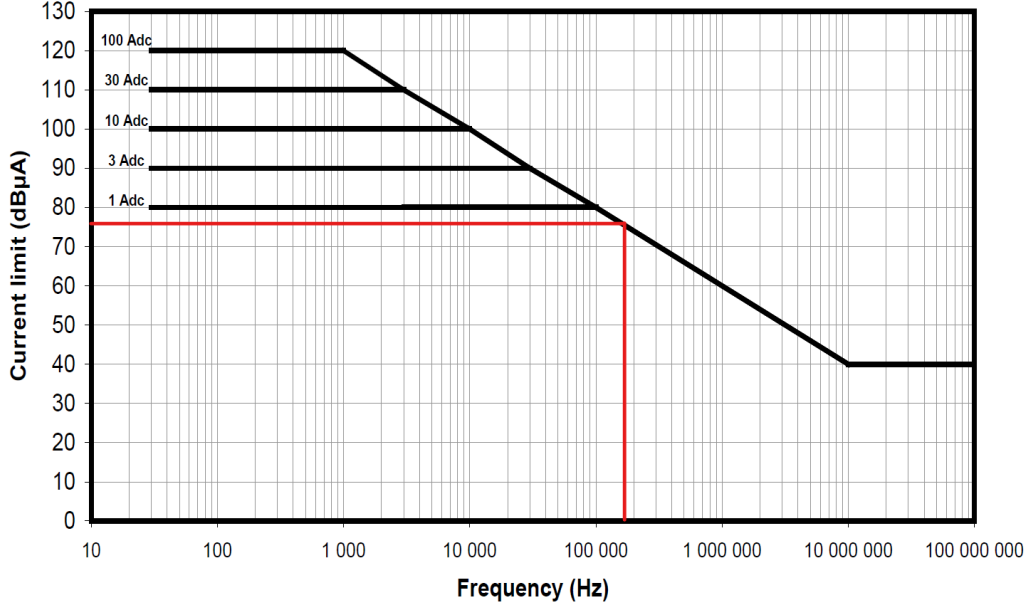


Figure 5.4: Conducted emissions on power leads [21].

For a second order filter, the cut-off frequency is given by

$$\omega_c = 2\pi f_c = \frac{1}{\sqrt{L_f C_f}}, \quad (5.28)$$

or

$$L_f C_f = \left(\frac{1}{2\pi f_c} \right)^2, \quad (5.29)$$

where L_f and C_f are the input filter inductance and capacitance.

5.4.1 Damping

The input filter being a LC circuit, it resonates at the cut-off frequency. In order to work properly, the filter has to be damped. Different ways of damping a filter are proposed in [22], such as series damped filter and parallel damped filter. The series damped filter consists of a resistor connected in series to an inductor, all connected in parallel to the filter inductor. It has the disadvantage of degrading the frequency response in high frequency, thus the attenuation of 40 dB / dec is no longer obtained. The parallel damped filter, has a damping resistance connected in series to a decoupling capacitor, all connected in parallel to the filter capacitance. This filter has the advantage of having no degradation in the high frequencies, and is also the most used. Figure 5.5 shows the parallel damped filter.

[22] shows that for optimal damping, the damping resistor

$$R_D = \sqrt{\frac{L_f}{C_f}} \quad (5.30)$$

and the damping capacitor $C_D = 4C_f$. However, for economical and space saving reasons, it is common to choose a damping capacitor

$$C_D = 3C_f, \quad (5.31)$$

while maintaining good performances [17].

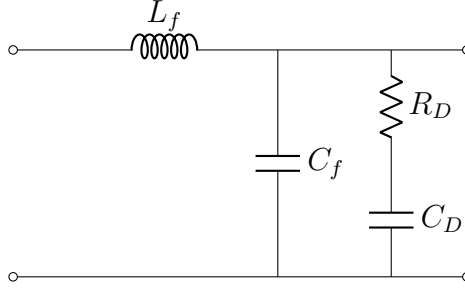


Figure 5.5: Parallel damped filter.

5.4.2 Sizing

The sizing of L_f , C_f and thus C_D and R_D remains to do. This can be done arbitrarily, as long as Equation 5.29 is respected. With the cut-off frequency $f_c = 2.3$ kHz, one finds

$$L_f C_f = 4.8 \times 10^{-9} \text{ s}^{-2}. \quad (5.32)$$

Since the the damping capacitor will consist of a much larger capacitor than C_f , it is preferable to choose C_f keeping in mind that C_D will require more space on the PCB.

It has finally been decided to choose $C_f = 80 \mu\text{F}$ and $L_f = 100 \mu\text{H}$. A summary of all components for the input filter is given in Table 5.2.

Symbol	Value
L_f	100 μH
C_f	80 μF
R_D	1 Ω
C_D	240 μF
f_c	1.8 kHz

Table 5.2: Components values for the input filter.

Finally, Figure 5.6 shows the frequency response of the filter, and a comparison for an undamped filter with the same values for L_f and C_f .

5.4.3 Effect of the filter on the stability of the converter

Frequently, when a converter is perfectly regulated, i.e. the output voltage is maintained constant and regulated, the input filter can cause stability issues for the controller [23]. Indeed, the addition of the filter can change the converter input or output impedance, and the line-to-output transfer function $G_V(s)$. Moreover, the impact of the input filter on the control-to-output transfer function $G_{VD}(s)$ is important as the duty cycle of the converter is controlled.

However, in the case of the CRP supply, the output is not regulated to maintain constant voltage nor constant power. This limits the instability caused by the input filter. Furthermore, as explained in Chapter 3, the scope of this document is not to design a controller for

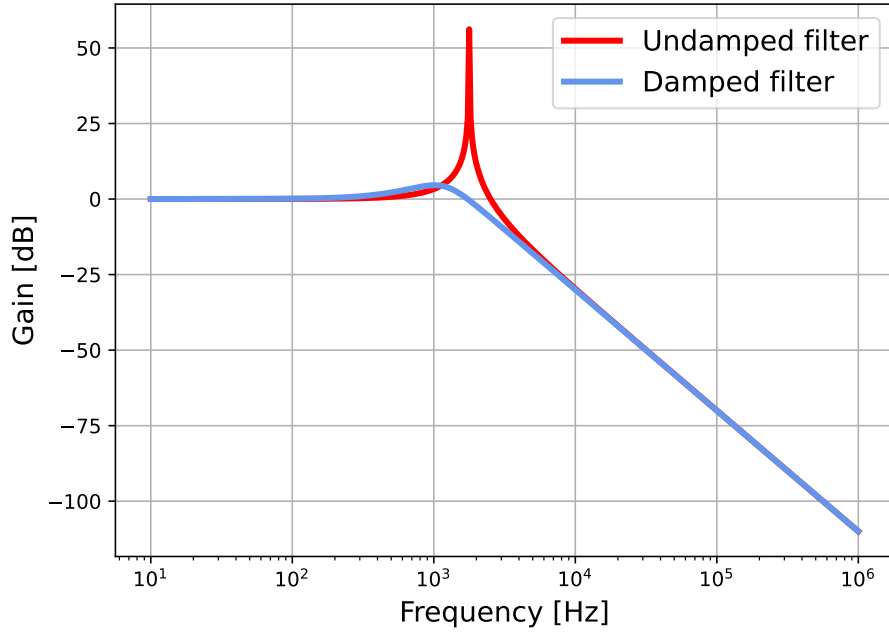


Figure 5.6: Frequency response of the damped and undamped filters.

the WJC but to show the possibility to use it as CRP supply in the PPU. Again, stability issues will have to be investigated by TAS for further use of the WJC.

5.5 Review of power electronic switches and active components selection

Now that the passive components (capacitor, inductor, filter) have been designed, there remains one set of key components to design and choose : the switches and their driving sub-circuits. This section will first review key concepts about power electronic switches. Then, a selection of switches will be done for the set-up realization.

Switches can be split in two categories: active switches and passive switches. An active switch is typically a transistor and is often controlled with a high frequency PWM control signal. The most commonly used transistors are MOSFET, BJT and IGBT. A passive switch, however, has no control signal and turns ON or OFF passively. The typical passive switch is the diode.

5.5.1 Power diode

A power diode, or a diode, is used as a passive switch to block current when a negative voltage is applied to its terminal, and conducts otherwise. Commonly, a diode is made of a p-type semiconductor associated to a n-type semiconductor : a PN junction.

The current in the diode can only flow in one direction, from the anode to the cathode. In the ideal case, the diode conducts when the voltage across its terminals is zero, and

thus has no power loss. In practice, a diode will conduct if the voltage is greater than the forward voltage (V_F), usually around 1 V to 2.5 V, and has an additional resistive loss when it conducts [24]. The voltage drop across the diode is given by

$$V_{D,on} = V_F + R_{D,on}I_{on} \quad (5.33)$$

and the conduction loss is given by

$$P_{cond} = V_{D,on}I_{on} = V_F I_{on} + R_{D,on}I_{on}^2 \quad (5.34)$$

A diode also contributes to additional losses when switching. Indeed, by the nature of the PN junction, when the diode is forward biased, charges are stored at the junction of the two doped semiconductors. At the time the diode is reverse biased, these stored charges have to be removed from the junction. A current will therefore flow in the diode in the opposite direction, called reverse current (i_{RR}). During this short transition, the reverse recovery current multiplied by the voltage across the diode creates additional losses. The reverse recovery current i_{RR} is proportional to the charges stored at the junction Q_{RR} , and the time required to remove them (t_{RR}). Unfortunately, the reverse recovery loss is difficult to estimate, as the reverse recovery charge is often given for a specific point of operation, which does not necessarily reflect the point of operation of the diode in the converter.

Finally, this reverse recovery current can be mitigated by the usage of a different type of diode : the Schottky diode [25]. This diode is not a PN junction, but a metal-semiconductor junction. The nature of this junction has advantages and drawbacks. The Schottky diode usually has a lower forward voltage V_F , stores almost no charges at its junction thus has really low reverse recovery current, and allows for very fast switching. However, it also has a larger reverse leakage current (i.e. the leakage current flowing when the diode is reverse biased), and smaller blocking voltage capability.

5.5.2 Power MOSFET

Different types of transistors can be used as switches, but n-type MOSFET are the most widely used transistors for low voltage and high switching frequency application [26]. An active switch can be either ON, ideally conducting current in both directions, or OFF, ideally blocking current in both directions. Because of the structure of the MOSFET, a superposition of p-type and n-type semiconductors causes an intrinsic body diode. Therefore when the n-type MOSFET is OFF, it can only block current if the voltage across its terminals (V_{ds}) is positive. Otherwise, the intrinsic body diode will be forward biased and the current will flow through. Ideally, in the ON state, the MOSFET has no conduction loss. In practice, the transistor acts as a resistor, and the conduction loss is given by

$$P_{cond} = R_{DS,on}I_{D,on}^2, \quad (5.35)$$

with $R_{DS,on}$ the ON state drain-source resistance and $I_{D,on}$ the drain current.

In order to switch the transistor ON and OFF, a control signal has to be applied on the gate of the transistor. For power MOSFET, the typical gate-source voltage (V_{gs}) that must be applied is in the range of 10 V to 20 V. When turning a MOSFET on and off, the voltage and current do not change instantaneously. This causes additional losses known as switching losses. During a turn-on (resp. turn-off) transient, the drain-source voltage (V_{ds}) is high, and

the current start rising (resp. falling). When the current (resp. voltage) has risen, voltage (resp. current) starts falling and the transistor is turned ON (resp. turned OFF). Figure 5.7 depicts this transient, and the associated power loss. Additionally, the output capacitance of the MOSFET is being charged (resp. discharged) during each transient, creating additional capacitance losses [27].

The total switching loss is given by:

$$P_{sw} = f_{sw} \left(\int_0^{t_{on}} V_{ds} I_d dt + \int_0^{t_{off}} V_{ds} I_d dt \right) = f_{sw} \left((t_{on} + t_{off}) \frac{V_{ds} I_D}{2} + \frac{C_{oss} V_{ds}^2}{2} \right), \quad (5.36)$$

where f_{sw} is the switching frequency, C_{oss} the output parasitic capacitance and the drain current $I_d = I_D + C_{oss} \frac{dV_{ds}}{dt}$.

Typical values of C_{oss} are in the range of few hundreds of pF to a few nF, which makes the capacitance loss negligible when the MOSFET operates at full load.

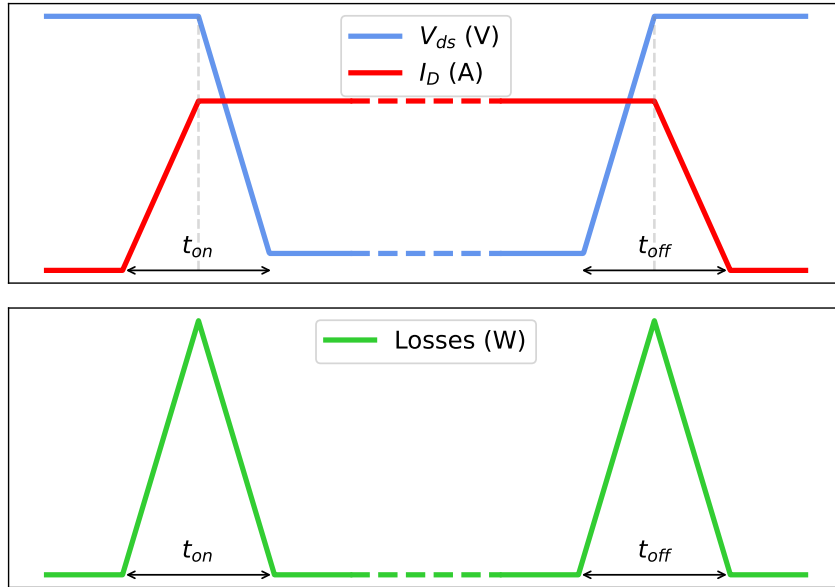


Figure 5.7: MOSFET switching loss.

5.5.3 Active switches selection

Key behaviours and their associated losses have been presented in the previous section. The choice of components can now be done accordingly. The selection of MOSFET and diodes is very important, as they must have a sufficient blocking voltage capability in order to block the voltage in the OFF state, but also the lowest possible ON resistance such that the conduction loss is minimized. For the diode, the forward voltage V_F must also be as small as possible, and for the MOSFET, the parasitic capacitances must be minimized as well, in order to minimize the switching loss.

The components that have been selected are the diode STTH2002 from STMicroelectronics [28] and the MOSFET IPP041N12N3 from Infineon Technologies [29], whose simplified data sheet can be found in Table 5.3 and Table 5.4.

Parameter	Symbol	Value
Maximal blocking voltage	V_{RRM}	200 V
Forward voltage	V_F	0.75 V
Maximal average forward current	I_F	20 A
ON state resistance	R_{on}	10 m Ω

Table 5.3: Simplified data sheet of STTH2002.

Parameter	Symbol	Value
Maximal drain-source voltage	V_{DS}	120 V
Drain-source resistance	$R_{DS,on}$	3.8 m Ω
Maximal drain current	I_D	120 A
Approximated ON time at $I_D = 20$ A	t_{on}	20 ns
Approximated OFF time at $I_D = 20$ A	t_{off}	20 ns

Table 5.4: Simplified data sheet of IPP041N12N3.

A quick estimate of the power loss can be done using Equations 5.34, 5.35, 5.36 and Table 5.3 and Table 5.4. The power loss for the diode is given by

$$P_{diode} = V_F I_{avg} + R_{D,on} I_{RMS}^2 \quad (5.37)$$

and for the MOSFET by

$$P_{MOSFET} = R_{DS,on} I_{RMS}^2 + f_{sw} (t_{on} + t_{off}) \frac{V_{ds} I_D}{2} \quad (5.38)$$

Table 5.5 gives an estimate of those losses for the minimal duty cycle for switch S_4 . The losses might be under-estimated since in reality, lots of complex mechanism happen in such semiconductors. However, it gives a first good approximation and will help selecting the technology for the converter.

Component	Conduction loss [W]	Switching loss [W]	Total loss [W]
MOSFET	1.08	2.7	3.78
Diode	11.04	-	11.04

Table 5.5: Approximate estimation of the losses in a diode and a MOSFET for switch S_4 .

From this table, it seems that using a MOSFET as a switch instead of a diode will clearly decrease the total loss of the converter. This can be done at the expense of a more complicated driving scheme and will require more space on the PCB. Requiring four driving units will obviously take more space than if only two were required. Then, the problem of driving each MOSFET and avoiding cross conduction of S_1 and S_4 , and S_2 and S_3 will have to be managed, in order not to destroy the components. It has anyway been decided to use only MOSFET, as it should increase the efficiency of the converter.

5.5.4 Gate driver design

Upon applying gate-source voltage to the gate, the gate voltage does not rise to its final value instantaneously and a delay is occurring between the gate-source voltage increase and the drain current and drain-source voltage changes. Understanding what happens when a switch must turn-on or turn-off is important, in order to avoid cross conduction of two switches, which would cause huge power loss.

Indeed, the MOSFET has parasitic capacitances which have to be charged in order for the gate voltage to rise. Furthermore, it also has an intrinsic gate resistance and an external gate resistance is added in the design of the driver in order to avoid over-currents on the gate. The typical MOSFET, with its simplified driving circuit during a switching transient on an inductive load is shown in Figure 5.8. In this circuit, V_{gg} is the command voltage, assumed to be instantaneous, R_g the gate resistance, C_{gd} and C_{gs} the gate-drain and gate-source capacitances. The diode and the current source i_L represent the body diode of the second MOSFET of the branch, and the current flowing through the inductor.

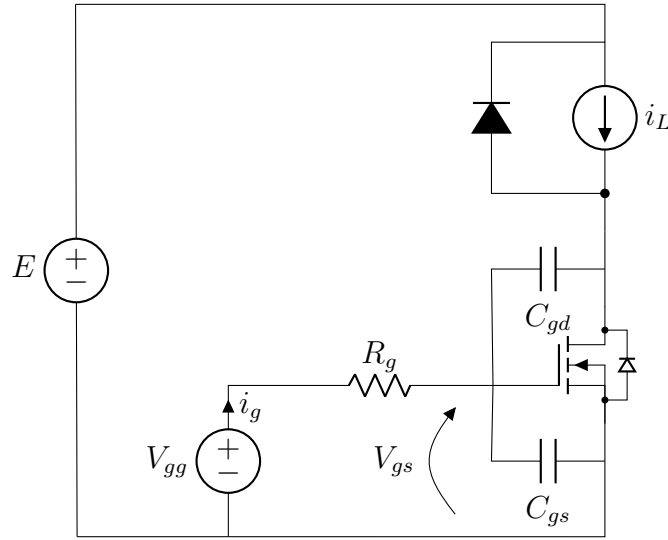


Figure 5.8: Driving circuit of a MOSFET.

The turn-on transient of the switch will be analysed. Figure 5.9 shows the turn-on and turn-off transients of the MOSFET.

- At t_0 , V_{gg} rises instantaneously, the gate voltage V_{gs} starts rising as the capacitances charges. Until V_{gs} reaches the threshold voltage V_{th} , the switch remains OFF and the current i_L flows through the free wheeling diode. The diode is forward biased and the voltage across its terminals is 0 V.
- When $V_{gs} \geq V_{th}$, at time t_1 , the transistor turns-on and current starts flowing. At this point, V_{gs} continues to rise, and the diode still conducts part of the current because the MOSFET is not able to conduct the current entirely yet. The diode remains forward biased.
- When V_{gs} has increased further to a value called $V_{plateau}$, all the current is flowing through the MOSFET (t_2). The diode does not conduct and becomes reverse biased. The voltage across the transistor can start falling, as until that point it was maintained to the value E because of the forward biased diode. Since the current already flows

through the MOSFET, its gate source voltage cannot increase further. During this time interval, the gain of the transistor ($\frac{V_{ds}}{V_{gs}}$) is infinite because V_{ds} changes though V_{gs} remains constant, and C_{gd} is infinite as seen from the gate due to Miller effect [26] [30]. Therefore, all the gate current flows to C_{gd} .

- Finally, at t_3 , the drain-source voltage has reached 0 V, Miller effect stops occurring, and V_{gs} continues to rise by charging C_{gd} and C_{gs} , until it reaches its final value V_{gg} .

At turn-off, the same behaviour occurs in a reverse sequence.

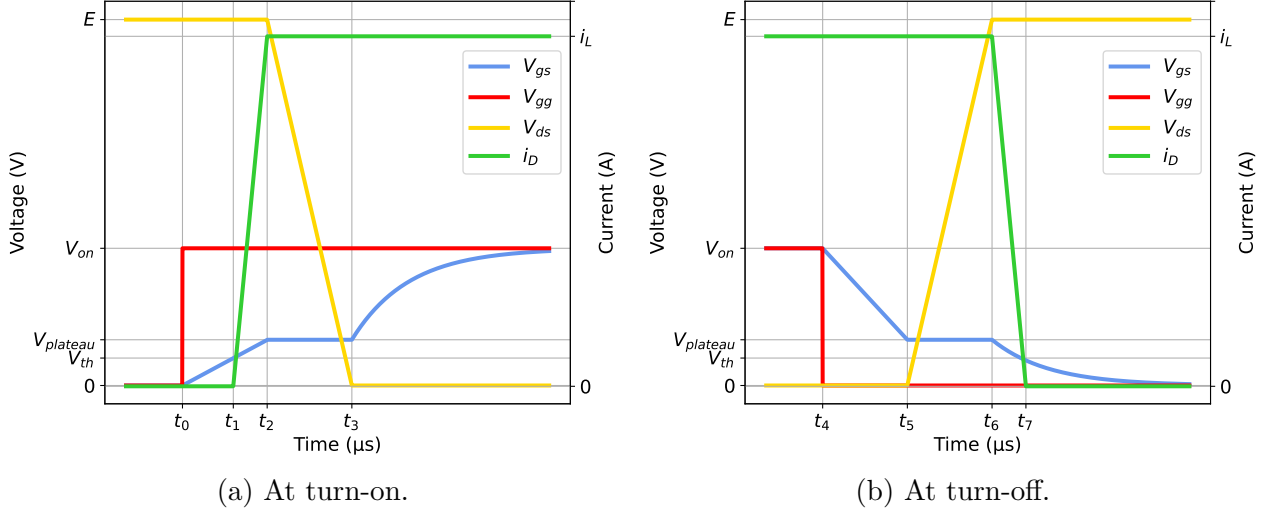


Figure 5.9: MOSFET switching transient.

These transient phenomenon slow-down the turn-on and turn-off processes of the MOSFET. In order to avoid cross-conduction of two MOSFET, a dead-time (i.e. a blanking time where the two switches are OFF) will have to be introduced in the PWM signals. Indeed, as the PWM signals change values, the MOSFET turning-on will conduct current before V_{gs} reaches $V_{plateau}$. But the MOSFET turning-off will first have its drain-source voltage rise, and go through the Miller plateau before the current stops flowing through the drain. The two transistors could therefore conduct current at the same time, create a short-circuit and cause large power loss.

Gate driver

In order to reach faster turn-on and turn-off times, and to mitigate the Miller plateau, the design of the gate driving unit is crucial.

First, as explained previously, in order to turn-on, the gate-source voltage V_{gs} must reach a value that, for power switches, is recommended to be between 10 V and 20 V. However, in the Watkins-Johnson converter's topology, not all switches have their source connected to the ground. In fact, only switch S_4 has its source grounded. As the other switches have a different source voltage, which can eventually vary, supplying a gate source voltage of a specific value is more complex. It is done by supplying a DC floating voltage, which is in practice delivered by a very small, low power, integrated flyback converter. The flyback converter provides galvanic isolation while performing DC/DC conversion. Finally, it has been decided to work with a 5 V/15 V converter, thus supplying 15 V to the MOSFET's gate. This flyback, as well as all the other driving components require a 5 V input supply. This

means that for the measurements, one auxiliary power supply will be needed to drive all the components.

Then, an Integrated Circuit (IC) supplies this floating voltage based on a low voltage PWM signal. The PWM signal is a 5 V logic signal. For this application, the IC is Infineon's 2EDF7275F [31]. This IC has an output current limit of 4 A when sourcing (at turn-on), and of 8 A when sinking (at turn-off). This difference in current limitation allows for faster turn-off time, since gate charges are removed more quickly. In order to remain below the gate driver limits, it has been decided to use a 5 Ω gate resistor, such that the sourced peak current is

$$I_{gate} = \frac{V_{gg}}{R_G} = 3 \text{ A.} \quad (5.39)$$

In order to sink a higher current, a second 5 Ω gate resistor in series with a diode is added in parallel to the first gate resistor. Doing so, when current is flowing from the gate to the IC (at turn-off), the diode is forward biased. Neglecting the low forward voltage drop of the diode, the two gates resistors are seen in parallel and twice as much current can be sunk. Lastly, the value of the gate resistors, and thus the speed at which gate charges are removed, may have an impact on the transients of the circuit. Indeed, the faster the gate voltage increases, the faster the current will flow through the drain. Such a fast change in current, coupled with the parasitic inductance of the circuit and the components, can create voltage oscillations as $V = L \frac{di}{dt}$. Choosing the right gate resistor is thus a compromise between faster switching transient, and large voltage oscillations.

Finally, one last improvement can be done in order to improve the switching speed and be more robust against the oscillations. Instead of supplying a gate voltage of 0 V or 15 V, the gate source voltage at turn-off can be negative. Since the gate driver's voltage is floating, this is easily achievable by means of a reverse biased Zener diode.

A Zener diode is a diode that is reverse biased and that has a precise breakdown voltage for a Zener current. This means that for a given current flowing from the cathode to the anode (reverse current), the diode enters in breakdown, meaning that it produces a voltage drop in the opposite direction than the usual forward voltage drop. The Zener current is fixed though a resistor placed in series with the Zener diode. For this converter. It has been decided to use a 3.5 V Zener diode, which requires about 10 mA to operate. The Zener resistor is found with

$$R_{zener} = \frac{V_{supply} - V_{zener}}{I_{zener}} = \frac{15 - 3.5}{0.01} = 1.5 \text{ k}\Omega \quad (5.40)$$

Finally, small capacitors are placed in parallel with the resistor and the diode, to smooth the voltage and feed the instantaneous current. The gate voltage at turn-on is therefore $V_H = 11.5 \text{ V}$ and at turn-off $V_L = -3.5 \text{ V}$.

A full schematic representing the gate driver, including the galvanic isolation, the two gate resistors and the Zener diode is shown in Figure 5.10.

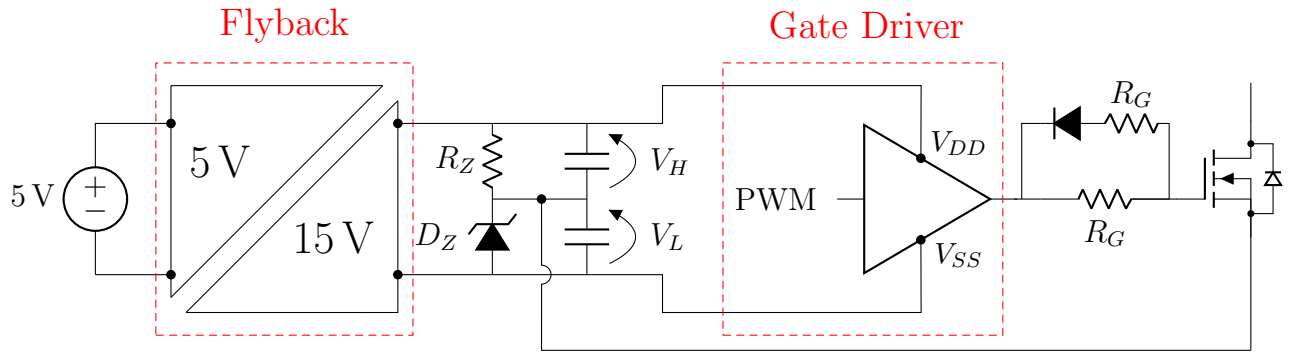


Figure 5.10: Driving unit design.

Finally, the gate-source voltages of the four cases have been simulated during a turn-off transient at full load and are shown in Figure 5.11. The first scenario, "basic design", is the design in which no parallel gate resistors are used, nor the Zener diode. The second scenario does not use the Zener diode, but has the two parallel gate resistors. In the third case, the Zener diode is used to have a negative V_{gs} but the parallel gate resistor is not present. The last scenario includes the complete design described above, with parallel gate resistors and the use of a Zener diode.

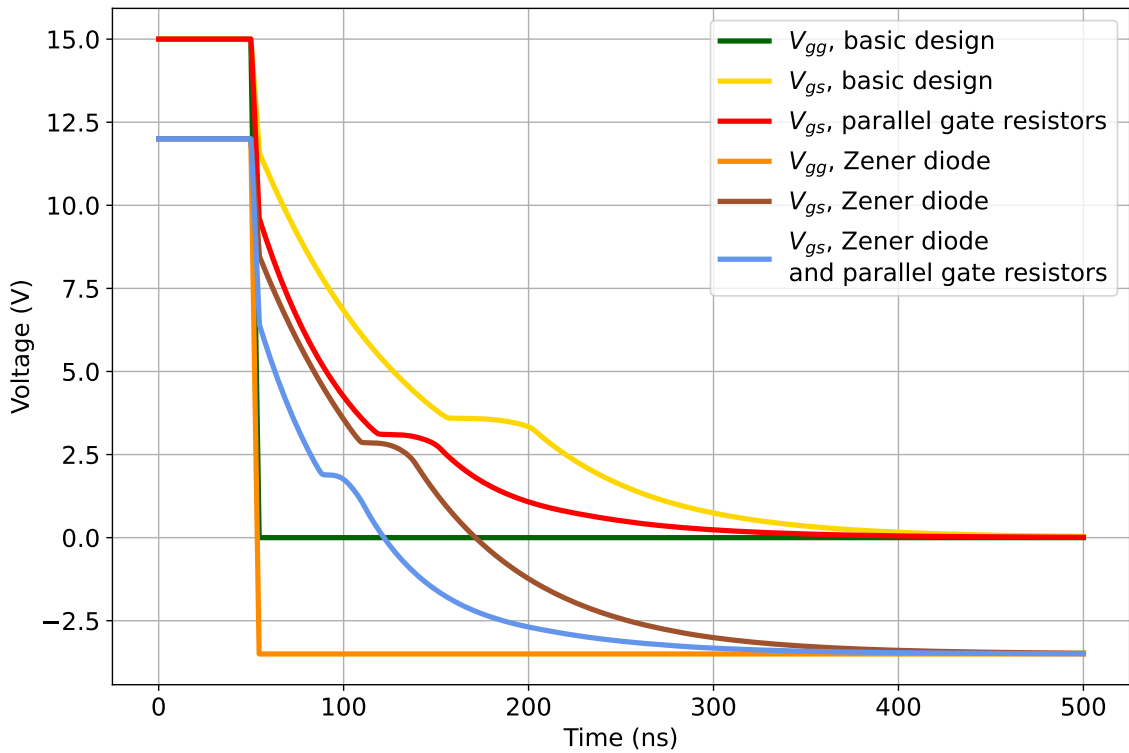


Figure 5.11: Simulated gate-source voltage (V_{gs}) and V_{gg} during turn-off transient for four gate driver designs.

One can see that the most basic scenario is the one that requires the longest time to turn-off the MOSFET, while the design of the gate driver with all the improvements allows for the fastest turn-off time among the different scenario. Furthermore, it also allows to be more robust against voltage oscillations, because if the voltage were to increase slightly, the gate voltage would remain below the threshold voltage, thus avoiding to turn-on the MOSFET because of parasitic oscillations.

5.6 Thermal management

The losses in the semiconductors and those due to the parasitic resistances of the components are inevitable, and the power that dissipates in the components creates heat. The electrical power dissipated in the components has to be extracted in order to keep the component working. Dissipated power can be related to a temperature rise through :

$$\Delta T = R_{th}P, \quad (5.41)$$

where R_{th} is the thermal resistance, in K W^{-1} and ΔT the temperature change. This is the thermal analogy to Ohm's law. In order to decrease the temperature rise inside a component, the thermal resistance has to be decreased, using heat sinks for example. Also, the more power is dissipated, the harder it gets to cool down components, because of the fixed thermal resistances of the heat sink, the packaging, etc. Minimizing the power loss is thus essential.

For low power converters such as this CRP supply, cooling down components using heat sinks thanks to the natural convection of the air works well enough, though for more dissipative converters, the use of fans or even heat pipes is sometimes necessary. Moreover, as the CRP supply is a prototype rather than a product designed to operate in space, the use of heat sinks is acceptable. In space however, it would not be possible to use natural convection since the medium is vacuum. Therefore, this thermal analysis is only valid for the prototype designed in this thesis, and would have to be reconsidered if the CRP supply were to operate in vacuum.

The thermal resistance of the MOSFET package is $R_{th,jc} = 0.5 \text{ K W}^{-1}$, and that of the selected heat sink is $R_{th,hs} = 2.6 \text{ K W}^{-1}$. In the end, the junction temperature of the components should remain at acceptable values.

5.7 LTSpice validation

Finally, simulations have been performed with LTSpice in order to validate the design. Those simulations have been done using all the components designed in this chapter, also including the gate driver and the input filter. For the load, a constant current source was used to simulate the 10 A load. The schematic of the LTSpice simulation is shown in Figure 5.12.

As mentioned previously, a dead-time had to be introduced in the control signals of the gates to ensure that no cross-conduction was happening. The choice of this duration is a trade-off between a large security margin and better performances. For this design, the chosen dead-time was $t_{dead} = 180 \text{ ns}$. The introduction of this dead-time leads to two consequences : a change in the transfer function and increasing power losses. Indeed, as none of the MOSFET are conducting for a certain time, the current flows through the forward biased body diode. This causes conduction loss as those diodes usually have relatively large threshold voltage, and increased switching loss due to the high amount of reverse recovery charges. In addition to that, since the body diode of two MOSFET continues to conduct current although the MOSFET is OFF, it slightly changes the output voltage value for a given duty cycle.

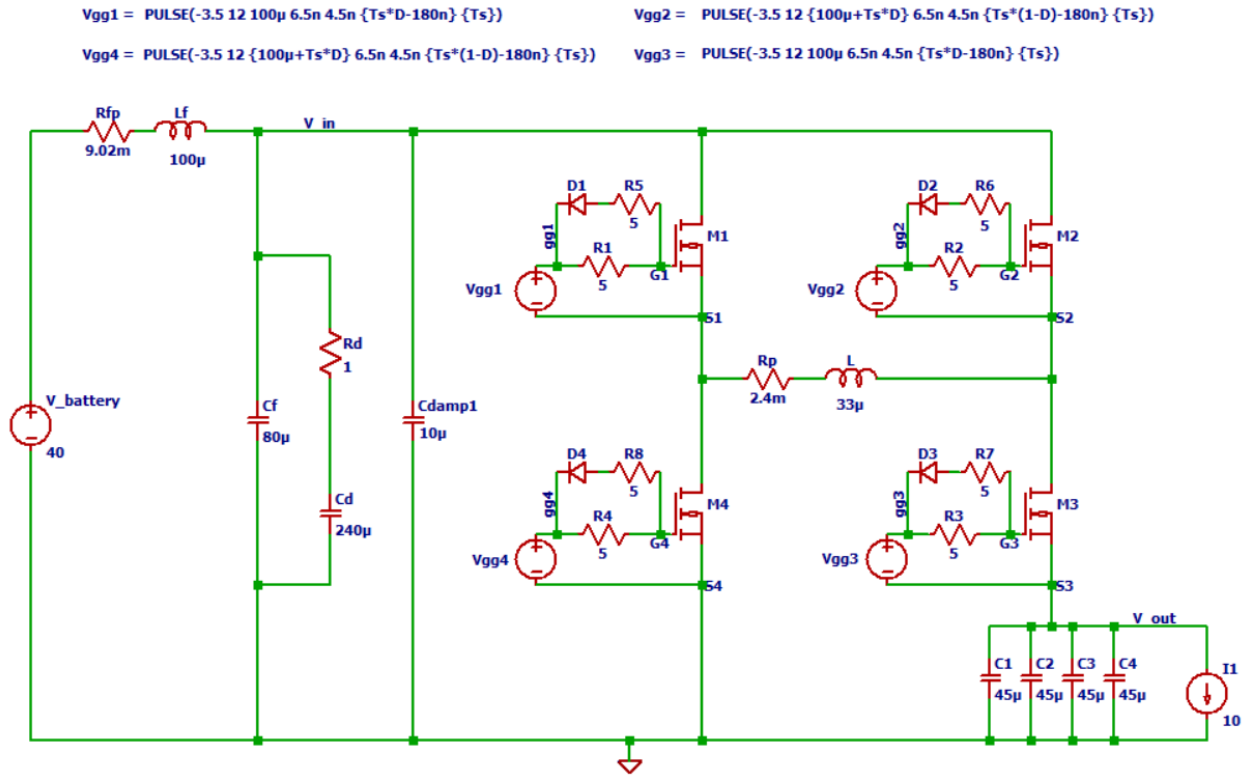


Figure 5.12: LTSpice schematic of the WJC.

Figure 5.13 shows the gate source voltages of the switches S_1 and S_4 at $D = 0.48$. The input voltage of the converter V_{in} (i.e. the drain voltage of S_1 and S_2 , or the voltage at the output of the input filter) and the voltage at the output of the converter V_{out} are shown in Figure 5.14, for duty cycles $D = 0.48$ and $D = 0.6$, allowing to reach $V_{out} = -10 \text{ V}$ and $V_{out} = 10 \text{ V}$.

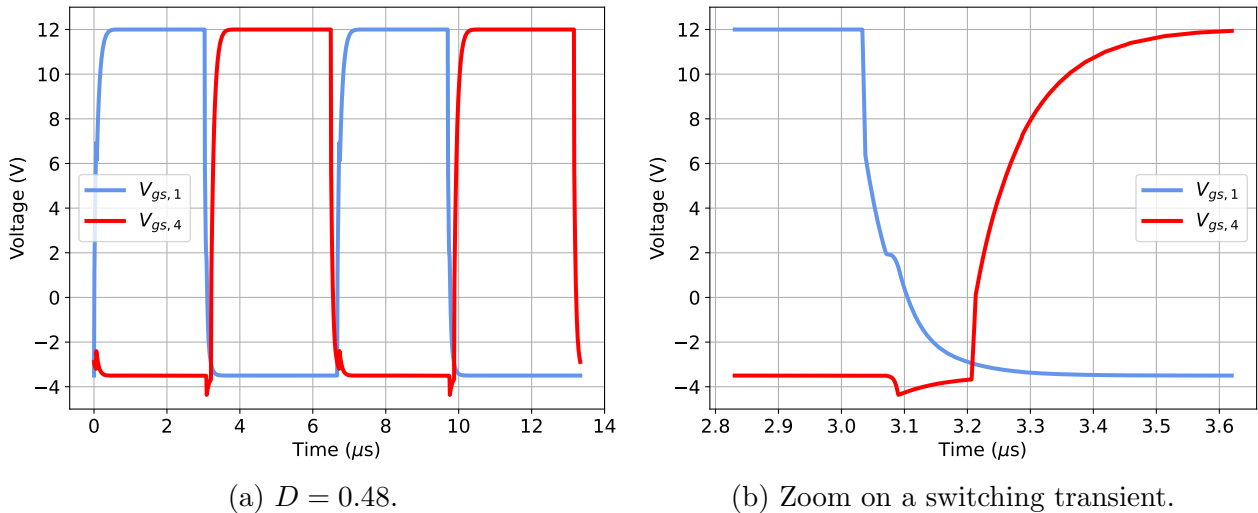


Figure 5.13: Gate-source voltage of S_1 and S_4 .

From these simulations, one can see that the converter seems to function properly. In the next chapters, the practical implementation of the converter as well as lab measurements will be detailed.

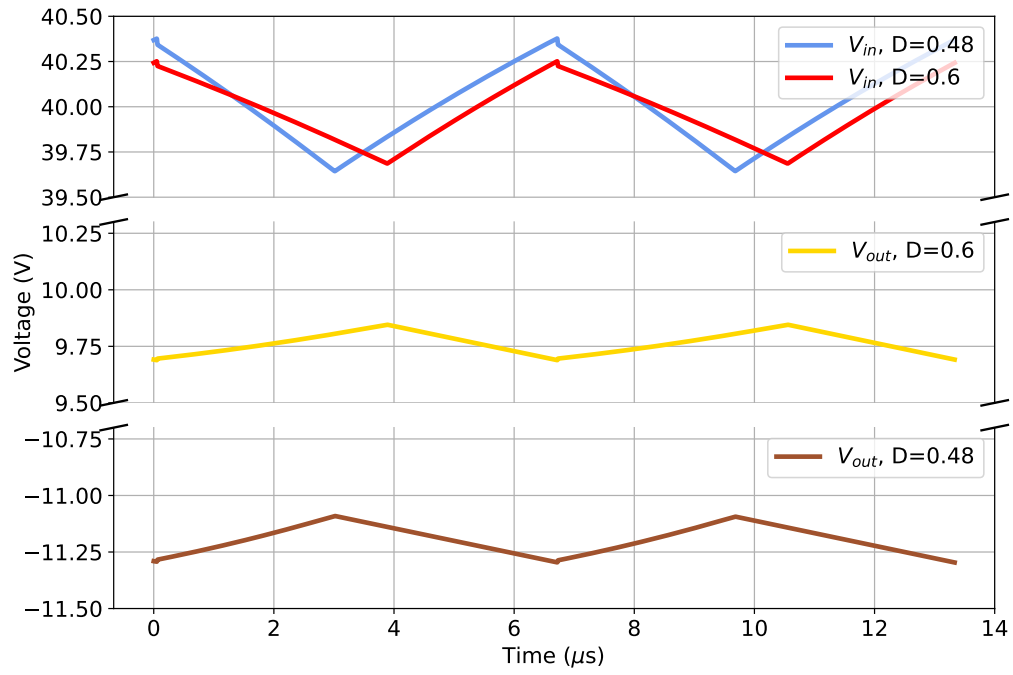


Figure 5.14: Input voltage V_{in} (drain voltage of S_1 and S_2) and output voltage of the converter (V_{out}) at $D = 0.48$ and $D = 0.6$.

6 | Practical implementation

In order to perform measurements, the circuit has to be implemented in practice. Going from theoretical design to real measurements can be quite complex, as *"in theory there is no difference between theory and practice, while in practice there is"*.

This chapter will first go through the schematic design and the PCB layout. Then, the practical implementation of the gate driver will be explained. A well designed gate driving unit allows for faster turn-on and turn-off transient, therefore minimizing switching losses.

6.1 Schematic

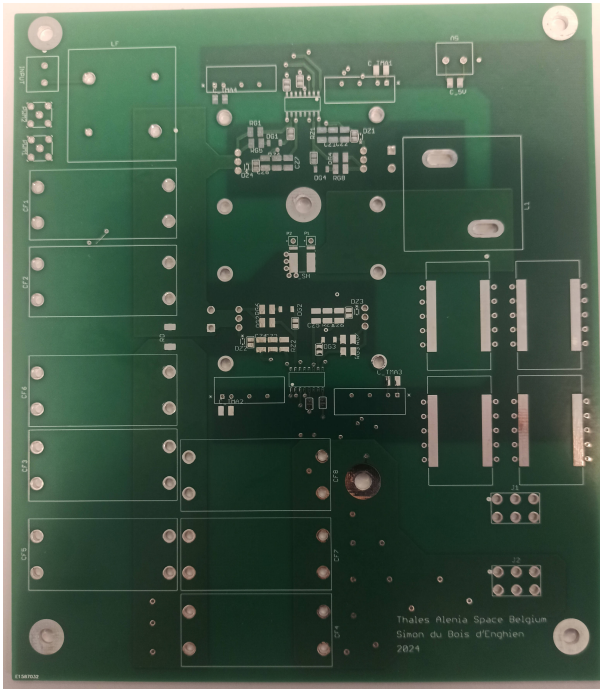
In order to perform real measurements and to validate the design, the WJC has to be crafted. The design of the PCB was done using Autodesk Eagle. First, a schematic was created, where all the components were placed and connections were made. The whole schematic is shown in Figure 6.1.

In addition to the theoretical design detailed in previous chapters, the gate driver design and small components were added thanks to the insightful advices of TAS electronic designers. On a PCB, the traces (the conducting metallic lines) have a parasitic inductance of around 10 nH cm^{-1} . The parasitic inductance can therefore oppose fast variations of current, such as the current flowing through the switches. It has therefore been advised to add small capacitors really close to the switches in order to feed instantaneous current during small transients. Then, linear regulators were added in order to supply the gate driving IC. Other added components are small capacitors and resistors needed for the different IC to function properly.

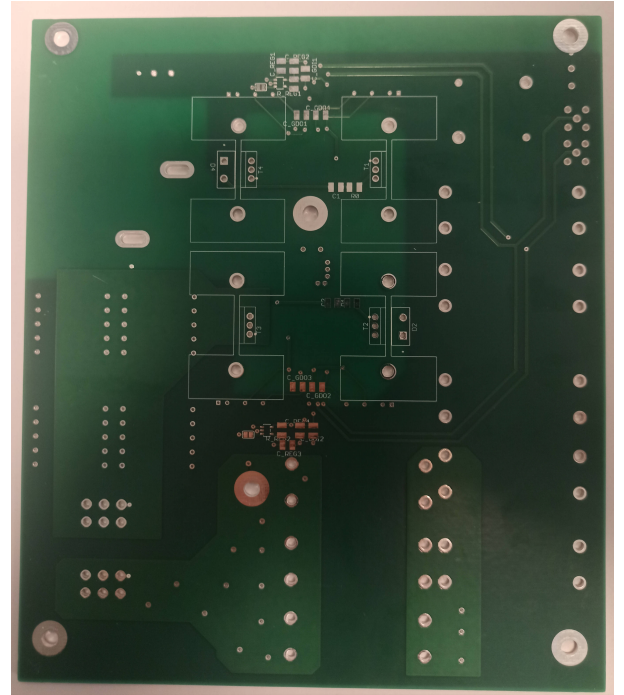
Figure 6.1: PCB schematic designed in Eagle.

6.2 Printed Circuit Board (PCB)

The schematic has been implemented in a board layout in order to print the final PCB. During the layout process, close attention has been paid in order to minimize the length of the traces, so that the parasitic inductances are minimized. The PCB has four layers of conducting surfaces : top and bottom layers for various traces connecting all the components, and two middle layers, namely a layer for the ground of the circuit and a layer for the 5 V supply needed for the drivers. These middle layers also serve as insulators in order for top and bottom signals not to suffer from distortion. However, using multiple layers can create parasitic capacitances, for example between the ground layer and the signal layers. Consequently, the ground layer does not occupy the entire area of the board, limiting the parasitic capacitance where the signals undergo a large voltage change. Figure 6.2 shows the top and the bottom of the PCB that has been manufactured.



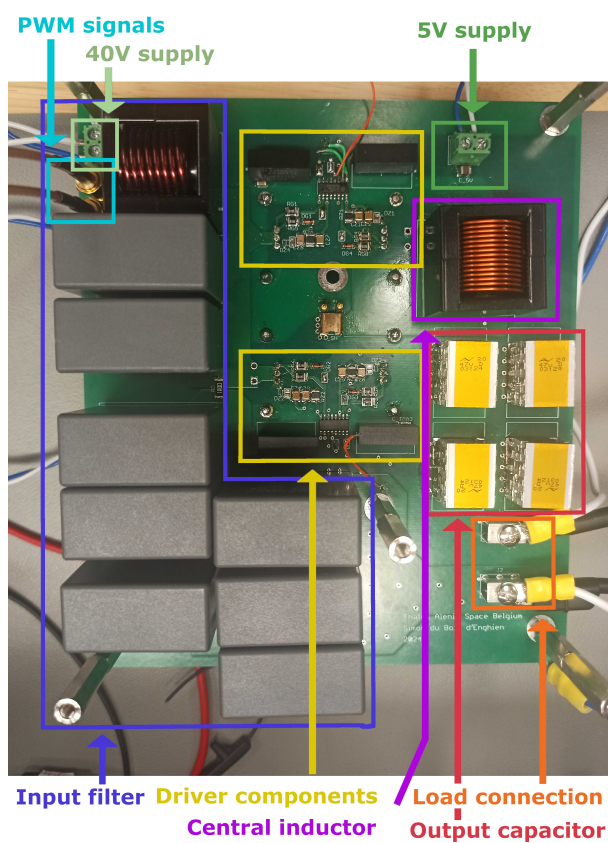
(a) Top part.



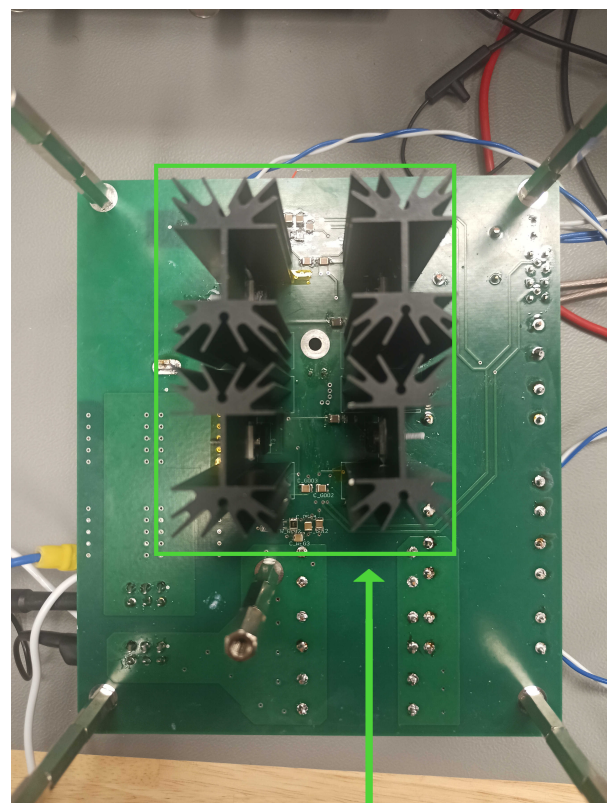
(b) Bottom part.

Figure 6.2: View of the PCB routing. The dimensions are 190 mm $\times$ 160 mm.

Finally, all the components have been soldered on the PCB. The PCB with the soldered components is shown in Figure 6.3. In order to save space, the components have been placed on both sides of the board.



(a) Top part.



MOSFET with heatsink

(b) Bottom part.

Figure 6.3: View of the assembled PCB.

7 | Measurements

Various measurements have been done in TAS laboratory in order to validate the design of the CRP supply. This chapter will first detail the measurement set-up and its associated measurements tools. Then, waveforms, power loss and efficiency curves will be shown in order to characterize the performances of the converter. A mathematical model will also be derived in order to estimate the losses of the converter for any duty cycle and load current. Finally, this chapter will highlight possible further improvements.

7.1 Measurement set-up

The measurement set-up is actually quite complex. Because the Watkins-Johnson converter is bipolar in output voltage, and the load is unipolar in current (only sinking current), the WJC is bidirectional in power. For duty cycles $D < 0.5$, the power is sinked at the high voltage side (which was typically called input in the previous chapters), and for $D > 0.5$, the power is sourced by the high voltage input side and consumed by the load. In addition to that, at the high voltage side, the voltage should remain constant, while the output, low voltage, can have a varying voltage but sinks a constant current.

7.1.1 Lab power supply

In order to have a constant input voltage, a power supply can be used. The power supply must always source power, and the input voltage can be selected by the user. Power supplies also have a maximal output current, which can be controlled in order to make sure that it does not exceed a certain value. They can also be controlled in voltage or in current. When controlled in voltage, the source adapts its output current to the circuits needs (while remaining below the current limit, but regulates its output voltage to remain constant). In current control mode, the source adapts its voltage to the circuit needs but keeps feeding a constant current. Finally, the power supply also have a maximal power rating. The supply used for the measurements is the HP 6002A DC power supply, whose maximal ratings can be found in Table 7.1.

Parameter	Maximal value
Power	200 W
Output voltage	50 V
Output current	10 A

Table 7.1: HP 6002A DC power supply maximal ratings.

7.1.2 Active load

In order to consume power at a constant current, an active load can be used. This latter consist of electronic circuits (such as bipolar junction transistors) which dissipate the power either acting as a resistor, as a current load or as a voltage load. Only the current load mode of operation will be used, as it is the type of load that would be encountered in the propulsion system for which the CRP supply has been designed. The electronic load also has maximal power, voltage and current ratings, but also minimal voltage rating. Indeed, the load cannot sink the full current without having its voltage above a certain threshold. The I-V characteristic of the load is given in Figure 7.1.

The active load used to perform the measurements is Keysight N3306A electronic load [32]. It consist of one frame that can handle three electronic loads. Its maximal and minimal ratings are given in Table 7.2.

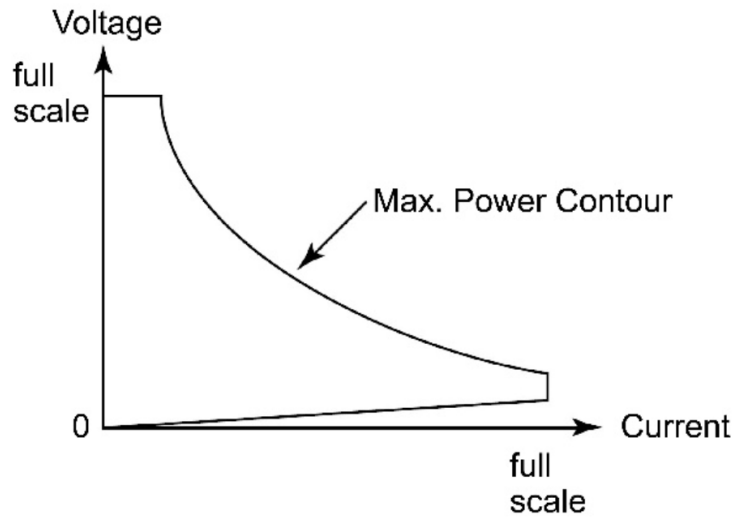


Figure 7.1: Electronic load operating area [32].

Parameter	Minimal value	Maximal value
Power	-	600 W
Input voltage	1.4 V	60 V
Input current	-	120 A

Table 7.2: Keysight N3300A electronic load ratings.

7.1.3 Bidirectional voltage supply and current load

In the case of a duty cycle $D > 0.5$, the set-up could be quite simple : the power supply is used as voltage source and the active load as current load. However, at $D < 0.5$, it would not work since the voltage source can only source power and the current load consume the power. Therefore, a bidirectional voltage and a bidirectional current load has to be implemented.

Bidirectional voltage supply

The most classic bidirectional voltage supply is a battery : the battery can charge and discharge (thus consume and feed power) while maintaining constant voltage. In order to simulate this behaviour, an current load (I_{sink}) has been placed in parallel with the power supply. At $D < 0.5$, this means that the current load will consume power, which will be fed by the converter and by the voltage supply. If the load's input current is set to a larger value than the converter's high side current, the converter and the voltage supply will feed power. At $D > 0.5$, the power supply must feed power to the current sink and the converter. By controlling the power supply in constant voltage and setting the maximal current to $I_{source} > I_{sink} + I_{in,converter}$, the power supply will be able to supply correctly the load and the converter.

The load current I_{sink} has been set to a constant 3 A current load.

Bidirectional current load

In order for the output current load to work in two voltage quadrants as well, an additional voltage source has been added in series to the active load (V_{bias}). By doing so, when the output voltage is negative, the voltage source increases this negative voltage to a positive one, such that the electronic load always sees a positive voltage across its terminals. When the output voltage of the converter is positive, the load will anyway see a positive voltage across its terminals.

Since the output voltage is not expected to go beyond -10 V , it has been decided to work with a constant voltage source V_{bias} of 15 V . If the converters output voltage is positive (e.g. 10 V), the power consumed by the active load will be

$$P = I_{load} \cdot (V_{out} + V_{bias}) = 10 \cdot (10 + 15) = 250\text{ W}, \quad (7.1)$$

which is acceptable because it remains below the loads maximal power rating.

7.1.4 Full set-up

The full set-up of the test bench is represented in Figure 7.2, and a picture of the lab set-up is shown in Figure 7.3.

In addition to the aforementioned battery simulator and bidirectional current load, the full set-up includes multiple multimeters, a four channel oscilloscope, an electronic circuit which creates the PWM signals (ZedBoard) and an auxiliary 5 V power supply. This auxiliary power supply is only needed to supply the low voltage components needed to drive the MOSFET's gates.

Multimeter

The multimeters are used as voltmeter or ammeter. A voltmeter is placed in parallel to the measured voltage, and can be approximated as an open circuit. Therefore, the current flowing through it can be considered null and the voltmeter does not create any power loss.

An ammeter is placed in series with a conductive wire in order to measure the current flowing through it. Again, it can be seen as a perfect measurement tool, which has no voltage drop and that does not consume power.

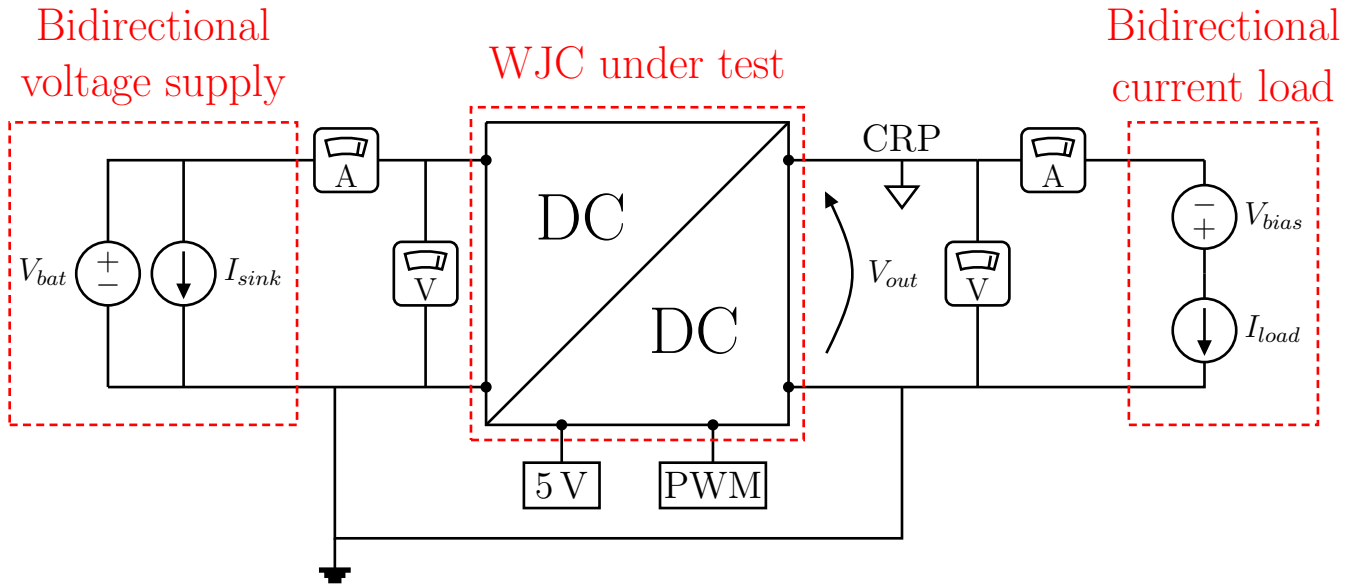


Figure 7.2: Schematic of the measurement setup.

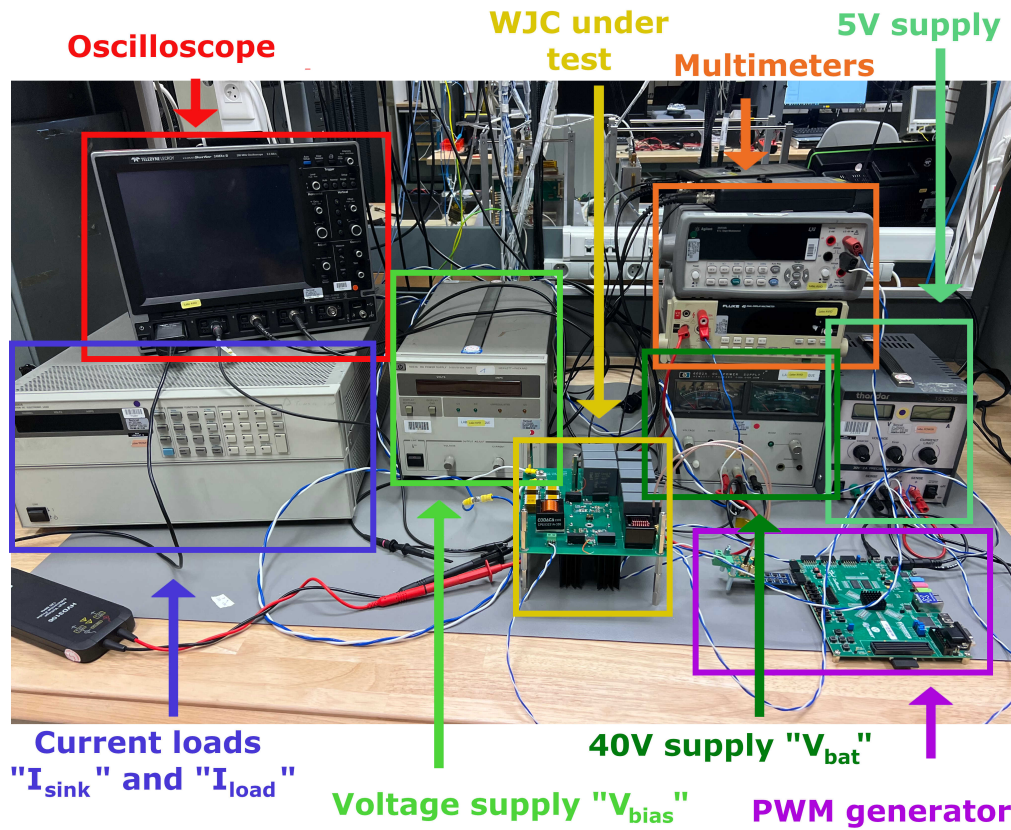


Figure 7.3: Lab measurement setup.

In the set-up, a voltmeter and an ammeter are placed at the high voltage side of the converter, to measure the input power fed through the converter. At the low voltage side, the ammeter is included in the electronic load, and the voltage measurement is done through the oscilloscope's average function.

Oscilloscope

The oscilloscope is used to visualize different waveforms across the circuit. It has four channels, meaning that four different waveforms can be seen at the same time.

In order to measure a voltage in the Watkins-Johnson converter, a basic probe can be used to measure it with reference to the ground. To measure a floating voltage (e.g. V_{gs} , where the source is not grounded), differential probes can be used. Those probes compute the difference between the two measured voltages.

To measure an alternating current, a Rogowski probe was used and works as follow. A helical wire is placed around the conductor in which the current has to be measured, forming a closed loop. It then measures and integrates the current induced in the probe, as it is proportional to the magnetic field captured by the helical wire [33]. In the lab, the Rogowski probes used measured an induced voltage of 50 mV A^{-1} .

Finally, the oscilloscope can also perform mathematical operation, such as computing the average value, RMS value, etc. of a signal. The average function was used in order to measure the output voltage instead of using an additional voltmeter.

PWM generation

The PWM signal are generated by an external electronic circuit and its associated software. The electronic card is Diligent's ZedBoard Zynq-7000 Development board [34] and is controlled by Farnell's SP-Pulse program. This allows to create synchronous PWM signals, by manually setting their period, pulse width and dead-time.

7.2 Lab measurements

Various measurements have been done in the lab in order to characterize the converter and to validate its design. The measurements that have been done using the set-up presented previously and that will be explained in this section are listed below.

- Output voltage - duty cycle characteristic
- Transient waveforms
- Efficiency of the converter
- Power loss of the converter
- Conduction losses estimation of the PCB

The output voltage-duty cycle relationship is represented in Figure 7.4, for different load currents, at $V_{in} = 40 \text{ V}$.

It would be expected to have only one curve, which would be valid independently of the load current and match the theoretical curve. At no load, the theoretical and experimental curves match almost perfectly, but it is not the case if a current load is connected. Two explanations can be given to explain this unexpected behaviour.

First, assuming there is a load current and that the converter operates in CCM, because of the introduced dead-time, the input-output relationship is slightly changed. For a given

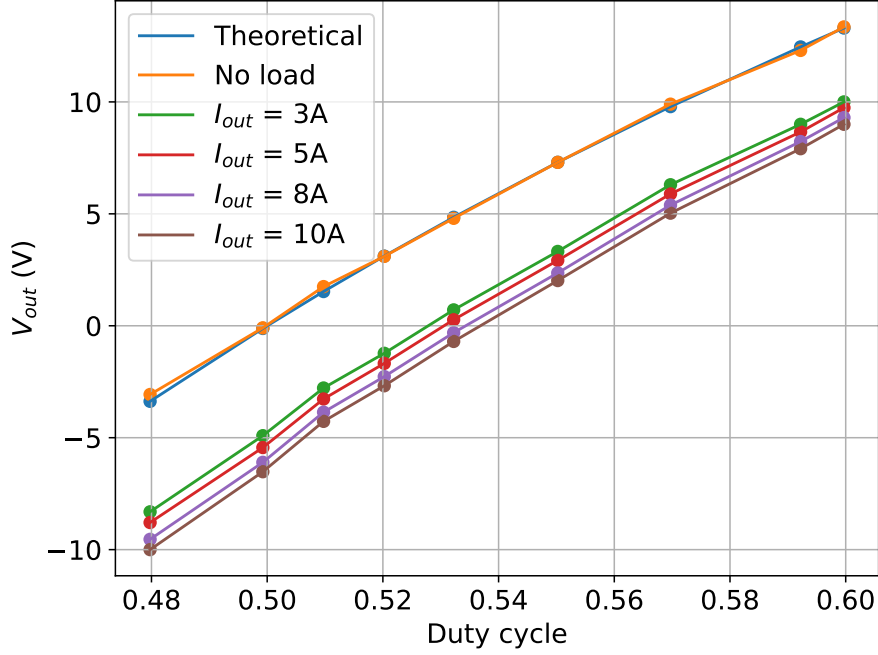


Figure 7.4: Output voltage vs duty cycle at $V_{in} = 40$ V.

duty cycle, the switches S_1 and S_3 will conduct for a shorter time than expected. Indeed, during the dead-time, the body diode of switches S_2 and S_4 will conduct, thus changing the effective conduction time of all switches. This explains why there is such a difference between the theoretical curves and the measured one. This difference is not observed at no load, because the average current on the inductor can be considered as null. Therefore, the body diode of S_1 and S_3 will conduct during the dead-time former to turn-on of S_1 and S_3 , because the inductor current is negative and flowing in the other direction. Similarly, the body diode of S_2 and S_4 will conduct during the dead-time prior the the turn-on of S_2 and S_4 . The initial transfer function $V_{out} = \frac{(2D-1)}{D}V_{in}$ is thus preserved.

Then, one can seen that the output voltage-duty cycle relationship varies due to the load current. This can be explained with the Thevenin equivalent circuit of the converter shown in Figure 7.5. At no load, the Thevenin equivalent sees an open circuit and the output voltage $V_{out,meas} = V_{out,conv}$. However, when the load is connected, a voltage divider is created between the equivalent output impedance of the converter and that of the load. While ideally, the DC output impedance of the converter is null, in practice, the small parasitic resistance of the component create a non-zero DC output impedance. This explains the output voltage difference between the measurements for various load currents.

7.2.1 Waveforms

The most critical measurement is the one at the minimal duty cycle (i.e. the duty cycle required to obtain -10 V at the output), since it is for that measurements that the current in the inductor and MOSFET will be the highest. This minimal duty cycle has been identified and is $D = 0.48$.

The gate-source voltage of the transistors S_1 and S_4 at $D = 0.48$ are shown in Figure 7.6. In the figure's grid, a rectangle represents 5 V in amplitude and 1 μ s in time.

It can be seen that the gate-source voltage has large parasitic oscillations each time the

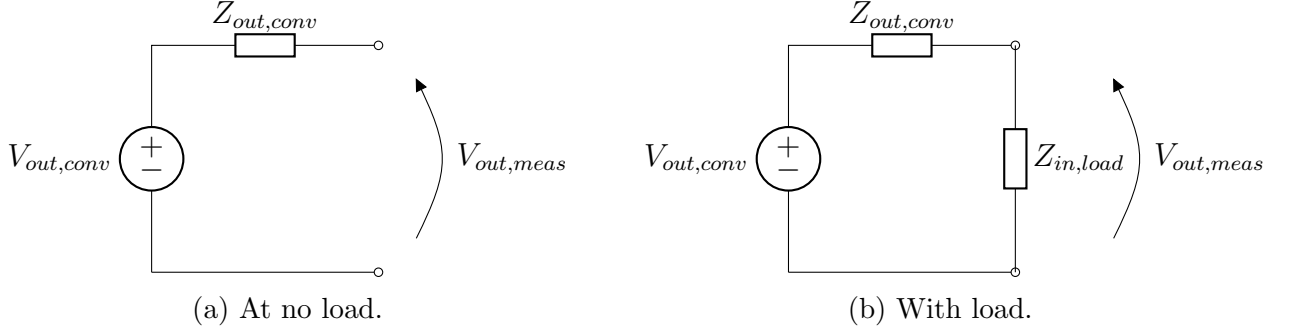


Figure 7.5: Thevenin equivalent of the converter seen at the output.

switch S_1 turns-on. This undesired behaviour has been identified and is due to the reverse recovery of the body diode of switch S_4 . Indeed, the large reverse current flowing through the diode flows through the parasitic inductance of the components and create a voltage drop, which also resonates with the parasitic capacitances of the MOSFET. Additional measurements showing switching transients are displayed in Appendix B.

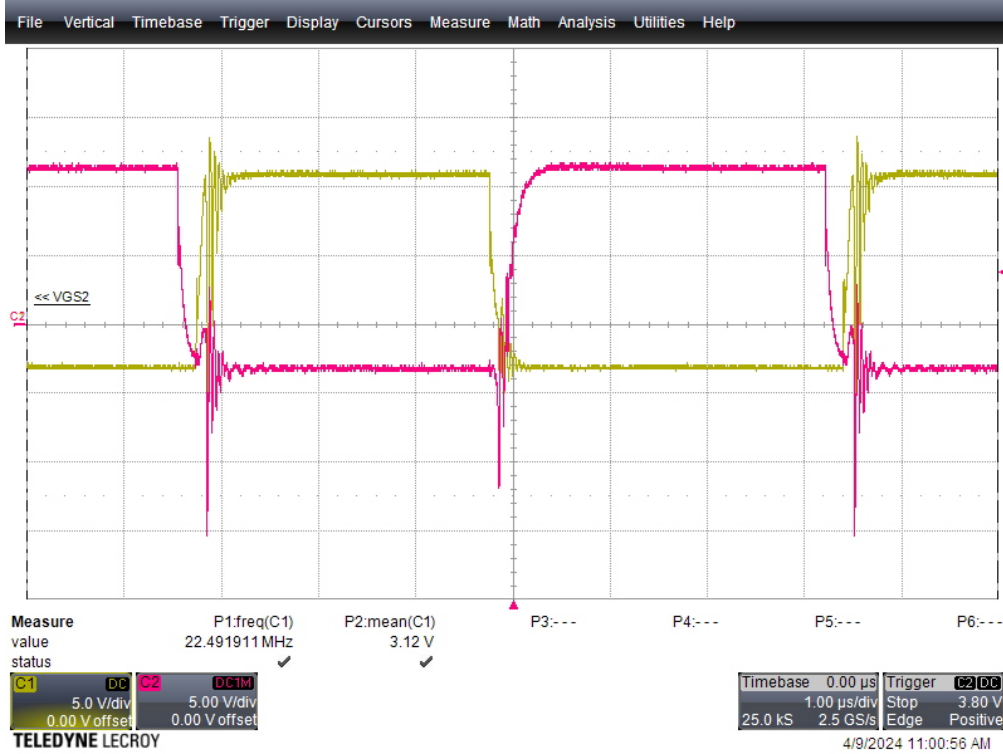


Figure 7.6: Gate-source voltage of S_1 (yellow) and S_4 (red) at $D = 0.48$ and $I_{load} = 10$ A. Timebase of 1 $\mu\text{s}/\text{div}$, and amplitude of 5 V/div on both channels.

The input filter voltage and output voltage of the converter for $D = 0.48$ are shown in Figure 7.7. The input filter voltage represents the voltage at the output of the input filter, or equivalently, the voltage at the drain terminal of MOSFET S_1 or S_2 . In the figure, the output voltage (yellow) was measured with a 10 V offset, meaning that the 0 V reference shown on the oscilloscope actually measures -10 V in reality. Additionally, each rectangle measures 200 mV in amplitude. The output voltage ripple is approximately 120 mV, which is slightly above the maximal output voltage ripple allowed by the design requirements. Parasitic oscillations are also present, and are also thought to be caused by the same phenomenon as

described earlier.

The input filter voltage (red) was measured without offset and a rectangle represent 20 V of amplitude. Again, this voltage has parasitic oscillations at each switching time. Finally, output voltage waveforms at different duty cycle are also shown in Appendix B.

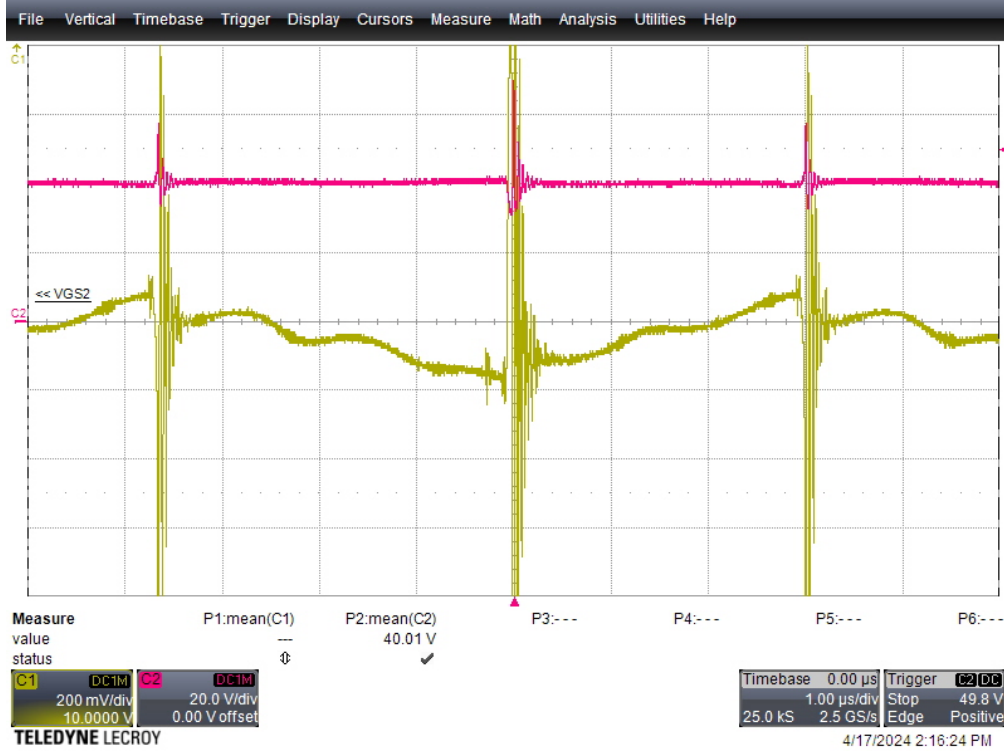


Figure 7.7: Input filter voltage (red) and output voltage (yellow) at $D = 0.48$ and $I_{load} = 10$ A. Timebase of $1 \mu\text{s}/\text{div}$ for both channels, and amplitude of $200 \text{ mV}/\text{div}$ and 10 V offset on channel 1 (yellow), and $20 \text{ V}/\text{div}$ and 0 V offset on channel 2 (red).

7.2.2 Efficiency and power loss

The efficiency of a converter is usually one of the most important attribute of a power converter. The efficiency of the converter has therefore been characterized, for different output voltages and load current, as shown in Figure 7.8. In order to measure it, the input and output power have been measured with ammeters and voltmeters, and the mean power sourced and consumed are $P = VI$. The efficiency is computed as

$$\eta = \frac{P_{consumed}}{P_{sourced}} \quad (7.2)$$

The efficiency of the converter looks quite odd : it can range from more than 80% down to 0%. Indeed, as the application for this converter is to cancel leakage current in the satellite by adapting its output voltage, the goal is not exactly to transfer power, but rather to regulate the output voltage to some reference. Therefore, when the output voltage is close to 0 V, the efficiency of the converter will obviously drop down to 0%, but in practice the lost power might be relatively small, in the range of a few watts. Therefore, the efficiency is not a good way to characterize the performances of the converter. Instead, the power loss is a much better candidate, as it will directly show how much power the system will dissipate in order to regulate its output voltage to the desired value.

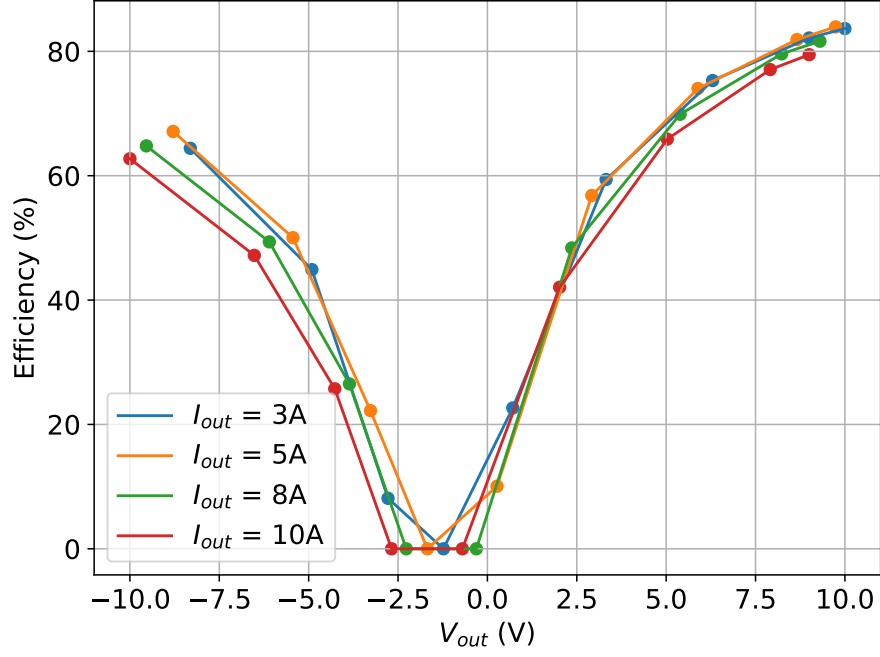


Figure 7.8: Efficiency vs output voltage. Dots represent the measurements.

The power loss is simply measured as

$$P_{Loss} = P_{sourced} - P_{consumed}, \quad (7.3)$$

where $P_{sourced}$ and $P_{consumed}$ are again measured by multiplying the voltage and currents measured with the multimeter. Figure 7.9 shows the loss for different load currents and duty cycles. These losses are caused by multiple factors, namely conduction losses, switching losses, no-load losses, and body diode conduction losses.

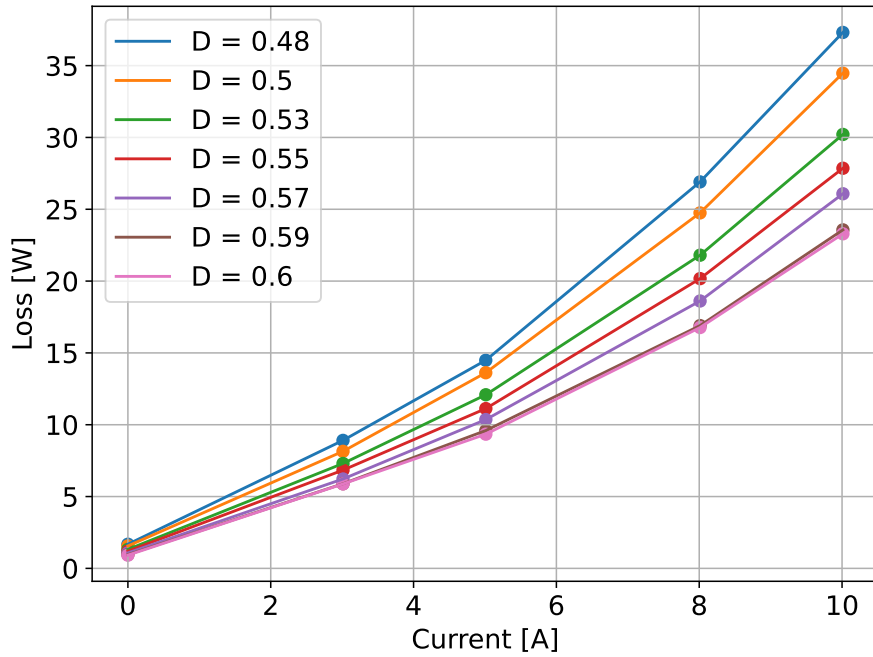


Figure 7.9: Loss measurements for different duty cycle. Dots represent the measurements.

In the following, the conduction losses of the PCB and the components will be measured.

Conduction loss estimation of the board

The conduction loss of the PCB and those of the components can be estimated. This is done for the different paths that the current is flowing through, by controlling the switches to create the desired path and supplying constant current at the input. By measuring the voltage drop across all the components and all the traces of the PCB, the conduction loss can be estimated. This test has been done first with switches S_1 and S_3 ON, and supplying 10 A at the input (path A). Then, it has been done a second time with S_2 and S_4 ON and supplying the same current (path B).

Using the DC state averaged model, the converter can essentially be split in three parts, which are shown in Figure 7.10. The first part goes from the input of the input filter, to the drain of the upper MOSFET and from ground of all parts of the circuit to the ground input port of the converter. In this part, the current is given by $I_1 = \frac{2D-1}{D} I_{out}$. The second part goes from the drain of the upper MOSFET to the source of the lower MOSFET. There, the current has the same value as the inductor current, and is $I_2 = \frac{I_{out}}{D}$. The last part goes from the source of MOSFET S_3 to the input connection of the load, where $I_3 = I_{out}$.

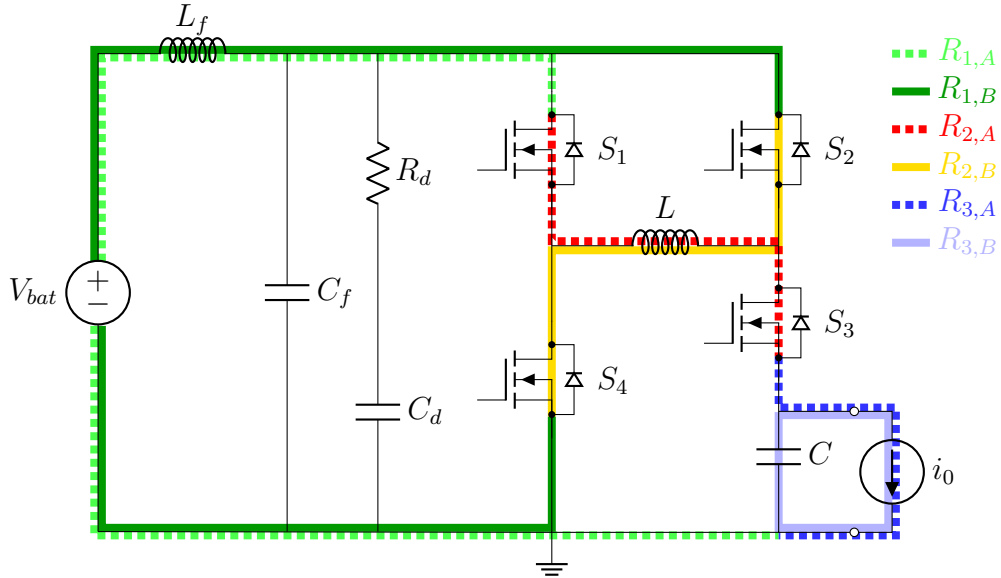


Figure 7.10: Current path of the circuit and associated parasitic resistances. Dashed lines represent path A and solid lines represent path B .

Table 7.3 shows a summary of the measured resistances across each part of the circuit, for the two path identified previously.

Circuit part	Path A (S_1 & S_3 ON)	Path B (S_2 & S_4 ON)
1	$R_{1,A} = 18.55 \text{ m}\Omega$	$R_{1,B} = 22.60 \text{ m}\Omega$
2	$R_{2,A} = 15.86 \text{ m}\Omega$	$R_{2,B} = 13.99 \text{ m}\Omega$
3	$R_{3,A} = 1.73 \text{ m}\Omega$	$R_{3,B} = 1.20 \text{ m}\Omega$

Table 7.3: Measured parasitic resistances of the PCB and components for different paths.

State averaging is done to give an average value combining the two paths, depending on the value of duty cycle. The equivalent output resistance is the parasitic resistance seen at the output of the converter, combining the three parts of the circuit using the state-space model :

$$\begin{aligned}
R_{out,avg} = & (R_{1,A}D + R_{1,B}(1 - D)) \left(\frac{2D - 1}{D} \right)^2 \\
& + (R_{2,A}D + R_{2,B}(1 - D)) \left(\frac{1}{D} \right)^2 \\
& + (R_{3,A}D + R_{3,B}(1 - D)),
\end{aligned} \tag{7.4}$$

where $R_{i,j}$ represents the measured parasitic resistance of part i of the circuit in the path j .

The average output resistance and the associated conduction loss are computed for few values of the duty cycle in Table 7.4. The conduction loss is computed as

$$P_{cond} = R_{out,avg} I_{out}^2. \tag{7.5}$$

D	$R_{out,avg} [\text{m}\Omega]$	$P_{cond} [\text{W}]$
0.48	$0.14 + 64.62 + 1.45 = 66.22$	6.62
0.55	$0.37 + 49.65 + 1.49 = 51.82$	5.18
0.6	$2.24 + 41.98 + 1.52 = 45.74$	4.57

Table 7.4: Average output resistance ($R_{out,avg}$) and conduction loss (P_{cond}) for different duty cycles (D) at load current $I_{out} = 10 \text{ A}$.

It can be seen that the conduction loss is mainly due to the conduction loss in part 2 of the circuit. In the loss model approximation that will be derived in next section, $R_{out,avg}$ could therefore be approximated as

$$R_{out,avg} = (R_{2,A}D + R_{2,B}(1 - D)) \left(\frac{1}{D} \right)^2 = R_{2,eq} \left(\frac{1}{D} \right)^2. \tag{7.6}$$

7.3 Loss model approximation

Recall that power loss had been measured for different duty cycles at different load currents. Considering all of these measured points, an approximation model can be derived, in order to estimate the loss for any configuration of load current and duty cycle.

As it is obvious that the model will have dependencies in duty cycle (D) and load current (I), finding the best suited model can be quite complex, since the easier the model, the more approximated it will be, and the more complex the model, the more it could give unrealistic results.

In all generalities, losses can be split in three categories : no-load losses which are independent of the current, switching losses and diode conduction losses which are proportional to the current, and conduction losses which are quadratic to the current :

$$P(D, I) = A(D) + B(D)I + C(D)I^2 \quad (7.7)$$

In order to address the dependencies in D , each type of loss is approximated:

$$\begin{cases} A(D) = \alpha + \frac{\beta}{D^2} \\ B(D) = \frac{\gamma}{D} + \frac{\delta}{D^2} \\ C(D) = \frac{\epsilon}{D^2}, \end{cases} \quad (7.8)$$

where α and $\frac{\beta}{D^2}$ address constant losses and the capacitance loss of the MOSFET, which are proportional to V_{ds}^2 (Equation 5.36), where $V_{ds} \approx aV_{in} + b\frac{V_{in}}{D}$. $\frac{\gamma}{D}$ expresses the body diode conduction loss and part of the switching loss, whose voltage is independent of the duty cycle but the the conducted current is $I = \frac{I_{out}}{D}$. $\frac{\delta}{D^2}$ represents the second part of the switching loss decomposition, whose voltage is inversely proportional to the duty cycle, with the same current $I = \frac{I_{out}}{D}$. Finally, $\frac{\epsilon}{D^2}$ accounts for the conduction loss, and its dependency in $\frac{1}{D^2}$ was explained previously.

Using all the data measured in Figure 7.9, a least square approximation can be performed for all the load current and duty cycle combinations as follow:

$$\begin{bmatrix} P_{1,mes} \\ P_{2,mes} \\ \dots \\ P_{ij,mes} \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{D_A^2} & \frac{I_1}{D_A} & \frac{I_1}{D_A^2} & \frac{I_1^2}{D_A^2} \\ 1 & \frac{1}{D_A^2} & \frac{I_2}{D_A} & \frac{I_2}{D_A^2} & \frac{I_2^2}{D_A^2} \\ \dots & \dots & \dots & \dots & \dots \\ 1 & \frac{1}{D_j^2} & \frac{I_i}{D_j} & \frac{I_i}{D_j^2} & \frac{I_i^2}{D_j^2} \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \\ \gamma \\ \delta \\ \epsilon \end{bmatrix} \quad (7.9)$$

More generally, it can be rewritten as

$$\mathbf{P} = \mathbf{MC}, \quad (7.10)$$

with $\mathbf{M}$ the measurements and $\mathbf{C}$ the coefficients.

The coefficients are then found by

$$\mathbf{C} = (\mathbf{M}^T \mathbf{M})^{-1} \mathbf{M}^T \mathbf{P} \quad (7.11)$$

Applying this method to the data measured and shown in Figure 7.9 gives the following coefficients :

$$\begin{cases} \alpha = 0.285 \text{ W} \\ \beta = 0.322 \text{ W} \\ \gamma = -0.221 \text{ V} \\ \delta = 0.511 \text{ V} \\ \epsilon = 0.041 \Omega \end{cases} \quad (7.12)$$

These coefficients have been used in order to fit the model to the data. Figure 7.11 shows the measured data and its associated approximation. It can be seen that the model matches really closely the reality.

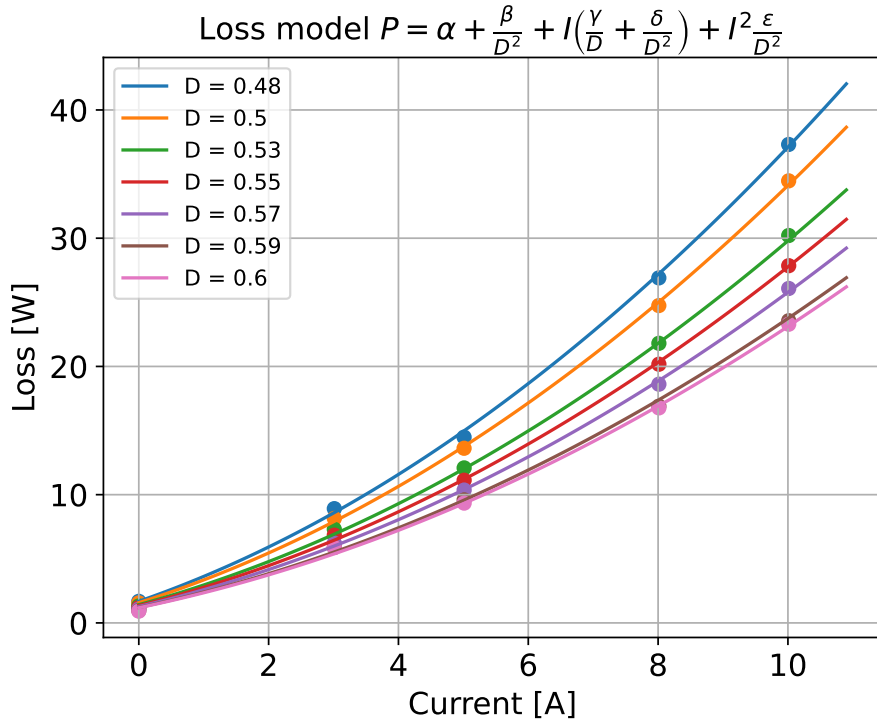


Figure 7.11: Loss measurements and model approximation for different duty cycle. Dots represent the measurements, and the lines are computed with the approximation model.

Finally, the coefficients can be paralleled with their physical values in order to estimate parameters of the circuit.

From β , the output capacitance of the MOSFET can be estimated as

$$C_{oss} = \frac{\beta}{2f_s V_{in}} = 0.67 \text{ nF}. \quad (7.13)$$

Approximating the switching time at turn-on and turn-off to be the same, they can be estimated with

$$t_{on} = \frac{\delta}{4f_s V_{in}} = 21.2 \text{ ns} \quad (7.14)$$

As γ expresses a multitude of parameters combined together (including body diode conduction loss, switching loss, reverse recovery loss), it is hard to give it a physical interpretation. Finally, ϵ directly expresses the parasitic resistance, which was expected to be really close to

15 m Ω , as detailed previously when investigating the conduction loss of the PCB. The estimated parameters have therefore been matched to their physical quantities, and it can be seen their values have realistic magnitudes. The loss model presented in Figure 7.11 therefore matches well the measured data and is coherent with respect to physical nature of the estimated loss.

7.4 Further improvements

The presented topology works as expected, although the dissipated loss are quite important. At nominal current, between 23 W and 37 W are dissipated, which is relatively high. In this losses, the conduction loss can hardly be minimized, as it would require to select new components and design a new layout. Switching loss, and especially the losses due to the reverse recovery of the MOSFET's body-diode could be minimized.

First, the topology using two diodes instead of two MOSFET (which was previously detailed in Figure 2.5) has been investigated. Unfortunately, it has the disadvantage of having an extremely large voltage spike at each switching transient, which did not allow to operate at full load. However, from the measurements done with a smaller current load, it dissipated more power than the topology with four MOSFET.

Then, it has been decided to add Schottky diodes in parallel with the MOSFET whose body diodes are conducting, in order to bypass the body diodes' and their reverse recovery. Though it decreased the power loss in simulations, the results in practice fell well short of what was anticipated. The main explanation for that is that the Schottky diode did not have time to start conducting, because of the parasitic inductances present in the circuit. Unfortunately, very few measurements were done with this topology, because most of the measurement tools were utilized on other projects within TAS. Due to time constraints, it has not been possible to use them later on.

Finally, other possibilities could be to use different transistors. Ideally, it would be required to have a very low input capacitance, in order to decrease the turn-on and turn-off time, as well as a very good body diode, or by using a faster Schottky diode in parallel. The packaging could also play a crucial role, since the longer the pins of the package, the higher the parasitic inductance.

8 | Conclusion

The objective of this master thesis was to design, implement and test a new power supply, whose output voltage could be both positive or negative and connected to ground. This power supply was needed for a new kind of space electrical propulsion architecture called Direct-Drive.

First, an introduction to space electrical propulsion system detailed how satellites and other space vehicles can currently move through space thanks to hall effect thrusters and how the thruster is powered by the PPU. The emerging architecture called Direct-Drive architecture has been described, and shows promising results in terms of weight savings and efficiency improvements. The necessity of a new power converter was demonstrated by TAS in order to simulate the galvanic insulation that was previously obtained with a transformer.

Then, a state-of-the-art review has shown the different types of power converter that existed, and the Watkins-Johnson converter has been selected. Its state-space representation and its AC canonical model has been derived, and a schematic view of a control scheme has been presented in Chapter 3. Though the controller has not been designed in practice, it will be of great interest for TAS in case of further use of the WJC for the Direct-Drive architecture.

All the components of the WJC have been designed and carefully selected in order to meet the requirements specified for the power supply. This design has been validated by comprehensive simulations using LTSpice. Switching transients were carefully studied and a complete driver was designed in order to reach fast turn-on and turn-off times. A prototype has then been designed, including the schematic and layout design using Autodesk Eagle.

Finally, once assembled, many tests have been performed on this prototype. The test bench engineered in TAS's labs allowed for bidirectional power flow, in order to best reproduce the real operating conditions of the power supply. The converter operates as expected and is able to supply the necessary voltage at the maximal load current. However, its power loss is relatively large and more effort should be given in the future to decrease the loss. A summary of the Watkins-Johnson converter performances is shown in Table 8.1.

Measurement	Value
Maximal output voltage ripple ΔV_{out}	120 mV
Power loss at $V_{out} = -10$ V	37 W
Power loss at $V_{out} = 10$ V	23 W

Table 8.1: WJC converter performances at full load ($i_{load} = 10$ A).

Though the work done for this thesis has come to an end, there remains work ahead in order to validate the CRP supply for space applications. While minimizing the loss should be done by improving switching transients and avoiding over currents due to the reverse recovery of the MOSFET's body diode, the alternative topology presented in Chapter 2 could also be studied. Overall, it must be remembered that the Watkins-Johnson converter was a first working prototype, which will have to go through multiple iterations before being fully functional.

On a more personal note, I really enjoyed working on this master thesis and I am glad for all the new skills I learned. Through this work, I managed to tackle a big engineering project and divide it into smaller tasks, which allowed me to reach the goals that I defined and to have a fully functional prototype.

This work allowed me to use the knowledge I learned at university in order to tackle a larger engineering project. I was happy to put my knowledge of control systems and linear algebra into practice for some parts of this work such as the aspects of controllability, and the creation of an approximation loss model.

I also particularly enjoyed the practical aspects of this work such as the PCB design, PCB assembly, thinking about the test set-up and realizing the measurements. The practical aspects of this thesis were found to be very complementary to the more academic classes attended during my years in university. Finally, this work has given me an even stronger taste of what it is like to be a power electronic designer, and I aspire to pursue similar projects in my future career.

Appendix

A | Linearisation of the state-space model

This appendix gives more details about the linearisation of the state-space model.

As a reminder, the states equations are

$$\begin{cases} \frac{di_L}{dt} = \frac{v_{in} - v_o}{L} \\ \frac{dv_{out}}{dt} = \frac{i_L - i_o}{C} \end{cases} \quad (\text{A.1})$$

when S_1 and S_3 conduct (during dT), and

$$\begin{cases} \frac{di_L}{dt} = \frac{-v_{in}}{L} \\ \frac{dv_{out}}{dt} = \frac{-i_o}{C} \end{cases} \quad (\text{A.2})$$

when S_2 and S_4 conduct (during $(1 - d)T$). It can be rewritten as

$$\frac{d}{dt}\mathbf{x} = \mathbf{A}_1\mathbf{x} + \mathbf{B}_1\mathbf{u}, \quad (\text{A.3})$$

and

$$\frac{d}{dt}\mathbf{x} = \mathbf{A}_2\mathbf{x} + \mathbf{B}_2\mathbf{u}. \quad (\text{A.4})$$

State averaging gives

$$\frac{d}{dt}\mathbf{x} = (\mathbf{A}_1d + \mathbf{A}_2(1 - d))\mathbf{x} + (\mathbf{B}_1d + \mathbf{B}_2(1 - d))\mathbf{u}. \quad (\text{A.5})$$

Introducing small variations such that $\mathbf{x} = \mathbf{X} + \hat{\mathbf{x}}$, $\mathbf{u} = \mathbf{U} + \hat{\mathbf{u}}$ and $d = D + \hat{d}$, where the small variation is considered much smaller than the steady state value:

$$\hat{\mathbf{x}} \ll \mathbf{X}, \quad \hat{\mathbf{u}} \ll \mathbf{U}, \quad \hat{d} \ll D, \quad (\text{A.6})$$

the model becomes :

$$\begin{aligned} \frac{d}{dt}(\mathbf{X} + \hat{\mathbf{x}}) &= \left(\mathbf{A}_1(D + \hat{d}) + \mathbf{A}_2(1 - D - \hat{d}) \right) (\mathbf{X} + \hat{\mathbf{x}}) \\ &\quad + \left(\mathbf{B}_1(D + \hat{d}) + \mathbf{B}_2(1 - D - \hat{d}) \right) (\mathbf{U} + \hat{\mathbf{u}}). \end{aligned} \quad (\text{A.7})$$

Recalling that $\mathbf{A}_1 D + \mathbf{A}_2(1 - D) = \mathbf{A}$ and $\mathbf{B}_1 D + \mathbf{B}_2(1 - D) = \mathbf{B}$, and that

$$\frac{d}{dt}\mathbf{X} = 0 = \mathbf{A}\mathbf{X} + \mathbf{B}\mathbf{U}, \quad (\text{A.8})$$

Equation A.7 can be simplified as

$$\begin{aligned} \frac{d}{dt}\hat{\mathbf{x}} = & \left(\mathbf{A}_1 \hat{d} + \mathbf{A}_2(-\hat{d}) \right) (\mathbf{X} + \hat{\mathbf{x}}) + \left(\mathbf{B}_1 \hat{d} + \mathbf{B}_2(-\hat{d}) \right) (\mathbf{U} + \hat{\mathbf{u}}) \\ & + \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\hat{\mathbf{u}}. \end{aligned} \quad (\text{A.9})$$

Considering the hypothesis A.6, $\hat{d} \cdot \hat{\mathbf{x}} \ll \hat{d} \cdot \mathbf{X}$ and $\hat{d} \cdot \hat{\mathbf{u}} \ll \hat{d} \cdot \mathbf{U}$. Finally, the small signal state-space model can be rewritten as

$$\frac{d}{dt}\hat{\mathbf{x}} = \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\hat{\mathbf{u}} + ((\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U}) \hat{d}. \quad (\text{A.10})$$

The same approach can be used to find the output vector $\hat{\mathbf{y}}$.

B | Additionnal measurements

This appendix will present additional waveforms measured in TAS lab.

Figure B.1 and Figure B.2 show the gate-source voltage and drain currents of S_1 and S_4 at $D = 0.6$ and $D = 0.48$. In order to measure the current, two Rogowski probes were used. As a reminder, these probes can only measure alternating current. The addition of the current in S_1 and S_4 gives the inductor current. One can see that it has an average value of approximately 20 A and a ripple of approximately 2 A. The large current spikes present at turn-on and turn-off of the MOSFET is due to the reverse recovery of the MOSFET's body diode.

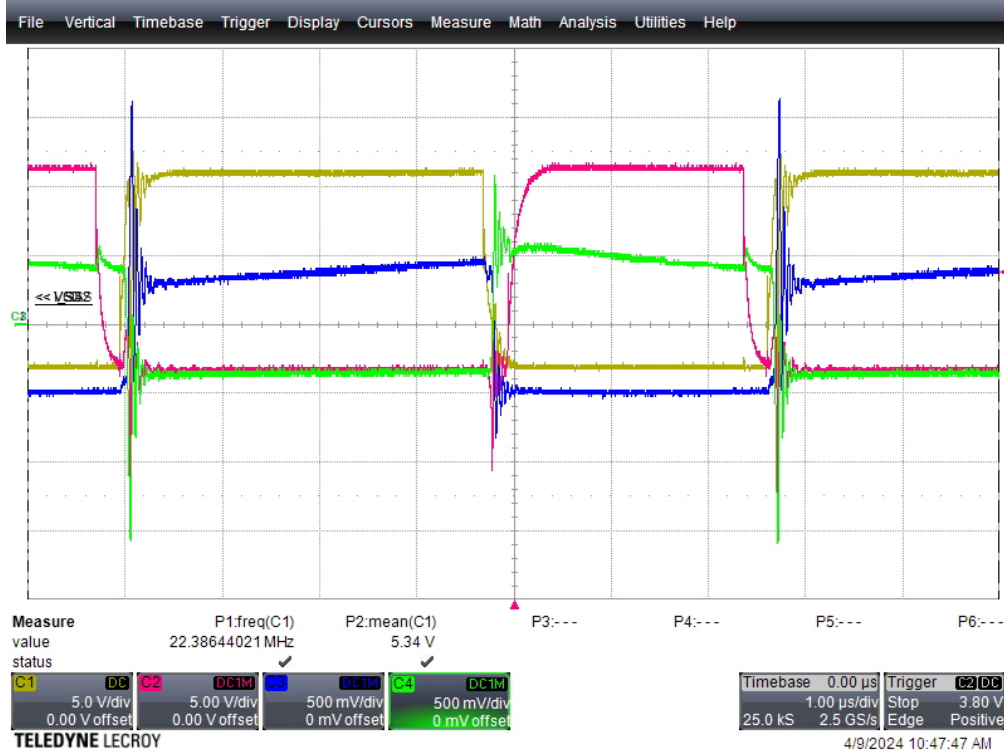


Figure B.1: Gate-source voltage of S_1 (yellow) and S_4 (red) and drain current of S_1 (blue) and S_4 (green) at $D = 0.6$ and $I_{load} = 10$ A. Timebase of 1 μ s/div, and amplitude of 5 V/div for channel 1 & 2 and amplitude of 10 A/div for channel 3 & 4.

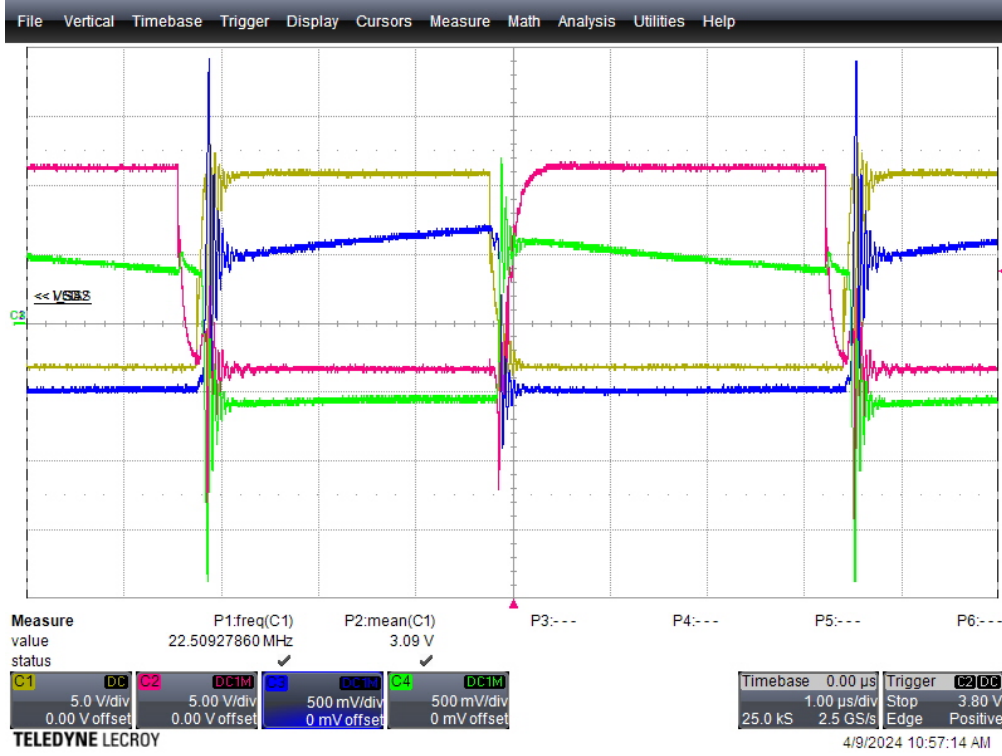


Figure B.2: Gate-source voltage of S_1 (yellow) and S_4 (red) and drain current of S_1 (blue) and S_4 (green) at $D = 0.48$ and $I_{load} = 10$ A. Timebase of $1 \mu\text{s}/\text{div}$, and amplitude of $5 \text{ V}/\text{div}$ for channel 1 & 2 and amplitude of $10 \text{ A}/\text{div}$ for channel 3 & 4.

Figure B.3 and Figure B.4 show a zoom on the switching transient, at $D = 0.6$ and $D = 0.48$. It can be seen that at turn-off of S_4 (red), the current continues to flow through its body diode during the dead-time (green). S_1 then turns-on, and the body diode of S_4 stops conducting. A large reverse recovery current flows through S_4 (and S_1 supplies this current). This large current spike creates a voltage drop due to the parasitic inductances since $V = L \frac{dI}{dt}$. Additionally, the current resonates with the MOSFET capacitances and this explains why multiple oscillation occurs. The frequency of those oscillations is approximately $f = 22.5 \text{ MHz} = \frac{1}{2\pi\sqrt{LC}}$. Assuming a parasitic inductance of 10 nH , it gives a capacitance of approximately 5.1 nF . This is in the right order of magnitude for a MOSFET capacitance, and makes physical sense. Finally, the current spike is larger at $D = 0.48$, which can be expected as the inductor current and current flowing in the switches is also larger.

Finally, Figures B.5 and B.6 show the input filter voltage and output voltage at $D = 0.6$ and $D = 0.53$. These waveforms show that the converter is able to operate at negative output voltage (shown in Figure 7.7), positive output voltage, and around 0 V .

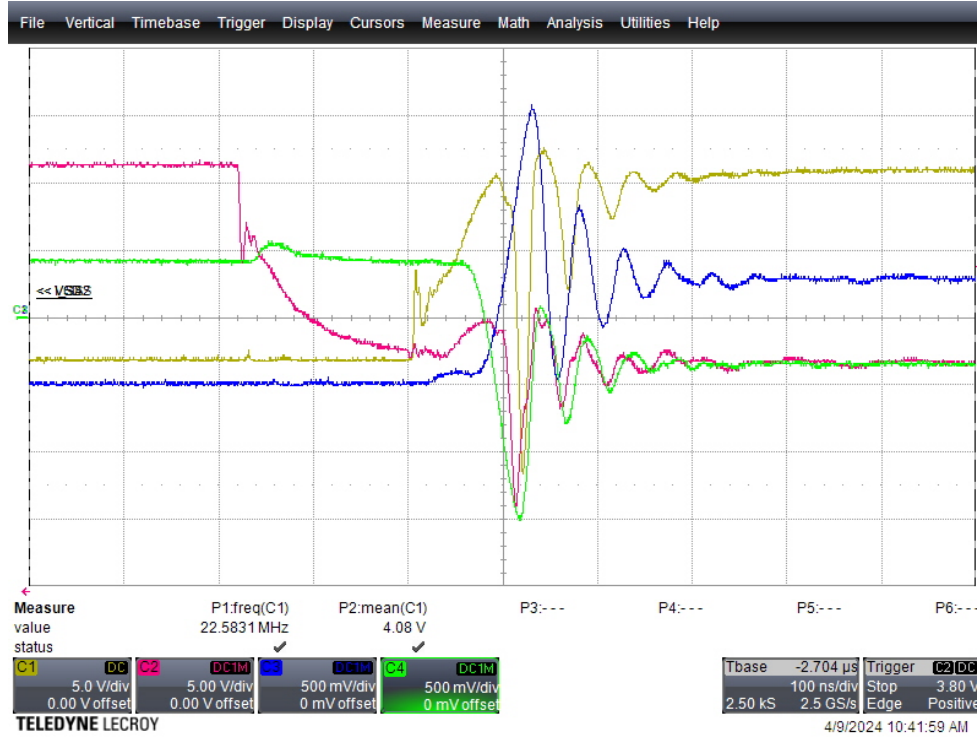


Figure B.3: Zoom on the switching transients at turn-on of S_1 . Gate-source voltage of S_1 (yellow) and S_4 (red) and drain current of S_1 (blue) and S_4 (green) at $D = 0.6$ and $I_{load} = 10$ A. Timebase of 100 ns/div, and amplitude of 5 V/div for channel 1 & 2 and amplitude of 10 A/div for channel 3 & 4.

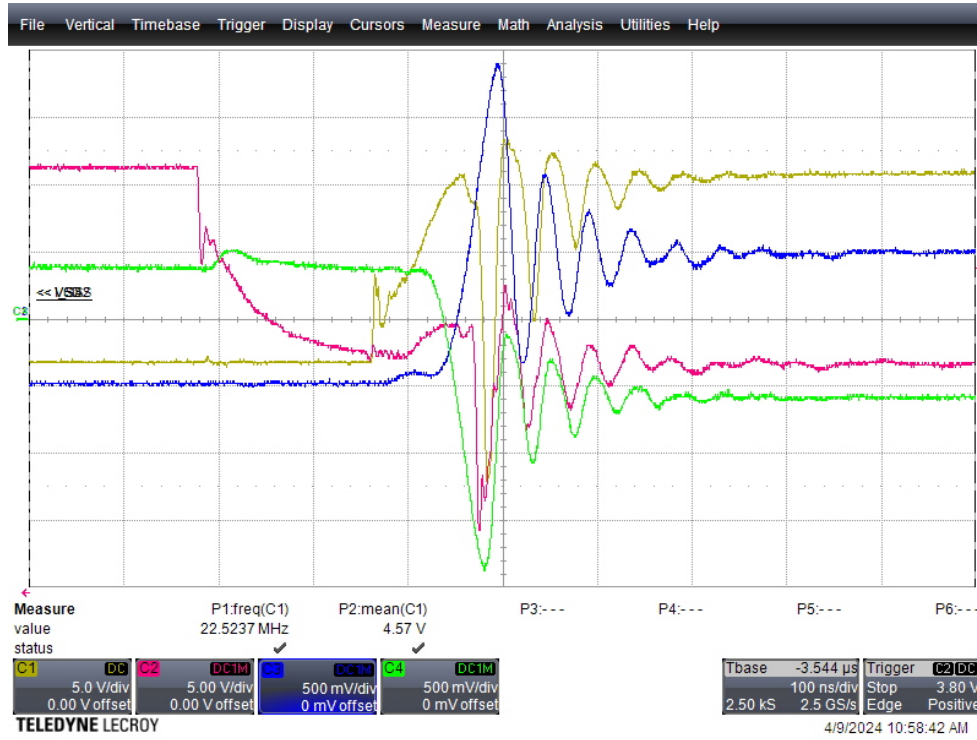


Figure B.4: Zoom on the switching transients at turn-on of S_1 . Gate-source voltage of S_1 (yellow) and S_4 (red) and drain current of S_1 (blue) and S_4 (green) at $D = 0.48$ and $I_{load} = 10$ A. Timebase of 100 ns/div, and amplitude of 5 V/div for channel 1 & 2 and amplitude of 10 A/div for channel 3 & 4.

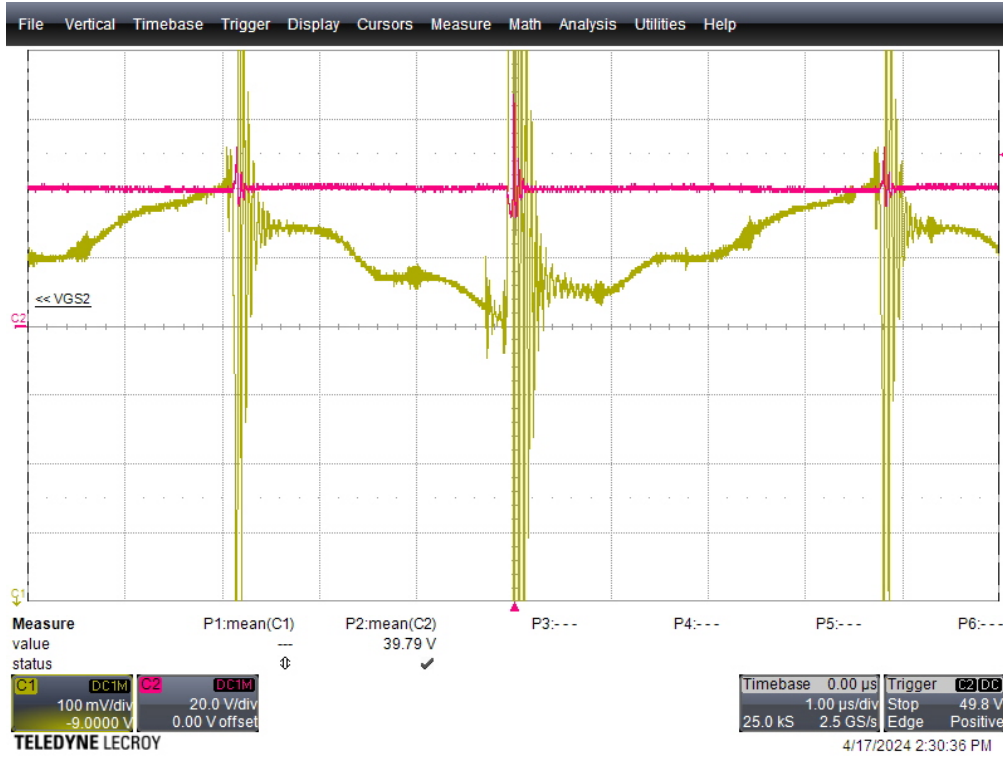


Figure B.5: Input filter voltage (red) and output voltage (yellow) at $D = 0.6$ and $I_{load} = 10$ A. Timebase of $1 \mu\text{s}/\text{div}$ for both channels, and amplitude of $100 \text{ mV}/\text{div}$ and -9 V offset on channel 1 (yellow), and $20 \text{ V}/\text{div}$ and 0 V offset on channel 2 (red).

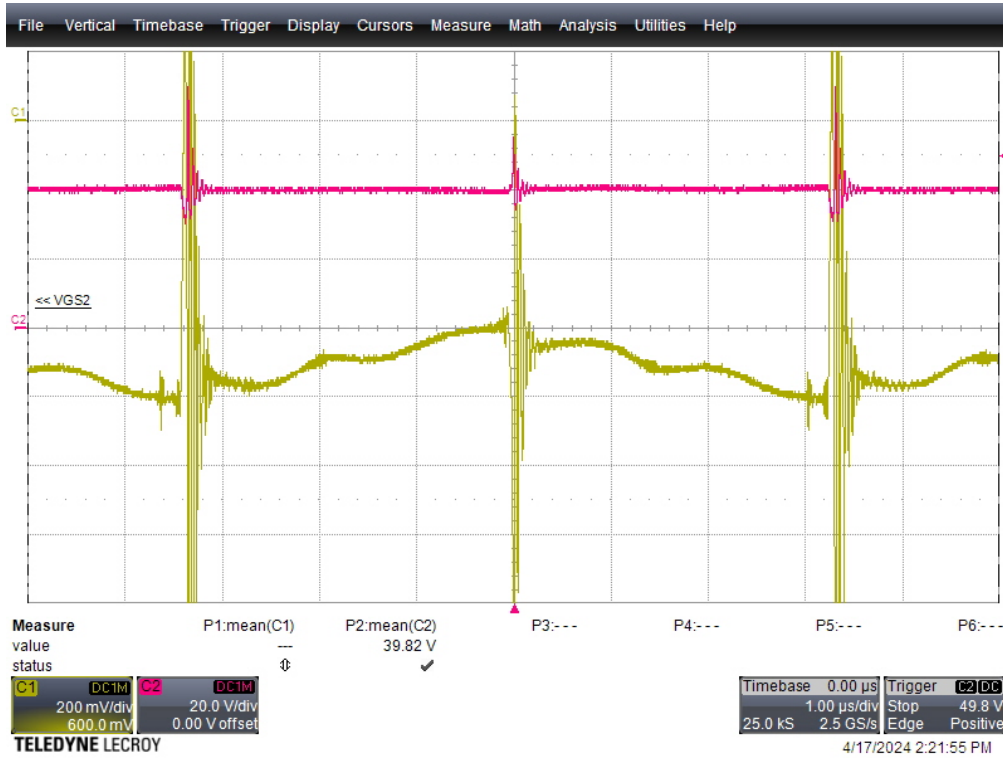


Figure B.6: Input filter voltage (red) and output voltage (yellow) at $D = 0.53$ and $I_{load} = 10$ A. Timebase of $1 \mu\text{s}/\text{div}$ for both channels, and amplitude of $200 \text{ mV}/\text{div}$ and 0.6 V offset on channel 1 (yellow), and $20 \text{ V}/\text{div}$ and 0 V offset on channel 2 (red).

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