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Power and area optimization of a dynamic vision sensor in 65nm CMOS

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Abstract

In this master thesis, a dynamic vision sensor (DVS) based on the DAVIS architecture is designed in 65nm CMOS. It aims at optimizing the architecture for this scaled technology. It firstly provides a overview of existing DVS architectures. An experimental analysis of different photodiodes is conducted to obtain both responsivity and dark current parameters. At the same time, a comparison between the four types of photodiode is done and results in the choice of an N-well/P-sub photodiode for this work. The pixel is then designed, based on the measured parameters, and following the target optimization in power and area. It ends up with an estimated $5\mu m$x$5\mu m$ pixel providing a power consumption of 16nW at high activity and 9nW of static power consumption. A latency of 7 μs and a dynamic range of 120dB are also reported but it is finally at the cost of increased contrast sensitivity (19 %) and FPN (9%). Problems encountered in this study are discussed and a set of design guidelines is proposed for future implementation of DVS in scaled CMOS technology.

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Introduction

Human body is an incredible machine. That might sound awkward but who would dare to deny it? Indeed, if the human was an artificial creation, it would probably be the most efficient among any other. The way it is actuated and even more the way it can sense the external world and process the huge amount of sensed data is absolutely unique. So unique that humans themselves cannot stop to study it and to daily discover new features.

For many years, scientists have been tending to mimic the human behavior to reach its performances, even dreaming to outperform them. From humanoid robot to neuromorphic electronics, many researches have been lead to artificially recreate human features, of which the vision. If electronic vision sensors appeared in the middle of the 20th century, their design were based on the refreshing of the full pixel array several times (50-60) per second. Such continuous data acquisition is much more power consuming than the human retina. But it was only in 1994 that the first bio-inspired vision sensor was proposed [16]. Instead of periodically updating the pixel array, this new sensor was designed to detect only change of light intensity so that if nothing moves in the field of vision of the sensor, it stays in a kind of sleep mode. The first neuromorphic CMOS imager was invented.

Following this template many other works have been conducted since to improve the performances and to build a practical vision sensor [17, 18, 6]. It has lead to the physical implementation of so-called dynamic vision sensors (DVS) that are used in several fields like high-speed robotics, movement tracking, 3-D reconstitution, etc [19, 20].

If they already show good performances such as high dynamic range, short latency or good contrast sensitivity (percentage of light intensity change detectable by the sensor), their sizing has not evolved much with time despite the scaling of the

CMOS technology. This work thus aims at trying to push the boundaries of a DVS architecture to a 65nm CMOS. Determining the possibility, the advantages and drawbacks to do so are one of the purposes of this study. As CMOS photodiodes have not been fully characterized yet in 65nm, and since it is the basic photosensing element of the sensor, an experimental analysis is also conducted and represent the second main purpose of this work. Finally, since it has not been already done, an optimization in power and area will be developed to determine the improvement possibilities of DVS in scaled CMOS technologies. The latter is obviously the main target of this master thesis.

In order to meet these objectives, this work will be organized as follows:

- The **first chapter** will introduce and review the existing DVS as well as the CMOS photodiode working principle and previous characterization.
- A **second chapter** will be dedicated to the experimental analysis of CMOS photodiodes in 65nm. Results will be presented and discussed.
- The **third chapter** is the main part of this work. It goes through the pixel design and optimization, one block at the time.
- **Chapter four** will extract the performances of the designed pixel. It shows the positive and negative aspects of the optimization process on the main performances presented in literature.
- The **fifth, and last, chapter** of this work is made of a discussion on the pixel design and its performances. Guidelines for future work are proposed.

Chapter 1

State-of-the-art of existing pixel architectures and photodiodes in CMOS

Contents

In this chapter, the evolution of CMOS image sensor is presented, from its apparition in the 60's to its current applications. An overview of its development over years allows to understand why they are more and more studied and used nowadays. A summary of existing dynamic vision sensor architectures is then exposed. Their differences are explained and their key performances with regards to this work are highlighted. Finally, the different CMOS photodiodes types are presented along with some of previous experimental measurements. It introduces the experimental characterization done in this master thesis.

1.1 A brief history of CMOS vision sensor

CMOS image sensor appeared in the early 60's with so-called MOS image sensors. They were composed NMOS, PMOS or bipolar cells and provided applications such as light's spot position determination [21] or scanning [22], i.e. producing an output pulse corresponding to the input light intensity. However, these devices did not use any on-chip signal-processing and were thus just able to generate an output signal purely proportional to the instantaneous local light intensity [1]. Later in the decade, a method to integrate the output signal on a junction capacitance and to read this new output is proposed by Weckler [23]. It lead to the creation of the Reticon Corporation, which was a pioneer in that field.

The 70's brought the apparition of charge-couple devices (CCD), which were much more suitable for vision sensors at that time. Indeed they were smaller and more simple to integrate, and the noise level was much lower than for the MOS image sensor, because of the premature MOS technology. MOS vision sensors has been almost completely neglected for more than a decade since the researches were focused on CCD image sensors. But in the late 80's, two fields in which MOS technology showed better performances has revived the interest in such technology: infrared detection which gave a much better temperature variation robustness than CCD and high energy physics particle detection in which CCD were too sensitive to radiations.

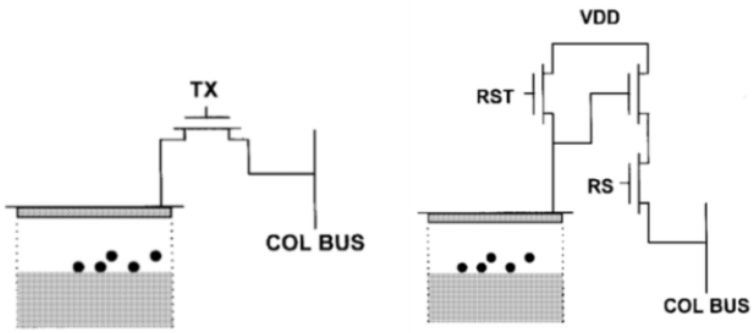

Figure 1.1: Basic architecture of passive (left) and active (right) pixels from [1]

The upcoming 90' and its linked industrialization has really launched the CMOS image sensor field. The quest for low cost in the industries, and of miniaturization and low power devices has increased the interest in CMOS image sensor. Moreover, as the technology became more mature, their results began to be promising, but still poorer than the CCD. Passive and active architecture came out at that time.

The first topology was based on Weckler work, it only used a charge integrator amplifier to convert the charges into a readable signal, as shown in Fig. 1.1. Noise, speed and scalability were limiting factor in such topology. The idea of active pixel sensor was thus to improve these performances by adding a amplifier/buffer in each pixel, see Fig. 1.1. Such architecture is still the basis of current APS.

In the meantime, M.Mahowald researches were focused on another type of pixel based on neuromorphic systems [16]. The idea was to mimic the working principle of a biological retina on an electronic device. His pixel, as the human retina 1.2, was composed of three main parts:

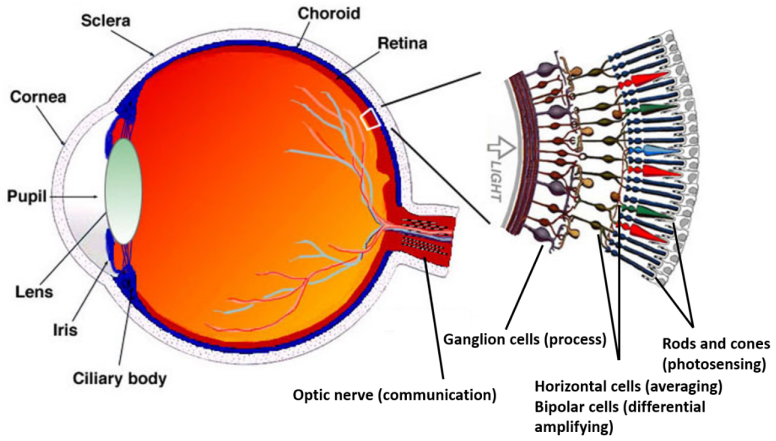

Figure 1.2: Simplified human retina comparison structure (adapted from [2])

- A phototransducing element, in charge of the logarithmic conversion of the light intensity, taking the rods and cones role.
- A temporal and spacial averaging resistor network, allowing to capture the background illumination, replacing the horizontal cells of the eye.
- A differentiating amplification stage between the sensed light of the phototransducing elements and the average background illumination given by the horizontal. It replaces the ganglion cells.

If his work did not result in any practical application because of the lack of maturity of CMOS technology, it has lead to a whole new type of thinking in CMOS pixel design: neuromorphic image sensor.

More recent researches in the 00' have deepened Mahowald's work and resulted in 2004 in a pixel proposed by Zaghoul and Boahen [24][25]. It aimed at accurately

mimicking the retina behaviour on silicon chip. They succeed to design a device with neuromorphic features such as spatio-temporal filtering, luminance adaptation, contrast gain control and temporal adaptation. However, as their purpose was not to build a real device, optimization on power, energy efficiency or pixel-to-pixel variation had not been explored at that time.

Meanwhile, in 2002 and 2005, two types of practical dynamic vision sensor have been proposed, by Kramer [18] and Mallik [4], using asynchronous and synchronous event-based image sensor, respectively. These architectures, especially the asynchronous one from Kramer, have been the foundation of dynamic vision sensors that are still designed today. The following section explains the working principle of such pixel and summarizes the existing designs in the literature.

1.2 Dynamic vision sensor architectures

Dynamic vision sensors (DVS) are based on the retina behavior. They are opposed to active vision sensors (APS) by their output: DVS respond to a change of light intensity, while APS sense absolute light intensity. They are thus used in very different ways since APS generally work as frame-based sensor, meaning that the whole pixels array (the frame) is refreshed several times per second to sense the absolute light intensity. On the contrary, a DVS pixel only responds to light change with an event, hence working as an event-based sensor. This event is then transferred to the "brain" with an address-event representation (AER). DVS have thus the advantage not to periodically refresh the entire pixel array but to use only spikes to respond to light intensity change, hence consuming much less power! However, since a signal processing must be done by each pixel, it complicates the architecture compared to APS.

1.2.1 Address-event representation

AER is an asynchronous neuromorphic chip-to-chip or intra-chip communication protocol founded in the 90's by M. Sivilotti in his PhD [26]. It is used to control the data acquired by DVS but it is also widely used in neuromorphic systems in general. Its main advantage is to work with spikes instead of transferring data, hence reducing the power consumption and the amount of transmitted data. Its working principle, illustrated in Fig. 1.3 for unidirectional communication, is the following: each transmitter element has a unique address, when an event occurs in one element, its address is sent through an high-speed single bus, the receiver reads the address and deduces that an event occurred at this address.

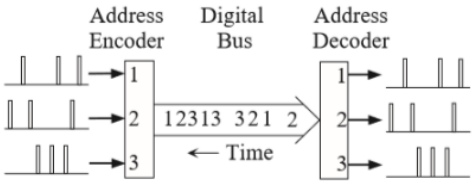

Figure 1.3: AER unidirectional communication protocol illustration [3]

However, since AER is not implemented in this work, no further analysis on its architecture will be done in this section.

1.2.2 Synchronous architecture

Mallik *et al.* has proposed a temporal change threshold detection imager [4]. It is composed of a standard APS, using three transistors and a photodiode, combined with a differential amplifier build with 2 capacitors and three other transistors, see Fig. 1.4.

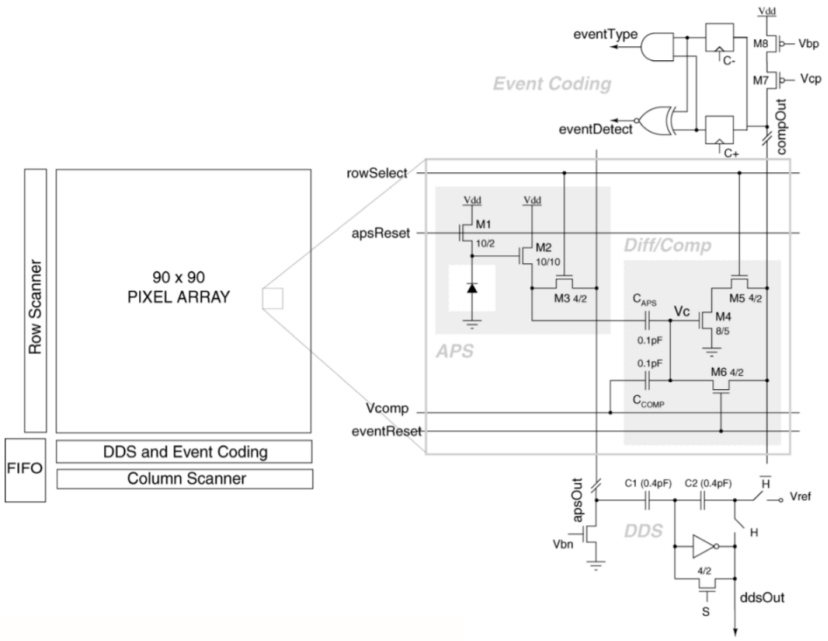

Figure 1.4: Modified APS proposed by Mallik *et al.* to feature a temporal threshold detection [4]

The complexity is thus kept simple. It also provides the advantage of being able to be used as both classic APS with built-in a 1-bit analog-to-digital converter (differential amplifier), and as an illuminance change detector between two frames, using the same differential amplifier to compare the sensed change of light intensity to a fixed threshold. Indeed, as it is detected between two frame updates, it gives a temporal aspect to the detection achieved by the sensor.

At the end, this sensor does not provide interesting features in the scope of this work since it is almost frame-based. But it is to be noticed that the low complexity of the pixel has enabled to keep the area much smaller than other ongoing works of that time.

1.2.3 Asynchronous architectures

Basis of current DVS, such topology has been introduced by Kramer [18]. He proposed the structure shown in Fig. 1.5 to sense temporal illumination changes.

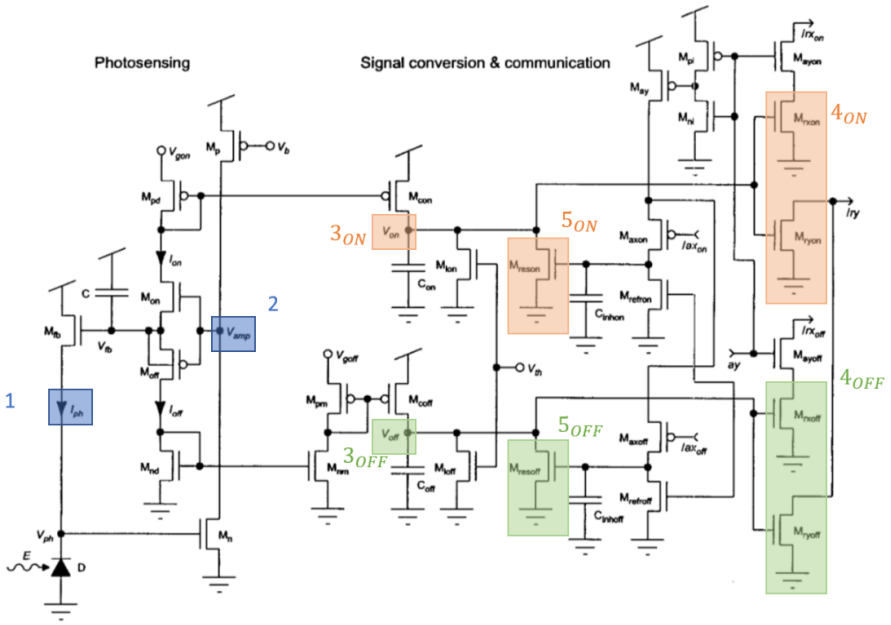

Figure 1.5: Pixel propose by Kramer, with the global data path highlighted. 1. Generated photocurrent, 2. Voltage conversion of photocurrent before ON and OFF voltage split at 3., 4. Comparison of ON and OFF voltage for the event generation, after the event reception and treatment (AER), reset is authorized by the arbitrator (signals 'ay' and 'IaxON/OFF') and done with a reset transistor in 5.

It is composed of three main parts used for:

- Photosensing
- Differential amplifying
- Processing and communication

Based on such circuit division, Lichtsteiner came out in 2008 with a very competitive dynamic vision sensor that had facilitated significant advances in this field [17]. It gave a wider dynamic range and a much more symmetrical response on ON and OFF events. The mismatch, which was an issue in previous publications of the same research group [27], has been handled to enhance the performance. They succeeded in the design of a pixel with wide dynamic range, low mismatch and relatively small latency while keeping the area reasonable for that time (40 μm of pitch).

At the same time, another research group proposed the idea of an asynchronous time-based image sensor (ATIS) [5]. It was the first image sensor combining both dynamic and absolute light detection. It ended in a physical chip presented in a 2011 paper [28]. The idea of combining DVS and APS will be further developed with the dynamic and active pixel vision sensor (DAVIS) in 2014 [6], and its improvements (color version cDAVIS in 2015 [29], better contrast sensitivity SDAVIS192 in 2018 [30]).

As these researches focused on practical outputs of a dynamic sensor (contrast sensitivity, events rates, dynamic range,...), and as this type of vision sensor is relatively recent, almost no optimization process have been conducted up to now, at the exception of the Samsung's pixel in 2017 [7], which targeted a smaller pixel pitch to fit in mass production, and the work of Naomi Rousseau in her thesis aiming at designing a low power version of a DVS [31].

Asynchronous time-based senor (ATIS)

The ATIS pixel schematic is presented in Fig. 1.6. It uses two different photodiodes for the APS and the DVS parts. While its APS periodically detect the absolute light intensity thanks to a PWM control wave the DVS asynchronously detects temporal contrast in illuminance. The AER protocol is then used to communicate the acquired data from the sensor.

If this pixel provides the advantage of a wide bandwidth and a lower power consumption thanks to the event-based configuration, its area is not optimized since two photodiodes are needed for each pixel.

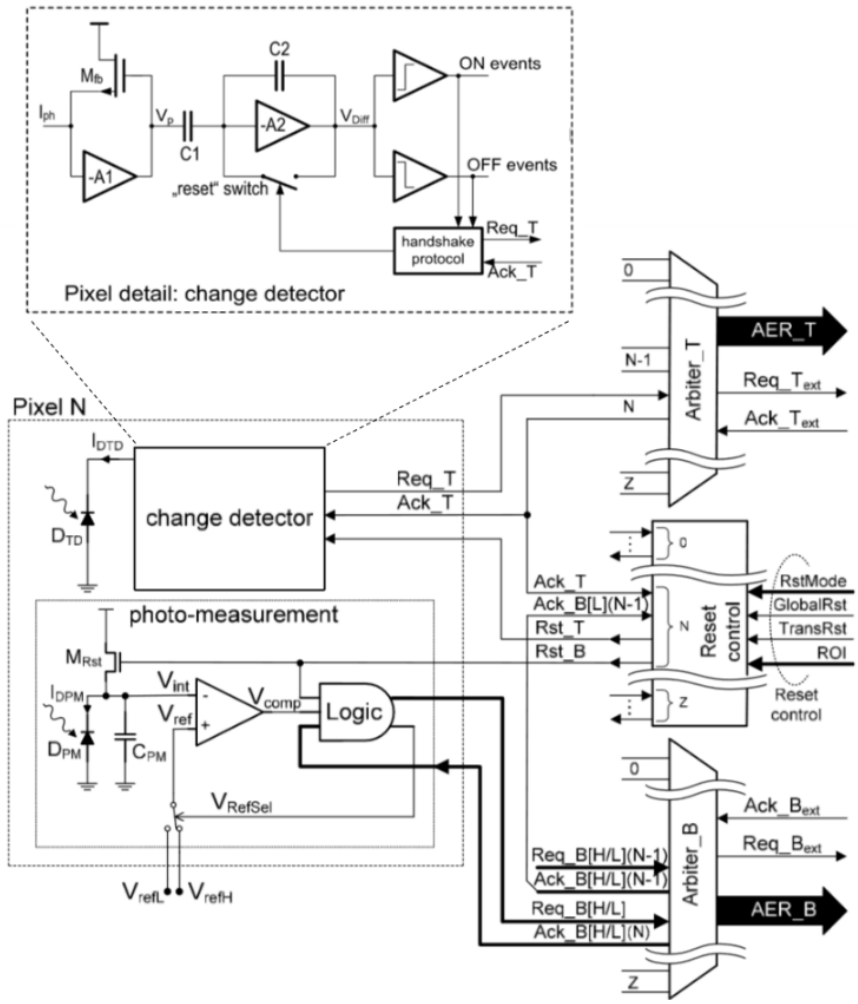

Figure 1.6: ATIS pixel implementation, from [5]

A modified version of this pixel has been proposed in 2011 by Barranco *et al.* [32]. It does not provide anymore a frame-based sensor and the DVS is enhanced with a pre-amplification stage at its output. This allowed to reduce the minimum contrast sensitivity at 10%. Obviously, the add of such amplification stage is at the cost of an higher power consumption. Two years later, they came out with an improved version giving a contrast sensitivity of 1.5% along with a huge power reduction thanks to their new low power and low mismatch pre-amplification stage [33].

Dynamic and active vision sensor (DAVIS) and improvements

This vision sensor is an improved version of the ATIS proposed by Brandli *et al.* in 2014. As its predecessor, it also provides both absolute and relative light detection, but this time using only one shared photodiode for both parts of the sensor as illustrated in Fig. 1.7 [6]. It comes with the advantage of a smaller pixel area.

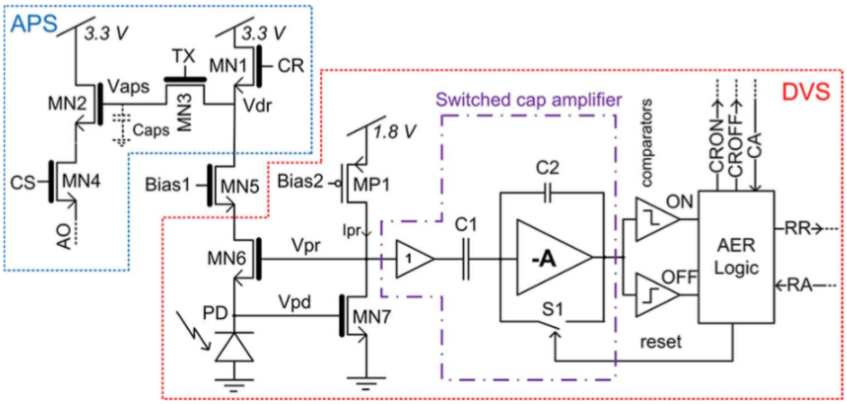

Figure 1.7: DAVIS pixel implementation [6]

The DVS part of the pixel, which is the part on which this work is focused, is made of the same classical blocks:

- The photoreceptor circuit followed by a buffer to isolate it from the differentiating amplifier
- The amplification is done by a self reset switched capacitor amplifier (SCA)
- The comparators that trigger ON and OFF event and the AER communication logic, to correctly interact with the arbitrator

This sensor reaches a contrast sensitivity of 11% with a dynamic range of 130dB. If the pixel area is reduced compared to previous work (18 μm of pitch), it is still not optimized... neither is the power consumption. It is only mentioned that the DVS part of the pixel consumes much more power that its APS part.

Based on this work, several improvements have been proposed such as the integration of color detection in 2015 [29] but as the aim was not similar, comparison is difficult to be made. Another pixel has been proposed in 2018: the SDAVIS192 [30]. Similarly to Barranco, this pixel implements a pre-amplification stage which allows to reduce the minimum contrast sensitivity, but still at the cost of a increased power consumption.

Samsung pixel

Samsung has presented in 2017 a pixel that showed a huge improvement in term of area. Its simple architecture is presented in Fig. 1.8.

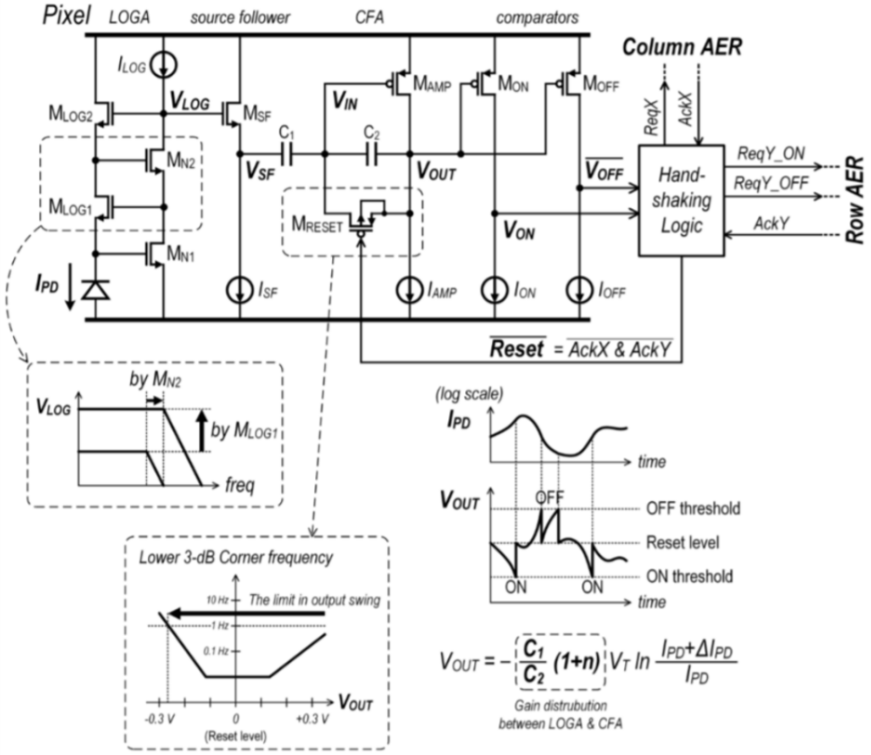

Figure 1.8: Samsung's pixel architecture [7]

It works following the DAVIS scheme but all amplification stage are done with a minimum number of transistors (pre-amplification, op-amp in the SCA, comparators). Moreover it is the first DVS that has ever been built using technology below $0.1\mu m$ (90nm BSI CIS). It also uses backside illuminated (BSI) photodiode, which allow to overlap the photodiode with the pixel circuitry, hence reducing the area. The power consumption is also kept small (88nW at low activity) and thanks to an arbitrator that process several pixels as one, they achieved a very high event rate of 300Meps and kept a contrast sensitivity of 9%. But they do not give precise information on the fixed pattern noise achieved in such pixel. Indeed, since their communication protocol treats multiple pixels as one, pixel-to-pixel variation might be compensated, but no further data has been furnished on this matter. The dynamic range is for its part only presented in a reconstructed image taken by their sensor, giving approximately 120dB, but once again, no clear data is given.

Naomi Rousseau's thesis

Finally, a pixel has been proposed in 2017 by Noami Rousseau [31]. It was based on the DVS part of the DAVIS architecture. It aimed at introducing this DVS in the low power CAMEL vision sensor developed at UCLouvain [34]. It thus had to satisfy the voltage requirements of the system, 0.75V and its technology 0.18μ CMOS. It ended with a simulated pixel with a pitch of $17\mu m$ giving a contrast sensitivity of 7%. She achieved reducing the power down to 21nW without activity while keeping the FPN around 3%. However it was at the cost an increased latency of the pixel. She has also proposed another metric to quantifiy the power consumption of the pixel independently of the event rate: the energy/pixel/event.

1.2.4 Summary

As this state-of-the-art of existing pixel architecture has shown, there has been almost no target optimization on both area and power. Besides, the scaling of the technology is almost not used in the DVS design as almost proposed pixels are using at least 0.18 μ CMOS technology. The aim of this work will thus to analyze the feasibility of such optimization in a more advanced 65nm CMOS technology. Main performances of existing pixels are summarized in Tab. 1.1 for an upcoming comparison.

It is to be noticed that since the energy/pixel/event has been introduced in very recent work, it should be extracted from the given data, if available. If the power consumption is known for a given event rate, it is estimated as $\frac{P_{tot}}{N_{pixel} \cdot E_{rate}}$ where P_{tot} is the total power consumption of the chip at the given event rate E_{rate} and N_{pixel} the number of pixel in the chip. If the power per pixel is mentioned at an known event rate, it is directly divided by the later to get the energy/pixel/event.

	Rousseau 2017 [31]	Samsung 2017[7]	DAVIS 2014	ATIS 2011 [28]	Barranco *et. al* 2013 [33]	Barranco *et. al* 2011 [32]	Lichtsteiner 2008 [17]
Fonction	DVS	DVS	DVS+APS	DVS+exp. meas.	DVS	DVS	DVS
CMOS Technology	0.18μm CIS	90nm 1P5M BSI CIS	0.18μm 1P6M MiM CIS	0.18μm 1P6M MiM CIS	0.35μm 4M2P	0.35μm 4M2P	0.35μm 4M2P
Chip (mm^2)	N.A.	8x5.8	5x5	9.9x8.2	4.9x4.9	5.5x5.6	6x6.3
Array	480x320	640x480	240x180	304x240	128x128	128x128	128x128
Pixel area (μm^2)	21x21	9x9	18.5x18.5	30x30	30x31	35x35	40x40
Fill factor (%)	10	≈100 (BSI)	22	30	10.5	8.7	8.1
Pixel complexity	50T 1PD 2C	N.A.	47T 3C 1PD	77T 3C 2PD	N.A.	N.A.	26T 3C 1PD
Supply (V)	0.75	2.8	3.3 (1.8 digital)	3.3 (1.8 digital)	3.3	3.3	3.3
Total power (mW)							24
High activity	>27.34	50	14	175	95 20Meps	231	N.A.
Low activity	>6.5	27	5	N.A.	4 100kep	132	N.A.
Static	>3.15	N.A.	N.A.	50	2.6 1keps	N.A	N.A
Power/pixel (μW)							1.46
High activity	0.18	0.16	0.324	2.4	5.8	8.85 1Meps	N.A
Low activity	0.043	0.088	0.116	0.685	0.24	N.A.	N.A
No activity	0.021	N.A	N.A	N.A.	0.158	N.A.	N.A
Energy/pixel/event (fJ)	721.4	879 (calc.)	N.A	N.A	2440 (calc.)	8850 (calc.)	N.A.
DR (dB)	140	120 (est.)	130 (DVS)	125	120	>100	120
Contrast sensitivity (%)	7	9	11	max 30	1.5	10	15
FPN (%)	2.78	N.A.	3.5	0.25	0.9	4	2.1
Latency min. 1klux (μs)	45	N.A	3	<4	<9	<11	15

Table 1.1: Performances summary from state-of-the-art

1.3 CMOS photodiodes

CMOS photodiodes are semiconductor devices that are sensitive to high energy particles or photon. They aim at transducing the received input energy into an electrical signal. But before going deeper into the details of their functioning, a brief recall of the light metrics is proposed.

1.3.1 Introduction to radiometric and photometric systems

Measuring light characteristics has always been a puzzle for scientists. Indeed, two approaches have been developed: photometric and radiometric.

The first one is based on the human eye spectral responsivity [35]. Indeed as the eye does not see all colors with the same efficiency, a system that fits the eye response have been created. However, the latter depends on many parameters such as light intensity, which is not very practical. This system has as units the lumen (lm) for luminous flux, the lumen per steradians or candela (cd) for the luminous intensity and the lux (lx) for the illuminance.

The radiometric system is based on the spectral determination of light intensity. It results in a more traditional units system composed of watts for the radiant power, watt per steradians for the radiant flux and watts per meter square for the irradiance. Generally speaking, it is possible to consider any photometric system as a radiometric system on which a filter modelling the spectral eye response has been applied [8].

To convert photometric units into radiometric units, the spectral responsivity of the human eye must be modelled. It is done by the luminosity function, also called eye sensitivity function, which is a well known standard in optometry (joint CIE/ISO standard) [36]. As it differs from dark and bright illumination, two modes can be observed in Fig. 1.9: scotopic and photopic, respectively. As this function is given in relative efficiency (values from 0 to 1), using it as filter and then applying a correcting factor of 683 representing the lumen equivalence of 1 W at $\lambda = 550nm$ (at luminosity function=1) gives a converting method between radiometric and photometric systems.

1.3.2 Photodiodes types and characterization

Photodiode are basically uncovered diode, or P-N junction. They provide a relationship between the received energy (photons) and the generated so-called photocurrent. Such behaviour comes from the photoelectric effect: when the light strikes the photodiode area, a part of the incident photons are absorbed and gives

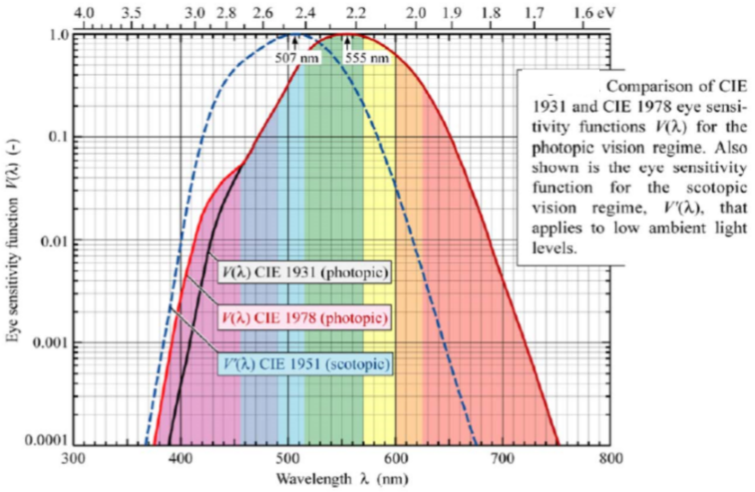

Figure 1.9: Luminosity function representing the spectral eye relative responsivity in photopic and scotopic mode [8]

energy to the carriers (electrons or holes). If this energy is sufficiently high, the carrier jumps from the valence band (where it is "bound" to its atom nucleus) to a conduction band (where it can freely move). Photodiode uses such phenomenon with the implementation given in Fig. 1.10.

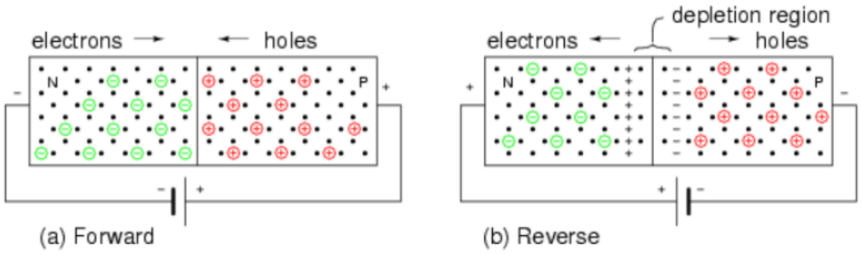

Figure 1.10: Model of a P-N junction implementation in forward and reverse biasing configurations [9]

A photodiode is nothing more than a reverse biased junction made of an N-type semiconductor, the cathode, doped with negative charges placed next to the anode, a P-type semiconductor (doped with positive charges, holes). The contact between oppositely doped parts leads to electron-hole pairs (EHP) generation due to the diffusion of the electrons and holes, hence delimiting a region where there is no more free carrier, the depletion zone. So when the photons give enough energy to a carrier in the depletion zone, and as the junction is reverse biased, the electrons

are drifted toward the anode and the holes towards the cathode, hence generating a photocurrent. Its I-V characteristics is given in Fig. 1.11 [10].

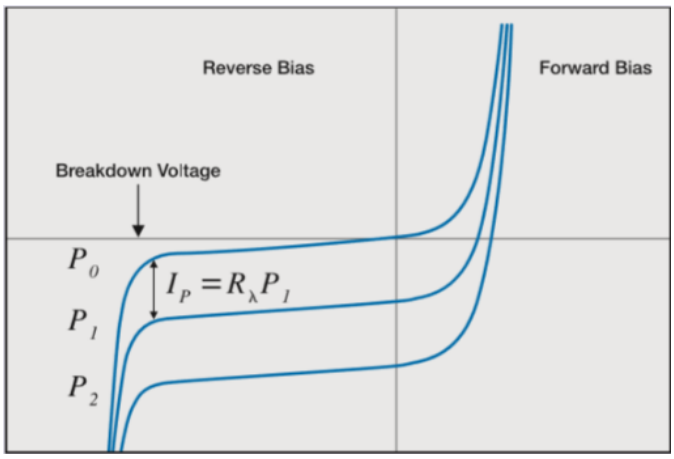

Figure 1.11: I-V characteristic of a photodiode, from [10]

As shown in Fig. 1.12, there are different manners to build such P-N junctions in CMOS but three are most common: N-plus/P-sub, N-well/P-sub or P-plus/N-well/P-sub [11]. It is to be noticed that the last one is only made of two P-N junctions put in parallel.

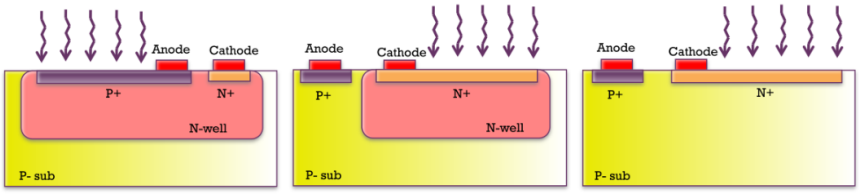

Figure 1.12: Different implementations of photodiode in CMOS technology from [11]

Experimental characterizations of such type pf photodiodes have been lead previously by Köklü in UMC 0.18μm CMOS [11]. He has studied the spectral responsivity of these photodiodes. They designed their layout and have applied a salicide blocking layer on each photodiode to avoid performance degradation due to opacity of the salicide layer, which will be discussed in Chapter 2. To do so he built simple APS with each kind of tested photodiode. His measurements were thus

voltage based (the output of the APS), and from them he was able to compute the responsivity of each photodiode in the current domain, given in Fig. 1.13.

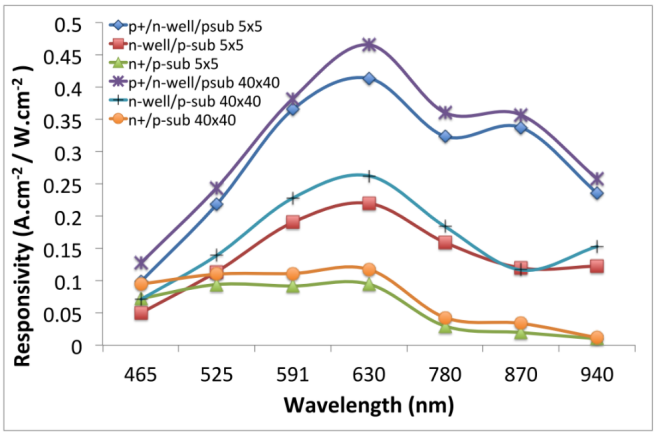

Figure 1.13: Responsivity obtained by Köklü in UMC 0.18μm for different types of photodiode [11]

Chapter 2

Experimental analysis of CMOS photodiodes

Contents

In this chapter, an experimental analysis of four different photodiode is conducted. Each layout is firstly explained and the experimental set up is described. The obtained results are finally shown and processed to be compared to former results from literature.

2.1 Photodiodes layout

As seen in Chapter 1, there are three main types of photodiodes: N-plus/P-sub, N-well/P-sub and P-plus/N-well/P-sub. All of them will be designed and measured. However, four types of photodiodes are studied in this work. It comes from the fact in scaled technologies, salicide (**s**elf-**al**igned sil**icide**) process is used to reduce the resistance of the junctions or poly-gate contacts, see Fig. 2.1 [12].

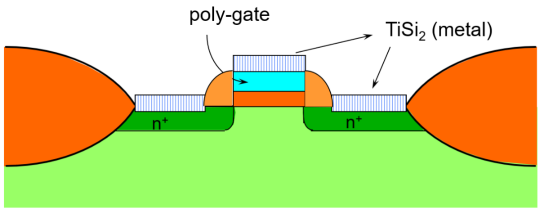

Figure 2.1: Example of salicide process using titanium, from [12]

In our case, the whole photodiode is made of a P-N junction (like a contact) and should thus, from a fabrication process point of view, be "improved" by the salicides, yet there is no absolute need for such process in the case of a photodiode. The latter are thus generally protected from this extra salicide process by a "salicide block" (SAB) layer added in the design. The purpose of the fourth tested photodiode is to determine what is the impact (if there is one) of salicide process on the photodiode responsivity. The N-plus/P-sub photodiode is thus tested with and without the SAB layer.

Each photodiode has been design to respect all process requirements. These are for instance the minimum metal, polysilicon or diffusion density. If they are not considered or manually handled, the manufacturer may add dummies: small block randomly placed on the layout, to respect the minimum density. As the photodiode must stay uncovered, dummy-block layers have been added above the pixel.

The final layout of each photodiode is presented in Fig. 2.2 and 2.3. All active areas (N-plus area for the N-plus/P-sub diode and the N-well area for the others) are $3\mu m$ long and 1.5 μm wide. Arrays of 40 x 100 pixels with a pitch of $4\mu m$ are then built from a mirrored version of the presented layout to facilitate the wiring. A micrograph of the chip used for the measurements is shown in Fig. 2.4.

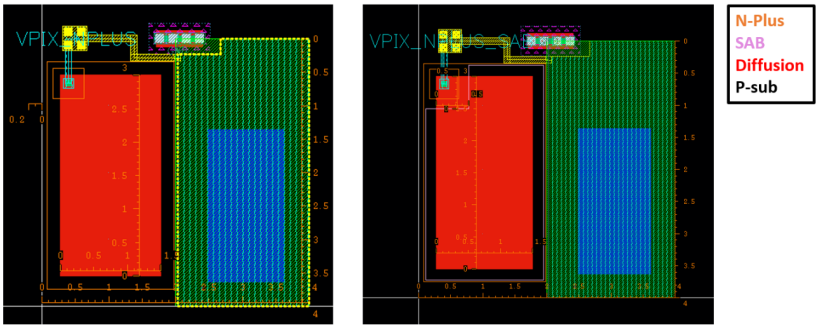

Figure 2.2: Implemented layout of the N-plus/P-sub photodiodes (with SAB layer on the right)

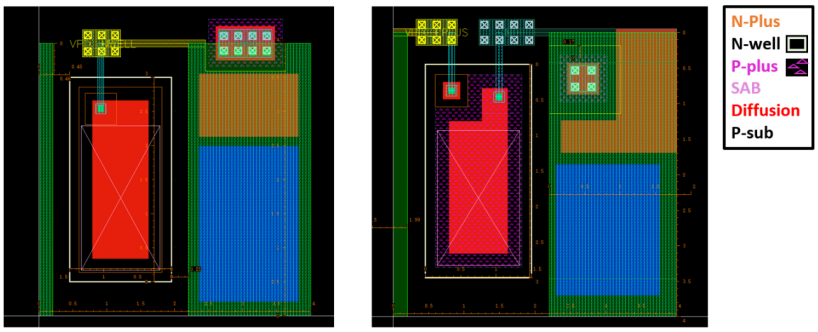

Figure 2.3: Implemented layout of N-well/P-sub (on the right) and P-plus/N-well/P-sub (on the left) photodiodes

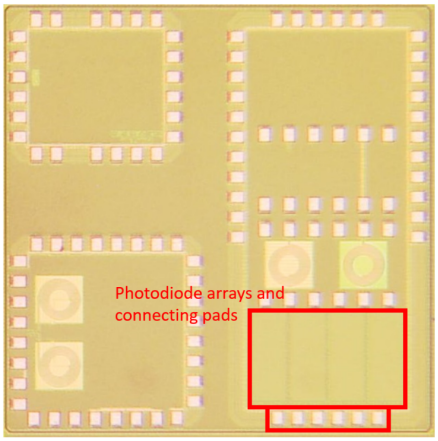

Figure 2.4: Micrograph of the chip containing the four photodiodes arrays used for the measurements

2.2 Experimental set-up

The experimental characterization aims at determining the spectral responsivity of each photodiode. To do so, they are illuminated with a monochromator that isolates a few wavelengths of the light spectrum from a white light source. As it uses prisms and adjustable mirrors to do so, the irradiance is neither constant over the light spectrum, neither tunable. So it must be measured to get a precise input value, key element to finally extract the responsivity of the diode. The complete set-up is presented in Fig. 2.5.

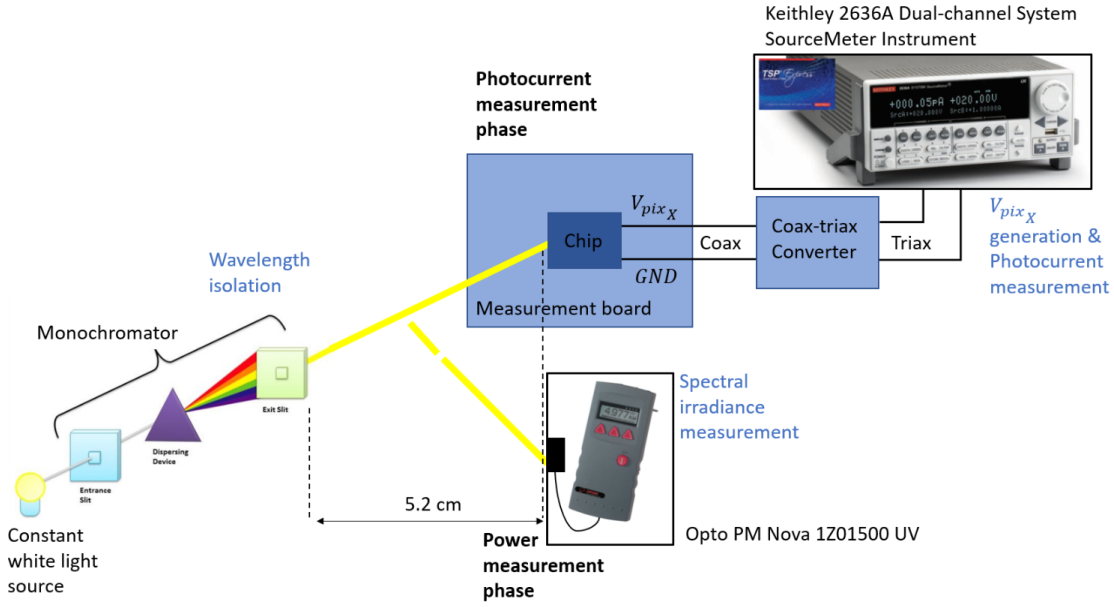

Figure 2.5: Experimental set-up used for the photodiodes characterization

Measurements of input irradiance is done using an Opto PM Nova 1Z01500 UV which gives the power intensity in watt for a given wavelength. A cover is applied to precisely determine the illuminated surface. The input irradiance for each wavelength can finally be computed as P_{meas}/A_{cover}.

The output current measurements is more sensitive to the choice of the instrumentation since the expected current value is small. Indeed, if the responsivity is similar to the one obtained in UMC 0.18μ [11], Eq. 2.1 gives the estimated photocurrent generated by each array.

$$I_{ph} \approx N_{pd} \cdot A_{pd} \cdot R_{UMC0.18\mu} \cdot E_{e,in} \tag{2.1}$$

Where N_{pd} is the number of photodiodes per array, A_{pd} the active area per photodiode [μm^2], $R_{UMC0.18\mu}$ the extracted responsivity [$\frac{A}{W}$] from [11], and $E_{e,in}$ [$W/\mu m^2$] the expected input irradiance. It gives a photocurrent to detect from approximately 100pA to 1nA when the chip is illuminated. In the dark, the SNR given by [11] leads to a current in the pA range of value. So co-axial and tri-axial cables connects the chip to the ammeter (Keithley 2636A Dual-channel System SourceMeter Instrument (1fA, 10A Pulse)) to reduce noisy signals in the measurements. Finally, to get more representative results, the same measurements have been realized on 10 chips.

2.3 Results, post-processing and discussion

This section will be dedicated to the presentation and analysis of the experimental results. Spectral responsivity is firstly extracted from measurements, then processed to be expressed in lux per watt. The dark current is also measured, and reliability of these results is discussed.

2.3.1 Responsivity

Spectral responsivity is computed from two measured values. The input irradiance [W/μm^2] and the output current. The photodiode is here reverse-biased with a 0.1V voltage. The responsivity is calculated in Eq. 2.2 for each wavelength, hence giving the spectral responsivity of the photodiode.

$$R_{meas} = \frac{I_{ph_{meas}}}{A_{tot}} \cdot \frac{1}{E_{e,in_{meas}}} \tag{2.2}$$

Where A_{tot} is the total active area in one array ($= 4000 \cdot 3\mu m$ x $1.5\mu m = 18000\mu m^2$). The average spectral responsivity of each photodiode is then presented in Fig. 2.6. It gives responsivities of similar amplitude than in [11], which is a promising outcome for this technology. However, a notch can be seen at a wavelength of 550nm (green). As the eye is more sensitive to this range of color, it might be problematic as the purpose of the final pixel is to mimic the eye behavior. It is to be noticed too that this notch is not present in Köklü's results but it might come from the fact that measurements have not been done at the exact same wavelengths. If this notch is located on a few wavelengths only, it might not have been detected by previous experimentation. Physically speaking, the notch possibly comes from optical phenomenons due to the stacking of layers around the photodiode, giving a spectral responsivity which is not flat over the visible range. Another explanation is the spectral response of the manufactured silicon itself.

Another interesting result is the poorer responsivity of the N-plus/P-sub photodiode without the SAB layer. If the difference is not significant at every wavelength, it is always less good than the same photodiode covered with the SAB. It thus experimentally confirms the expected behaviour predicted in [11].

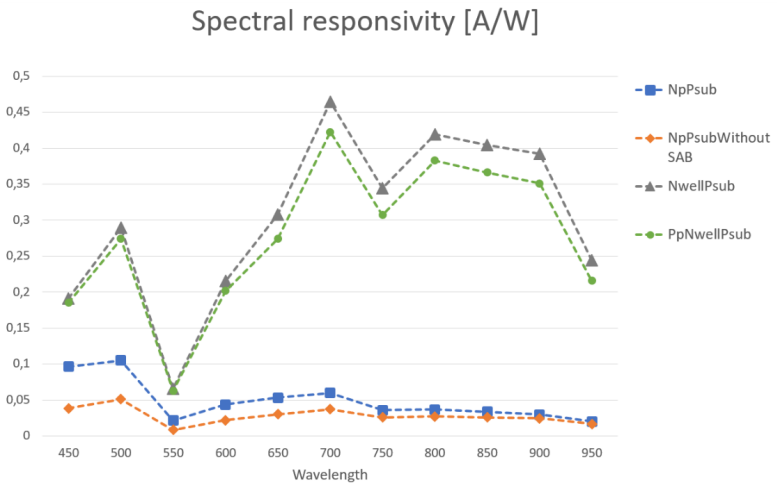

Figure 2.6: Extracted spectral responsivity of each photodiode from experimental measurement of photocurrent

If this spectral responsivity is very useful to characterize the photodiode behavior, it is not application related. As seen in Chapter 1, the luminosity function is used as a filter, giving the responsivity shown in Fig. 2.7. Finally, this responsivity function has to be integrated over the light spectrum to get the responsivity of the photodiode under a white light. It has been done using a classical trapezoidal rule, results are summarized in Tab. 2.1.

Photodiode type	Responsivity $[\frac{fA}{\mu m^2\, lux}]$
N-plus/P-sub	7.26
N-plus/P-sub without SAB	3.43
N-well/P-sub	25.7
P-plus/N-well/P-sub	24.2

Table 2.1: Integrated responsivities of the four tested photodiodes under a white light illumination

These final results shows the best responsivity of the N-well photodiode, which will thus be best suited for the coming pixel design.

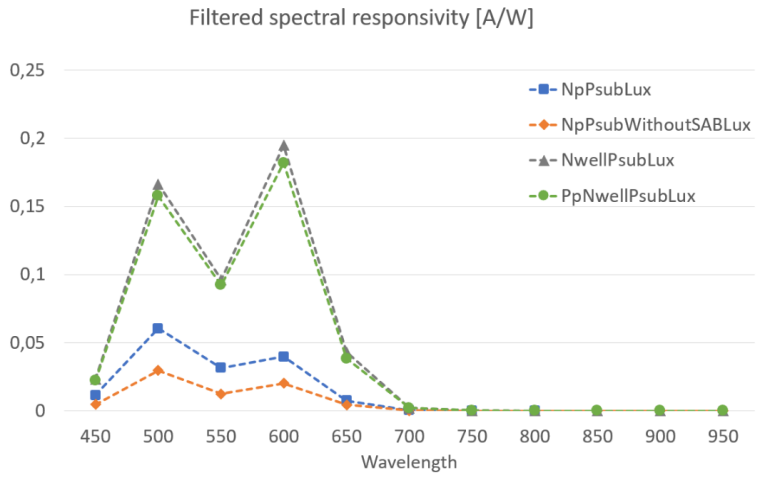

Figure 2.7: Filtered spectral responsivity using the luminosity function

2.3.2 Dark current

Dark current is an unwanted current that flows through the photodiode when it is not illuminated. It is an important parameter to determine in the case of a vision sensor since it defines the minimum current to be detected by the device. It is thus measured for each types of photodiodes at room temperature. But since the dark current value were close to the resolution of the ammeter, the measured values were a bit unstable and have been approximated.

To go further, the influence on the dark current of the applied reverse biasing voltage of the photodiode V_{pd} is analyzed. It is even more meaningful in this case since this biasing voltage is one of the tunable parameters in the pixel design (see Section 3.2). Results are presented in Fig. 2.8.

These measurements reveal a exponential behaviour. However, at low reverse bias voltage, the photocurrent should evolve almost linearly. After investigations, it appeared that the pad which connects the photodiodes array and the external pin was equipped with ElectroStatic Discharges (ESD) protection. It means that there were two diodes connected to the reverse bias voltage V_{pix}, one towards the supply voltage of the chip, the other from the ground. As the chip did not seemed to be supplied during the measurements since only V_{pix} and the ground were connected, the ESD protecting diode between V_{pix} and the floating supply node was conducting, hence providing the measured exponential current. A post layout simulation with the N-well photodiodes array and its V_{pix} I/O pad has been done to confirm this explanation and its result is shown in Fig. 2.9.

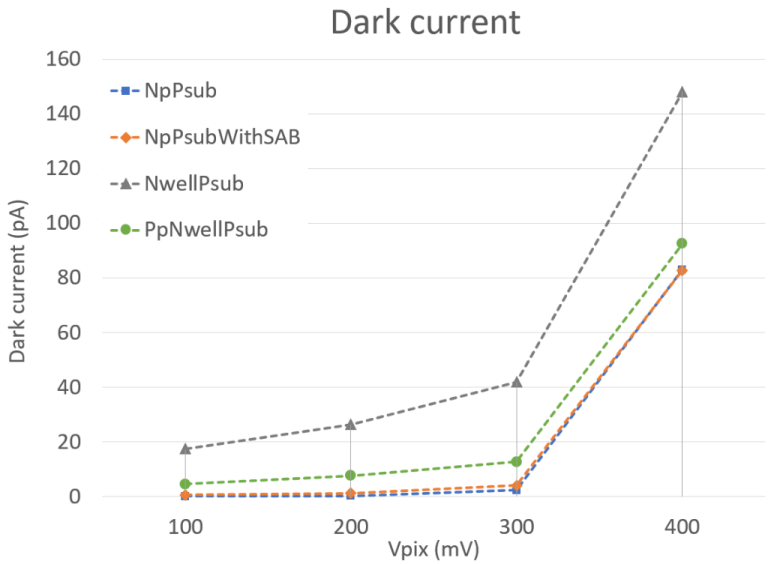

Figure 2.8: Measured dark current for different V_{pd} at room temperature

If this simulation confirms the origin of the measured exponential behavior, it also gives a lower dark current value around 0.5fA/photodiode. But as the configuration with a floating supply voltage was impossible to simulate because of convergence problems, the simulated values might not accurately represent the measurements conditions.

2.4 Summary

In this chapter, an experimental analysis of different types of photodiodes has been presented. From the experimental set-up to the final results comparison, it has met is expectation, namely the characterization of 65nm CMOS photodiode. The N-well/P-sub ends up with the best responsivity at 25.7 $\frac{fA}{\mu m^2 lux}$ and is the kept for the pixel design. The value of the added SAB layer has been proven as well. Finally, for the chosen photodiode, a total dark current 26.5pA is measured at a reverse bias voltage of 0.2V. Even though this value's uncertainty, previously discussed, it is taken as a starting point for the design of the pixel.

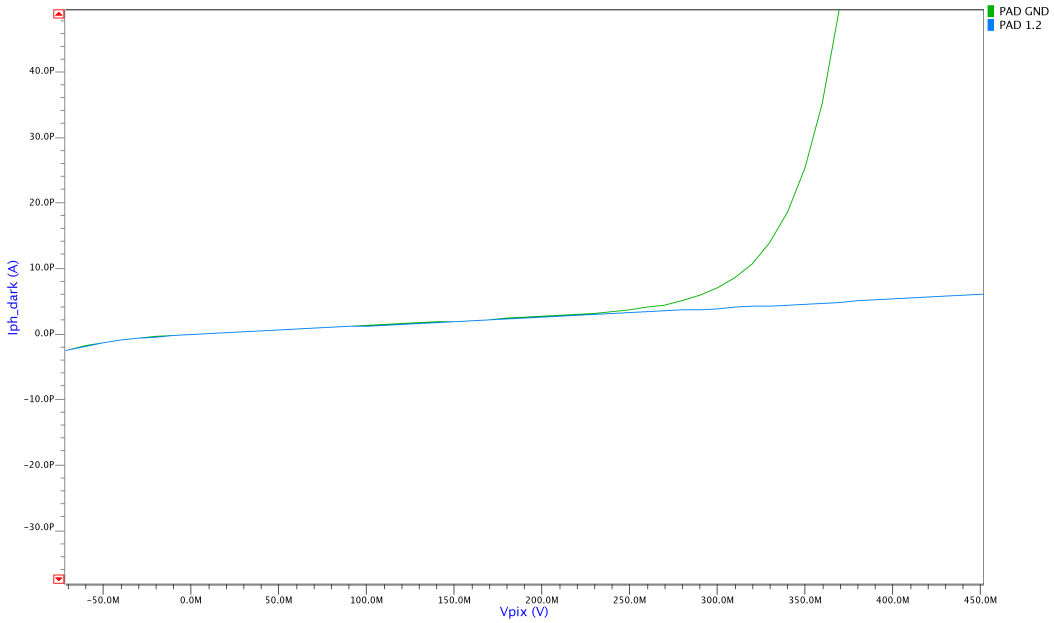

Figure 2.9: Simulated dark current at room temperature in function of the reverse bias voltage with the pad supply grounded (green) or at its nominal value of 1.2V (blue)

Chapter 3

Pixel design

Contents

This chapter is devoted to the design of the pixel, starting from its global architecture, then flowing through its composing blocks to design each of them for the target technology and optimization. The design of each part is discussed with regard to the performances and the encountered trade-offs are introduced. Since the proposed methodology is based on simulations in UMC 65nm, it might not be optimal for other technologies and should probably be adapted to fit another one.

3.1 Global architecture

The architecture used in this master thesis is adapted from the dynamic vision sensor of the DAVIS pixel. It pushes boundaries of work previously done in the thesis of Naomi Rousseau [31] to a more advanced technology, namely the UMC 65nm CMOS. This work is thus not focused on the architecture choice itself but well on its optimization. Hence, the studied architecture, from [31], is recalled in Fig.3.1.

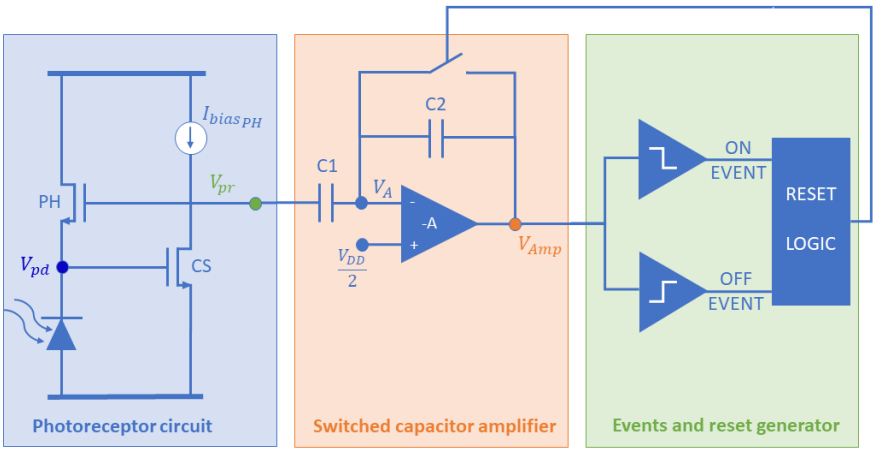

Figure 3.1: Pixel architecture studied in this work

It is composed of three main parts:

- **The photoreceptor circuit**, aiming at transducing the input light intensity into voltage.
- **The switched-capacitors amplifier (SCA)**, amplifying the produced voltage around the reset value.
- **The events and reset generator**, composed of two comparators and several logic gates to generate ON and OFF events as well as reset signals when the upper or lower threshold is reached.

It works as follows: the photodiode generates a photocurrent proportional to the input light intensity, it is then logarithmically converted into voltage. The latter is amplified by the SCA and compared to upper and lower threshold voltages. If the contrast sensitivity is reached, the corresponding event is sent and the reset of the SCA is done. This principle is illustrated in Fig. 3.2.

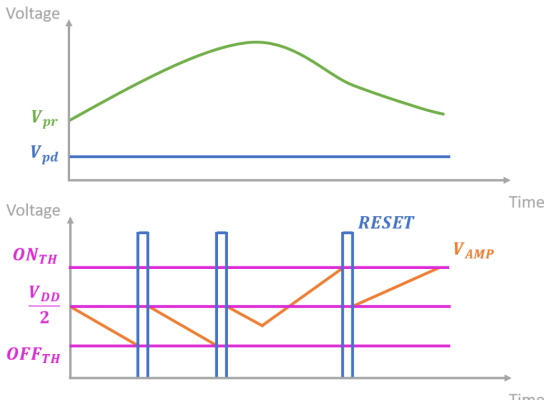

Figure 3.2: Working principle of the pixel

As it has already been mentioned, the purpose of this study is to optimize this architecture for the UMC 65nm technology. If the power and area will obviously be optimized in this work, other specifications are set to guide the design of the pixel.

- The contrast sensitivity is set at 10% avoid a too high event generation rate while being able to precisely track the movements.
- Minimum latency has to be minimized as much as possible, keeping in mind that it is not the main purpose of this study. Hence, latency may be degraded in favor of a better power optimization for instance!

The following sections go deeper into the details of implementation of each block, highlighting the major issues and their solutions in the design.

3.2 Photoreceptor circuit

The photoreceptor circuit aims at performing the conversion of the received light intensity into the photoreceptor voltage V_{pr}, output of this first stage. This conversion is done in two steps as represented in Fig. 3.3.

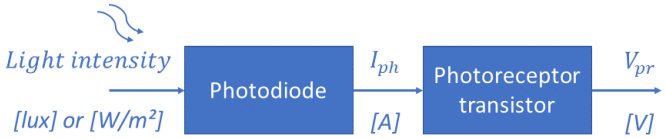

Figure 3.3: Schematic transduction processed in the photoreceptor circuit

The first transduction of light intensity into current is realized through the photodiode: photons are absorbed in the active area and generate a current, because of the electron-hole pair generation. As shown in Fig. 3.4, this photocurrent flows through **photoreceptor (PH) transistor** which logarithmically converts it into the output voltage V_{pr}, completing the second transduction. A few transistors are needed to bias both transducers. The **common-source (CS) transistor** produces the photodiode voltage V_{pd} which keeps the photodiode biased. The bias current of the CS transistor is provided by a current mirror, hence setting V_{pd} at the needed value.

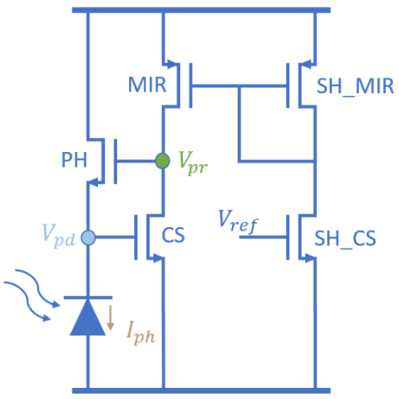

Figure 3.4: Photoreceptor circuit

The following elements are the most critical to optimize the area and the power consumption of the block:

- Photodiode area
- Photoreceptor transistor size
- Bias current
- Supply voltage

Reducing the photodiode area may seem obvious but it is not without consequences. It leads to a loss in generated current meaning that problems occur when the second transduction takes place since a bigger transistor is needed to sense the photocurrent. The two last items must be reduced as much as possible to fulfill the power optimization requirements of this work but must be kept high enough to ensure functionality of other blocks too !

A methodology is thus proposed to optimize both area and power consumption in the design of the photoreceptor circuit. Such methodology is valuable in scaled-down technologies because it takes into account the effects of reduced size. These induce variations in the classical model of transistors that cannot be processed "by hand". The following methodology thus results from analysis of simulation results that will not be shown in their entirety, but from which it had been possible to extract influences between parameters.

To build this methodology, an analysis of the different components has been done and their key parameters in the wanted optimization have been extracted.

3.2.1 Photodiode

The main purpose of the photodiode is to generate the photocurrent. There are two main parameters that play a role in the target performance: the type of photodiode and its area.

Type: As seen in Chapter 2, the different photodiodes (N-plus/P-sub, N-well/P-sub, P-plus/N-well/P-sub) give different responsivities and generate thus more or less photocurrent for a given input light intensity. In this work, the occupied area have to be minimized and the choice will thus be made for the photodiode that gives the best responsivity, namely the N-well/P-sub.

Area[1]**:** In one hand, current generated by the photodiode must be maximized in order to be able to detect it with the photoreceptor transistor. On the other hand, this current is directly proportional to the active area. Since the latter should be minimized, there is a conflict with the previous consideration. This is the key trade-off that has lead to the proposed methodology.

3.2.2 Photoreceptor transistor

As a reminder, the photoreceptor transistor is in charge of the logarithmic conversion of the photocurrent into the voltage V_{pr}. As it should detect the lowest current, it must operate in weak inversion and its current equation can be written as follows [37]:

$$I_D = \underbrace{2\mu(n-1)C_{ox}\frac{W}{L}U_T^2 e^{-\frac{V_{th}}{nU_T}}}_{I_{D0}} e^{\frac{V_{pr}}{nU_T}}(e^{-\frac{V_{pd}}{U_T}} - e^{-\frac{V_{DD}}{U_T}}) \tag{3.1}$$

Where I_{D0} is the characteristic current of the transistor representing its leakage, μ the mobility of the electron, n the body factor with typical value between 1 and 1.5[V/V], C_{ox} the gate oxide capacitance, W and L the width and length of the transistor, respectively, $U_T = kT/q$ the thermal voltage and V_{th} the threshold voltage.

In order to minimize the lowest detectable current (called I_{min} in the rest of this work), Equation 3.1 tells us that the threshold voltage and length of the transistor should be maximized and its width minimized. However, as detailed in

[1]It is to be remembered that the so-called "photodiode area" is not always the area occupied by the entire photodiode, but well the active area of the photodiode, namely the diffusion area for the N-plus/P-sub photodiode and the N-well area for the other types. This value might thus a bit underestimated compared to the area occupied by the photodiode in the layout!

Section 3.2.4, taking the minimum width of the transistor may not be the best choice to minimize the current, due to the scaling down of technology. Moreover, increasing the length is at the cost of an increased area and this action should thus be limited as much as possible to allow the optimization of the area. Finally, since the threshold voltage plays a role to decrease I_{min}, IO transistor is chosen instead of HVT or LVT, thus improving functionality at a lower cost in term of area.

Equation 3.1 gives another way to decrease I_{min}: reducing the difference between V_{pd} and V_{DD}. It can be done either by increasing the photodiode voltage, either by reducing the supply voltage, which comes with the other advantage of a lower power consumption.

3.2.3 CS transistor and bias point

As previously said, the CS transistor is used to set the voltage V_{pd}. As the latter has to be increased while keeping the area and power optimization in mind, the use of an HVT transistor is chosen. It allows to increase the gate voltage V_{pd} (thanks to the higher threshold voltage) while keeping a smaller area compared to the IO transistor, and a smaller current compared to the LVT transistor.

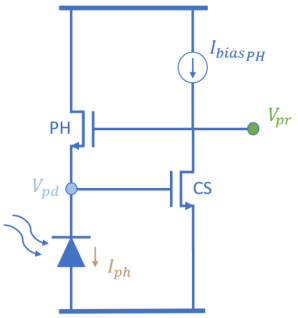

Figure 3.5: Simplified photoreceptor circuit

At first, the biasing point is set to keep the functionality under any conditions and the bias current is provided by a current source. Hence, at the highest temperature and with the FF corner, it is possible to determine the optimal size of the CS transistor using the circuit shown in Fig. 3.5.

At a later stage, the biasing current source is replaced by a current mirror, itself driven by a voltage controlled current source. One shared branch (prefix SH in Fig. 3.4), identical to photoreceptor biasing branch of each pixel, is used in mirror to provide the biasing current for each pixel.

3.2.4 Proposed methodology

As previously said, the proposed methodology, presented in Fig. 3.6, results from the analysis of several simulation results. It follows steps that have been thought to optimize area and power consumption while ensuring the functionality of the system under any conditions.

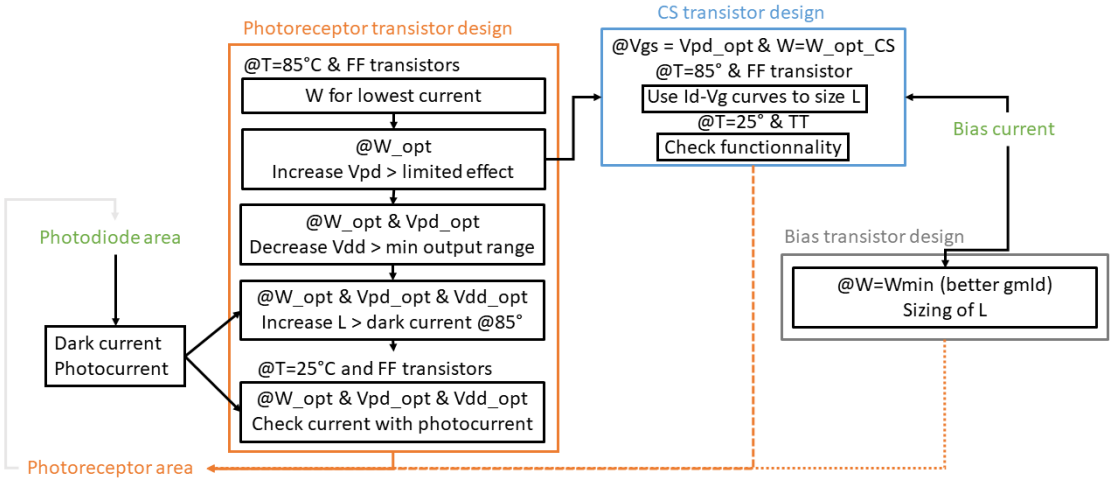

Figure 3.6: Proposed methodology for the area and power consumption optimization of the photoreceptor circuit

This method starts from a few choices: the photodiode area and the bias current. These choices allow to extract the needed parameters for the design, these are the size of all transistors, the supply voltage V_{DD} and V_{pd} the voltage across the photodiode.

From a first guess for the photodiode area, the corresponding lowest photocurrent to be detected is extracted. As it sets the target operating limit, the design of the photoreceptor, which is the most critical trade-off in the design of this first block, can begin. Several simulations are thus performed to successively size each parameter. The photodiode is modelled by an ideal current source with the actual N-well/P-sub diode wired in parallel. All the following figures show the results of the last loop of the design, which begins, after trials and errors, with a chosen area of $4.5\mu m^2$.

Photoreceptor transistor design

To design this first transistor, all simulations have been done using ideal voltage sources at each node.

At first, V_{pd} and V_{dd} are set at 0.1 and 1.8V, respectively. These values are the minimum and maximum values they can take because of the photodiode minimum bias voltage and the choice of the IO transistor (providing the higher threshold

voltage). No optimization on these parameters has been down at this step. As the device has to be operating properly under any conditions, the conditions are set at worst. The FF corner and the highest temperature increase the value of the minimum current detectable by the transistor and are thus chosen for these first simulations.

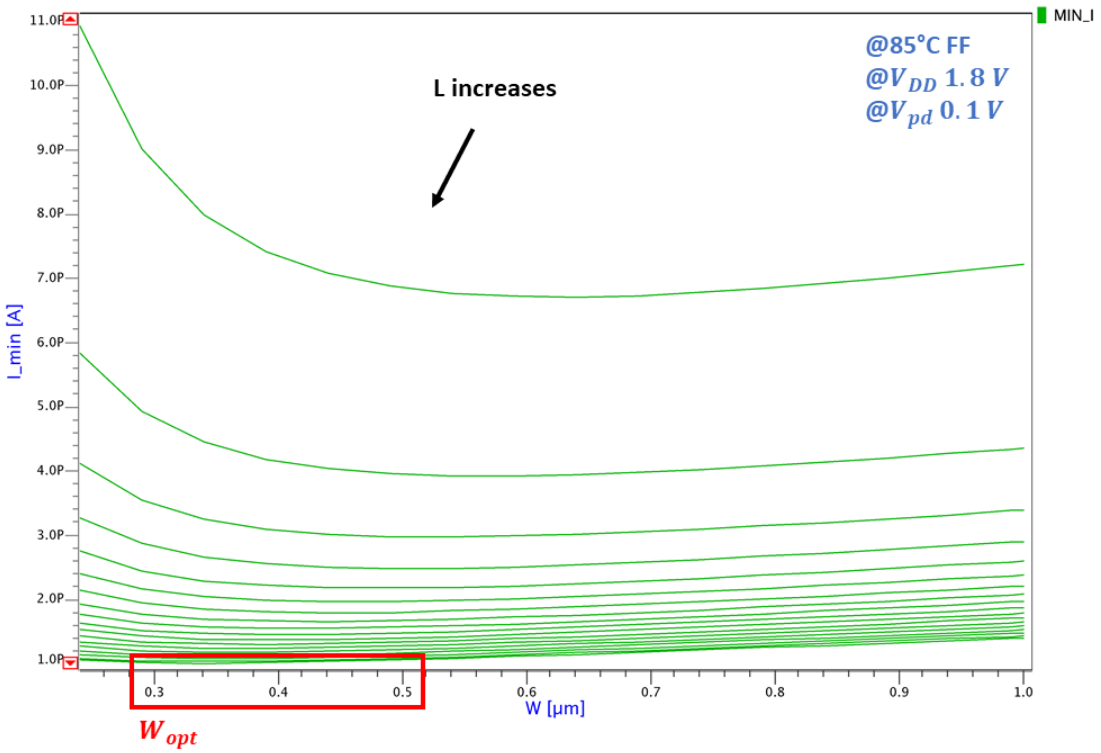

Figure 3.7: I_{min} in function of the width of the photoreceptor transistor for lengths from 240nm to 2μm, steps of 100nm

The variable parameters are the width and length of the photoreceptor transistor and the target is to extract the optimum width, i.e. the width for which the minimum current I_{min} is the lowest. Fig. 3.7 reveals that W_{opt} is between 0.3 and 0.5μm and a width of 0.3μm is chosen to optimize the area.

For the second simulation, same conditions are applied and the width of the photoreceptor transistor is set at W_{opt}, while V_{pd} values from 0.1 and 0.6V are tested, for different lengths. The optimum V_{pd} must ensure that I_{min} is below the the dark current at 85° (it guarantees the current detection under worst conditions). To know this value, dark current density of the photodiode is retrieved from the experimental data (see Chapter 2) giving 1.47fA/μm^2. Since the dark current

evolves with temperature, its behavior can be approximated such that it doubles every 10° of increase, which gives a current to detect of ≈ 424 fA at 85°.

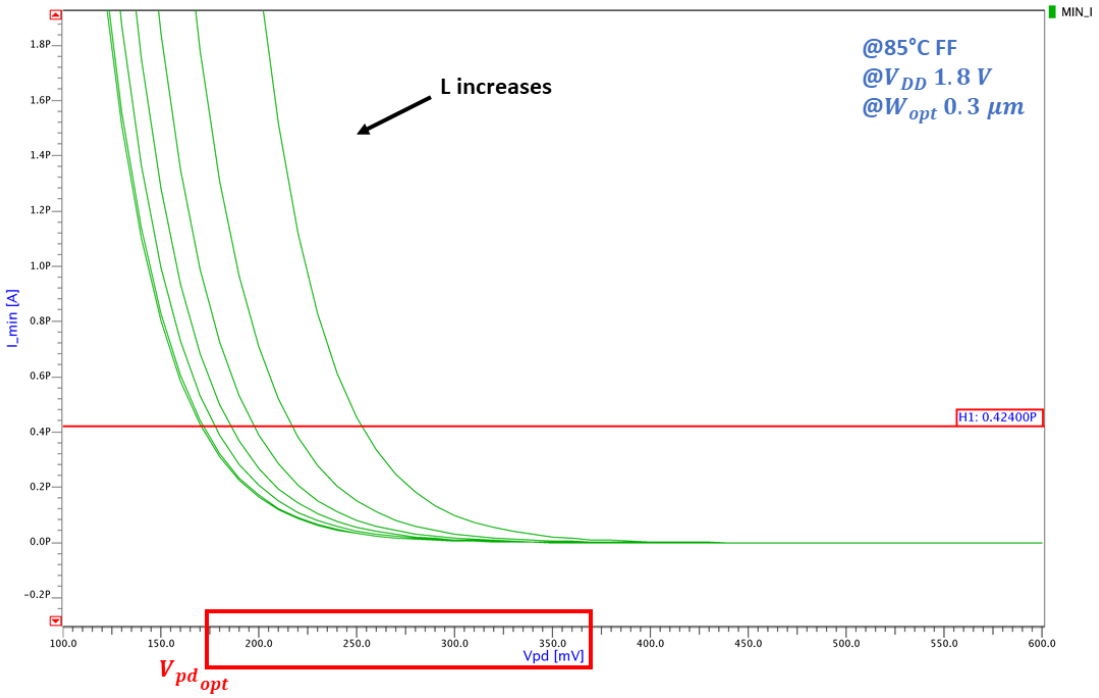

Figure 3.8: I_{min} in function of V_{pd} for different lengths (240nm to 2μm, steps 100nm) with the target minimum current highlighted (424fA)

As seen in Fig. 3.8, minimal value for V_{pd} is around 0.18V to detect the lowest current. Eventually, the choice has been made for $V_{pd_{opt}} = 0.25V$ to keep different possibilities to determine the length.

The third and fourth steps of the photoreceptor transistor design are done at the same time. Still keeping worst conditions and applying the optimal values for W and V_{pd}, variations on length and supply voltage are simulated.

Fig. 3.9 shows the low impact of V_{dd} on the functionality, but as the power consumption has to be optimized, supply voltage should be lowered as much as possible. The only lower limit is that the transistors must stay in their required operating mode, but also that this supply voltage has to satisfy the same condition for the other blocks too. Trials and errors results in a final value of 1V of supply. Length is then chosen to satisfy the minimum current value and a value of 240 nm is set.

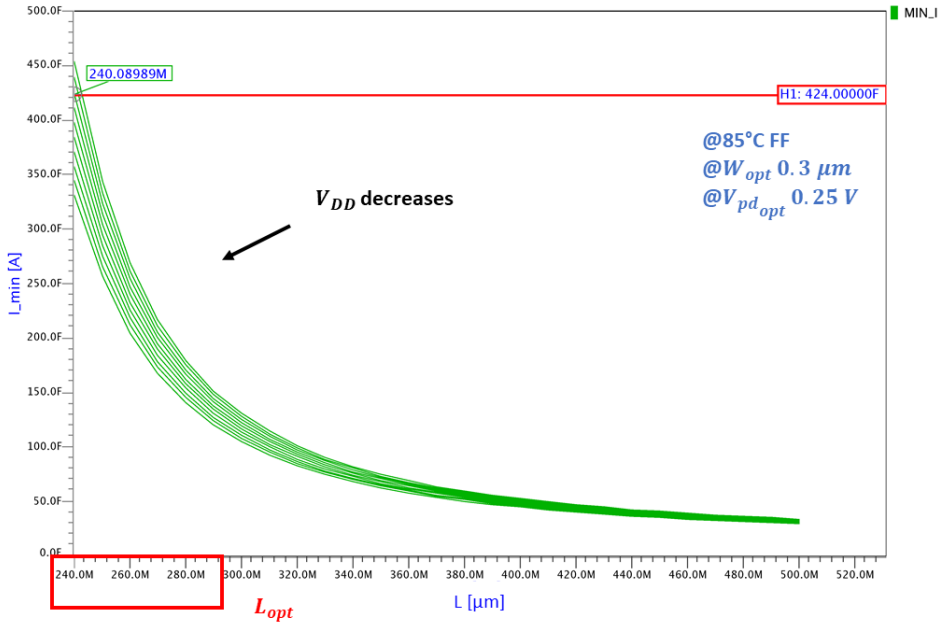

Figure 3.9: I_{min} in function of the length of the photoreceptor transistor for different V_{dd} (1.8 to 0.9V, steps of 0.1V) with the current target highlighted

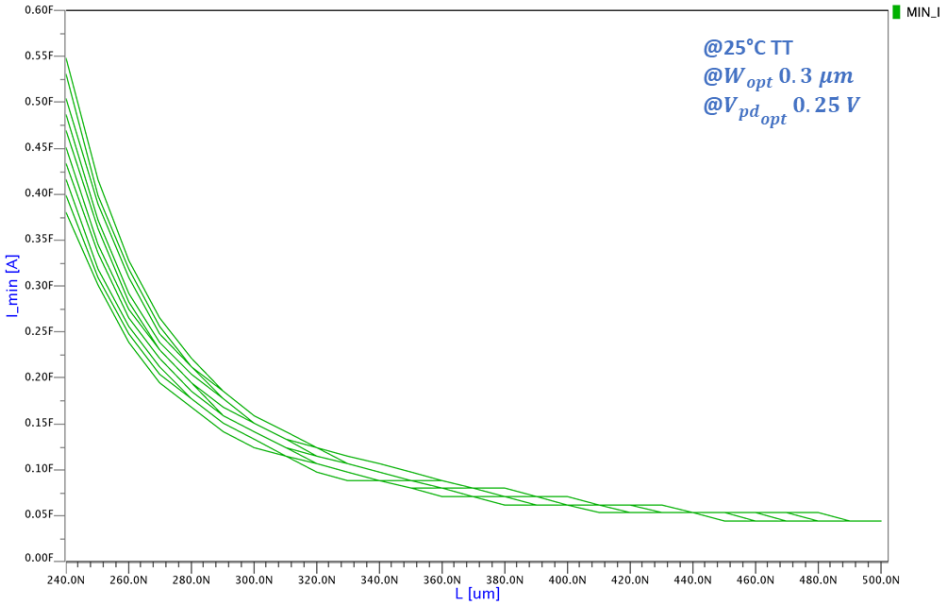

Figure 3.10: I_{min} in function of the length of the photoreceptor transistor for different V_{dd} (1.8 to 0.9V, steps of 0.1V) under typical conditions

The last step to design the photoreceptor transistor is to check under typical conditions if the requirements on the minimum current are met. The temperature is thus set at 25° and the transistor is set in TT mode for this last simulation. All the other parameters are set at their optimal values determined before. Fig. 3.10 proves that the minimal current detectable is significantly below the condition given by the dark current at 25°, 6.6 fA[2].

CS transistor design

The circuit used to size the CS transistor is a simplified version of the photoreceptor circuit previously shown in Fig. 3.5. Just as it has been done to size the photoreceptor transistor, the first step to design the common source transistor is to determine its optimal width for which the current is minimal. As the CS transistor is chosen to be an HVT device (reduced area), Fig. 3.11 shows that the result slightly differs from the IO transistor.

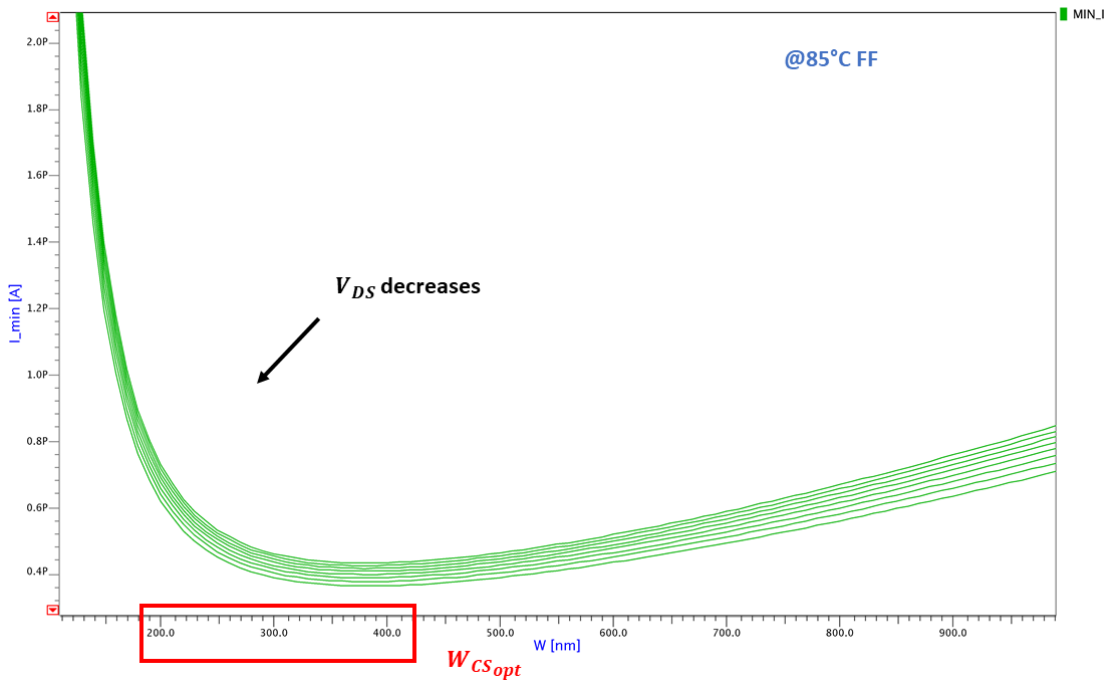

Figure 3.11: I_{min} in function of the width of the CS transistor under worst conditions

A width of 200nm is finally selected. Even if it is not at the optimum, it allows to reduce the size of the device while staying close to the minimum current.

[2]It is to be noticed that this value is also below the simulated dark current in Chapter 2, which comforts the photoreceptor design, despite uncertainty on the dark current measurements

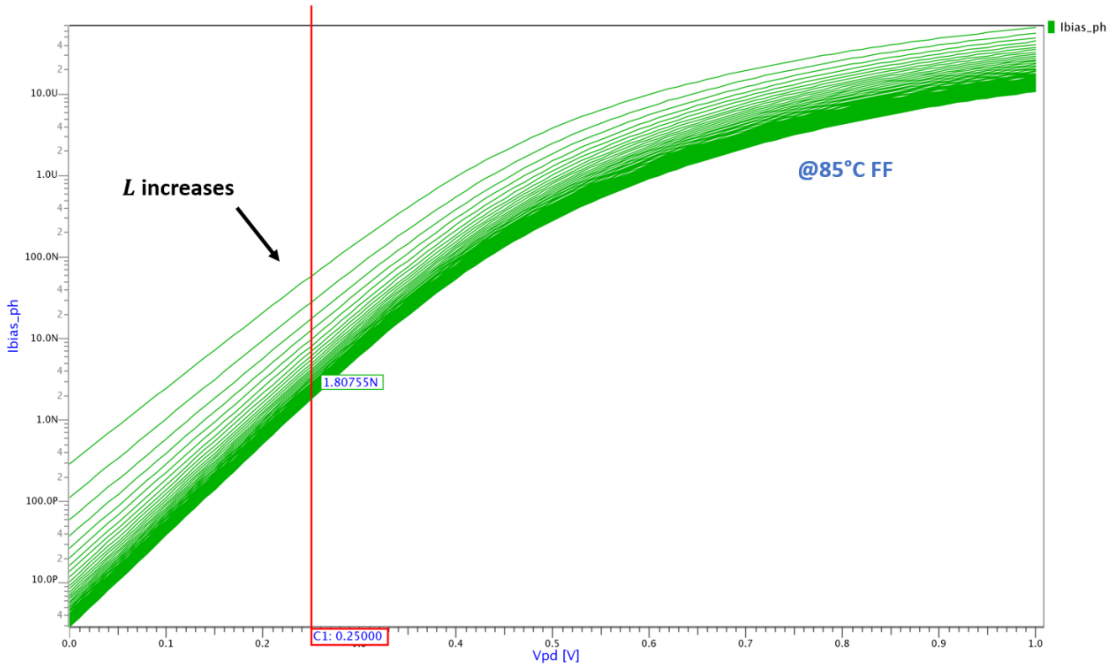

Figure 3.12: I-V curve of HVT transitor at 85° and FF transistor

Secondly, the I-V curve is used to determine both current biasing and length of the CS transistor, still under worst conditions. The wanted gate voltage is 0.25V and the simulation in Fig. 3.12 highlights the trade off between the size of transistor and the biasing current. As the length increases, the current needed decreases for a given gate voltage.

The final length of the CS transistor is set at 90nm and the biasing current at 1nA. It does not perfectly match the optimal value of 0.25V but it will be solved by changing the biasing circuit.

Biasing transistors

The bias current source is now implemented by a current mirror. In order to avoid too big corner variations, the shared biasing circuit is a copy of the branch in each pixel. Hence, the shared current source is voltage controlled and its reference voltage is set at $V_{pd_{opt}}$, there is thus no need to choose the bias current value anymore!

The current mirror is designed following the idea of the g_m over I_D ($g_m I_D$) method. The current mirror works better if a low $g_m I_D$ is chosen. To do so, the width of the transistor is reduced as much as possible, hence decreasing the $g_m I_D$

parameter and improving the quality of the current mirror. Then the length of the bias transistor should be increased to boost quality of the current mirror. However, the length is kept as small as possible to minimize the size of the transistor. It results in a 80nm-wide device and 250nm long.

Finally, the transfer function of the photoreceptor circuit is presented in Fig. 3.13 and the different component sizes are summarized in Tab. 3.1.

Photodiode	N-well/p-sub	$4.5\mu m^2$
PH transistor	IO	W=300nm L=240nm
CS transitors	Core HVT	W=200nm L=90nm
Bias transistors	Core LVT	W=80nm L=250nm

Table 3.1: Summary of photoreceptor circuit sizing

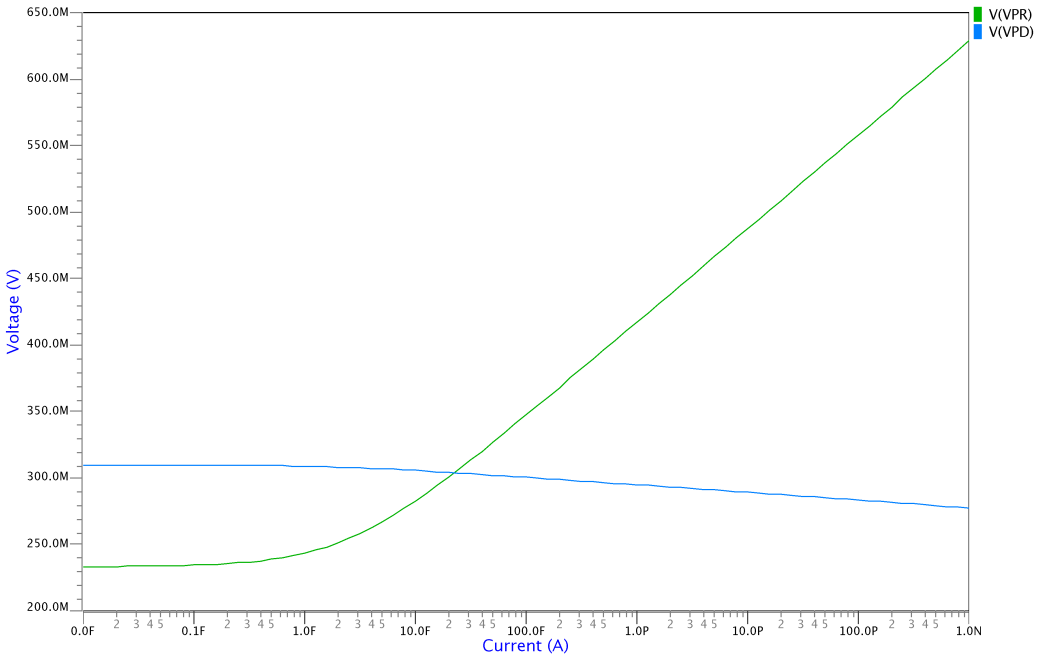

Figure 3.13: Transfer function of the full photoreceptor circuit under typical conditions

3.2.5 Corners and Monte-Carlo analysis

Now that the design of the circuit is done, its functionality over PVT corners and mismatch need to be checked. To do so, the criteria that ensure the functionality of the circuit are defined: limit of detection (LOD) and limit of functioning (LOF).

The LOD is defined as the illuminance at which the photoreceptor circuit begins to sense a change of light, LOF is the illuminance at which the photoreceptor begins to logarithmically convert the light intensity. Practically speaking, we compute the following derivative:

$$\frac{dV_{pr}}{d(\log I_{ph})} = \ln 10 \cdot I_{ph} \cdot \frac{dV_{pr}}{dI_{ph}}$$

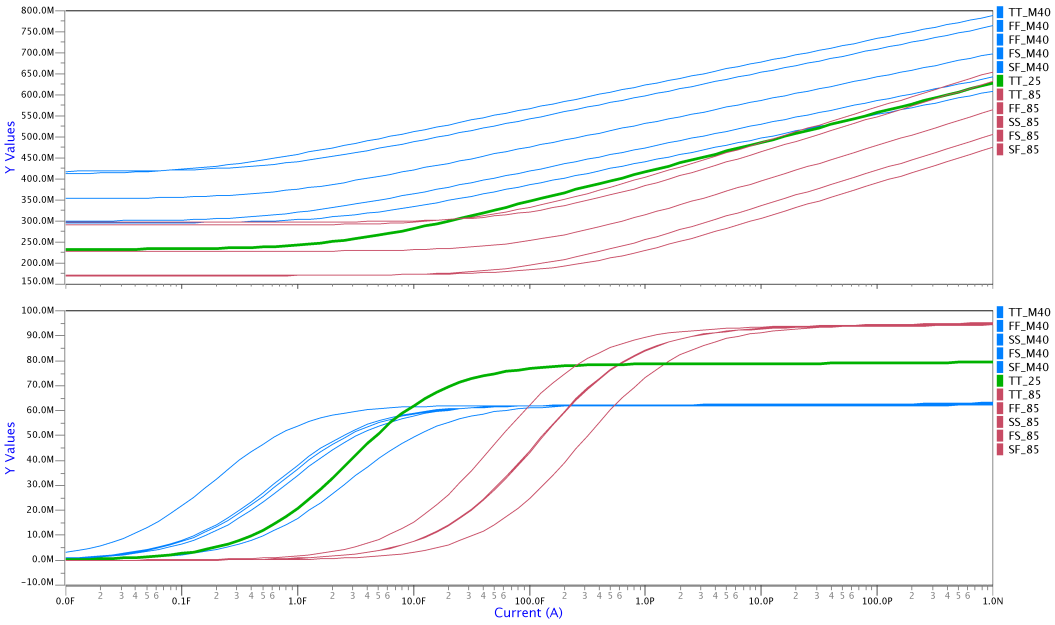

Figure 3.14: Corner analysis of the photoreceptor circuit transfer function (T=80° (red) and T=-40° (blue))

As shown in Fig. 3.14 representing the corner analysis of the transfer function, this derivative has two plateaus due to the two distinct slopes of the transfer function. The current corresponding to the LOD is then defined as the value of I_{ph} when the derivative is at 10% of its maximum value. Similarly, the current corresponding to the LOF is extracted when the derivative is equal to 90% of its maximal value. These definition allows to link the simulated results to application-related working

limits of the pixel studied in this master thesis.

From the corner analysis, worst LOD and LOF (FF 85°) are extracted at I_{ph} = 31.27 fA and 3.03 pA, which corresponds to 0.27 and 25.9 lux, respectively. It means that the photoreceptor circuit begins to detect a change of light intensity under a full moon night, while functioning totally normally in an illuminated street in the night.

A Monte-Carlo analysis is now done to check the robustness to mismatch. It is done in typical conditions (TT transistors and 25°) in Fig. 3.15 and 3.16. Two extreme corners (FF and 85°, SS and -40°) are also analyzed to check functionality in harsh conditions, their results are summarized in Tab. 3.2 and 3.3.

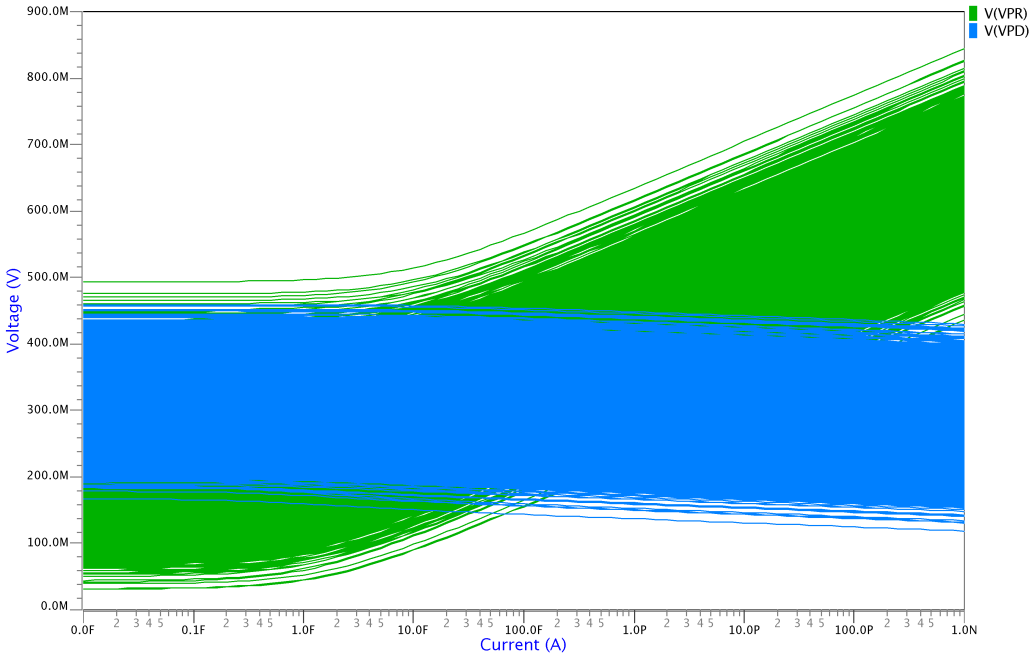

Figure 3.15: Monte-Carlo analysis of the photoreceptor circuit transfer function under typical conditions

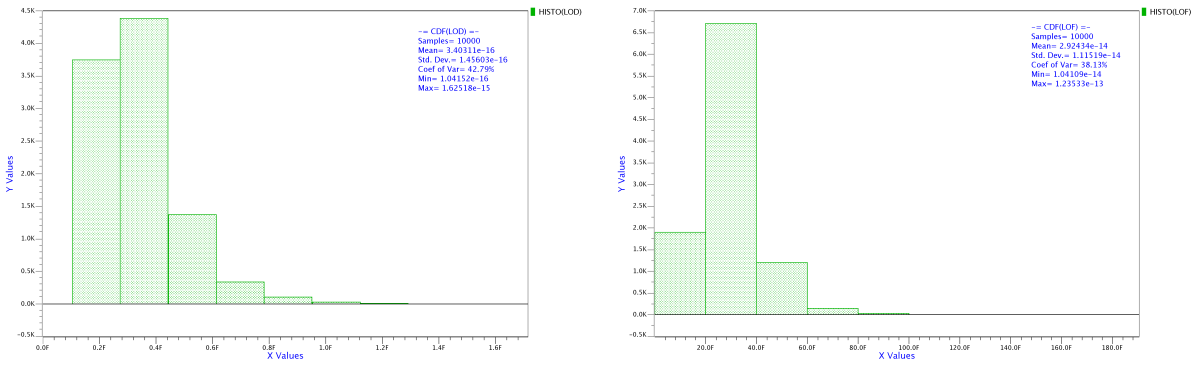

Figure 3.16: Extracted LOD (on the left) and LOF (on the right) from Monte-Carlo analysis under typical conditions

Condition	μ_{LOD} [fA]	σ_{LOD} [fA]	$\mu_{LOD} + 3\sigma_{LOD}$ [lx]
TT 25°	0.34	0.15	6.8m
FF 85°	31.91	1.49	0.25
SS −40°	0.014	0.011	0.41m

Table 3.2: Summary of LOD distribution during Monte-Carlo analysis under typical, FF 85° and SS −40° conditions

Condition	μ_{LOF} [fA]	σ_{LOF} [fA]	$\mu_{LOF} + 3\sigma_{LOF}$ [lx]
TT 25°	29.24	11.15	0.54
FF 85°	3090	190	31.65
SS −40°	1.55	0.79	34m

Table 3.3: Summary of LOF distribution during Monte-Carlo analysis under typical, FF 85° and SS −40° conditions

These results shows that, when the photoreceptor transistor is designed, the considered I_{min} is related to the LOD,meaning that the circuit will not logarithmically converts current into voltage from that point but well at a photocurrent approximately 100 times higher. From this analysis, the choice of the lower working limit between LOD and LOF is thus dependent on the parameter that has to be optimized: sizing increases when I_{min} decreases. A trade off between DR and area is thus highlighted from this analysis.

3.3 Switched-capacitor amplifier

The switched capacitor amplifier (SCA) is devoted the amplification of V_{pr}. Indeed, to reach the target contrast sensitivity, this voltage must be amplified to avoid unwanted event generation when it is compared to the threshold voltages. From the transfer function of the first stage, the voltage equivalence of contrast sensitivity can be found, a change of 2.715mV for a variation of 10% in light intensity is extracted from simulation. A gain of 15 is thus set as target in order to obtain threshold voltages equal to $\frac{V_{DD}}{2} \pm 40.725$ mV.

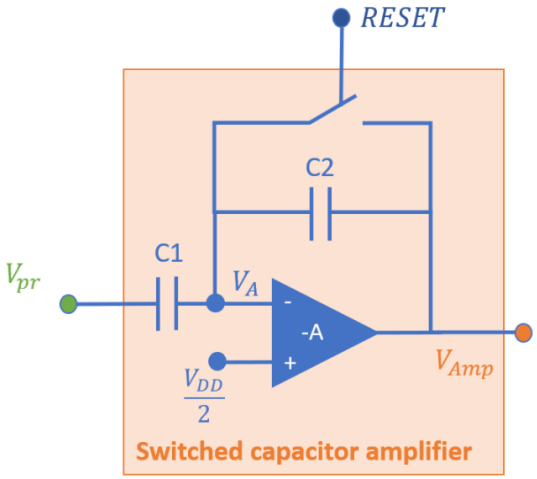

Figure 3.17: Switched capacitor amplifier circuit used in this work

The SCA is composed of three main components: two capacitors, an operational amplifier and a switch, as illustrated in Fig. 3.17. In this section, all of them wil be analyzed to reach the wanted area and power optimization. But first, let us briefly recall how the SCA operates.

It works in two phases, depending on the position of the switch. Once closed, V_A is shorted to the output voltage V_{amp}. Considering an ideal operational amplifier, V_A is equal to half of supply voltage so the output voltage is reset at this value. If open, charges are distributed over both capacitors. Putting all together, it gives

if the switch is closed

$$Q_1 = (V_{reset} - \frac{V_{DD}}{2}) \cdot C_1$$

if the switch is open

$$Q'_1 = (V_{pr} - \frac{V_{DD}}{2}) \cdot C_1 \qquad (3.2)$$
$$Q'_2 = (V_{DD} - V_{amp}) \cdot C_2$$

Where V_{reset} is the input voltage V_{pr} during the reset. Then applying charge conservation results in

$$\begin{aligned} Q_1 &= Q'_1 - Q'_2 \\ (V_{reset} - \frac{V_{DD}}{2}) \cdot C_1 &= (V_{pr} - \frac{V_{DD}}{2}) \cdot C_1 - (V_{DD} - V_{amp}) \cdot C_2 \\ \Leftrightarrow V_{amp} &= \frac{V_{DD}}{2} + \frac{C_1}{C_2}(V_{reset} - V_{pr}) \end{aligned} \qquad (3.3)$$

The SCA therefore has a negative gain fixed by the capacitance ratio, amplifying V_{pr} from the previous reset value. The sizing of the different components can now be discussed.

3.3.1 Capacitors

Capacitors are one of the main issue encountered in the design of the SCA. Indeed, they are generally a wide covering part of the pixel. They must then be chosen very carefully to keep the area as small as possible. Different choices of capacitors are proposed by UMC and listed below.

- Metal-Oxyde-Metal (MOM) capacitors
- Metal-Insulator-Metal (MIM) capacitors
- N/P capacitors

There are different types of implementation of MIM and MOM capacitors, see Fig. 3.18 [13]. These are composed of either metallic plates or fingers built on upper metal layers. They thus have the advantage of being able to placed above the circuitry using the substrate (except over the photodiode of course). However, their minimum size had not evolved much with the scaling of the technology and they still represent a huge area compared to the pixel size (MIM $5\mu m$ x $5\mu m$ minimum, MOM $0.2\mu m$ x $10\mu m$ minimum [38]). They are thus not suitable for this work.

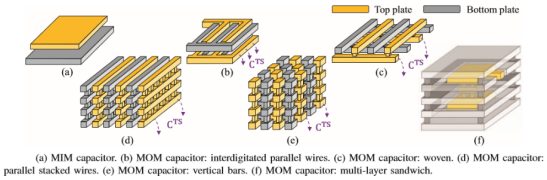

Figure 3.18: Different MIM and MOM layout implementations, from [13]

For their part, N and P capacitors provided by UMC are more transistor-like device. However, the pseudo drain and source doping is the same type as the bulk. N capacitors are thus built in an N-well while the P-type substrate of the P capacitor must be locked in an N-well ring and over a deep-N-well. Fig. 3.19 proves that the latter is thus much less compact. If they are smaller than MIM and MOM capacitors, their minimum sizes are still 1.63 x 2.44 μm^2 for the N-cap and 5.25 x 6.16 μm^2 for the P-cap. This is, once again, too covering to be implemented in this work.

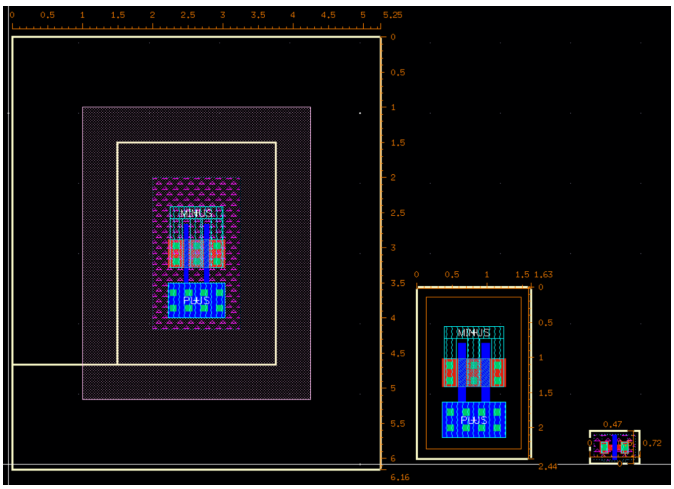

Figure 3.19: Layout comparison of, from left to right, minimum sized P-cap, N-cap and PMOS transistor

As the solution could not be found in the provided device of the UMC library, it had to be self-made. The retained idea has been to build the capacitor using the gate of a transistor. Indeed, if we shortcut the drain and source of a transistor, we build a capacitor across the gate oxide. It allows to choose the size of the device without any other constrains than the ones on the transistor itself.

The problem that appears when making use of a transistor as capacitor is that the capacitance is dependent on the voltage $V_{gs,d}$ across the gate. Indeed three

modes can be identified [39] [40]:

- **Surface accumulation mode:** For NMOS, $V_{gs,d}$ is below a negative flat-band voltage V_{fb}. There is thus a accumulation of negative charges on the gate and of holes at the interface between the gate oxide and the silicon substrate. The distance between the two charged plate is determined by the oxide thickness, the capacitance thus depends on C_{ox} and the size of the transistor.

- **Surface depletion mode:** $V_{gs,d}$ is between the flat-band voltage and the threshold voltage of the transistor. The charges present in the surface accumulation mode are pushed back, hence increasing the size of the depletion region. It increases the effective thickness of the dielectric of the capacitor thus reducing the capacitance.

- **Inversion mode:** $V_{gs,d}$ is now higher than the threshold voltage, the charges at the interface are not anymore of the type of the substrate. It reduces the dielectric thickness and increases the capacitance value. At this point, an increase of the absolute value of $V_{gs,d}$ does not lead anymore to a capacitance increase, it "saturates".

This has a huge impact on the design of the capacitor since the voltage across C_1 is varying a lot, V_{pr} range is from 100mV to 900mV with V_A equal to 500mV. The other capacitor C_2 also poses a challenge since its voltage $V_{AMP} - V_A$ is going to vary between around -40 and +40 mV, hence being in the depletion region, where the capacitance depends on $V_{gd,s}$. A test circuit is thus employed to correctly model the operating conditions of both capacitors and to extract their corresponding capacitance value. The circuit is presented in Fig. 3.20.

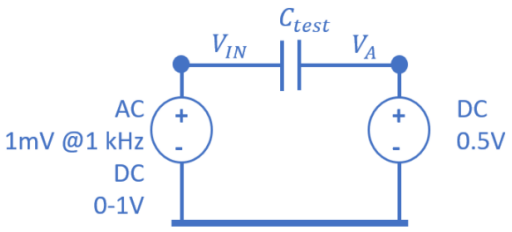

Figure 3.20: Test circuit to design transistor-based capacitor

As V_A is constantly kept at 0.5V by the OTA, we must take care of the parasitic PN junctions of the source and drain nodes. To avoid any of these junctions to

be on, we must have access to the bulk node of the transistor and the decision is made to shortcut it to the drain-source node. For layout facilities, a PMOS transistor is thus best suited since its bulk is an N-well already isolated from the common P-substrate. Still considering the layout, it is more compact to build only one N-well for both capacitors, the choice is thus made to connect the drain-source-bulk of both transistors to the common internal node of the SCA, namely V_A.

In such configuration, the capacitance value can be split into two main components, the overlap capacitance of drain and source, only depending on the sizing of the transistor, and the gate-channel capacitance, also depending on the dimension but on the operating region of the transistor too.

If the transistor is off, $V_g > V_{th} + 0.5$, the gate-capacitance will be small because of the thickness of the depletion region. It can thus be assumed that the dominant capacitance will be the overlap capacitance of both drain and source and that the influence of $V_{gd,s}$ on the total capacitance value will be small.

If the transistor is on, $V_g < V_{th} + 0.5$, the transistor is in its inversion mode, hence increasing the value of the gate-channel capacitance. However, this state is only reached when V_g is below $V_{th} + 0.5 \approx [0.1V(HVT); 0.3V(LVT)]$, which is not the needed voltage range. Moreover, when V_g is crossing this threshold between on and off states, it results in a significant variation of the capacitance value, which should be avoided as much as possible to keep the capacitance values constant. To put that threshold out of our operating voltage range, we thus need to increase the threshold voltage of the transistor, HVT transistor is thus the chosen device to implement the capacitors.

Obtained capacitance for lengths from 60nm to 200nm and widths from 80nm to 2μm are shown in Fig. 3.21. On one side, these results prove the feasibility of the needed ratio around 15 between the smallest and the biggest capacitance values. But on the other side, reaching such point is at the cost of a huge increase in the sizing of the device. It might raise the question of the use of the provided N and P capacitors instead of the one proposed. A comparison is thus made made with a sizing that respects minimum sizing conditions of each device, namely a gate 110nm-long and 400nm-wide.

Fig. 3.22 highlights the good performance of the proposed device. Indeed, it shows the best stability over the voltage range and its density is comparable to the one of the N capacitor if we consider the off-state of the latter. Eventually, the final capacitors are built using the PMOS HVT transistors with lengths of 60nm

and 200nm, and widths of 80nm and 2μm, for C_2 and C_1, respectively. It provides a gain for the SCA between 15 and 18 since the capacitances values are still slightly varying over the voltage range.

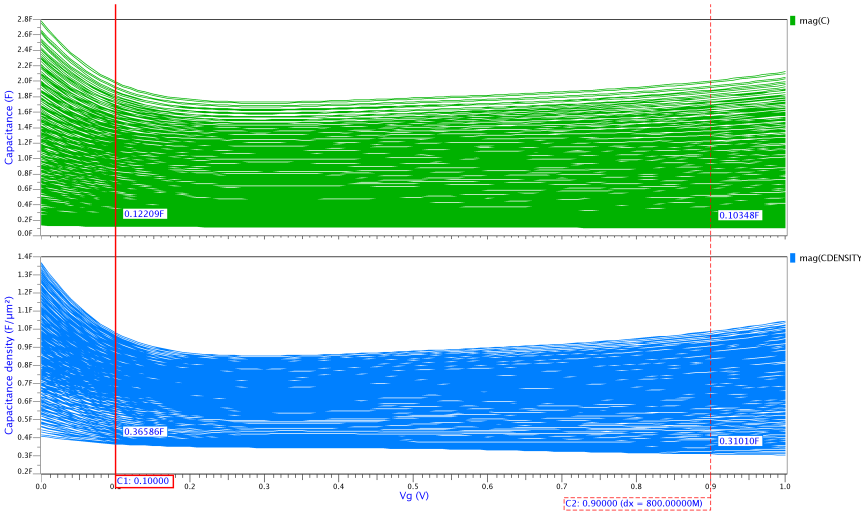

Figure 3.21: Capacitance and equivalent density of PMOS-based capacitor over the needed voltage range

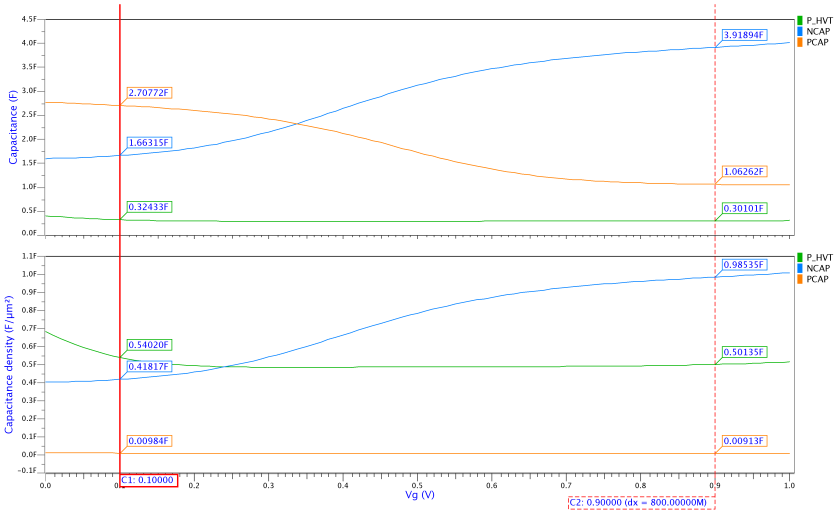

Figure 3.22: Comparison of the capacitance value and density between NCAP, PCAP and PMOS HVT

3.3.2 Operational amplifier

Many amplifier architectures are available, from a single stage OTA to cascoded, Miller or inverter based amplifier. However, as the architecture becomes more complex to enhance performances, other parameters of which area and power are generally degraded. The chosen amplifier is thus kept simple while being tunable enough to reach the needed performance. The architecture of the single-stage OTA used in this work is thus recalled in Fig. 3.23.

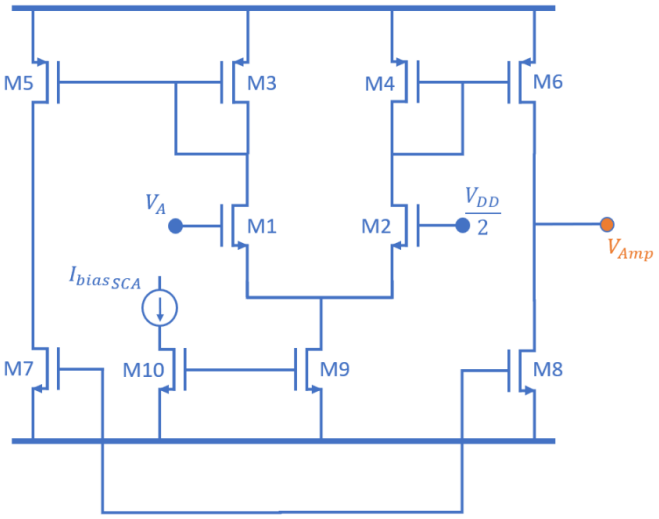

Figure 3.23: Single stage OTA used in the SCA

Besides power optimization, the design of this OTA is conducted by the following guidelines:

- The OTA **area** must be kept as small as possible, the size of all transistors is thus limited to 500nm, apart from the input differential pair to reduce pixel-to-pixel variation.
- The **open-loop gain** (A_{v0}) has to be maximize. It ensures to keep V_A as close as possible to $\frac{V_{DD}}{2}$ so that the output is well reinitialized during the reset phase.
- **Phase margin** need to be checked and a value above 75° is generally requested to avoid stability problems.
- The **slew rate (SR)** must be maximized. Indeed, it plays a role in the latency of the whole pixel. Moreover, if it is not high enough, it might cause problems

if its output is not set at $\frac{V_{DD}}{2}$ before the end of the reset phase. Eq. 3.4 shows that B factor and bias current must be increased to improve the SR. It is also to be noticed that since C_2 is small, it naturally enhances the slew rate.

$$SR_{OTA} = \frac{2 \cdot B \cdot I_{bias_{OTA}}}{C_2} \tag{3.4}$$

A $g_m I_D$ design methodology is then applied [41]. The gain is given in function of the $g_m I_D$ in Eq. 3.5 [42].

$$\begin{aligned} A_{v0} &= g_m I_{D1} \cdot V_{ea} \\ \text{with } V_{ea} &= \frac{V_{ea_5} V_{ea_7}}{V_{ea_5} + V_{ea_7}} \end{aligned} \tag{3.5}$$

To wisely design the OTA, the technology curves are first extracted using the minimum width, and several lengths (from 60nm to 500nm, steps of 10nm). The $g_m I_D$ (green) and the early voltage (blue) are plotted in function of the normalized current in Fig. 3.24 and 3.25, for LVT and HVT transistor respectively.

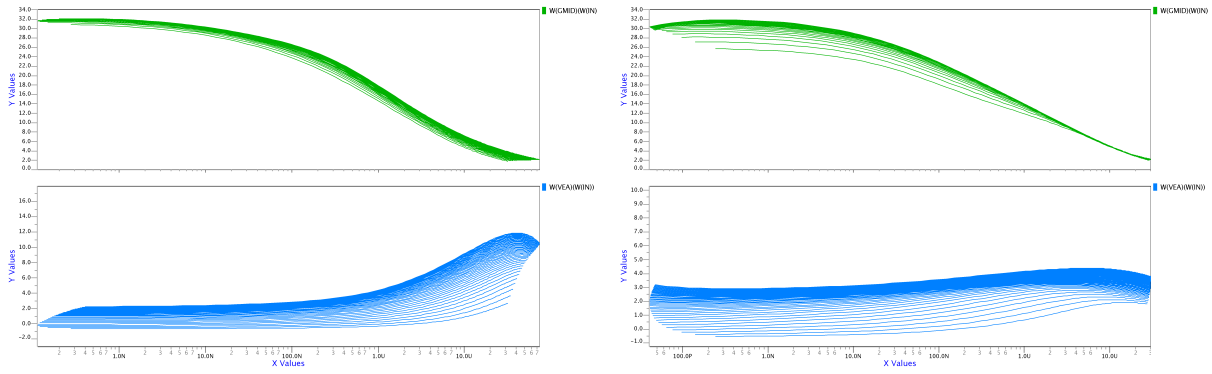

Figure 3.24: Technology curves of LVT transistor (NMOS on the left, PMOS on the right)

With the aim of maximizing the gain, Eq. 3.5 asks us to maximize both $g_m I_{D1}$ and early voltage of output current mirror. From the technology curves, we can affirm that LVT transistors give the higher $g_m I_D$ and are thus chosen to implement the input differential pair. Early voltage, for its part, is higher in HVT transistor, they are thus more adequate for the current mirrors. The complete design flow is available in Appendix A. Design choices are summarized in Tab. 3.4 and the corresponding sizing in Tab. 3.5. The simulated bode diagram presented in Fig. 3.26 shows a gain of 38.2dB and no problem of phase margin, the design is therefore validated.

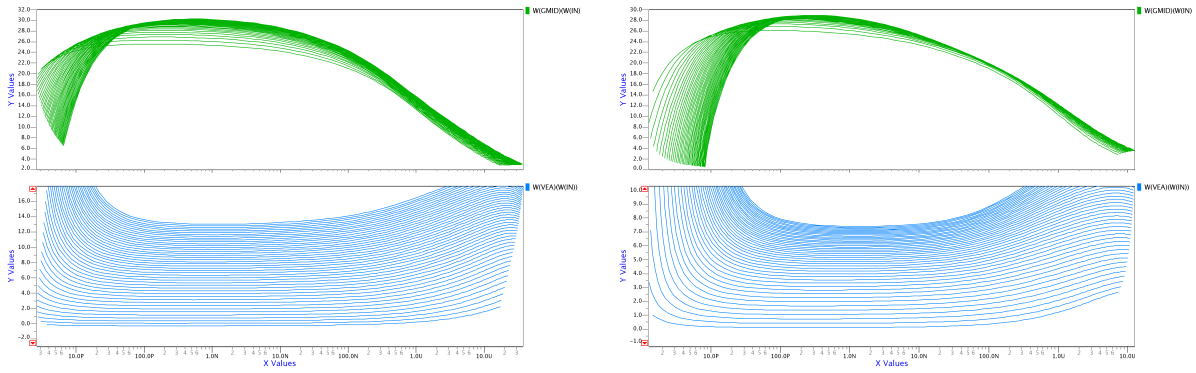

Figure 3.25: Technology curves of HVT transistor (NMOS on the left, PMOS on the right)

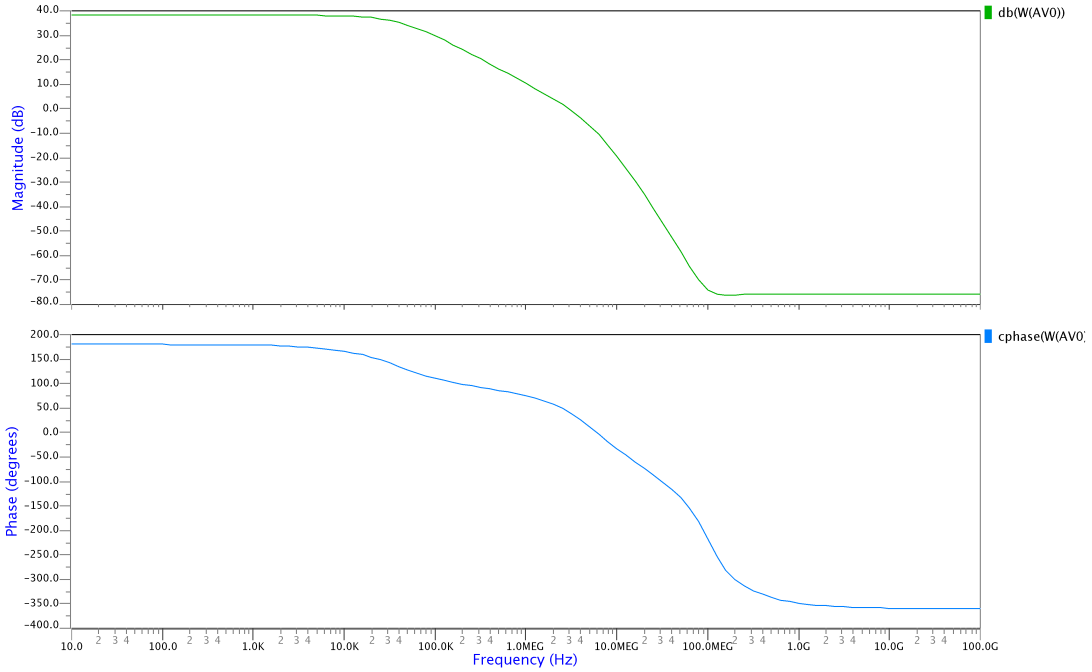

Figure 3.26: Bode diagram of designed OTA

A corner analysis is finally run to verify the functionality of the amplifier over variation in process, temperature and supply voltage. It results a gain that varies from 32.6dB (FF 85°) to 40.1dB (SS −40°), see Fig. 3.27. Constant-g_m biasing technique could reduce the variability of the op-amp, but at the cost of power and

$g_m I_{D1}$	$26[V^{-1}]$
$g_m I_{D3}$	$22.3[V^{-1}]$
$g_m I_{D7}$	$23[V^{-1}]$
$g_m I_{D9}$	$26[V^{-1}]$
B factor	2
Biasing current	$1[nA]$

Table 3.4: Design choices of the single stage OTA proposed in this work

M1/M2	Diff. pair	Core LVT	W=120nm	L= $1\mu m$
M3/M4	PMOS current mirror IN	Core HVT	W=80nm	L=500nm
M5/M6	PMOS current mirror OUT	Core HVT	W=80nm	L=250nm
M7/M8	NMOS current mirror	Core HVT	W=80nm	L=500nm
M9/M10	Biasing current mirror	Core LVT	W=80nm	L=350nm

Table 3.5: Summary of single stage OTA circuit sizing

area consumption. Such technique is thus not developed on this work.

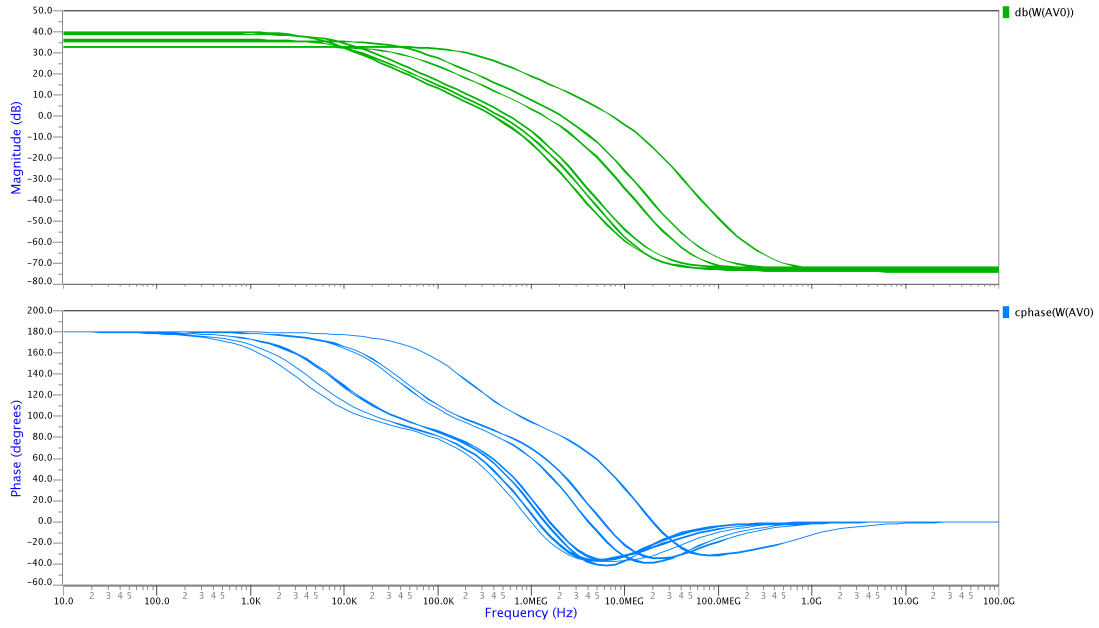

Figure 3.27: Corner analysis of OTA

3.3.3 Switch

The switch is used to control the connection between V_A, the floating voltage at the input of the OTA, and V_{AMP} the output of the whole amplification stage. A good switch design must take care of all phenomenons that can perturb the correct functioning of this block. In our case, two non-idealities of the switch are particularly problematical: charges injection and leakage. The first one may cause voltage drop or jump on the output voltage V_{AMP} after the falling edge of the reset, while the second leads to a constant decrease of the same output voltage. Both issues and their solutions are discussed below.

Charges injection

Charge injection is due to the parasitic capacitances of the switch. When the switch is on, these capacitors accumulate charges which are redistributed when the switch turns off. As represented in Fig. 3.28, two techniques may be used to reduce the injection, dummy and complementary switches [14].

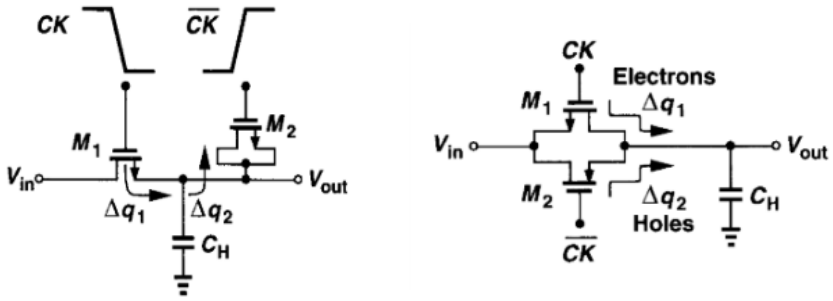

Figure 3.28: Charges cancellation techniques illustration (dummy switch on the left, complementary switch on the right) [14]

In the first case, parasitic charges are caught by the added NMOS transistor thanks to the opposite control signal. As demonstrated in Eq. 3.6, if the size of the dummy transistor is chosen as the half of the main switch transistor ($W_2 = 0.5W_1$), all the charges are caught and no charges injection is to be noticed. However, this method was not enough to practically avoid charge injections while inserted into the circuit. As it lead to dysfunction of the whole circuit, dummy switch had not been selected for this work.

$$\begin{aligned} \Delta q_1 &= \frac{W_1 L_1 C_{ox}}{2}(V_{CK} - V_{th1} - V_{in}) \\ \Delta q_2 &= W_2 L_2 C_{ox}(V_{CK} - V_{th2} - V_{in}) \end{aligned} \tag{3.6}$$

The second idea is to inject the same amount of charges but with an opposite sign with a PMOS transistor. This architecture is only allowed for symmetrical circuit. Indeed, Equation 3.7 shows that there can be a cancellation only if the voltages are symmetrical. In our case, V_{CK} is the reset voltage (1V) and V_{in} is the floating node V_A (≈0.5V). Therefore, if the transistors sizes match, the charges cancel each other and have thus no effect on the output voltage. As it gave the best result in term of charge cancellation in our circuit, this architecture is chosen as switch.

$$\begin{aligned} \Delta q_1 &= W_1 L_1 C_{ox}(V_{CK} - V_{th1} - V_{in}) \\ \Delta q_2 &= W_2 L_2 C_{ox}(V_{in} - |V_{th2}|) \end{aligned} \tag{3.7}$$

Leakage

As we scale the technology, we know that the leakage is getting higher. Reducing the size and the distance between each device increases the parasitic effect such as leakage. In our case, the node V_{AMP}, output of the amplification stage, is really sensitive to this non-ideality. It comes from the small capacitance value of this node, C_2 being very small (≈ 0.1fF). It follows that the node can not keep its voltage constant over a long period of time if the leakage is too important. The latter should thus be reduced as much as possible.

The leakage sources in MOSFET can be summarized as shown in Fig. 3.29 [15]. In our case, the most annoying effect is the subthreshold leakage, which is basically an exponential function of the threshold voltage, the higher V_{th}, exponentially less leakage. The use of an HVT type transistor is thus more than justified.

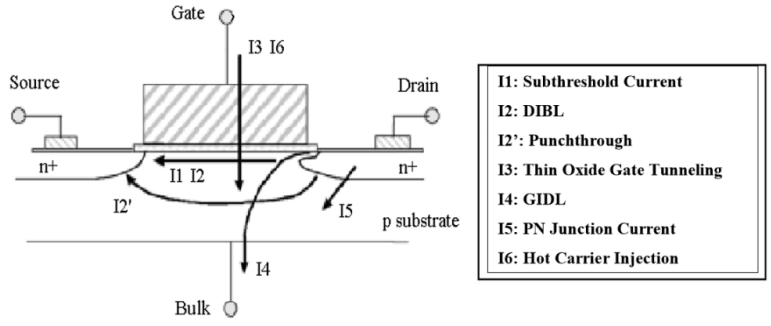

Figure 3.29: Leakage source in MOSFET devices [15]

To size the switch, a first guess might suggest to keep the transistor as small as possible to reduce the current. However, reducing length degrades the threshold

voltage as shown in Fig. 3.30 (short-channel effect). Moreover, if reverse short-channel effect (RSCE) is present (impurities gathering at the edge of drain and source), it results in an increase of the threshold voltage at a few channel lengths. It comes from these extra charges that have to be inverted too. When the length increases, these "halo" have less effect on the amount charges that have to be inverted, the threshold voltage becomes thus stable, as illustrated in 3.31. It results that an optimum length can be found where the threshold voltage is maximum.

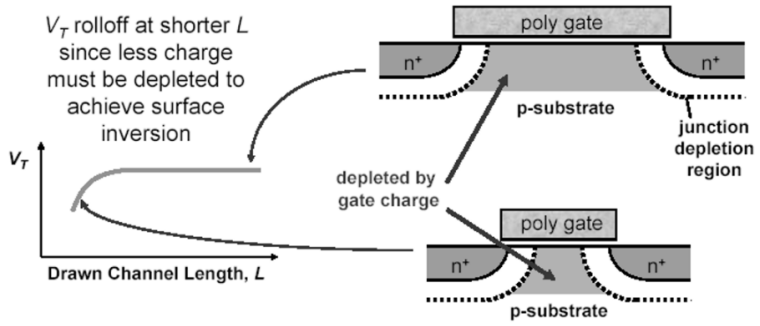

Figure 3.30: Illustration of short-channel effect [15]

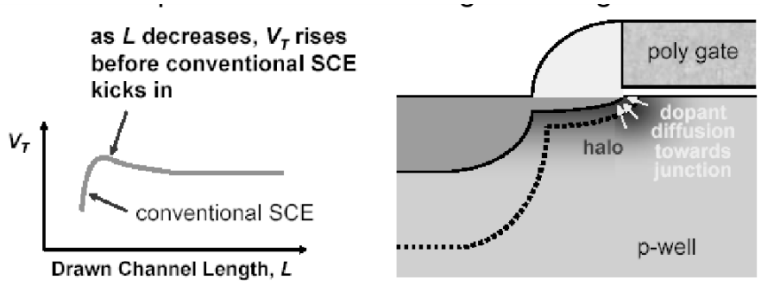

Figure 3.31: Illustration of reverse short-channel effect [15]

Sizing

Combining both charge injection and leakage, we ended to the design of a complementary switch with minimum width (to reduce parasitic capacitances) to basically reduce charge injection. Then several lengths had been tested to find the optimal one as far as the leakage is concerned, keeping in mind that it should be minimized to optimize the area. The obtained leakage current (for NMOS, PMOS and their sum) are shown in Fig. 3.32 and confirms the expected RSCE.

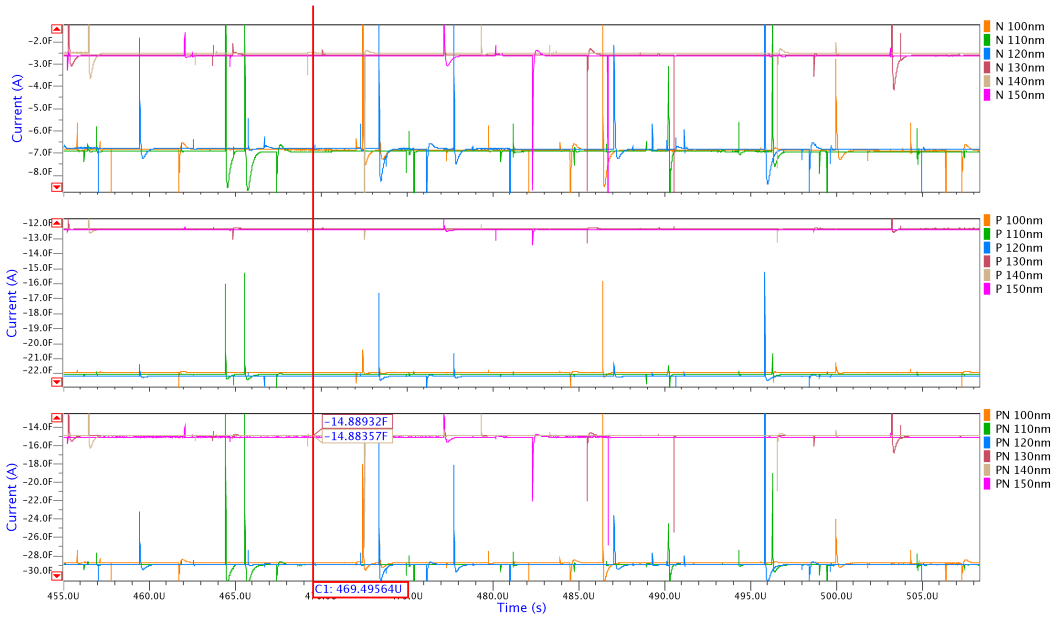

Figure 3.32: Leakage in NMOS and PMOS of complementary switch at V_{AMP} node

It can be observed that both lengths 130nm and 140nm exhibits a lower leakage ($\approx$ 14.9fA) but considering charge injection and area optimization, a length of 130nm is chosen. The final design of the switch is summarized in Tab. 3.6.

MSWN	Core HVT	W=80nm	L= 130nm
MSWP	Core HVT	W=80nm	L=130nm

Table 3.6: Summary of switch sizing

3.4 Events and reset generator

The last part of the pixel is devoted to the generation of the ON- and OFF-events as well as the reset signal needed by the SCA. As shown in Fig. 3.33, it is composed of two main blocks: two comparators and the reset logic block to control the reset signal. The latter should be replaced by an asynchronous events representation (AER) logic block which generates row and column requests in addition to reset signal. However only the design of the logic block used in this work will be discussed.

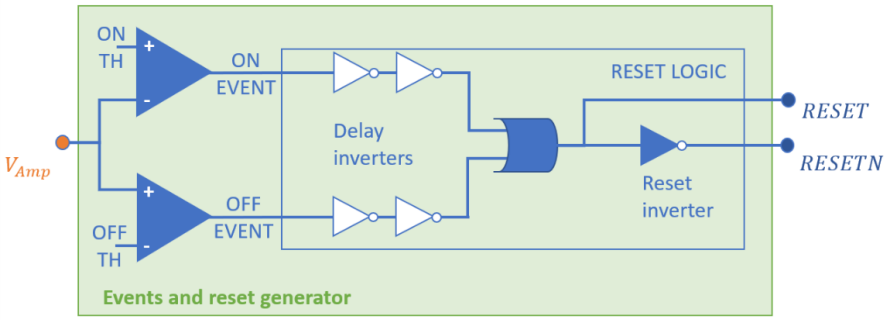

Figure 3.33: Event and reset generator circuit

The input of this stage is V_{AMP}, which is as reminder the amplified voltage representing the variation of input light intensity. V_{AMP} is firstly compared to threshold voltages modelling the contrast sensitivity of $\pm 10\%$. The output of these comparators are the ON- and OFF-events, they are put at V_{DD} if the event is generated.

These events are handled by the logic block which will control of the delay of the reset signal. Indeed the reset signal must be long enough to allow the SCA to reset its output at half V_{DD}. However, during the reset signal, the pixel is not able to detect any change of light intensity, it should thus not be overestimated not to miss events. The design of each block is eventually discussed below.

3.4.1 Comparators

The comparators are operational amplifiers used in open-loop. They aim at directly amplifying the difference between their inputs. Ideally, the gain of such block should be infinite so that the output is set at V_{DD} or 0 as soon as V_{AMP} crosses one of the thresholds. For its part, the slew rate is not a critical performance of the comparators, it might thus be reduced to lower the power consumption without impacting the functionality.

following these guideline, the design methodology of the SCA amplifier is reused for the comparator. The sizing itself is thus identical to the SCA (Tab. 3.4) since it had already been optimized in term of area. To reduce power consumption, it is here allowed to lower the biasing current. Hence, the transfer function of the comparators using a 0.1nA biasing current instead of 1nA is given in Fig. 3.34. The comparator exhibits a gain of 36.3 dB but also and mainly a huge power consumption reduction.

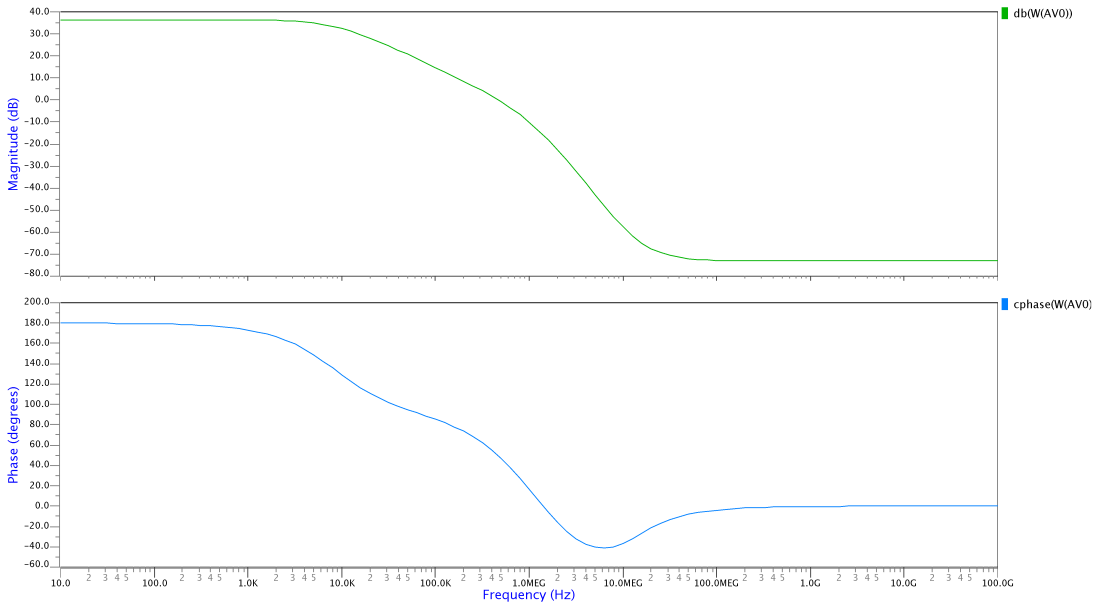

Figure 3.34: Transfer function of the comparators (0.1nA biasing current)

The threshold voltages must be designed as well. Indeed, these thresholds are the voltages that set the contrast sensitivity of the pixel. At the V_{pr} level, the 10% contrast sensitivity represents 2.715mV, as the gain of the SCA is around 15 most of the time, the equivalent change in V_{AMP} is 40.725mV, meaning that the thresholds should be set at $\approx 0.5 \pm 0.04[V]$. However, since the gain of the comparator is not infinite, these values might have to be adjusted to fit the target contrast sensitivity. Discussion on these thresholds will be deepened in Chapter 5.

3.4.2 Reset logic

The purpose of this block is to generate a long enough reset signal when an event occurs. To do so, two "delay inverters" are put after each event node. These delayed event are then connected to an OR gate, providing the reset signal. The reset is

thus held at V_{DD} until the delayed event is cleared. The reset duration is thus well controlled by the first inverters. In order to reduce leakage, only HVT transistors are used in this part.

Delay inverters

The delaying inverter must be designed to keep their dimension as small as possible, while their delaying functionality requests their lengths to be increased. From this consideration, the maximum authorized size will be fixed at 500nm.

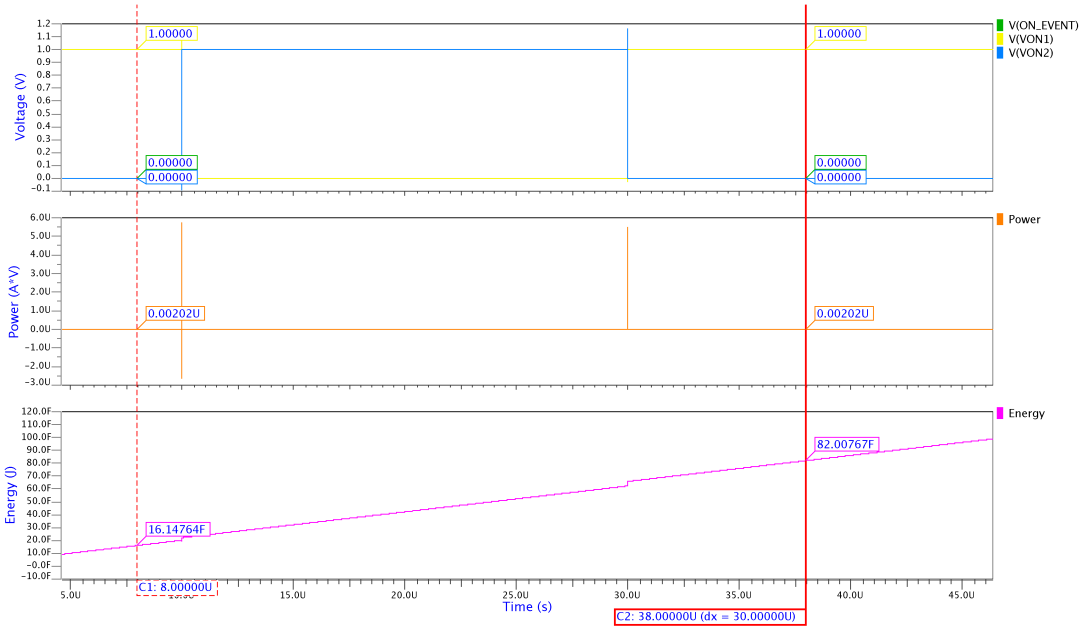

Figure 3.35: Rising and falling time of 2 inverters in serie

Fig. 3.35 shows the delay of two inverters in serie with lengths fixed at 500nm and width at 80nm and 500nm for NMOS and PMOS, respectively. This sizing has been obtained by trials and error to get the longer delay. The simulated delay is too short anyway (around 2ns) and does not match the requirements on the signal when tested in the circuit.

As we need to further increase the produced delay, we try to limit the current flowing through these inverters. However, it is to be considered that we do not need the rising edge of the reset to be delayed. Actually it only increases the time before the reset is generated which is not needed since it degrades the latency of

the pixel. To avoid that, we can put a limiting current mirror only on the top of the PMOS of the first inverter and another one on the bottom of the NMOS of the second inverter, see Fig. 3.36. This would only impact the delay of the falling edge of the reset, hence improving the latency and reaching a longer delay for the falling edge.

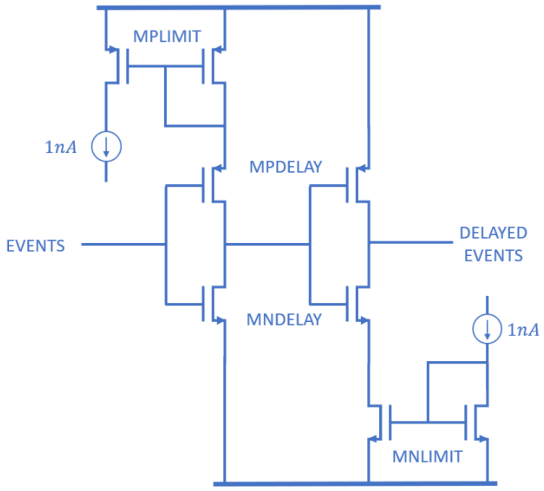

Figure 3.36: Current limited inverter architecture used in this work

As we can see in Fig. 3.37, the rising time is not impacted but the falling time is clearly increased to the micro-second order of magnitude, which is expected to ensure the functionality of the whole circuit. Moreover, since the current is limited, it reduces the instantaneous power consumption during the reset, the peak power at the positive edge is much higher than the one at the negative edge of the reset. This design can thus be approved in the scope of this work.

Reset logic

The reset logic is composed of digital gates: an OR-gate (NOR-gate + inverter) and a reset inverter. They are designed following the minimum size inverter. Indeed, since the delay is controlled by the previous inverters, they can be optimized in size.

For the sizing of the OR-gate and more particularly its NOR-gate, the W over L ratio of the PMOS must be four times the one of the NMOS. If we keep the minimum sizing for the NMOS, the width of the PMOS must be multiplied by 4. To reduce the area, it is possible to increase the length of the NMOS by a factor 2,

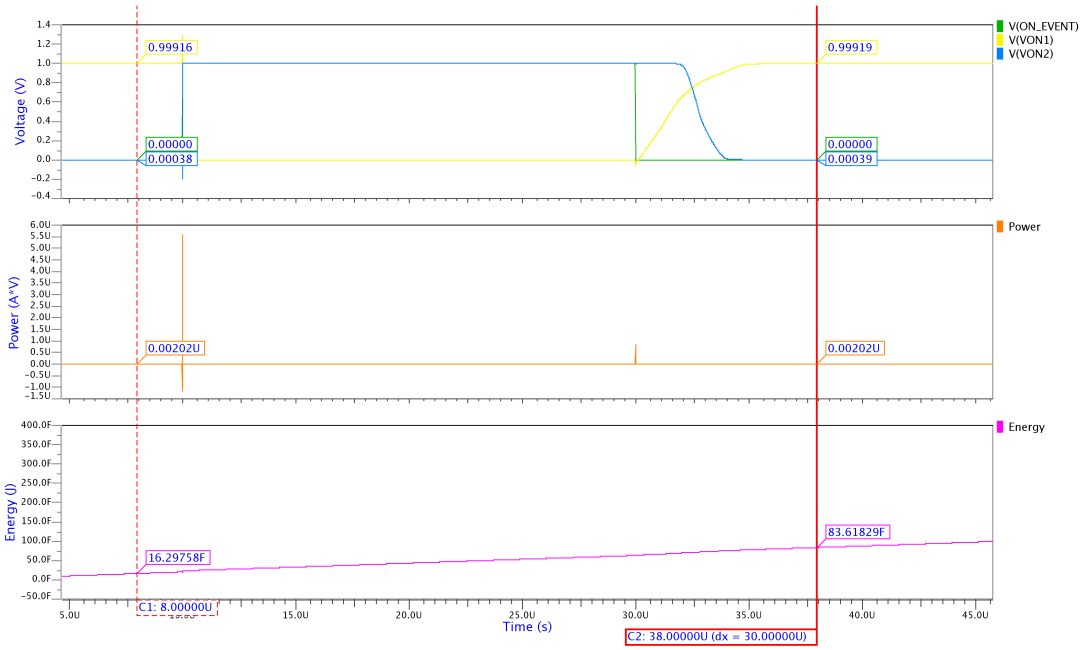

Figure 3.37: Rising and falling time of 2 inverters in serie with the current limitation

the width of the NMOS has just to be multiplied by 2 as well. Dimensions of all transistors used in the event and reset generator is summarized in Tab. 3.7.

MNDELAY	Core HVT NMOS	W=80nm	L= 500nm
MPDELAY	Core HVT PMOS	W=500nm	L=500nm
MNLIMIT	Core HVT NMOS	W=80nm	L=100nm
MPLIMIT	Core HVT PMOS	W=80nm	L=100nm
MPNOR	Core HVT PMOS	W=160nm	L=60nm
MNNOR	Core HVT NMOS	W=80nm	L=120nm
MPINV	Core HVT PMOS	W=160nm	L=60nm
MNINV	Core HVT NMOS	W=80nm	L=60nm

Table 3.7: Summary of events and reset generator design

3.5 Summary

In this chapter, a complete DVS pixel has been designed. Optimization in area and power has been thought at each level of the circuit. It results in a design methodology for each block that already seems to give good performances in the

target optimization.

In term of area, at the exception of the differential pairs at the input of the OTA's, no transistor exposes a length or a width above 500nm and minimum sizing has been used as a priority. The biasing has been reduced as much as possible to reduce the power consumption as well. A complete summary of the pixel sizing is available in Appendix B.

The other performances of the pixel will now be evaluated to see the impact of such optimization on its behaviour.

Chapter 4

Pixel validation and performances

Contents

In this chapter, the whole pixel is simulated to validate its behavior and to characterize its performances. Different photocurrent patterns are tested to analyze the response of the circuit in several cases. Self-triggered events are also discussed and the limitations of both architecture and technology are highlighted. A comparison is finally made between the performances of this work and the literature.

4.1 Validation

Now that the circuit is fully designed, it is tested with rising and falling photocurrent patterns to check functionality on both ON- and OFF-events. Applied patterns are piece-wise-linear and cover the possible range of photocurrent, from the fA to the nA.

The main purpose of this validation is to check if the designed blocks are working properly, and to apply slight modification if necessary. Practically speaking, the gain of the SCA and the related contrast sensitivity will be analyzed over the range of photocurrent. As the capacitors are not perfectly constant over the operating range, it is interesting to check in which proportion these parameters are going to be impacted. Finally, leakage (of which the one from the switch) consequences will be discussed as well.

4.1.1 Rising pattern

A first rising pattern is applied to the pixel. However, its response were not good enough because of the poor gain of the comparators. Indeed, when V_{AMP} crosses the threshold, the output of the comparator was not high enough to trigger the event. A modification on these threshold is thus applied resulting in $V_{ON_{TH}} = 0.470$ and $V_{OFF_{TH}} = 0.530$. The pixel response is eventually given in Fig. 4.1.

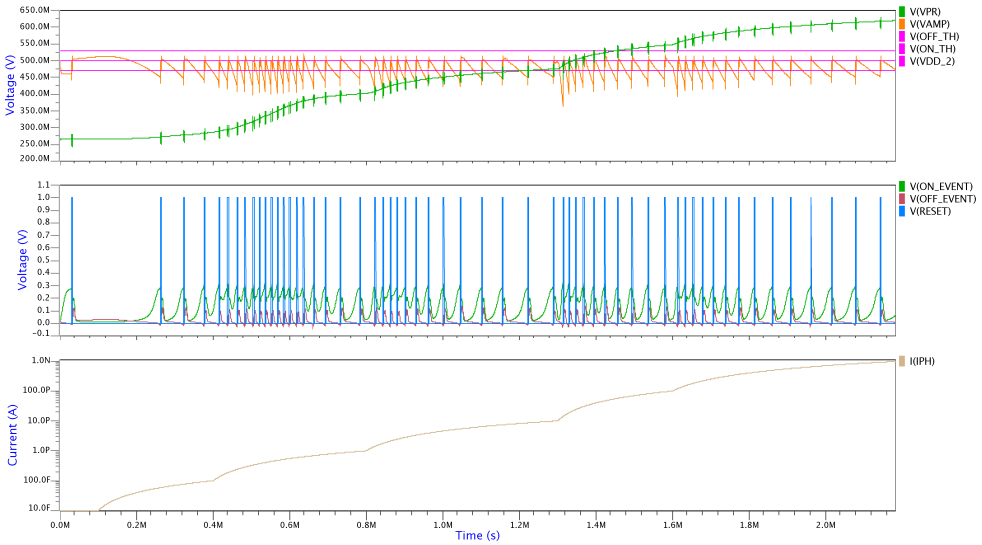

Figure 4.1: Response of the pixel with a rising photocurrent pattern

Different values are extracted from this simulation, ΔV_{pr} and ΔV_{AMP} between the falling edge and the next rising edge of the reset, the related contrast sensitivity and the gain of the SCA (representing the ratio $\frac{C_2}{C_1}$). They are summarized in Tab. 4.1.

I_{ph} [A]	ΔV_{pr} [mV]	ΔV_{AMP} [mV]	SCA gain [V/V]	Contrast sensitivity [%]
60f	4.96	56.88	11.47	28
378f	6.29	78.72	12.5	7
2.87p	5.24	66.53	12.7	15
8.65p	3.78	52.29	13.83	13
81.31p	4.51	60.54	13.42	15
820.31p	3.38	49.95	14.78	11

Table 4.1: Extracted characteristics of the pixel with a rising photocurrent pattern

There are several comments to be done on these results:

1. There is a sort of dysfunction of the pixel at low photocurrent values. This can be explained by the simulation model of the photodiode as a diode in parallel with an ideal current source. Indeed, a part of the current generated by the source is caught by the photodiode instead of flowing in the photoreceptor transistor, see Fig. 4.2. As the current value gets lower, the proportion of current flowing in the photodiode increases, which degrades the pixel response. As the real circuit will not be in such configuration (all photocurrent and dark current will be flowing in the photoreceptor transistor), it should not be considered as problematic.

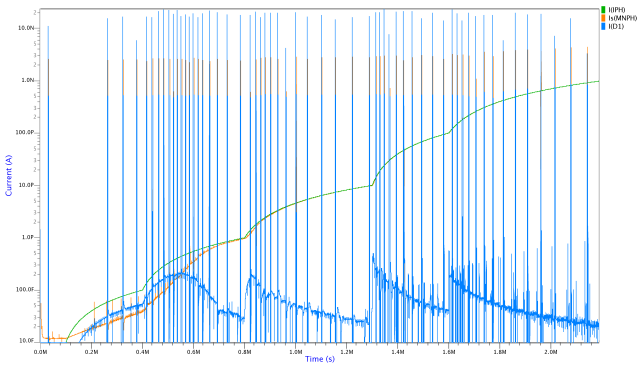

Figure 4.2: Currents flowing in the photoreceptor transistor (orange), the modelled photodiode (blue) and the ideal source (green)

2. Contrast sensitivity is not constant over the range of photocurrent. Which is due to both the variation of the SCA gain and the performance of the comparator. Indeed, the later does not show a very high gain, which leads to a difference between the set threshold and the actual one.

4.1.2 Falling pattern

The same analysis is performed with a falling pattern. The photodiode is now represented only with an ideal current source to avoid interferences at low photocurrent. Results are presented in Fig. 4.3 and Tab. 4.2.

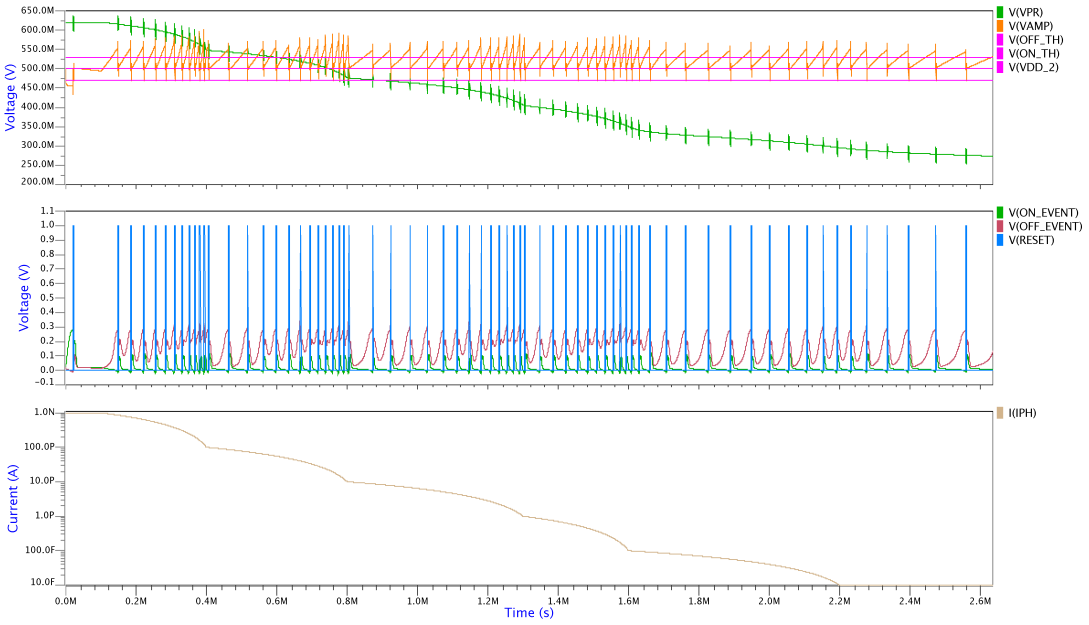

Figure 4.3: Response of the pixel with a falling photocurrent pattern

It can be observed from these results that:

1. At low current, the ideally generated current flows almost entirely in the photoreceptor transistor, hence the response of the pixel is no more impacted. However, at very low current, there is still a difference between both currents, it comes from the gate leakage of the CS transistor that biases the photodiode.

2. The contrast sensitivity is once again varying over the operating range of photocurrent, which sticks to the expected behavior.

I_{ph} [A]	ΔV_{pr} [mV]	ΔV_{AMP} [mV]	SCA gain [V/V]	Contrast sensitivity [%]
56f	3.64	47.91	13.16	15
365f	5.04	64.0	12.7	18
2.17p	5.05	64.27	12.73	15
8.66p	3.49	46.25	13.25	10
85.0p	4.45	53.96	12.13	13
846p	4.06	54.48	13.42	12

Table 4.2: Extracted characteristics of the pixel with a falling photocurrent pattern

4.1.3 Self-triggered events

Up to now, it has not be shown that the circuit generates events even when the photocurrent stays constant, even if it works correctly when a patterned photocurrent is applied. Ideally, the pixel should not generate these events when it is not excited, however, as the leakage modify the internal node (V_{AMP}) of the pixel, ON- or OFF- events are self-triggered. This effect, which has been kept as limited as possible, is analyzed in this section.

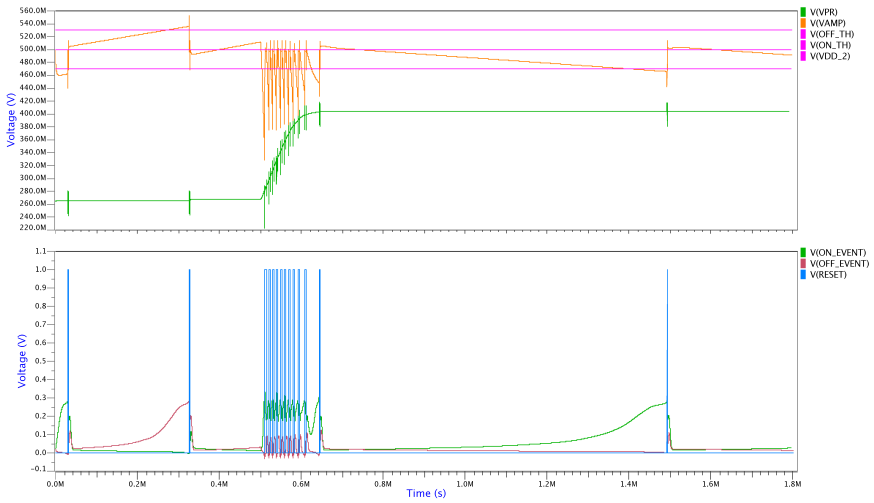

Figure 4.4: Illustration of self-triggered events at 10fA and 1pA of photocurrent

The pixel has been tested with different levels of photocurrent (kept constant) and two modes have been observed: if the photocurrent is low (below $\approx$ 100fA), V_{AMP} increases continuously and it leads to OFF-event generation. If the photocurrent is high (above $\approx$ 100fA), the output of the SCA decreases and thus

generates ON-events. This phenomenon is shown in Fig. 4.4. Further analysis on the generation rate of such events is conducted at different photocurrent level and summarized in Tab. 4.3.

I_{ph} [A]	Event generated	Generation rate [Event/ms]
10f	OFF	3.3
100f	OFF	0.25
1p	ON	1.13
10p	ON	1.86
100p	ON	1.76
1n	ON	2.5

Table 4.3: Mean self-triggered events generation rate at different levels of photocurrent

These events obviously perturb the pixel behaviour as they do not represent any change of light intensity. But they also degrade the power consumption of the pixel since event are generated even when it is not needed. Reducing the self-triggered event generation rate of such pixel architecture is one of the key point that should be improved in future works and that will be discussed in Chapter 5.

4.2 Performances

In this section, the performances of the pixel are analyzed. Power consumption and area are the most relevant in this case but in order to compare the whole pixel with the literature, minimum latency, dynamic range, contrast sensitivity and fixed-pattern noise will also be discussed.

4.2.1 Power consumption and energy per event

Power consumption is computed by taking the product of current and voltage of the supply source. To take into account the self-triggered event in the total consumption, the mean is taken by integrating the power consumption over time to get the total energy consumption, this amount is divided by the period of time to get the mean power consumption. It is done without activity at low and high photocurrent (10fA and 1nA) and with high activity (transition between no activity levels) as shown in Fig. 4.5. It gives a static power consumption of 8.93 and 9.73 nW, at low and high photocurrent, and 16.0 nW with high activity.

The energy per event is computed from the integrated instantaneous power consumption. It is defined as the energy difference between two rising edge of the

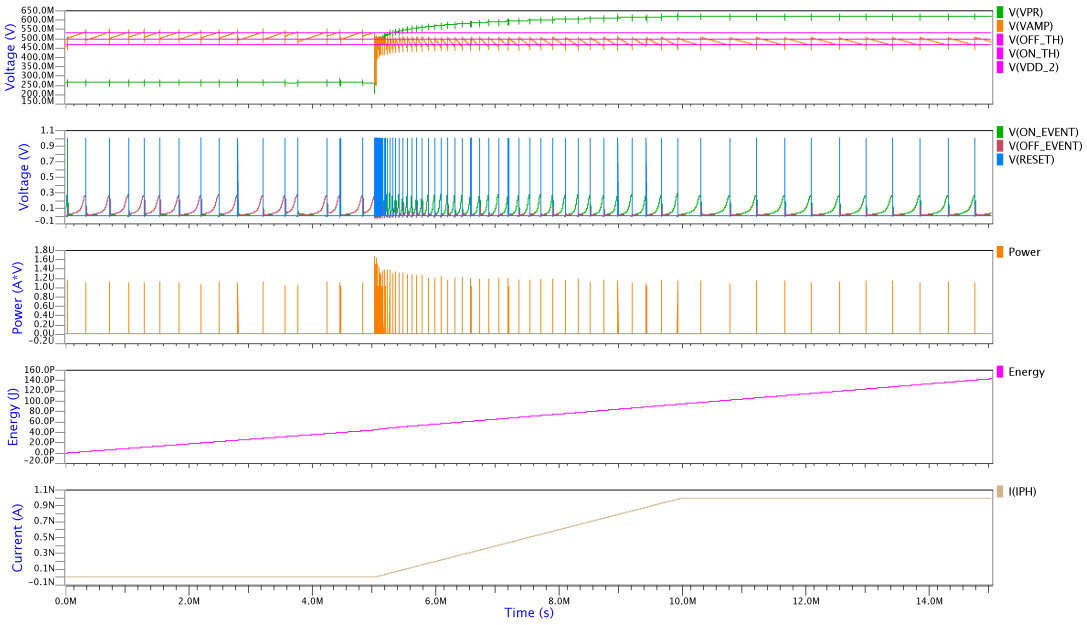

Figure 4.5: Power consumption extraction from simulation

reset signal, divided by the number of events generated in this period. It is done during the high activity period and it gives a energy per event of 181.89 fJ/event.

4.2.2 Area

The pixel area is computed from the active area of the designed transistors and photodiode. However, this area does not represent the real one in the layout. Then, an estimation is done that transistors use, in average, four times more space than their active area on the layout (considering their drain and source plus the spacing rule). The photodiode area is, for its part, well represented by its active area since it is a N-well/P-sub photodiode, it uses only the N-well area on the layout. With such approximation, the estimated pixel area is equal to 17.23 μm^2.

The whole circuit should thus fit in a 5 μm x 5μm pixel. The area contribution of each part of the circuit is represented in Fig. 4.6. In the case of a pitch of 5μm, it is possible to approximate the fill factor around 18%, representing the ratio between the photodiode and the pixel area.

It shows that the biggest block is the logic part of the events and reset generator. It is due to the delay inverters that have been designed to increase the delay.

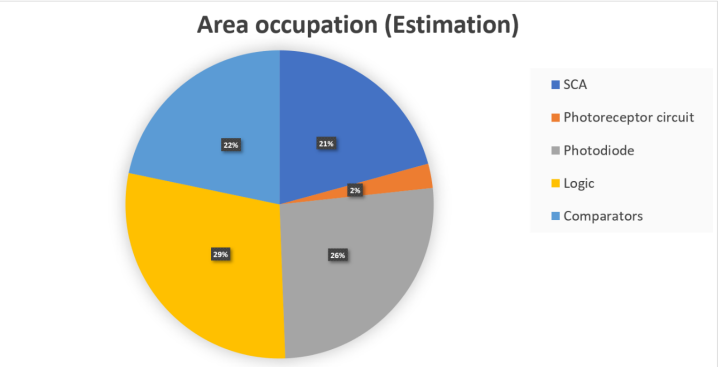

Figure 4.6: Estimated area occupied by each block in one pixel

However, the size of these inverters might be reduced since the we are able to control the falling delay thanks to the limiting current mirror. It might thus be feasible to keep the smallest size for the inverters and to tune the current limitation to obtain the wanted delay. If such sizing might have positive effects: a lower inverting threshold voltage, which compensates the poor gain of the comparators, lower area and power consumption, it also comes with its uncertainties such as the variability of this inverting threshold voltage and of its delay, its effect on the response of the SCA after the reset... It could be studied in future work but it is more likely that if one set of parameters will give better performance in one case, this set will not be robust against variations.

4.2.3 Minimum latency

Minimum latency of the pixel is defined as follows: at 1 klux, a step of 30% in light intensity is applied, the time between the input step and the first reset signal rising edge (meaning that an event has been generated) is the minimum latency. Fig. 4.7 shows the obtained minimum latency of 7.05 μs. This latency is comparable to previous results of literature and does represent neither a good performance neither a poor one.

4.2.4 Dynamic range

The dynamic range is determined by the ratio between minimum and maximum light intensity that can be sensed by the pixel. As a photocurrent range from approximately 10fA to 10nA can be detected, see Fig. 4.8, representing approximately 0.1 and 100 000 lux, hence giving a dynamic range of 120dB. It has already been discussed in Section 3.2.5 that a DR boost could be considered at the cost of harder constrains on the photoreceptor circuit, hence leading to an increased area.

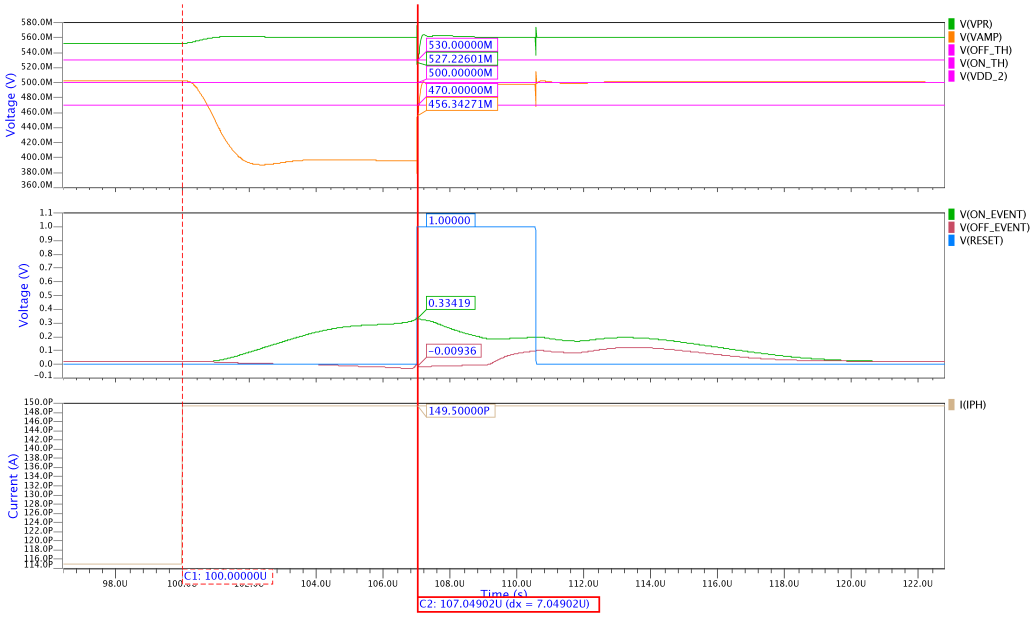

Figure 4.7: Minimum latency extraction from simulation

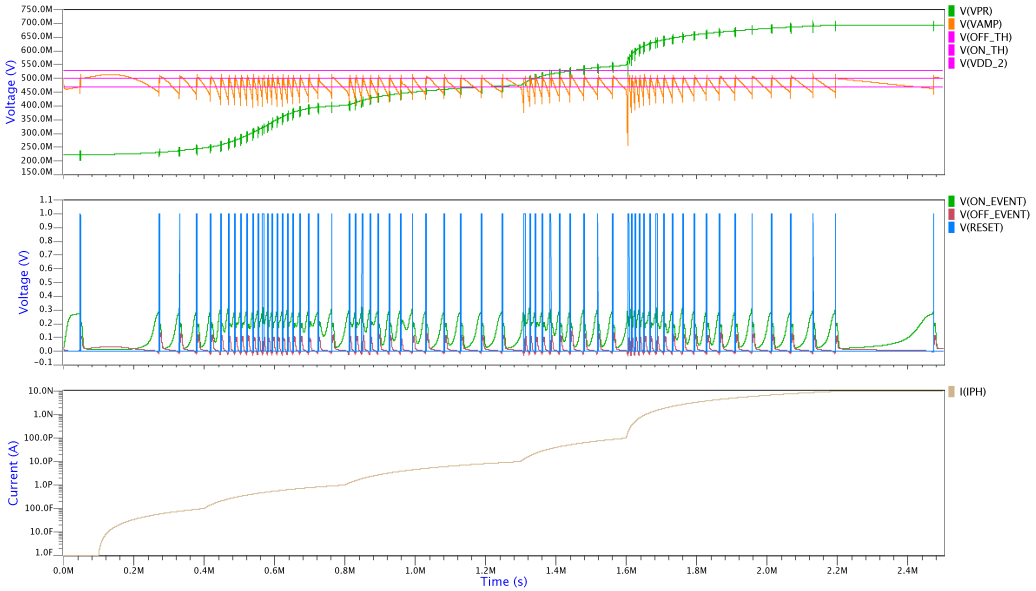

Figure 4.8: Dynamic range extraction from simulation

4.2.5 Contrast sensitivity and fixed-pattern noise

Fixed-pattern noise defines the non-uniformity of the full DVS response. Due to mismatch introduced during the manufacturing, each pixel is not exactly identical and thus does not give the same contrast sensitivity, creating a pattern on the pixel array with hot (white) and cold (dark) pixels. In this case, as the contrast sensitivity is already varying in one pixel depending on its input illumination, FPN is not expected to be good. Moreover, since the pixel is optimized in term of area, the use of minimum width will lead to more variation between pixel. To quantify this, a Monte-Carlo simulation is run with a light intensity variation from 1 klux to 1.77 klux in 100 μs. The FPN is then defined as the standard deviation of the photocurrent ratio measured at rising edge of two reset signals. It is expressed in percentage of illumination change. Fig. 4.9 shows a mean contrast sensitivity of 19.4 % and a FPN of 8.4%.

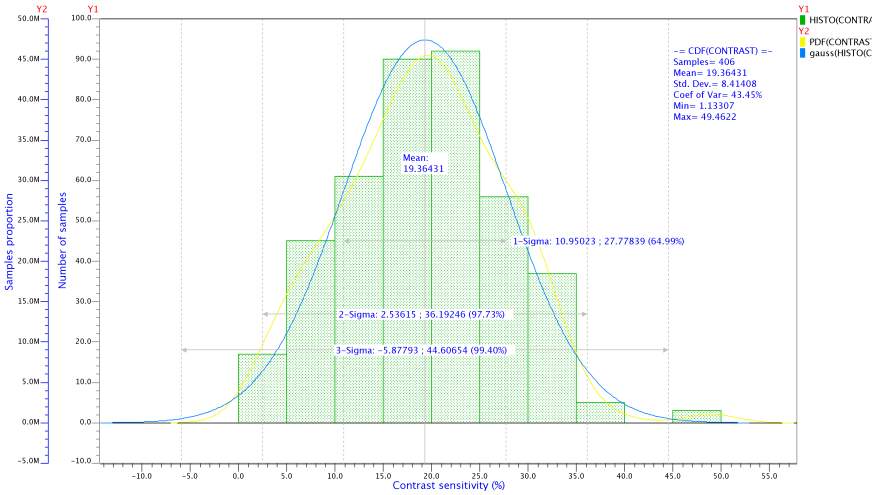

Figure 4.9: FPN extracted from simulation

It is to be noticed that the contrast sensitivity is higher than the expected one, mean at 19.4%. But since it is already varying in one pixel, depending on its illumination, this parameter is hardly tunable. It shows one of the limitations of the proposed architecture in this technology.

A second remark is that this contrast sensitivity also depends on the input light intensity changing speed. Indeed, as the output slew rate of the comparator is limited (for power reduction), if the input is varying too fast, the event might be generated with a small delay. If the light intensity is still varying during this delay, the measured light intensity at the reset might not represent correctly the light

change that has caused the event. This might be expressed by a degraded contrast sensitivity but also by its dependence on the input light variation.

Finally, on a thousand runs, only 406 attempts have resulted in the generation of two valid events allowing the computation of the contrast sensitivity. It highlights the high sensitivity of the pixel to mismatch. It is due to the optimization in term of area, increasing the use of minimum sizing, which degrades the robustness of the pixel to mismatch. The design of the op-amps is particularly sensitive to this phenomenon. Mismatch is able to completely kill the open-loop gain of the OTA, resulting in a state which is completely blocked since the comparators are used in such configuration. Achieving an higher robustness to mismatch is one of the main improvements that have to be done to build a functioning device.

4.3 Summary

The performances of the proposed pixel has two distinct aspects. On one side, they show a huge improvement in the area and power consumption. The optimization process on this architecture for this technology has proven its worth while keeping other performances like minimum latency comparable to previous works. It is thus promising for future works since this study has proven that their is room for optimization in the design of DVS.

On the other side, the performance analysis ends up with the conclusion that the pixel is far too sensitive to mismatch, leading to inoperative pixels in more than half of the cases. If some tips to improve the basic architecture have been proposed in the design (e.g. limiting current mirror, transistor choices), there were no significant changes in the circuit that might have helped to reduce the variation of the pixel. Guidelines for future works will be discussed in Chapter 5.

Finally, a comparison between this work and the literature is done in Tab 4.4.

	This work	Rousseau 2017 [31]	Samsung 2017[7]	DAVIS 2014	ATIS 2011 [28]	Barranco *et. al* 2013 [33]	Barranco *et. al* 2011 [32]	Lichtsteiner 2008 [17]
Fonction	DVS	DVS	DVS	DVS+APS	DVS+exp. meas.	DVS	DVS	DVS
CMOS Technology	65nm UMC 1P10M	0.18μm CIS	90nm 1P5M BSI CIS	0.18μm 1P6M MiM CIS	0.18μm 1P6M MiM CIS	0.35μm 4M2P	0.35μm 4M2P	0.35μm 4M2P
Chip (mm^2)	N.A	N.A.	8x5.8	5x5	9.9x8.2	4.9x4.9	5.5x5.6	6x6.3
Array	N.A.	480x320	640x480	240x180	304x240	128x128	128x128	128x128
Pixel area (μm^2)	5x5 (est.)	21x21	9x9	18.5x18.5	30x30	30x31	35x35	40x40
Fill factor (%)	18 (est.)	10	≈100 (BSI)	22	30	10.5	8.7	8.1
Pixel complexity	52T 1PD	50T 1PD 2C	N.A.	47T 3C 1PD	77T 3C 2PD	N.A.	N.A.	26T 3C 1PD
Supply (V)	1	0.75	2.8	3.3 (1.8 digital)	3.3 (1.8 digital)	3.3	3.3	3.3
Total power (mW)								24
High activity	N.A.	>27.34	50	14	175	95 20Meps	231	N.A.
Low activity	N.A.	>6.5	27	5	N.A.	4 100kep	132	N.A.
Static	N.A	>3.15	N.A.	N.A.	50	2.6 1keps	N.A	N.A
Power/pixel (μW)								1.46
High activity	0.016	0.18	0.16	0.324	2.4	5.8	8.85 1Meps	N.A
Low activity		0.043	0.088	0.116	0.685	0.24	N.A.	N.A
No activity	0.009	0.021	N.A	N.A	N.A.	0.158	N.A.	N.A
Energy/pixel/event (fJ)	181.9	721.4	879 (calc.)	N.A	N.A	2440 (calc.)	8850 (calc.)	N.A.
DR (dB)	120	140	120 (est.)	130 (DVS)	125	120	>100	120
Contrast sensitivity (%)	19.3	7	9	11	max 30	1.5	10	15
FPN (%)	8.4	2.78	N.A.	3.5	0.25	0.9	4	2.1
Latency min. 1klux (μs)	7	45	N.A	3	<4	<9	<11	15

Table 4.4: Performances comparison between this work and literature

Chapter 5

Discussion and perspectives

Contents

This chapter concludes the main contents this thesis has addressed so far. Several aspects in the design and the obtained results are discussed and potential sources of improvement are introduced. This parts is completed with the establishments of future perspectives for this master thesis.

5.1 Discussion

Several limitations of the proposed pixel have been already introduced in previous chapters. They are firstly summarized and linked to the studied architecture and technology. This discussion will then focus on the determination of design constrains that includes the detrimental effects observed in this study.

5.1.1 Architecture and technology limitations

If the pixel design has shown good performances in term of optimization, several problems appeared in the process. They will be recalled for each block hereunder.

The **photoreceptor** design was the most successful. Indeed, thanks to the optimization process, it results in a photosensing circuit providing an already high dynamic range (120dB), a good ratio between the photodiode size and the circuitry and minimum robustness against corner and pixel-to-pixel variation. The definition of LOD and LOF has also enabled to give a former definition the lower working limits, hence delimiting in a more precise way the dynamic range. This lower limit has been fixed by the dark current generate by the photodiode. However, as the gate leakage of the CS transistor tends to be higher than the dark current, it might play a role in the lower limit of functioning. Since the CS transistor is already an HVT transistor, meaning that it already limits the leakage, a technological limitation appears here. More advanced technologies cope with this problem by the implementation of high-k oxide/metal gate transistor [43], which limits in a much more efficient way the gate leakage.

In the **SCA**, many more problems appeared: limited gain and phase margin of the proposed OTA to optimize area and power, leakage and charge injection from the switch, capacitors sizing.

Firstly, the limited gain of the OTA causes an offset at its input, which prevents the output to be correctly reset. Samsung has proposed much more simpler op-amp in its pixel [7], using the intrinsic gain of transistor. However, it is at the cost of a power increase (88nW low activity) to keep a sufficiently wide bandwidth. In the pixel presented here, the OTA has also a response to the reset falling edge that lead to small oscillations at V_{AMP}, probably due to the slightly too low phase margin. Even though this phenomenon was very limited in time, it delayed a bit the proper functioning of the amplification stage, leading to a variation in the contrast sensitivity.

Secondly, the leakage, which has already been discussed in section 3.3.3, leads to the generation of incorrect events. By discharging the capacitance of V_{AMP} voltage node, it periodically triggers events, even when the illuminance is constant.

Obviously, such phenomenon is not limited to this work but it has only been reported by Samsung that proposed a shortcut between the bulk and the drain of its PMOS switch to reduce the substrate leakage. Nonetheless, if leakage causes the problem, its reduction is not the only way to cope with it. Indeed, as shown in Fig.5.1, capacitance value of C_2 is also a key parameter to reduce self-triggered event generation: the higher the capacitance, the longer it takes to discharge it. This observation supports again the need of new capacitor implementations to increase the density while offering small sizing and stability with regards to applied voltage.

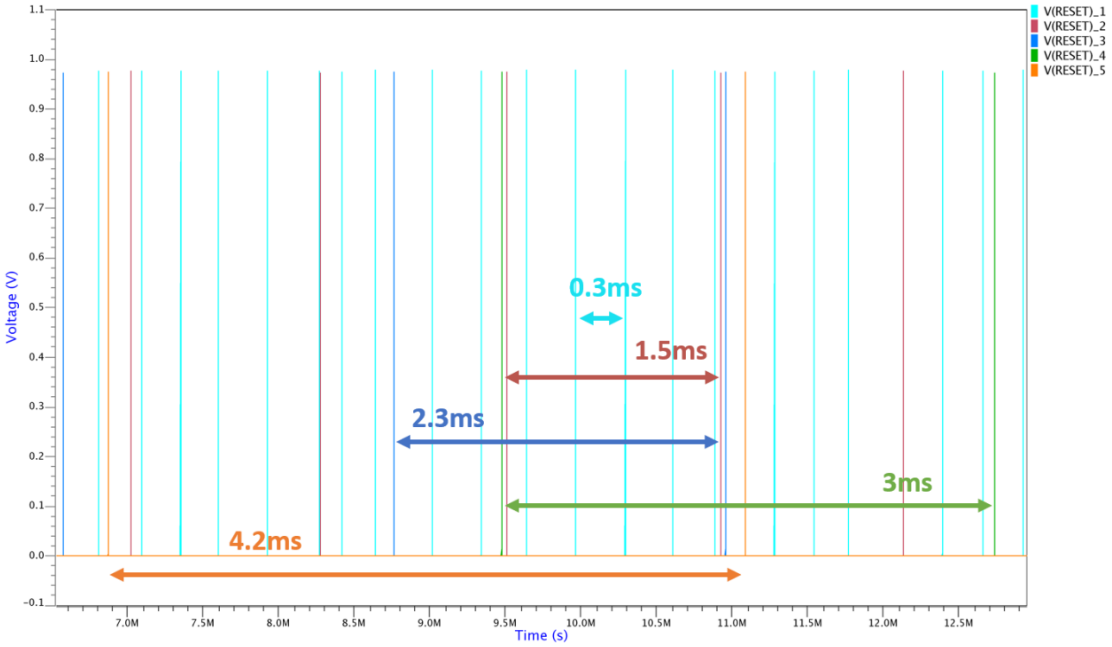

Figure 5.1: Analysis of the capacitance value on the self-triggered events generation rate: reset signal occurences, at constant photocurrent, simulated with ideal capacitors (C_1 capacitance from 0.2fF to 2.2fF, step 0.5fF, $C_2 = 15C_1$)

Concerning the SCA, the question might eventually be risen of its compatibility with DVS in scaled technologies. Indeed, this study has highlighted the technological limits inherent in the use of such amplification stage. Maybe switching current topologies might offer a novel solution to be tried in future implementation of such amplification block [42].

Thirdly, the **event and reset generator** design has also faced some problems. As the comparator are based on the same OTA architecture, they also provide a

limited gain, which is more problematic in the case of a comparator, the lower the gain, the bigger is the difference between its inputs when the output reaches the switching threshold of the following delay inverter. A solution, discovered when trying to reduce the size of the delay inverter as explained in 3.4.2, is to lower that switching threshold, hence reducing the needed voltage $\mid V_{AMP} - V_{TH} \mid$ at the input of the comparator to generate an event. It resulted in better controlled thresholds and a significant area reduction. However, modification on ON and OFF voltage thresholds should have been applied to set again the wanted contrast sensitivity and influences on V_{AMP} after the reset has been observed and should thus be further studied before including such modification in a pixel. Another drawback of such implementation might be the increased number of generated events due to noise or leakage as the switching threshold is more easily reached.

5.1.2 Proposed design guidelines for future works

A summary of constrains that should be taken into account for future pixel design is proposed hereunder. It has been built as a result of the encountered problems in this study.

The photoreceptor circuit should:

- Provide the highest possible dynamic range. If the dark current is technology related, the leakage must be reduced as much as possible to keep the lower limit fixed by the photodiode itself.
- Adapt its design methodology to the considered technology. Scaling down must be taken into account to optimize the design.
- Potentially already provide a pre-amplification stage, to reduce the gain constrain on the second block.

The differential amplification stage should:

- Provide enough gain to prevent noise interferences.
- Be asynchronously resettable to keep a temporal contrast sensitivity.
- Be as insensitive as possible to leakage and charge injection to avoid unwanted output variation.
- Provide a quick response to a reset edge.

- Provide an high output slew rate not to miss events.
- Avoid mismatch variation leading to variable gain

Finally the event an reset generator should:

- Provide precise and input independent threshold levels to avoid variation on the contrast sensitivity.
- Control the delay of the reset signal
- Avoid mismatch variation, especially in the comparators to avoid blocked states.

Following these guidelines might lead to novel implementation of DVS or to a change of technology to meet more easily these requirements. The next section will introduce the linked future perspectives for this work.

5.2 Perspectives

With the pixel design completed and discussed, the aim of the given perspectives is to highlight the future possible to study based on this master thesis.

- **FPN and mismatch correction:** it is the most important parameter to improve from this work before going further in other analysis. But since the pixel has been consequently optimized in area and power, it lets room for a few adds or modifications (feedback loops, increased size) that could correct the mismatch variability.
- **New capacitor implementation:** this work has particularly highlighted the need of smaller capacitor implementation. The idea of transistors used as capacitor has shown is limitation since even carefully designed, it provides too much variation on the capacitance value. New compact, high density and with reduced minimum sizing capacitors implementation could significantly improve the pixel as well as other capacitor based circuits.
- If the mismatch variation has been solved, the **integration of the AER communication protocol** to each pixel and to the whole sensor would be an appreciable outcome. It could allow to compare actual performance of a complete sensor with the litterature.

- Again, in the case of mismatch correction, **post-layout simulation** could be interesting, notably to see the impact of parasitic capacitances on the SCA gain. If the simulation gives promising results, **prototyping** might be considered.
- Finally, in term of optimization, the **study of backside illuminated devices** could lead to a big step in the pixel area reduction.

Conclusion

As this master thesis reaches completion, time has come to review its constituting parts and to recap their outcomes. In the first instance, a summary of existing DVS architecture has een completed. It allowed to extract two important facts:

- At that time, no optimization on area or power haad been explicitly conducted
- DVS did not take advantage of the scaling of CMOS technology

The interest in the proposed optimization in 65nm CMOS has thus been enhanced.

After their introduction in the first chapter, each photodiode type has been designed and manufactured to be tested. It resulted in a promising measured responsivity for two of the four experimented photodiode, the P-plus/N-well/P-sub and the N-well/p-sub. As the latter was slightly better, it has been chosen for the following implementation. Dark current has also been discussed. As it is supposed to be the main factor influencing the lower working limit of the pixel, it has been measured too. However, a practical and unexpected issue has added uncertainty on these results. They have been discussed and it appeared later that this mistake had had no negative impact on the designed pixel.

The main part concerning the optimized design of the pixel has been successful, at least in the main target performances, area and power. Indeed, from the photoreceptor to the event and reset generator, everything has been set up to save power and area. The proposed methodology to design the photoreceptor circuit has taken into account the scaling effect to optimize the sizing of each transistor while ensuring a good functionality over a wide range of illuminance. Technology analysis has also been carried out to wisely choose the transistor type to be used. It allowed, among other things, to boost the OTA gain without increasing the

occupied area.

The design phase ended up with a pixel presenting a pitch of $5\mu m$ which is the best area performance up to now, even without backside illuminated device as the one proposed by Samsung. It also provides a stunning power consumption of 16nW at high activity, and only 9nW at rest, which is once again the best result up to now. The latency is also kept at 7.05 μs and the dynamic range at 120dB. However the price to pay was a poorer contrast sensitivity of 19% and FPN of 8%. Moreover, in some cases, mismatch just prevents the pixel to work at all. Another type of problem also appeared in the DVS design: self-triggered events. It is defined as incorrect generated event, occuring when there is no light change. The problem and its origin has been discussed and it appeared as an architecture/technology limitation.

These limitations and guidelines to avoid them have been finally discussed in the last chapter. It proposes a set of design constrains on each block for future implementations. Next architecture and technology choices should thus consider them to avoid the encountered problems in this study.

At the end of this master thesis, it can be said that its three main targets have been met even though there is still room for improvement to possibly reach the human retina performances.

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Appendix A

OTA design flow

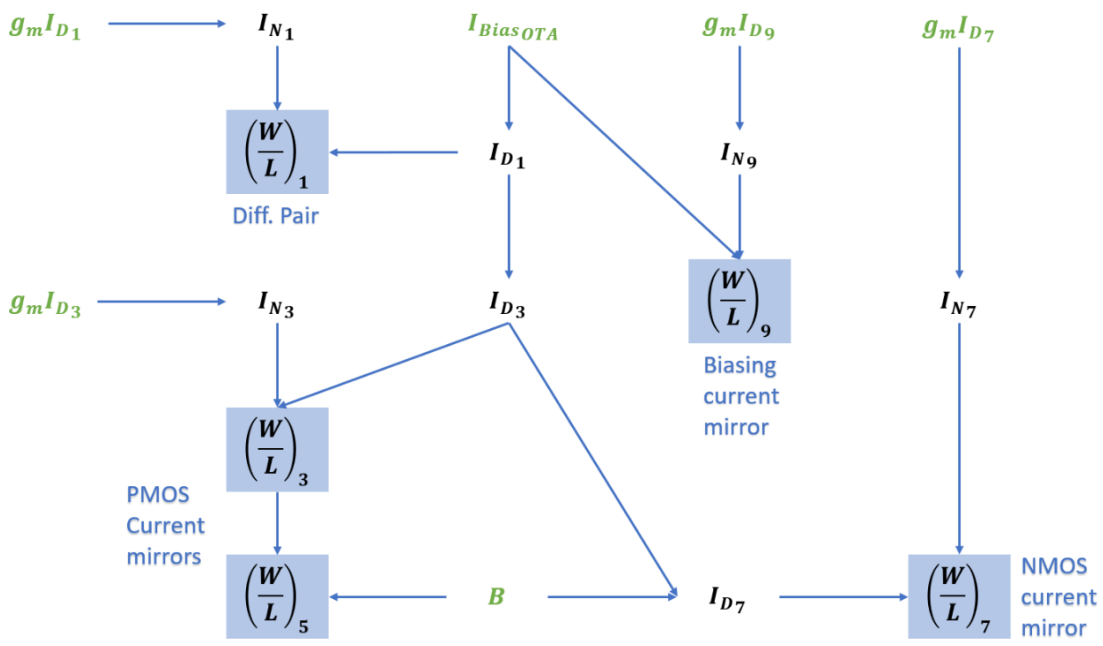

Figure A.1: Design flow of the OTA based on the $g_m I_D$ methodology

Appendix B

Pixel sizing

Photoreceptor			
Photodiode	N-well/p-sub	$4.5\mu m^2$	
PH transistor	IO	W=300nm	L=240nm
CS transitors	Core HVT	W=200nm	L=90nm
Bias transistors	Core LVT	W=80nm	L=250nm
OTA (SCA & comparators)			
M1/M2	Core LVT	W=120nm	L= $1\mu m$
M3/M4	Core HVT	W=80nm	L=500nm
M5/M6	Core HVT	W=80nm	L=250nm
M7/M8	Core HVT	W=80nm	L=500nm
M9/M10	Core LVT	W=80nm	L=350nm
SCA			
MNC1	Core HVT	W=80nm	L=60nm
MNC2	Core HVT	W=$2\mu m$	L= 200nm
MSWN	Core HVT	W=80nm	L= 130nm
MSWP	Core HVT	W=80nm	L=130nm
Event and reset generator			
MNDELAY	Core HVT NMOS	W=80nm	L= 500nm
MPDELAY	Core HVT PMOS	W=500nm	L=500nm
MNLIMIT	Core HVT NMOS	W=80nm	L=100nm
MPLIMIT	Core HVT PMOS	W=80nm	L=100nm
MPNOR	Core HVT PMOS	W=160nm	L=60nm
MNNOR	Core HVT NMOS	W=80nm	L=120nm
MPINV	Core HVT PMOS	W=160nm	L=60nm
MNINV	Core HVT NMOS	W=80nm	L=60nm

Table B.1: Summary of pixel sizing

Appendix C

Eldo Code

```
1  ************************************************
2  *
3  * Dynamic vision pixel
4  * Author: Igor Remy
5  *
6  ************************************************
7  ************************************************
8  * LIBRARIES
9  ************************************************
10
11
12 .include "Lib_access.lib"
13
14
15 ************************************************
16 * OPTIONS
17 ************************************************
18
19
20 .option be
21 *.option eps=1e-9
22 .option alignext
23 .option gmin=1e-24
24 .option aex
25 .option hmax=5n
26
27 .temp 25
```

```
.param mismatch=1
.param hfnoise=0

**********************************************
* SIZING
**********************************************

*Photoreceptor
.param par_w_photo = 0.3u
.param par_l_photo = 0.24u
.param par_l_cs = 90n
.param par_w_cs = 200n
.param par_l_bias = 250n
.param par_w_bias = 80n


*OTA's
.param l12=1u
.param w12=120n
.param l34=500n
.param w34=80n
.param l56=250n
.param w56=80n
.param l78=500n
.param w78=80n
.param l9=350n
.param w9=80n

*SCA
.param lC1= 200n
.param wC1= 2000n
.param wC2= 80n
.param lC2= 60n

*.param par_C=0.175f

.param lSW=130n
.param wSW=80n

*Logic
```

```
68
69 .param l_inv=60n
70 .param w_inv=80n
71
72
73 ********************************************
74 * SOURCES
75 ********************************************
76
77
78 .param par_vdd=1.0
79 .param par_vpd=0.25
80 vgnd gnd 0 dc 0
81 vvdd Vdd gnd dc par_vdd
82 vsub sub gnd dc 0
83
84 von_th ON_TH gnd dc 0.47
85 voff_th OFF_TH gnd dc 0.53
86 vpdref vpd_ref gnd dc  par_vpd
87 vvdd_2 VDD_2 gnd dc 0.5
88
89
90 ********************************************
91 * CIRCUIT
92 ********************************************
93
94
95 * Photoreceptor circuit *
96 ************************
97
98 *Photoreceptor transistor
99 xMNPH Vdd Vpr Vpd sub n_18_ll w=par_w_photo l=par_l_photo
100
101 *Common source transistor
102 xMNCS Vpr Vpd gnd sub n_12_llhvt w=par_w_cs l=par_l_cs
103
104 *Bias transistor
105 xMPBias Vpr shared_bias Vdd Vdd p_12_lllvt w=par_w_bias l=
      par_l_bias
106
```

```
*Shared branch
xMPBias_SH shared_bias shared_bias Vdd Vdd p_12_lllvt w=
    par_w_bias l=par_l_bias
xMNCS_SH shared_bias vpd_ref gnd sub n_12_llhvt w=par_w_cs
    l=par_l_cs

*Photocurrent generator

*Tests
*IPH Vpd gnd dc 2p PWL(0 20p 0.1m 13.3p 0.1001m 10p)
*IPH Vpd gnd dc 2p PWL(0 10p 0.1m 11p 0.1001m 14.3p)

*Rising and falling patterns + DR
*IPH Vpd gnd dc 2p PWL(0 1f 0.1m 1f 0.4m 100f 0.8m 1p 1.3m
    10p 1.6m 100p 2.2m 10n)
*IPH Vpd gnd dc 2p PWL(0 1n 0.1m 1n 0.4m 100p 0.8m 10p 1.3m
     1p 1.6m 100f 2.2m 10f)
*Power consumption
IPH Vpd gnd dc 2p PWL (0 10f 5m 10f 10m 1n 10m 1n )
*Minimum latency
*IPH Vpd gnd dc 2p PULSE (115p 149.5p 0.1m 1f 1f 40m 100m)
*FPN
*IPH Vpd gnd dc 2p PWL(0 115p 0.1m 115p 0.2m 200p)


*Photodiode
D1 gnd Vpd dionw_ll w=1.5u l=3u

* SCA *
*******

xMAMP1  N3 VA N4 sub n_12_lllvt w=w12 l=l12
xMAMP2  N1 VDD_2 N4 sub n_12_lllvt w=w12 l=l12
xMAMP3  N3 N3 Vdd Vdd p_12_llhvt w=w34 l=l34
xMAMP4  N1 N1 Vdd Vdd p_12_llhvt w=w34 l=l34
xMAMP5  N2 N3 Vdd Vdd p_12_llhvt w=w56 l=l56
xMAMP6  VAMP N1 Vdd Vdd p_12_llhvt w=w56 l=l56
xMAMP7  N2 N2 gnd sub n_12_llhvt w=w78 l=l78
xMAMP8  VAMP N2 gnd sub n_12_llhvt w=w78 l=l78
xMAMP9  NB NB gnd sub n_12_lllvt w=w9  l=l9
```

```
xMAMP10 N4 NB gnd sub n_12_lllvt w=w9  l=l9
IAMP    Vdd NB dc 1n

*Real cap
xMC1  VA Vpr VA VA p_12_llhvt w=wC1 l=lC1
xMC2  VA VAMP VA VA      p_12_llhvt w=wC2 l=lC2

*Ideal cap
*C1 VA Vpr '15*par_C'
*C2 VA VAMP par_C

xMSWN   VAMP RESET VA gnd n_12_llhvt w=wSW l=lSW
*Complementary
xMSWP   VAMP RESETN      VA Vdd p_12_llhvt w=wSW l=lSW

*Dummy
*xMSWDUM VAMP RESETN VAMP Vdd n_12_llhvt w=wSW l=lSW
*Ideal
*ysw vswitch VA VAMP RESET RESETN VON=0.51 VOFF=0.49 LEVEL
   =1 RON=10

* Comparators *
***************

xMCOMPON1 N3ON VAMP N4ON sub n_12_lllvt w=w12 l=l12
xMCOMPON2 N1ON ON_TH N4ON        sub n_12_lllvt w=w12 l=l12
xMCOMPON3 N3ON N3ON Vdd Vdd p_12_llhvt w=w34 l=l34
xMCOMPON4 N1ON N1ON Vdd Vdd p_12_llhvt w=w34 l=l34
xMCOMPON5 N2ON N3ON Vdd Vdd p_12_llhvt w=w56 l=l56
xMCOMPON6 ON_EVENT N1ON Vdd Vdd p_12_llhvt w=w56 l=l56
xMCOMPON7 N2ON N2ON gnd sub n_12_llhvt w=w78 l=l78
xMCOMPON8 ON_EVENT N2ON gnd sub n_12_llhvt w=w78 l=l78
xMCOMPON9 NBON NBON gnd sub n_12_lllvt w=w9  l=l9
xMCOMPON10 N4ON NBON gnd sub n_12_lllvt w=w9  l=l9
ICOMPON Vdd      NBON dc 0.1n

xMCOMPOFF1 N3OFF OFF_TH N4OFF sub n_12_lllvt w=w12 l=l12
xMCOMPOFF2 N1OFF VAMP N4OFF sub n_12_lllvt w=w12 l=l12
xMCOMPOFF3 N3OFF N3OFF Vdd Vdd p_12_llhvt w=w34 l=l34
xMCOMPOFF4 N1OFF N1OFF Vdd Vdd p_12_llhvt w=w34 l=l34
```

```
182 xMCOMPOFF5 N2OFF N3OFF Vdd Vdd p_12_llhvt w=w56 l=l56
183 xMCOMPOFF6 OFF_EVENT N1OFF Vdd Vdd p_12_llhvt w=w56 l=l56
184 xMCOMPOFF7 N2OFF N2OFF  gnd sub n_12_llhvt w=w78 l=l78
185 xMCOMPOFF8 OFF_EVENT N2OFF       gnd sub n_12_llhvt w=w78 l=
    l78
186 xMCOMPOFF9 NBOFF NBOFF gnd sub n_12_lllvt w=w9  l=l9
187 xMCOMPOFF10 N4OFF NBOFF gnd sub n_12_lllvt w=w9  l=l9
188 ICOMPOFF Vdd NBOFF dc 0.1n
189
190 * Logic reset *
191 ***************
192
193 IinvVdd biasp gnd 1n
194 Iinvgnd Vdd biasn 1n
195
196 xMINVNB gnd1 biasn gnd sub n_12_llhvt            l=100n w=80
    n
197 xMINVNB_SH biasn biasn gnd sub n_12_llhvt        l=100n w=80
    n
198
199 xMINVPB Vdd1 biasp Vdd Vdd p_12_llhvt            l=100n w=80
    n
200 xMINVPB_SH biasp biasp Vdd Vdd p_12_llhvt        l=100n w=80
    n
201
202 * Inverters ON_EVENT
203
204 xMINVONN1 VON1 ON_EVENT gnd sub n_12_llhvt w=80n l=500n
205 xMINVONP1 VON1 ON_EVENT Vdd1 Vdd p_12_llhvt w=500n l=500n
206
207
208 xMINVONN2 OR_ON VON1 gnd1 sub n_12_llhvt w=80n l=500n
209 xMINVONP2 OR_ON VON1 Vdd Vdd p_12_llhvt w=500n l=500n
210
211 * Inverters OFF_EVENT
212
213 xMINVOFFN1 VOFF1 OFF_EVENT gnd sub       n_12_llhvt w=80n  l
    =500n
214 xMINVOFFP1 VOFF1 OFF_EVENT Vdd1 Vdd p_12_llhvt w=500n l=500
    n
```

```
215
216
217 xMINVOFFN2 OR_OFF VOFF1 gnd1 sub n_12_llhvt w=80n l=500n
218 xMINVOFFP2 OR_OFF VOFF1 Vdd Vdd p_12_llhvt w=500n l=500n
219
220
221 * Inverter RESET
222
223 xMINVRESN  RESETN RESET gnd sub n_12_llhvt w=w_inv    l=
        l_inv
224 xMINVRESP  RESETN RESET Vdd Vdd p_12_llhvt w=2*w_inv l=
        l_inv
225
226 *OR1_ON_OFF
227 xMOR1 NOR1 OR_OFF Vdd Vdd p_12_llhvt w=2*w_inv l= l_inv
228 xMOR2 NOR2 OR_ON NOR1 Vdd p_12_llhvt w=2*w_inv l= l_inv
229 xMOR3 RESET NOR2 Vdd Vdd p_12_llhvt w=2*w_inv l= l_inv
230 xMOR4 RESET NOR2 gnd sub n_12_llhvt w=w_inv l= l_inv
231 xMOR5 NOR2 OR_ON gnd sub n_12_llhvt w=w_inv l= 2*l_inv
232 xMOR6 NOR2 OR_OFF gnd sub n_12_llhvt w=w_inv l= 2*l_inv
233
234
235 ********************************************
236 * SIMULATIONS
237 ********************************************
238
239
240 *.step param par_C 0.2f 2.2f 0.5f
241 .ic v(RESET)=0v v(VAMP)=0.5v v(VA)=0.5v v(RESETN)=1v
242 .tran 0.1m 15m
243 *.mc 1000 all
244 *.meas tran IPH1 FIND I(IPH) WHEN v(RESET)=0.5 RISE=1 TD
        =0.1m
245 *.meas tran IPH2 FIND I(IPH) WHEN v(RESET)=0.5 RISE=2 TD
        =0.1m
246 *.extract tran label=Contrast ((IPH2/IPH1)-1)*100
247 *.step param lSW 100n 180n 10n
248
249
250 .probe all
```

```
251
252
253 ********************************************
254 *  END
255 ********************************************
```

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