

École polytechnique de Louvain

RF test structures with a limited metallization stack for evaluation of the upcoming 10 nm FD-SOI technology

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Abstract

The European Chip Act and France 2030 plan invested in the development of a new generation of Fully-Depleted-Silicon-on-Insulator (FD-SOI), aiming to go to 10-nm node and beyond [1]. This work takes place in the context of the *NextGen* project. CEA is actively working on it, along with other industrial and academic organisations. This work focuses on RF test structures, more specifically, analytical and EM simulation tools that can help backup design choices in the conceptualization of RF test structures for a first FD10 test mask.

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List of Symbol

μ_r Permittivity.

$\tan\delta$ Loss tangent.

Z_c Characteristic impedance.

ϵ_r Relative dielectric constant.

ϵ_{eff} Effective dielectric constant.

ρ Conductivity.

l_{eff} Effective electrical length.

t_{cond} Conductor thickness.

t_{substr} Substrate thickness.

List of Acronyms

ADS Advanced Design Systems.

BOX Buried Oxide.

CAD Computer-aided design.

CILD Controlled Impedance Line Designer.

CPW Coplanar Waveguide.

DUT Device Under Test.

EM Electromagnetic.

FD-SOI Fully-Depleted-Silicon-on-Insulator.

FD28 Fully Depleted (SOI) 28 nm.

GaN Gallium Nitride.

GSG Ground-Signal-Ground.

HR High Resistivity.

ICs Integrated Circuits.

IF Intermediate Frequency.

IoT Internet of Things.

ISS Impedance Standard Substrate.

LO Local Oscillator.

LRM Line-Reflect-Line.

LRRM Line-Reflect-Reflect-Match.

MOSFET Metal–Oxide–Semiconductor Field-Effect Transistor.

MTRL Multiline Thru-Reflect-Line.

PD-SOI Partially-Depleted-Silicon-on-Insulator.

S-parameter Scattering parameter.

SCEs Short-Channel effects.

SOI Silicon-on-Insulator.

SOLT Short-Open-Load-Thru.

STD Standard.

TEM Transverse Electromagnetic.

TRL Through-Reflect-Line.

TV0 Test Vehicule 0.

UTB Ultra-Thin Body.

UTBB Ultra-Thin Body and Ultra-Thin BOX.

VNA Vector Network Analyser.

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Chapter 1

Introduction

1.1 Semiconductor devices scaling

The semiconductor industry follows a roadmap dictating the future needs of the industry. In 1965, Moore published a paper [2] stating that the number of transistors per chip would double every two years. This trend has been followed for years until the downscaling has reached the 100-nm range, where it becomes increasingly difficult to continue the downscaling due to multiple undesirable effects, such as the Short-Channel effects (SCEs) and high leakage currents, that appear in smaller dimension devices. To overcome SCEs, researchers have then investigated the use of new materials with a lower dielectric constant, new metals, strains or new architectures Silicon-on-Insulator (SOI) technology [3].

Although investigations of devices made with alternative channel materials, such as Gallium Nitride (GaN) used in power devices, Silicon (Si), SiGe and GaAs to name a few are still the leading materials used in the semiconductor industry. Silicon substrate is the type of substrate of interest in this work.

1.2 Silicon-on-Insulator (SOI)

Silicon-on-Insulator (SOI) technology has been investigated in recent decades because the traditional bulk Si substrate Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) has reached its limits in terms of downscaling. SOI technology has offered a breakthrough, allowing further downsizing in the nanometer range. Nowadays, SOI technology is widely used in Integrated Circuits (ICs) and all kinds of electronics. It has replaced its conventional bulk Si substrate counterpart thanks to its better reliability, larger temperature range, less parasitic capacitances and greater operating speed and performance [4].

SOI technology is done by placing an insulating layer, Buried Oxide (BOX), under the channel. This addition helps to reduce parasitic capacitances and leakage currents. This technology results in faster and less energy-intensive chips compared to the conventional MOSFETs on bulk Si. Moreover, SOI has a similar fabrication to CMOS but it does not need separated n-well and p-well, simplifying the manufacturing process [3].

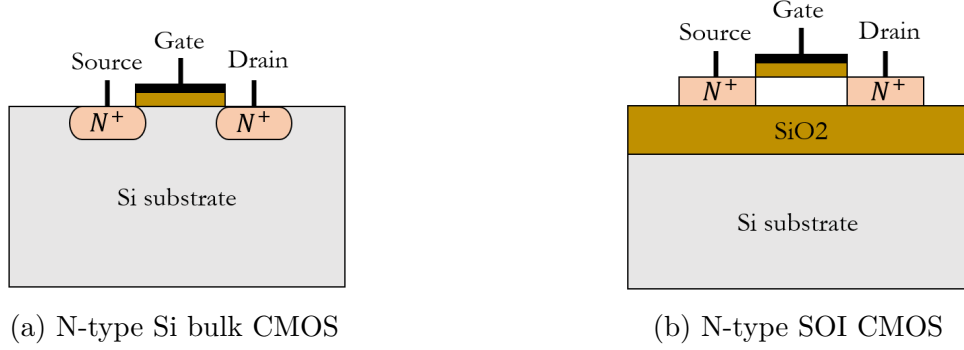


Figure 1.1: Si bulk and SOI CMOS comparison.

There are two types of SOI: Partially-Depleted-Silicon-on-Insulator (PD-SOI) and Fully-Depleted-Silicon-on-Insulator (FD-SOI). The main differences between the two reside in the thickness of the silicon layer and the doping of the channel. The FD-SOI has a thinner silicon layer on top of its BOX. This allows the FD-SOI to have a channel with no mobile charges, preventing it from suffering the floating body effects like the PD-SOI does [3].

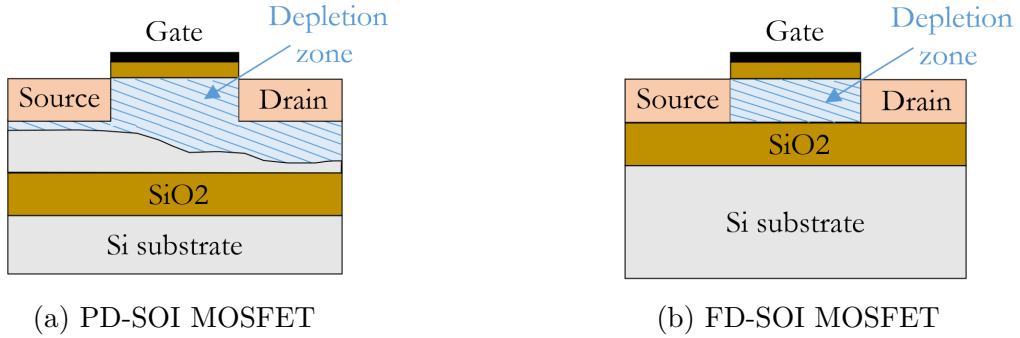


Figure 1.2: PD-SOI and FD-SOI MOSFETs comparison.

1.2.1 Fully-depleted-Silicon-on-Insulator (FD-SOI)

The focus of this work is FD-SOI technologies, more specifically, planar FD-SOI. There are two types of FD-SOI: planar and three-dimensional (3D). The planar FD-SOI have a very thin layer of silicon and can also be called Ultra-Thin Body (UTB) devices. A more advanced variant is the Ultra-Thin Body and Ultra-Thin BOX (UTBB), with a BOX that is thinned out. There are also multiple types of three-dimensional FD-SOIs with different shapes of channels, but these types of devices are not the subject of discussion in this work [3].

1.3 Context and motivation

Europe has historically been active in manufacturing, design and R&D in the micro-electronic field, in particular a leader in SOI. The COVID-19 pandemic has brought to light the dependency of the European Union on Asian microelectronic manufacturers. After that revelation, different investment plans, such as the European Chips Act and the France 2030 plan, were launched to revive the microelectronic activities in the European and French technological hubs so to regain sovereignty and competitiveness in future markets [5].

This work was done alongside an internship at the "Commissariat à l'énergie atomique et aux énergies alternatives" (CEA). Its English name is the "French Alternative Energies and Atomic Energy Commission". I worked under the supervision of Dr. Luca Lucci, as my industrial supervisor and Prof. Jean-Pierre Raskin as my academic supervisor. CEA is a major Research and Technology Organisation based in France delving mainly into low-carbon energy, digital technology, medicine for the future and defence and national security [5]. I was hired in the context of the "NextGen" project that takes place as part of the European Chips Act and the France 2030 plan. CEA, Soitec, GlobalFoundries and STMicroelectronics collaborate together in the scope of this project [6]. The goal is to develop a new generation of FD-SOI chips, going beyond the 10-nm nodes, for quicker and less energy-expensive chips. In the current industry, 28 and 22 nm FD-SOI components are already being massively produced. The will is to further scale down to be able to meet the future needs for faster and low-cost chips used in communications, automobiles and Internet of Things (IoT) for instance [1].

At the present stage, researchers are working on the conceptualizing towards a first FD10 test mask. This work in particular focuses on the RF applications of said new generation of FD-SOI.

1.4 Goal and methodology

In this work, transmission lines and simple test structures from different technologies were investigated. The test structures were characterised using various methods and simulation tools, each with different accuracy and level of setup complexity. To test the reliability of those characterization techniques and tools, they were first applied to an Impedance Standard Substrate (ISS) and a FD28 experiment for which measurements are available and can help to evaluate the performance of the simulations.

The final goal is to be able to use those techniques on a real set of unmeasured lines that need to be analyzed. In this case, the targeted lines to characterize are lines designed for a first FD10 test mask. That test mask is still in the design phase and is to be sent out for manufacturing for future on wafer tests and characterizations. What is done in this can help the design of the FD10 RF test structures because if properly done, the simulations can give an insight on the de-

signed structures' behaviors. It will help to optimize the structure's geometry to get close to the desired characteristics and avoid sending bad test structures for manufacturing and discover later on that what was designed is far from what was expected.

Chapter 2 is dedicated to the theoretical background needed in the scope of this work. The theory behind transmission line will be detailed. A quasi-TEM description of coplanar lines will be explained. VNA calibration techniques and de-embedding techniques used on the results are also summarized in this chapter. Finally, the simulation tools used on the different sets of data are briefly introduced.

In Chapter 3, the Impedance Standard Substrate (ISS) lines and the structures available for the FD28 experiment are detailed and illustrated.

Chapter 4 reproduces the results perceived from the data presented in the previous chapter. The different characterization techniques and simulators are tested and accessed.

Chapter 5 is dedicated to the analysis for the first FD10 test mask (TV0). The BEOL and the lines of interest are presented. Then, the results of the simulations done on those lines are showcased. It illustrates how the techniques discussed so far can be used on unknown lines to reach a desired behavior.

This work finishes with conclusions and perspectives.

Chapter 2

Theoretical background

2.1 Transmission lines

A transmission line is "a manufactured transmission medium used to convey electromagnetic energy between two points with a minimum of radiation" [7]. They are usually composed of two or more conductors with dielectric materials between them.

Transmission lines can serve different purposes, ranging from linking circuit components to being part of passive circuits, e.g. filters or power dividers [8]. Depending on the usage of the transmission lines, they can have different configurations, exhibiting distinct behaviors and properties.

First, the theory behind transmission lines will be explained. Then, three popular line types used in this work will be detailed.

2.1.1 Transmission line theory

Pozar gave an extensive explanation of the theory behind transmission lines in his book [9]. Due to its small size, a transmission line is considered as a distributed-parameter network. It can be characterized entirely by its characteristic impedance, propagation constant and line length, giving insight into the transmission line's behavior. Mongia states that the characterization of transmission lines can be further boiled down to the single determination of the capacitance of the structure [10].

A transmission line can be schematized as a two-wire line, along the z -direction, as shown in Figure 2.1. It is highly desirable to have Transverse Electromagnetic (TEM) or quasi-TEM propagation mode. To be able to carry those types of waves, there are always at least two conductors in the line. TEM waves happen between two or more conductors and have no electric or magnetic wave components in the direction of the propagation.

The voltage and current can vary along the line. Therefore, we only look at an infinitesimal segment of it. The lumped-element equivalent circuit, shown in Figure 2.2, is often used to model that infinitesimal part. This equivalent circuit is called the

$RLGC$ equivalent circuit because it is composed of those four lineic circuit elements, as described as follows.

R is a per unit length resistance [Ohm/m] which is a consequence of the non-infinite conductivity of the transmission line conductors. L is the total self-inductance [H/m] present between the conductors. The per-unit length capacitance C [F/m] is caused by the closeness of the conductors and finally, the shunt conductor G [S/m] represents the loss of the dielectric situated between the conductors.

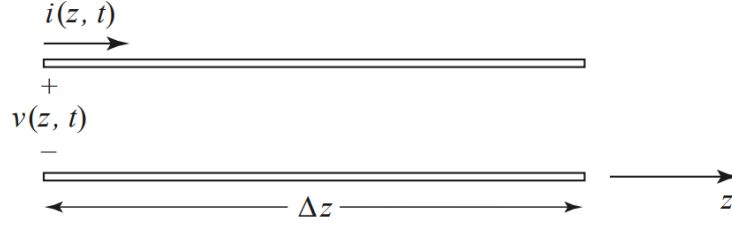


Figure 2.1: Two wires transmission line representation [9].

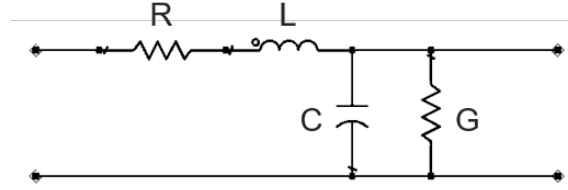


Figure 2.2: $RLGC$ lumped-element equivalent model.

A transmission line can be described in the time domain by the *Telegrapher equations* [9]:

$$\frac{\partial v(z, t)}{\partial z} = -R i(z, t) - L \frac{\partial i(z, t)}{\partial t}, \quad (2.1)$$

$$\frac{\partial i(z, t)}{\partial z} = -G v(z, t) - C \frac{\partial v(z, t)}{\partial t} \quad (2.2)$$

These equations are obtained by applying Kirchhoff's laws on the $RLGC$ equivalent model and by performing some simple mathematical operations [8].

The Telegrapher Equations can be simplified using the phasor notation in a sinusoidal steady-state condition as:

$$\frac{dV(z)}{dz} = -(R + j\omega L)I(z), \quad (2.3)$$

$$\frac{dI(z)}{dz} = -(G + j\omega C)V(z). \quad (2.4)$$

By taking the square of the equations 2.3 and 2.4 and by defining a complex propagation constant as:

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}, \quad (2.5)$$

in $[1/\text{m}]$, with α the attenuation constant $[\text{Np}/\text{m}]$ and β the phase constant $[\text{rad}/\text{m}]$. We thus have:

$$\frac{d^2 V(z)}{dz^2} - \gamma^2 V(z) = 0, \quad (2.6)$$

$$\frac{d^2 I(z)}{dz^2} - \gamma^2 I(z) = 0. \quad (2.7)$$

By solving 2.6 and 2.7, the solutions to the Telegrapher equations can be deduced:

$$V(z) = V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z}, \quad (2.8)$$

$$I(z) = I_0^+ e^{-\gamma z} + I_0^- e^{\gamma z}, \quad (2.9)$$

where $e^{-\gamma z}$ and $e^{\gamma z}$ represent the wave propagation in the $+z$ and $-z$ directions, respectively. This solution 2.8 is the superposition of two exponentially decaying voltage waves travelling in opposite directions. From that, it can be seen that the propagation constant γ has a controlling effect on the attenuation and wavelength, making it one of the key parameters to characterize a transmission line [8, 9].

By injecting 2.8 into 2.3, the current in a transmission line can be then expressed as follows:

$$I(z) = \frac{\gamma}{R + j\omega L} (V_0^+ e^{-\gamma z} + V_0^- e^{\gamma z}). \quad (2.10)$$

By definition, the characteristic impedance of the line is the following ratio of the voltage and current waves, making it possible to express it with the *RLGC* elements:

$$Z_c := \frac{V_0^+}{I_0^+} = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}. \quad (2.11)$$

The phase velocity of such a line is:

$$v_p = \frac{\omega}{\beta} = \lambda f, \quad (2.12)$$

in $[\text{m}/\text{s}]$, with the angular frequency ω in $[\text{rad}]$, the frequency f in $[\text{Hz}]$ and the wavelength λ in $[\text{m}]$.

Likewise, the *RLGC* parameters can be expressed with the characteristic impedance as follow [11]:

$$R = \text{Re}(\gamma Z_c) \quad (2.13)$$

$$L = \text{Im}(\gamma Z_c)/\omega \quad (2.14)$$

$$G = \text{Re}(\gamma/Z_c) \quad (2.15)$$

$$C = \text{Im}(\gamma/Z_c)/\omega \quad (2.16)$$

These formulas hold under quasi-static conditions [10].

Lossless and low-loss lines

When the line is lossless or can be considered as nearly lossless, the expressions mentioned above can be simplified, thus significantly decreasing the computational time, and making the characterization easier to perform. Therefore, in practice, transmission lines are often intently designed to achieve low losses [8].

In lossless lines, it is considered that R and G are equal to zero, leading to the following simplification of the propagation constant [8]:

$$\gamma = \alpha + j\beta = j\omega\sqrt{LC}, \quad (2.17)$$

$$\alpha = 0, \quad (2.18)$$

$$\beta = \omega\sqrt{LC}, \quad (2.19)$$

The characteristic impedance and propagation velocity are also simplified:

$$Z_c = \sqrt{\frac{L}{C}}, \quad (2.20)$$

$$v_p = \frac{\omega}{\beta} = \frac{1}{\sqrt{LC}}. \quad (2.21)$$

The propagation constant under lossless conditions is purely imaginary and the characteristic impedance becomes purely real and independent of the frequency.

Real transmission lines are longer and are not able to remain lossless due to the decay of the waves propagated along the line. This has been observed from the solution of the Telegrapher equations in 2.8. Longer lines therefore have non-zero attenuation constant. It was shown in [8] that the lossless characteristic impedance and phase constant β are acceptable approximations of the low-loss case. The attenuation constant α is the sum of the dielectric and metallic losses, which depends on the losses R and G in the equivalent circuit.

Transmission line characterization reduced to a problem of capacitances

As mentioned previously, Mongia explains in his book [10] that the determination of the characteristic impedance and the propagation constant boils down to the determination of two capacitances. It states: "For TEM (or quasi-TEM) modes, the determination of important characteristics (such as the characteristic impedance and phase velocity of single and coupled lines) reduces to finding the capacitances associated with the structure".

If the dielectric medium surrounding the transmission line conductor is homogeneous, the propagation of the wave is TEM. In practice, a lot of transmission lines do not meet this criteria. In that case, Mongia states: "If the separation between the conductors of an inhomogeneous transmission line is very small compared to the wavelength; the mode of propagation on the line can be considered to be close to TEM; called quasi-TEM" [10].

Characteristic impedance can be expressed with propagation velocity and capacitance. In the end, the problem of finding it can be reduced to the problem of determining capacitance.

In TEM propagation mode, the following formulas stand:

$$Z_c = \frac{1}{v_p C} \quad (2.22)$$

$$v_p = \frac{c}{\sqrt{\epsilon_r}} \quad (2.23)$$

$$Z_c = \frac{\sqrt{\epsilon_r}}{cC} \quad (2.24)$$

$$= \frac{1}{c\sqrt{\epsilon_r}C_0} \quad (2.25)$$

with C_0 the capacitance for a transmission line in a dielectric material of unity dielectric constant [F/m], ϵ_r the relative dielectric constant [/] and c the speed of light [m/s].

For the quasi-TEM case, an effective dielectric constant ϵ_{eff} is introduced because the dielectric medium is not homogeneous.

$$\epsilon_{eff} = \frac{c^2}{v_p^2} \quad (2.26)$$

$$\beta = \frac{\omega}{v_p} = \frac{\omega\sqrt{\epsilon_{eff}}}{c} \quad (2.27)$$

In quasi-static limits, it can be assumed that:

$$\epsilon_{eff} = \frac{C}{C_0} \quad (2.28)$$

with C and C_0 the capacitance of the transmission line in the inhomogeneous and the one between the same conductors but in empty with all dielectrics removed, respectively.

Then, the characteristic impedance becomes:

$$Z_0 = \frac{\sqrt{\epsilon_{re}}}{cC} \quad (2.29)$$

$$= \frac{1}{c\sqrt{CC_0}} \quad (2.30)$$

$$= \frac{1}{c\sqrt{\epsilon_{re}C_0}} \quad (2.31)$$

This highlights the importance of the capacitance associated with the structure in the determination of the characteristic impedance and the overall characterization of a transmission line. The accuracy of that capacitance needs to be high in order to correctly characterize a transmission line.

2.1.2 Types of transmission lines

There exist multiple types of transmission lines that can serve different purposes. Coaxial lines and striplines have homogeneous dielectric medium around the conductors and therefore support TEM mode of propagation. Microstrip lines and coplanar waveguides are types of planar transmission lines. They can only support quasi-TEM mode of propagation.

Microstrip and Coplanar Waveguide (CPW) are the types of transmission lines of interest in this work. They are described more in detail in the following.

Microstrip

Microstrip lines are composed of a strip conductor placed on top of a dielectric substrate with a ground plane on the bottom, as illustrated in Figure 2.3. The dielectric medium surrounding the conductor is not homogeneous. The microstrip line has part of the fields in the dielectric region and also in the air above the conductor (see Figure 2.4). The phase velocity in the dielectric region and the one in the air are different, so this type of transmission line does not support pure TEM wave propagation. However, in the case where the dielectric substrate is thin enough ($d \ll \lambda$), the fields are quasi-TEM. The static solutions provide good approximations for the characterization of a microstrip line at low frequency [9].

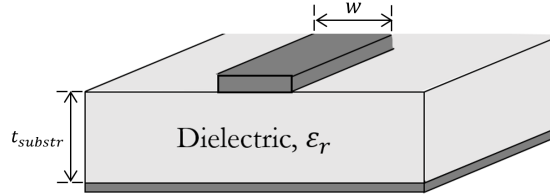


Figure 2.3: Geometry of a microstrip line.

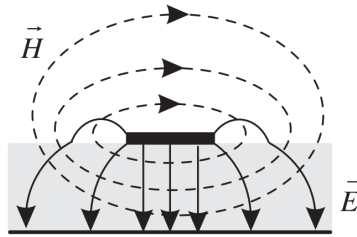


Figure 2.4: Electric and magnetic fields distribution for a microstrip line [8].

Coplanar Waveguide

Coplanar Waveguide (CPW) lines also have a strip conductor carrying the signal. What makes the coplanar line different is the fact that there are two ground planes located on the same plane as the signal strip, on each side of it, as shown in Figure 2.5. In real coplanar waveguides, the two ground planes are of finite widths. The electric fields are concentrated in the region of the conductor strip and the ground

planes. Like the microstrip line, coplanar lines carry quasi-TEM waves due to the inhomogeneous dielectric medium (see Figure 2.6). This type of lines are used in active circuits because of how close the grounds are to the signal strip [8, 9].

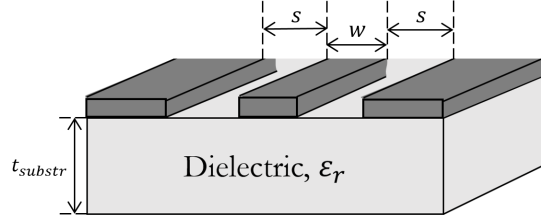


Figure 2.5: Geometry of a CPW line.

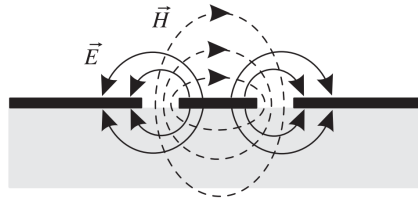


Figure 2.6: Electric and magnetic fields distribution for a CPW line [8].

2.1.3 Quasi-TEM description of coplanar lines

Wolfgang Heinrich has proposed in his paper closed-form equations for describing CPW transmission lines [12]. The described method performs an approximation of a CPW line based on its physical parameters to extract, in quasi-TEM conditions, the *RLGC* elements from the equivalent circuit drawn in Figure 2.2.

The paper describes in detail the closed-form mathematical expressions used to approximate the full-wave model. It results in a considerable saving in computational expenses and allows it to be reproduced and applied using Computer-aided design (CAD) tools. In the paper, the errors of the approximations are evaluated and compared to the full-wave results. They are considered acceptable for practical instances of CPW lines. Effects such as the non-ideality and finite thicknesses of the transmission lines conductors as well as the losses in the substrate are being considered in the proposed model. The consideration of these non-idealities is proven to be required for a reliable model of the transmission lines.

From the full-wave solutions, C and G/ω can be considered as frequency independent. On the other hand, a dependency of the R and L to the frequency can be perceived due to the skin effect, which occurs at high frequencies when the current distribution is concentrated close to the surface of the conductors.

The behavior of the lineic capacitance C changes with the thickness of the conductors. By assuming infinite ground planes and by not considering the impact of the backside metallization, the extraction of the C can be equivalent to the extraction

of the quarter of that capacitance. A first-order approach is used to approximate the quarter capacitance for a small finite thickness. When the conductor thickness exceeds half of the spacing between the signal strip and the ground planes, the capacitance is modelled as a parallel-plate capacitance. The G is computed similarly, with the knowledge of the loss tangent.

The R and L are frequency dependent. The R tends to its DC value at low frequencies. In the skin depth range, the R can be extracted through perturbation approach. The intermediate frequency range between the close to DC frequencies and the skin effect range, exhibits a different behavior that is modelled by a segmentation approach. The L , at skin effect range, can be separated into an internal and an external inductances, L_i and L_e . The two inductances can then be expressed as follows:

$$\begin{cases} L_e = L_{e\infty}, \\ \omega L_i = R, \end{cases} \quad (2.32)$$

with $L_{e\infty}$ being the inductance value for ideal conductors.

Below the skin effect frequency range, the lineic inductance L increases as the frequency decreases towards saturation at its DC value. The lineic inductance is determined by interval, like the lineic resistance, according to its change in behavior throughout the frequencies.

The mathematical expressions presented in Heinrich's paper are valid, up to mm-wave frequencies, for CPW lines with substrates of infinite thickness and with no backside metallization. In practice, the substrate thickness is finite. This leads to errors. A deviation of 1% was observed in the approximation of the propagation constants.

The full development is available in his paper [12], with the evaluation of the method accuracy, compared to the full-wave solutions.

Heinrich has also written a similar model for a microstrip line in [13]. It is not covered in this work but will be looked upon for further investigation.

2.2 Vector Network Analyser

A Vector Network Analyser (VNA) is a computer aided measurements instrument. It is a type of network analyzer. Unlike the scalar network analyser where only the amplitude of the signals are measured, a vector network analyser also measures the phase. It has two (or four) coaxial measurement ports with a characteristic impedance of 50 Ohm.

Scattering parameters

The Scattering parameter (S-parameter) is a highly used parameter for high-frequency measurements. It is easy to extract the impedance admittance and the $ABCD$ matrix from it, as well as other important parameters such as the characteristic impedance. Transmitted and reflected power waves can be measured by a VNA. It becomes more difficult to measure the voltage and current at higher frequencies. From the previous development, the solution to the Telegrapher equations is a combination of a forward and reflected voltage wave. Due to the difficulty of measuring voltages and currents at high frequencies, we derive the normalized power waves by taking the ratio of the voltage waves to the square root of the characteristic impedance. This gives forward and backwards propagating normalized power waves:

$$a_i = \frac{V_{0i}^+}{\sqrt{Z_{ci}}}, \quad (2.33)$$

$$b_i = \frac{V_{0i}^-}{\sqrt{Z_{ci}}}, \quad (2.34)$$

with i the port index. These power waves are expressed in $[\sqrt{W}]$.

In a two-port network, the two power waves can be linked as follows:

$$b_1 = S_{11}a_1 + S_{12}a_2, \quad (2.35)$$

$$b_2 = S_{21}a_1 + S_{22}a_2, \quad (2.36)$$

where S_{ij} are entries of the 2-ports S-parameter matrix:

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \quad (2.37)$$

The power waves and S-parameter entries are illustrated for a 2-port network in Figure 2.7.

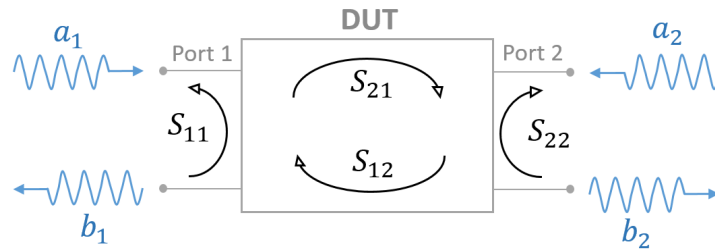


Figure 2.7: S-parameter schematic for a 2-port network.

Therefore,

$$S_{ij} = \left. \frac{b_i}{a_j} \right|_{a_k=0, k \neq j} \quad (2.38)$$

The S_{ii} entries are the input and output reflection coefficients. The other two entries are the forward and backward transmission coefficient [8, 11].

Operation principle of a VNA

Figure 2.8 illustrates the block diagram of a typical 4 channels network analyzer. During the measurements, for each frequency, a forward power wave a_i , as defined in the Equation 2.33, is generated by the RF source and injected into the Device Under Test (DUT). The VNA then measures the reflected and transmitted b_i waves.

Following the annotations on the block diagram (Figure 2.8), in the forward direction case, the incident a_1 , reflected b_1 and transmitted b_2 waves are then separated with the help of directional couplers. The VNA converts the high-frequency signals, measured from the DUT, into ones at lower frequencies (Intermediate Frequency (IF)). This is done by mixing the high-frequency signals with signals generated by the Local Oscillator (LO). Having intermediate frequency signals facilitate further transformation of them. The waves are then digitised into a_0 , b_0 and b_3 .

With that, the VNA is able to compute the reflection and transmission coefficients of the S-parameter. The other entries of the matrix are extracted by swapping the generator and termination at the RF source [8, 14, 15, 16].

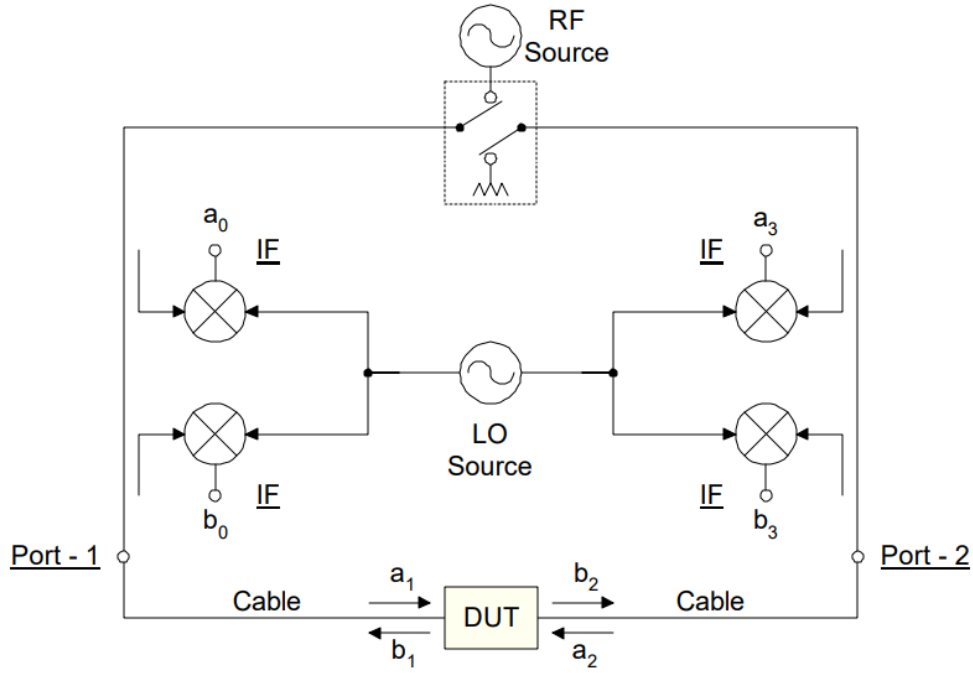


Figure 2.8: Block diagram of a 4 channel network analyzer [15].

For networks where the number of ports exceeds the ones available on the VNA, the ports that are not connected need to be terminated by the port characteristic impedance. All the scattering parameters can then be measured by connecting the ports one by one to the VNA measurement ports.

2.3 Calibration

In order to perform reliable and accurate measurements, the VNA needs to be correctly calibrated before doing the measurements. There are multiple calibration techniques available. They are also called error correction methods. They rely on the measurements of calibration standards. The calibration of a VNA before measurement can suppress the losses and reflections from the connectors, line transitions and the VNA itself by moving the reference plane at the edges of the probe tips [8]. The calibration algorithms rely on the error box model [14]. The initial reference plane before calibration is located inside the VNA [9].

2.3.1 Error box model

The error box model is a linear system modelling the systematic errors of the VNA measuring process. It has a number of error terms that need to be determined by measuring calibration standards to rid the measurements from those systematic errors. There are different error models that exist with different levels of complexity and error correction ability.

Most traditionally, the 12-Term error model is used for 2-port network calibration. The 8-Term, 10-Term and 16-Term error models, among others, were developed afterwards.

The 12-Term error model is the one used traditionally in older VNAs and is still widely used nowadays. This model, as its name suggests has 12 error terms: 6 in the forward direction and 6 in the reverse direction. This model reduces the losses and errors due to port mismatches but does not help with noise and linearity errors.

The 8-Term error model can be derived from the 12-Term error model. It makes the assumption that there is no crosstalk leakage and that the VNA switch is perfect. This error model is simpler to use and provides more accuracy, under the assumptions made.

The 16-Term error model can be considered as a variant of the 8-Term one but with the leakages taken into account, which adds 8 leakage terms. Leakage can be negligible for coaxial lines or waveguides but it can become significant in wafer probe measurements [15, 16].

8-Term error model illustration

The model is constituted of 2 error boxes modelled by two S-parameters located at the input and output of the DUT, as shown in Figure 2.9. The entries of the two S-parameters are the error terms of the model. There are therefore 8 error terms in total (e_{ij} and e'_{ij} for $i, j \in \{1, 2\}$). In practice, only 7 error terms are needed to perform the calibration. The error terms e_{12} , e_{21} , e'_{12} and e'_{21} can not be equal to zero. Any one of them can be set to a non zero value without changing the wave

quantity ratio. By fixing one of these entries to 1 for instance, that leaves only 7 error terms to be determined [14].

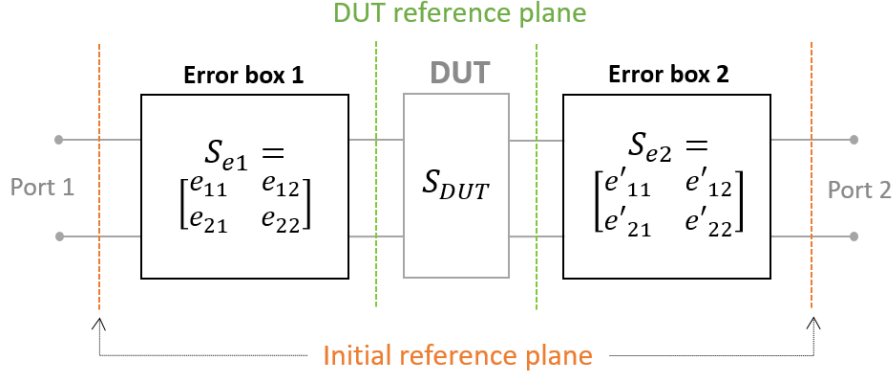


Figure 2.9: 8-Term error box model illustration.

The system to solve is a system of 8 equations with 7 unknowns, meaning that there is no need to fully know all the standards [14].

The error box model is a cascade of 2-port networks, so it is more convenient to use $ABCD$ matrix representation. The $ABCD$ matrix of the DUT (at the probe tip) can be extracted as shown in the following equations [9]:

$$\begin{bmatrix} A_{meas} & B_{meas} \\ C_{meas} & D_{meas} \end{bmatrix} = \begin{bmatrix} A_{e1} & B_{e1} \\ C_{e1} & D_{e1} \end{bmatrix} \begin{bmatrix} A_{DUT} & B_{DUT} \\ C_{DUT} & D_{DUT} \end{bmatrix} \begin{bmatrix} A_{e2} & B_{e2} \\ C_{e2} & D_{e2} \end{bmatrix} \quad (2.39)$$

$$\begin{bmatrix} A_{DUT} & B_{DUT} \\ C_{DUT} & D_{DUT} \end{bmatrix} = \begin{bmatrix} A_{e1} & B_{e1} \\ C_{e1} & D_{e1} \end{bmatrix}^{-1} \begin{bmatrix} A_{meas} & B_{meas} \\ C_{meas} & D_{meas} \end{bmatrix} \begin{bmatrix} A_{e2} & B_{e2} \\ C_{e2} & D_{e2} \end{bmatrix}^{-1} \quad (2.40)$$

The accuracy of the calibration depends on the model used or on the quality and stability of the calibration standards used. It is also relevant to note that it might be necessary to perform a calibration multiple times on a time span because the error correction can drift with time and temperature, or if the cables have moved after the calibration.

2.3.2 Calibration techniques

Short-Open-Load-Thru (SOLT), Line-Reflect-Line (LRM) and Through-Reflect-Line (TRL) are commonly used on-wafer calibration techniques with 2-port VNA. SOLT uses the 12-Term. TRL and LRRM both use the 8-Term error model [11].

SOLT

The Short-Open-Load-Thru (SOLT) calibration uses the measurements of the short, open, load and thru like its name suggests. The reference impedance is set by the load standard. This calibration method needs a precise knowledge of all the standards and accurate modelings. It can become problematic at higher frequencies as the ability of the models to predict the behavior of the standards can decrease as the frequency increases [11, 14]. This calibration technique was not used in this work.

Self-calibration techniques

Self-calibration methods do not require full knowledge of the standards. Line-Reflect-Line (LRM) and Through-Reflect-Line (TRL) are self-calibration techniques. They rely on the redundancy in the measurements and error-terms to reconstruct the missing information. They are preferred in high frequency measurements because they provide better accuracy with less constraints on the knowledge of the standards [11].

TRL and MTRL

TRL calibration relies on the measurements of a thru, reflect and a line to determine the propagation constant and the reflect standard reflection coefficients. The reference impedance is fixed by the characteristic impedance of the line standard and the reference plane is fixed in the middle of the thru. This technique has a limited range of frequency. Multiline Thru-Reflect-Line (MTRL) is a variant using more line standards measurements to perform a statistical analysis to broaden the frequency range and remedy to the disadvantage of the TRL calibration [14, 11].

In TRL, there is a trade-off between the minimizing of the error done on the propagation constant and the frequency range. Increasing the length difference between the pair of lines taken for the calibration decreases the error on the propagation constant but also reduces the frequency range. This bottleneck is remedied with MTRL [11].

For a more detailed explanation of the TRL calibration technique, please refer to [17].

LRM and LRRM

LRM calibration needs load, reflect and thru standards measurements. The load and thru must be precisely known and the reflect reflection coefficients are computed during the calibration. Like the SOLT calibration, the reference impedance is fixed by the load standard, but LRM has a wider frequency range. This calibration technique is faster to perform because it uses the same probe-to-probe distance. However, it is harder to implement [11, 14].

For a more detailed explanation of the LRM calibration technique, please refer to [18].

Other calibration techniques exist but they will not be discussed here. Only the ones used in this work are explained.

2.4 De-embedding

De-embedding is a different concept from calibration. Calibration has the goal of ridding the measurements of the systematic errors from the VNA and connections, in

order to shift the reference plane to the measuring probe tips. De-embedding has for the goal to extract the characteristics of the DUT itself in the case where the DUT is not directly accessible by the measuring probes. Then, pads and small transmission lines are needed to give access for the probes. Performing a de-embedding will move the reference plane even close to the DUT [19].

2.4.1 Common de-embedding techniques

Short de-embedding

The short "dummy" models the series parasitics in the measurements. The T-equivalent model (Figure 2.10) is used with the impedance matrix of the series parasitics [19]:

$$Z = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_1 + Z_3 & Z_3 \\ Z_3 & Z_2 + Z_3 \end{bmatrix} \quad (2.41)$$

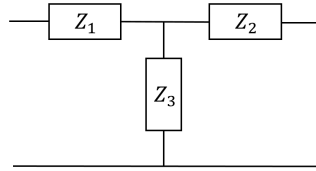


Figure 2.10: T-equivalent model of the short.

The short de-embedding subtracts the series parasitic effects by performing the following operation:

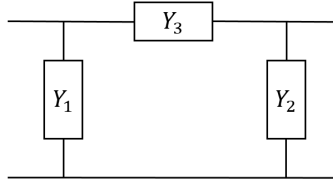
$$Z_{ShortDemb} = Z_{meas} - Z_{Short}, \quad (2.42)$$

with Z_{meas} , Z_{Short} and $Z_{ShortDemb}$ the impedance matrices of the measurements, the short dummy and the measurements after short de-embedding respectively.

Open de-embedding

The open dummy models the parallel parasitics. For convenience of manipulation of shunt elements, the admittance notation is used to model the parallel parasitics. The π -equivalent model (Figure 2.11) is used with the admittance matrix of the parallel parasitics [19]:

$$Y = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} Y_1 + Y_3 & -Y_3 \\ -Y_3 & Y_2 + Y_3 \end{bmatrix} \quad (2.43)$$


 Figure 2.11: π -equivalent model of the open.

The open de-embedding is done so that the parallel parasitic effects are removed. It is done using the following computation in admittance mode:

$$Y_{OpenDemb} = Y_{meas} - Y_{Open}, \quad (2.44)$$

with Y_{meas} the admittance matrix of the measurements, Y_{Open} the one of the open dummy and finally the admittance matrix after open de-embedding $Y_{OpenDemb}$.

Open-short de-embedding

As the name suggests, the open-short de-embedding is the combination of both the open and short de-embedding techniques. Is is performed as follow:

$$Z_{OpenDemb} = \frac{1}{Y_{OpenDemb}}, \quad (2.45)$$

$$Y_{Short} = \frac{1}{Z_{Short}}, \quad (2.46)$$

$$Z_{ShortOpen} = \frac{1}{Y_{Short} - Y_{Open}}, \quad (2.47)$$

$$Y_{OpenShortDemb} = \frac{1}{Z_{meas} - Z_{ShortOpen}}. \quad (2.48)$$

The final de-embedded results being the admittance matrix $Y_{OpenShortDemb}$.

2.4.2 Reference plane position

The reference plane of a measured S-parameter can be located at three different levels with the help of calibration and/or de-embedding: at the probe tip, on the top metal layer and at the lowest metal layer on the terminals of the transistors. These 3 positions can be visualized on Figure 2.12: at the probe tip (N° 1), at the top metal layer (N° 2) and at the device terminals (N° 3). Calibration brings the reference plane to the tip of the probes. Then, depending on the use of the measurements, the reference plane can be brought close to the device using appropriate de-embedding techniques. Some will want to include the BEOL parasitics while others desire to go down to the transistor itself for intrinsic device modeling.

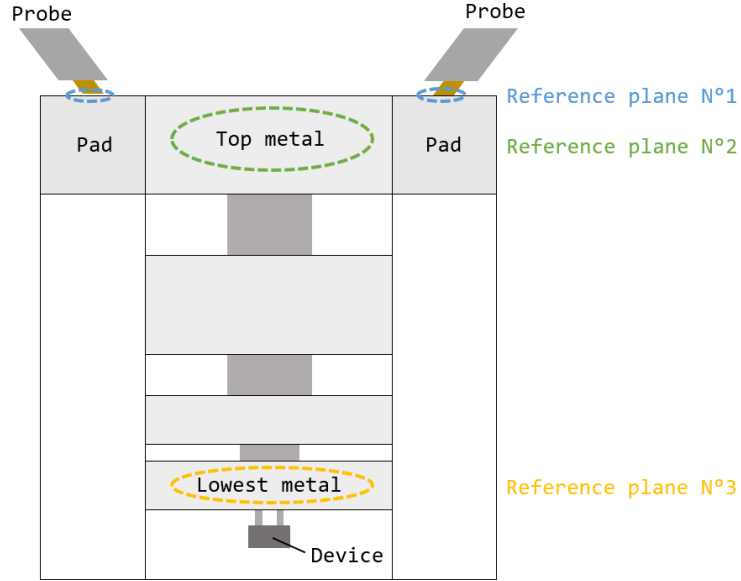


Figure 2.12: Three reference plane locations in the DUT.

When using *regular* open and/or short dummies for the de-embedding, the reference plane is brought to the top metal layer and the vias connecting the different metal layers are not modelled. In order to get to the terminal of the device, at the level of the lowest metal layer, *complete* short and/or open dummies are needed. They both replicate the metal and via stack of the DUT. The *complete* short is the replica of the DUT with the transistor removed and replaced by a line to short it. The *complete* open on the other hand is the copy of the DUT without the contact vias. *Complete* dummies allow to bring the reference plane to the device terminals but lead a significantly bigger test chip [19].

2.4.3 Mangan de-embedding

Mangan, Voinigescu, Yang and Tazlauanu have introduced a de-embedding technique for transmission line measurement in their paper [20]. This de-embedding technique is referred in this work as the *Mangan de-embedding* for simplicity. The method is applied on symmetric transmission lines. The goal is to de-embed the parasitic part of the pad and the transient part of the line to extract only the measurements with a Quasi-TEM wave behavior of a symmetric line. As mentioned in the paper, instead of relying solely on lumped equivalent circuits, this method allow a modeling of the parasitic effects using symmetric transmission line test structures of different lengths.

This way, "there is not more need for explicit models of the pad parasitic or calibration of the VNA." This technique takes two transmission lines of lengths l_1 and l_2 , $l_1 < l_2$ and makes the assumption that "the left pad can be modeled solely by a lumped admittance, Y_L ". The de-embedding algorithm multiplies the $ABCD$ matrix of the long transmission line with the inverse of the short line matrix in order to extract the $ABCD$ matrix of a line segment of length $l_2 - l_1$. This operation is illustrated in Figure 2.13.

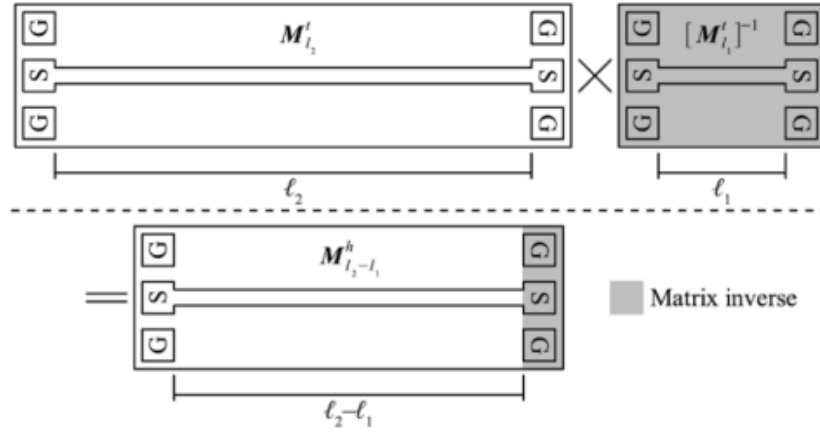


Figure 2.13: Illustration of the matrices operations for Mangan de-embedding technique [20].

Assuming that a lossy transmission line of length $l_2 - l_1$ can be modeled by

$$\mathbf{M}_{l_2-l_1} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \quad (2.49)$$

$$= \begin{bmatrix} \cosh \gamma(l_2 - l_1) & Z_c \sinh \gamma(l_2 - l_1) \\ Z_c^{-1} \sinh \gamma(l_2 - l_1) & \cosh \gamma(l_2 - l_1) \end{bmatrix} \quad (2.50)$$

with $\mathbf{M}_{l_2-l_1}$ the $ABCD$ matrix of the line with length $l_2 - l_1$, Z_c its characteristic impedance and γ its propagation constant. Then we can express the characteristic impedance and the propagation constant as

$$Z_c = \sqrt{\frac{B}{C}} \quad (2.51)$$

$$\gamma = \frac{\cosh A^{-1}}{l_2 - l_1} \quad (2.52)$$

Therefore, with just the S-parameter of two transmission line test structures, it is possible to deduct the characteristic impedance and the propagation constant of the segment of the long line without the parasitic effects of the pads and the transient region of the electromagnetic waves. A detailed description of the algorithm and examples of the method applied to measurements of microstrip test structures are shown in [20].

2.5 Simulation tools

Three different simulation tools, from Keysight ADS (Agilent) Technologies, with increasing levels of complexity were used in this work. *LineCalc* and *Controlled Impedance Line Designer (CILD)* are two analytical simulation tools while *Momentum* provide Electromagnetic (EM) simulation results.

2.5.1 LineCalc

LineCalc is "an analysis and synthesis program to compute physical and electrical parameters of single and coupled lines" [21]. The LineCalc window is shown in Figure 2.14. To launch a simulation, the line type and the different substrate parameters must be defined. There are two simulation modes available as highlighted in the window shown below. For a given frequency, the *synthesize* mode produces the physical parameters, e.g. the width and length, for a chosen characteristic impedance (Z_0 [Ohm]) and effective electrical length (E_Eff [deg]). Also for a specified frequency, the *analyze* mode does the opposite. It gives the corresponding characteristic impedance and effective electrical length for specified physical parameters.

The effective dielectric constant (K_Eff [/]), the attenuation (A_DB [dB]) and the Skin depth ($SkinDepth$ [mil]), on the lower right of the LineCalc window, are provided after each simulation no matter the mode chosen. This tool takes into account the main parameters of a transmission line applied to a generic line configuration for the line type chosen. It is a quick and simple way to have feedback on a line knowing its configuration and material properties. The definition of all the parameters and other information on the use of LineCalc are available in [21].

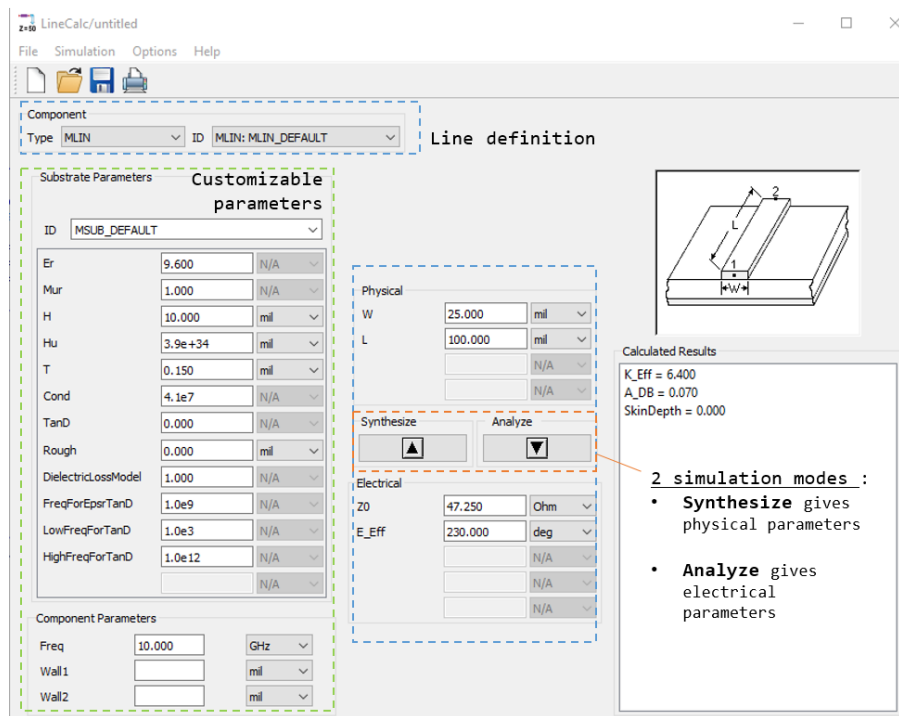


Figure 2.14: LineCalc window example (Keysight ADS).

2.5.2 Controlled Impedance Line Designer

Controlled Impedance Line Designer (CILD) is also "an analysis and synthesis program to compute physical and electrical parameters of single and coupled lines" [21]. The difference with LineCalc is that it allows the user to define the substrate stack and the materials used for each layer of the stack. An example of the CILD window

is showcased in Figure 2.15.

The transmission line properties such as the characteristic impedance, the effective dielectric constant and the *RLGC* parameters, located on the lower right of the CILD window, are computed by the program provided the user defines the line and the substrate stack used. There are in total four simulation modes.

Analyze mode performs the simulation for a single frequency for the given simulation setup defined. *Optimize* allows the user to choose a parameter, such as the characteristic impedance, as a goal with a target value and tune another parameter to achieve the goal. *Sweep* mode can perform a specified sweep on one or multiple parameters of choice. *Statistical* mode is used for sensibility analysis. Further reading on the CILD tool in [21].

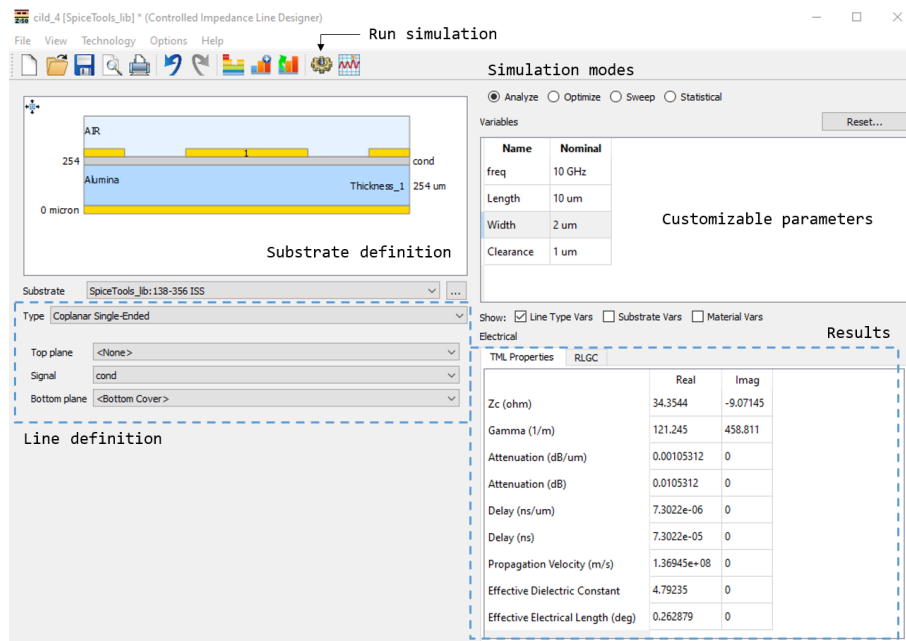


Figure 2.15: CILD window example (Keysight ADS).

2.5.3 Momentum

Momentum is "an electromagnetic simulator that computes S-parameters for general planar circuits, including microstrip, slotline, stripline, coplanar waveguide, and other topologies" [21]. Momentum computations are based on the method of moments. There are two modes of simulation in Momentum. *Microwave* which is the full-wave mode and *RF* which is the quasi-static mode. To perform an EM simulation with Momentum, one needs to draw a layout. An example is shown in Figure 2.16. The EM setup (Figure 2.17) also needs to be defined. In the setup window, the user has to define the simulation mode, the substrate stack, the arrangement of the port pins, the frequency plan and more. It is a more detailed and complex simulator that gives out results that are closer to reality. However, launching an EM simulation requires a lot more implementation beforehand compared to LineCalc and CILD.

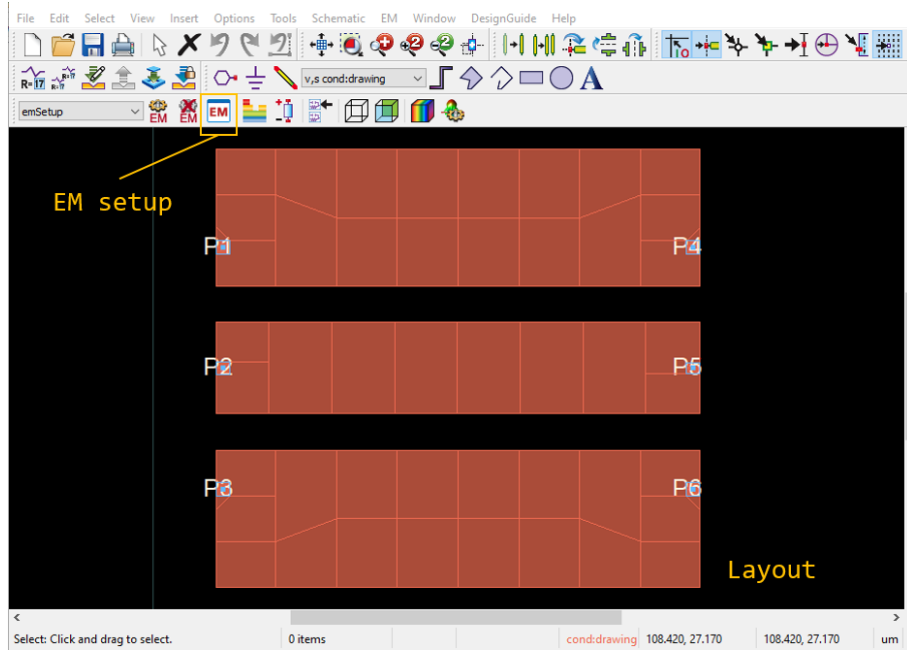


Figure 2.16: Momentum main window example (Keysight ADS).

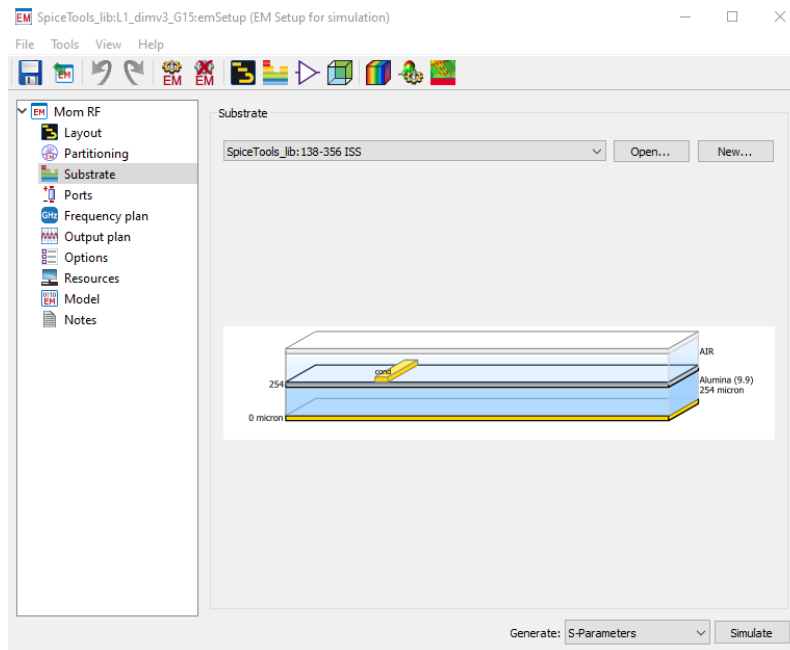


Figure 2.17: Momentum EM setup window example (Keysight ADS).

Chapter 3

Data treated

3.1 138-356 Impedance Standard Substrate (ISS)

Impedance Standard Substrates have a set of simple circuits such as open, short, thru and lines of different lengths. They are calibration standards used in high frequency on wafer measurement calibration. They are used to calibrate VNA's.

The structures measured and characterized in this work are from the 138-356 Impedance Standard Substrate (ISS) from Cascade Microtech. It has a Ground-Signal-Ground (GSG) configuration and a pitch of 50 to 75 μm . A top view of this specific ISS can be found in Figure 3.1).

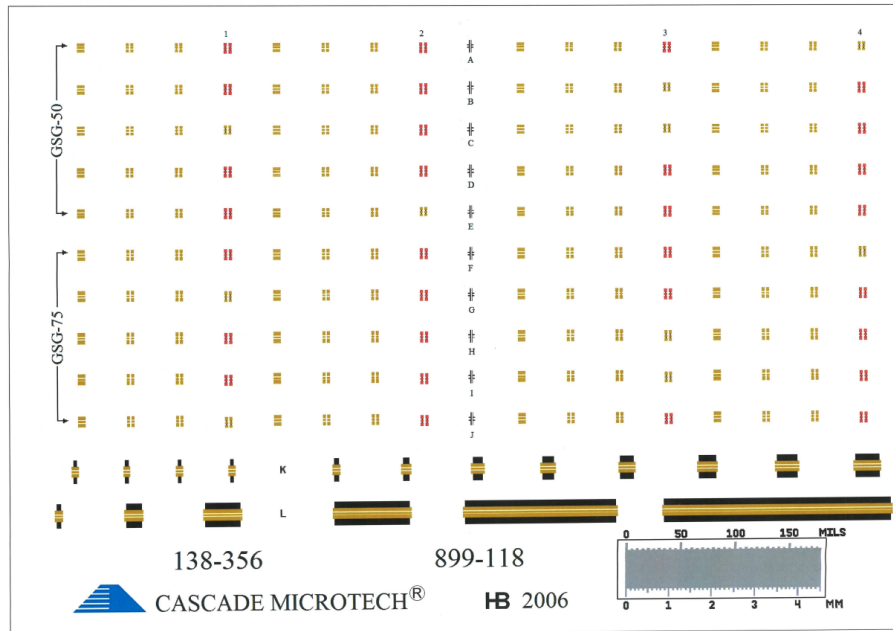


Figure 3.1: 138-356 Impedance Standard Substrate (ISS) top view.

The calibration standards are made with 3.5 μm thick gold. They are sitting on an Alumina substrate of 254 μm thick, with a dielectric constant of 9.9 [22]. The stack configuration is illustrated in Figure 3.2. This calkit has 18 verification lines in

total, listed in Table 3.1. These verification lines and the THRU are the structures of interest in this work.

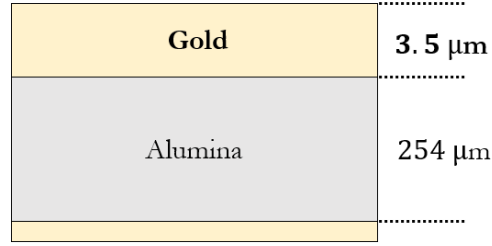


Figure 3.2: Stack illustration of the 138-356 ISS.

Line name	ps	Length (μm)	Line Name	ps	Length (μm)
K1	0.5	135	K10	3.2	485
K2	0.5	135	K11	3.8	570
K3	0.5	135	K12	4.5	655
K4	0.5	135	L1	1	200
K5	1.1	215	L2	3	450
K6	1.4	250	L3	7	900
K7	1.9	315	L4	14	1800
K8	2.3	365	L5	27	3500
K9	2.7	420	L6	40	5250

Table 3.1: Verification lines in the 138-356 ISS.

A picture of a thru line under the microscope was taken (Figure 3.3). With the knowledge of the length of this line, the other dimensions such as the width and the gap can be deducted. The deduced dimensions are illustrated in Figure 3.4. Knowledge of the real line configuration and dimensions will be beneficial for the setup of simulations to characterize the standards.

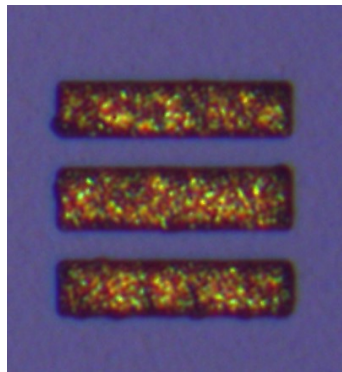


Figure 3.3: Picture of the 138-356 THRU under the microscope.

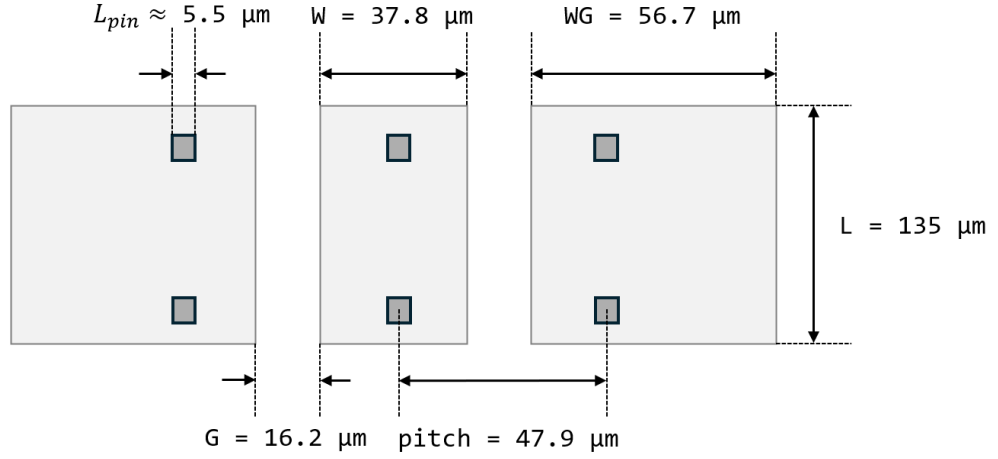


Figure 3.4: Dimensions of 138-356 THRU with the probing contacts, extracted from the microscope.

These ISS structures were measured from 10 MHz to 67 GHz with a VNA using three sets of frequency sweeps listed in Table 3.2.

N°	Start frequency	Stop frequency	Number of points	Step
1	10 MHz	90 MHz	9	0.001 GHz
2	100 MHz	900 MHz	9	0.01 GHz
3	1 GHz	67 GHz	133	0.5 GHz

Table 3.2: Frequency sweep for the measurements of 138-356 ISS lines.

The VNA used for the measurements was calibrated using the Line-Reflect-Reflect-Match (LRRM) and the Through-Reflect-Line (TRL) calibration techniques respectively, using the WinCal software from Cascade Microtech.

3.2 FD28 experiment

An experiment on a 28-nm technology was available and was used because it can give several interesting insights. This experiment only has three metal layers illustrated in Figure 3.5. A cross-section capture under the microscope of the wafer allowed the extraction of the BEOL layer thicknesses. However, there was a lack of information on the BEOL dielectric materials used and uncertainties on the dielectric constant of certain layers. Some assumptions were made later on in the simulations.

Two designs, with and without a ground plane exist on the wafer. An illustration of the substrate stackup and BEOL, for both designs, is depicted in Figure 3.5. The first design, represented on the left, has M1 acting as a ground plane, shielding the signal (travelling in LB) from the substrate. The second design does not have this shielding. The information available on the different layers is summarized in Table 3.3.

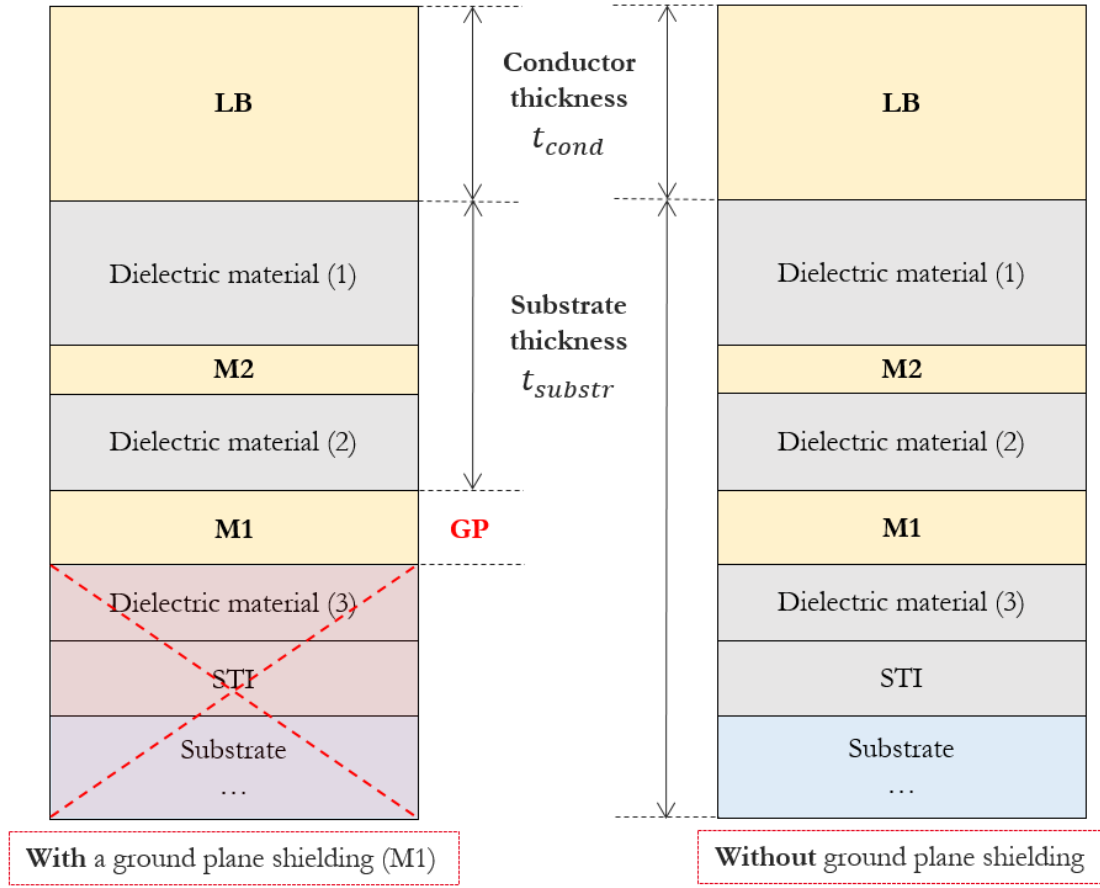


Figure 3.5: FD28 experiment substrate stackup and BEOL.

Layer name	Material	Thickness
LB	Copper	$\geq 0.75 \mu\text{m}$
Dielectric material (1)	-	400 nm
M2	Copper	50 nm
Dielectric material (2)	-	100 nm
M1	Copper	150 nm
Dielectric material (3)	-	230 nm
STI	-	475 nm
Substrate	Silicon	1 mm

Table 3.3: Description of the substrate stackup and BEOL of the FD28 experiment.

The FD28 experiment was done on two wafers with different resistivity: a standard low-resistivity wafer (*STD*) and a wafer with a high-resistivity substrate (*HR*). They are listed in Table 3.4.

Wafer type	Resistivity Ω cm/Wafer#
STD	10
HR	< 500

Table 3.4: Types of wafer measured with increasing resistivity.

The FD28 experiment was measured according to the frequency sweep described in Table 3.5. The LRRM calibration technique was performed on the VNA for the set of measurements available.

Start frequency	Stop frequency	Number of points	Step
500 MHz	40 GHz	80	0.5 GHz

Table 3.5: Frequency sweep for the measurements of the FD28 experiment structures.

3.2.1 Design with ground plane

The first design is a 28-nm technology with M1 shielding the signal from the substrate. For this design, measurements of an open, a short and two lines were available. The top views of the layouts are shown in Figure 3.6, showcasing the location of the different metal layers.

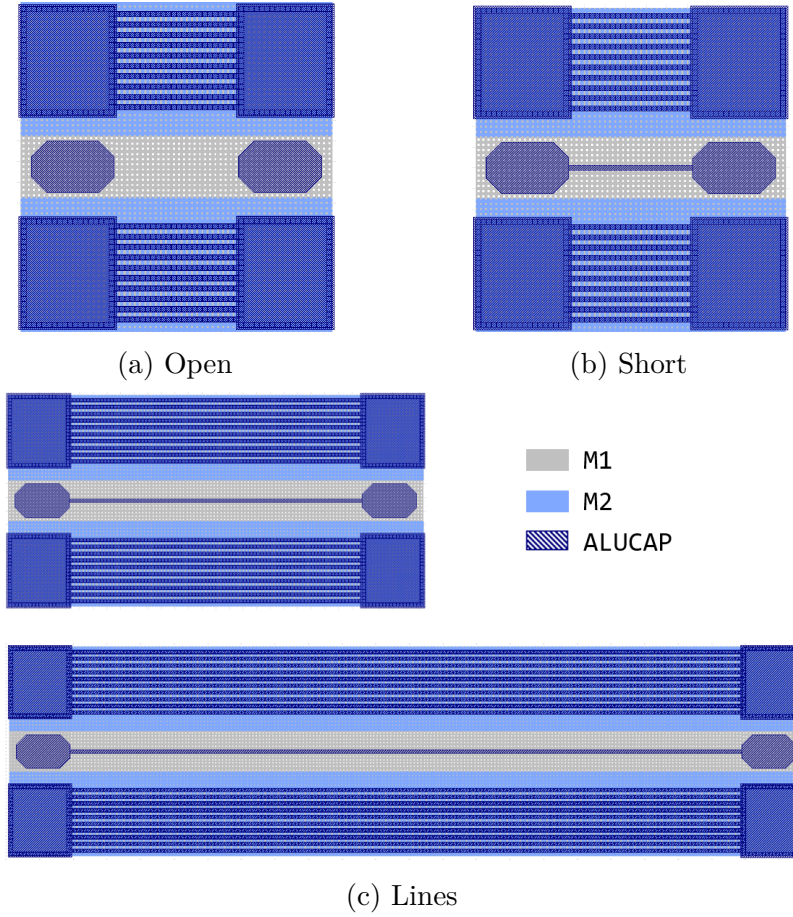


Figure 3.6: FD28 with ground plane: layouts of the open (a), short (b) and two lines (c).

The lengths of the two lines shown above are listed in Table 3.6.

Line name	Length	Unit
THRU	108	μm
L1	387	μm
L2	900	μm

Table 3.6: Lines for FD28 with ground plane.

The signal pads are hexagonal. The dimensions of the pads and the line are depicted in Figure 3.7.

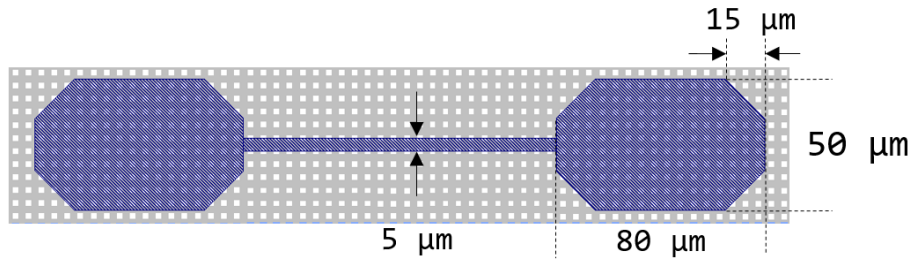


Figure 3.7: FD28 with ground plane: dimensions of the signal pad of the short layout.

3.2.2 Design without ground plane

The FD28 without ground plane design has M1 is only present underneath the pads. The line is directly exposed to the substrate. A pad, an open, a short and an inductor were available. There are no lines in this design.

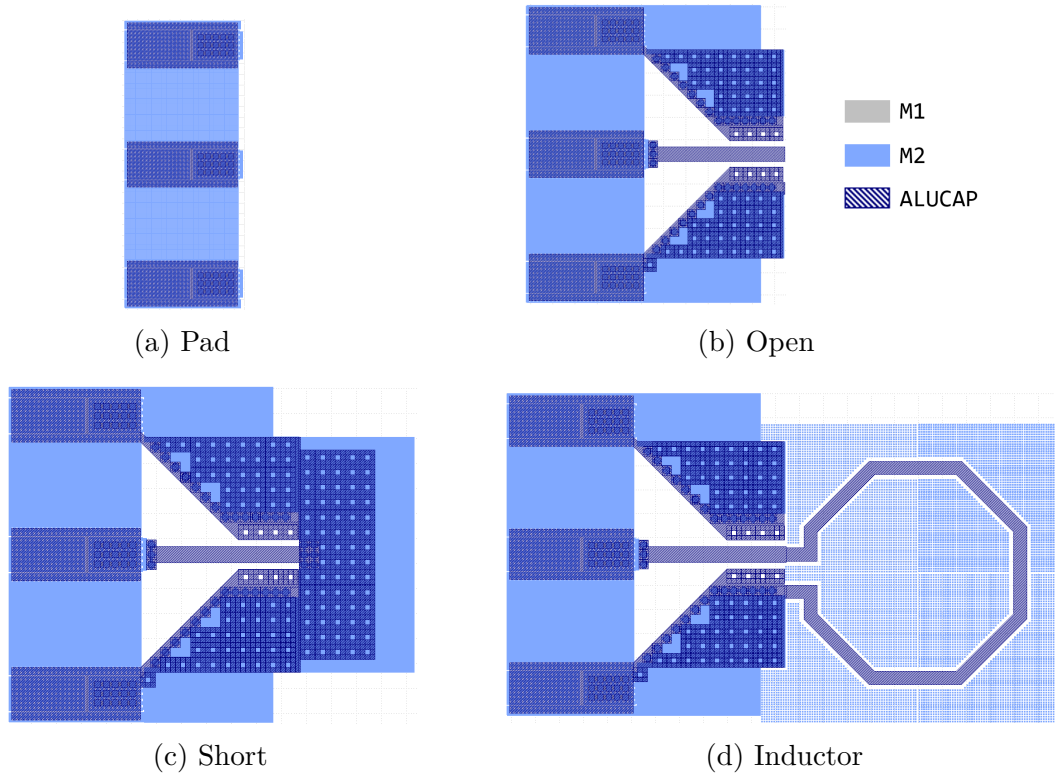


Figure 3.8: FD28 without ground plane: layouts of the open (a), short (b) and two lines (c).

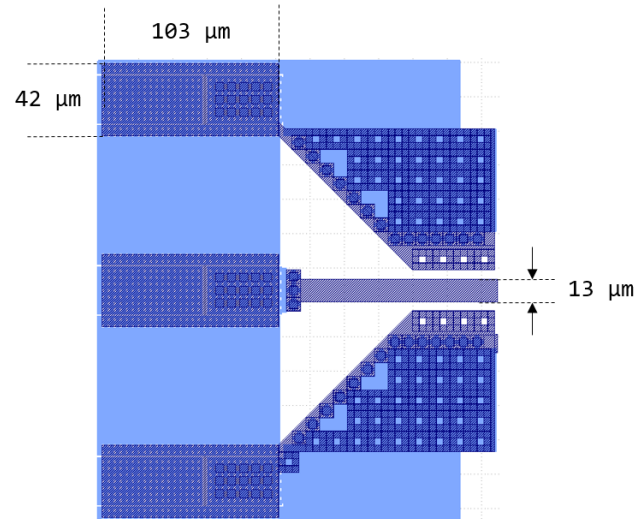


Figure 3.9: FD28 with ground plane: dimensions of the signal pad for the open layout.

Chapter 4

Results

4.1 138-356 ISS: lines characterization

4.1.1 EM simulations: Momentum

The 138-356 Impedance Standard Substrate (ISS) was simulated using the EM simulation tool *Momentum* from Keysight ADS. The EM simulation setups were chosen to mimic the real conditions as much as possible. The layouts were drawn with the dimensions extracted from the microscope as shown in the previous chapter, with the substrate as described in the datasheet [22]. The simulations used the same frequency sweep as the measurements to facilitate comparison 3.2.

There are two sets of measurements. One was done with a LRRM calibration (*meas LRRM*) while the other one was performed with a TRL calibration (*meas TRL*). Two EM simulations were performed. The only difference between the two is the size of the gap between the signal strip and the ground planes. The first simulation, referred to as *EM15*, has a gap of 15 μm . The second one, referred to as *EM16.2*, has a slighter bigger gap of 16.2 μm . Figures 4.1, 4.2 and 4.3 are the comparisons of the *RLGC*, characteristic impedance and effective dielectric constant between the measurements and the EM simulations for a short (L2), an intermediate (L4) and a long (L6) lines. Both measurements and EM simulations are de-embedded with the Mangan technique to get rid of the parasitic effects. The de-embedding was done by defining the short line as the line with a length just underneath the one that is de-embedded. For instance, L6 is de-embedded with L5. These EM simulations are the best results achieved for the ISS lines, approaching the measurements with an acceptable accuracy.

In Figure 4.1, the difference in the gap size for the two EM simulations leads to a negligible difference in the EM results. The R of *EM15* and *EM16.2* are very similar and follow the sloping trend of *meas TRL*. The other loss parameter G is underestimated by the EM simulations. The simulations give out a near zero G due to the very small loss tangent (0.0003) used.

The characteristic impedance, Z_c , is the most important parameter. Good accu-

racy is desired from the simulations. By considering the lines as low-loss ones, the characteristic impedance is an expression of the inductance L and the capacitance C as demonstrated in 2.20. In Figure 4.2, it can be seen that the EM simulations of the L are sandwiching the *meas LRRM*. The Results of the C are less accurate but are still close to the *meas TRL*. The simulation results deviate even more from the measurements as the line gets longer, with a deviation going up to 10 pF for L6-L5.

The performance of the EM simulations to predict the L and the C directly impact the accuracy of the results for the characteristic impedance. The EM simulations are capable of predicting the Z_c up to a precision of 1 to 2 Ohms for the three lines simulated in Figure 4.3. On the other hand, the effective dielectric constant is systematically underestimated by the simulations by about 0.3 to 0.4. This showcases that simulations using the Momentum tool can help the designer to get a characterisation of acceptable accuracy when measurements are not available and insight into the structure's behavior is needed.

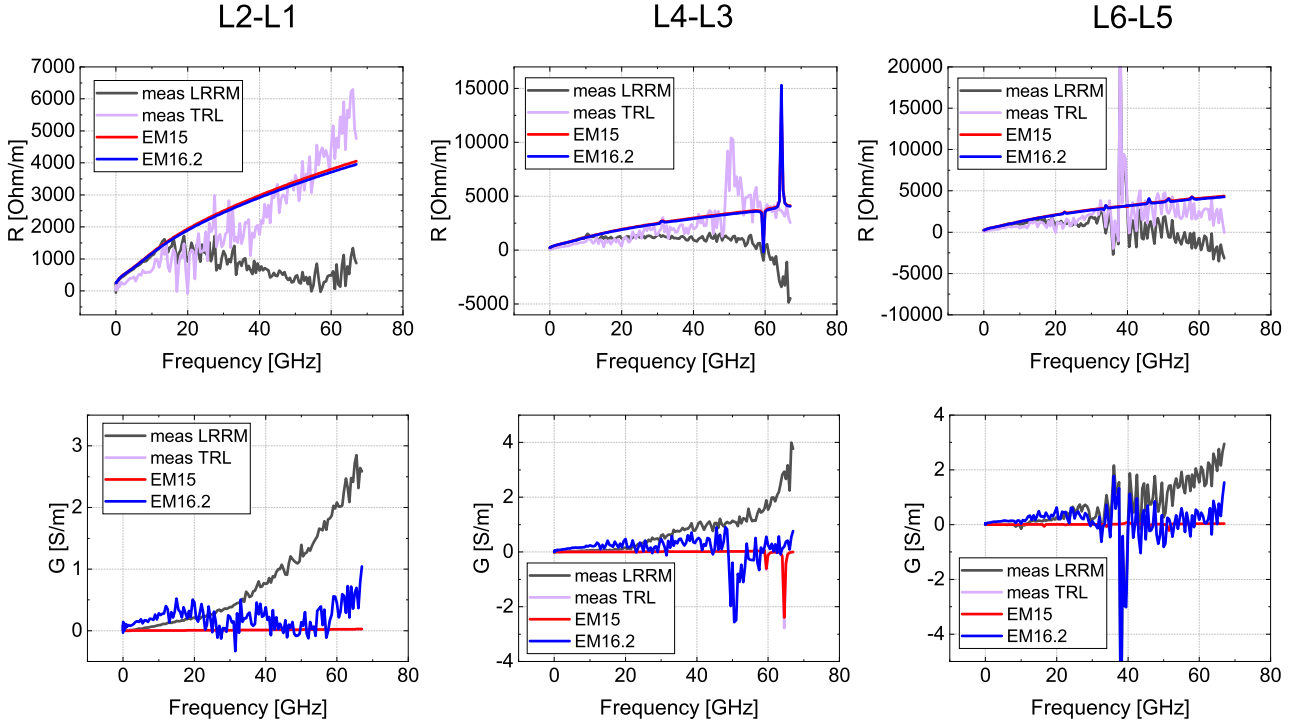


Figure 4.1: Losses (R and G) of 138-356 L2, L4 and L6 with Mangan de-embedding: comparison of LRRM, TRL measurements and EM simulation results with $G = 15 \mu\text{m}$ and $16.2 \mu\text{m}$.

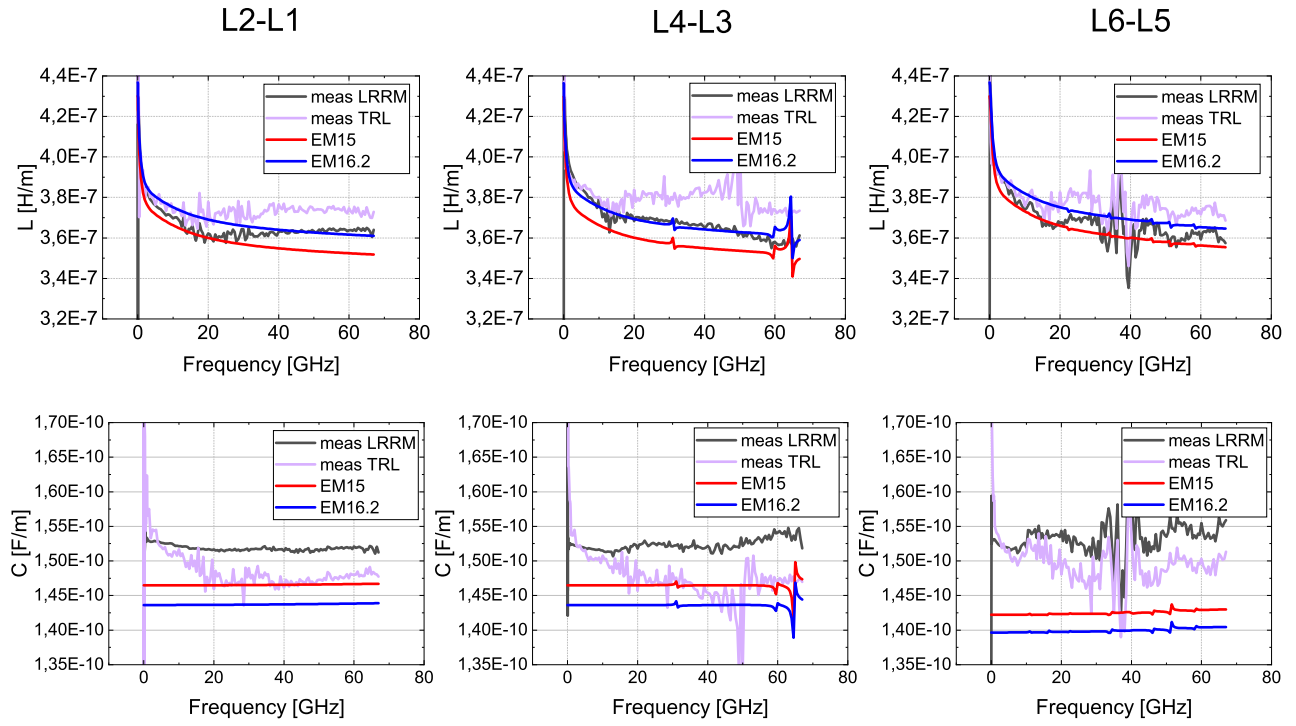


Figure 4.2: L and C of 138-356 L2, L4 and L6 with Mangan de-embedding: comparison of LRRM, TRL measurements and EM simulation results with $G = 15 \mu\text{m}$ and $16.2 \mu\text{m}$.

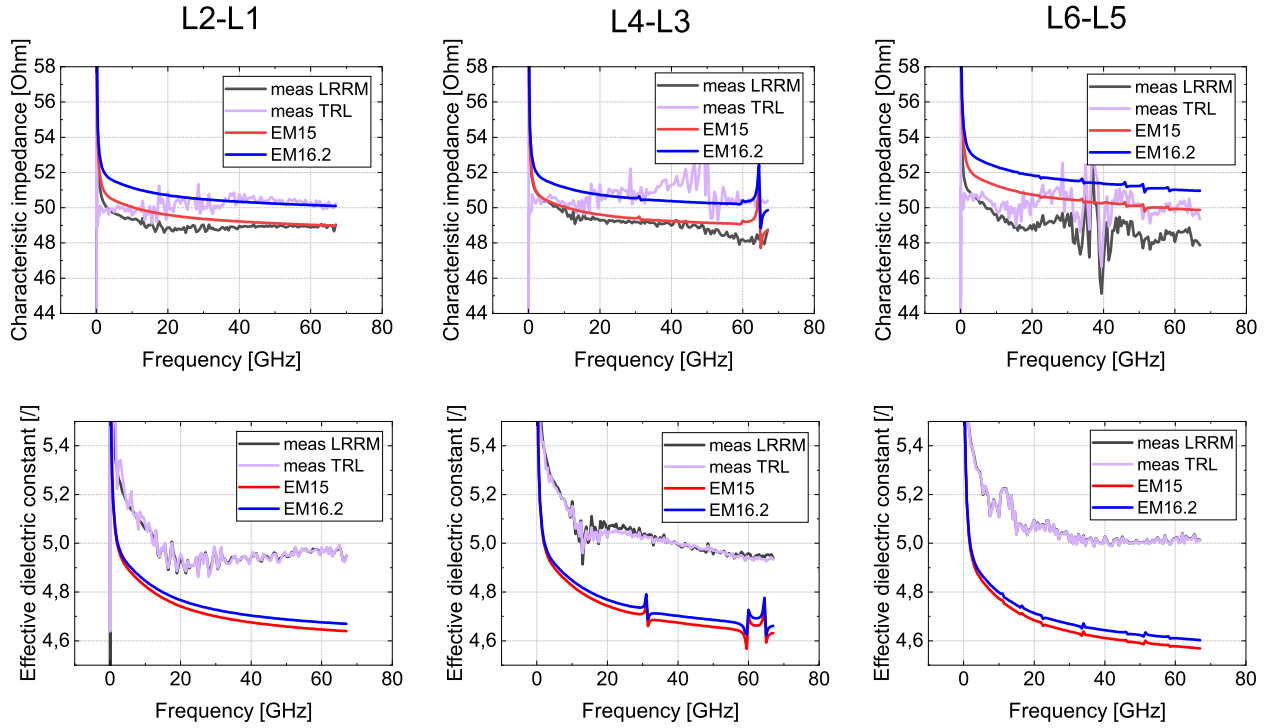


Figure 4.3: Z_c and ϵ_{eff} of 138-356 L2, L4 and L6 with Mangan de-embedding: comparison of LRRM, TRL measurements and EM simulation results with $G = 15 \mu\text{m}$ and $16.2 \mu\text{m}$.

4.1.2 Enhancement techniques for cleaner results

The results seen in the previous section 4.1.1, were Mangan de-embedded to have cleaner results, intrinsic to the lines themselves. In this section, we investigate the techniques that can be used on measurements or EM simulation results to enhance their quality, i.e. length adjustment and Mangan de-embedding.

Length adjustments

Length adjustment is a simple addition or subtraction done on the line length that mirrors the fact that the measurement probes have to be placed on the conductor layer of the ISS lines, thus reducing the actual measured length of the line. The decision on whether to add or subtract length and by how much depends on the topology of the lines and the pads and on how the measurement probes are placed during the measurements.

Here, for the 138-356 ISS lines, the probe tips are placed inside the lines to contact the gold. A length adjustment of $-70 \mu\text{m}$ was chosen by trial and error as it results in the best scaling of the L and C (especially the lineic capacitance). That can be observed in Figure 4.5, where the L and C for four lines of different lengths (THRU, L2, L4 and L6) are plotted and compared using their nominal length from the datasheet 3.1 and after length adjustment.

The characteristic impedance is not greatly impacted by the length adjustment (Figure 4.6). The effects on the L and C compensate each other. The effective dielectric constant is also scaled after length adjustment (Figure 4.6). The impact of the length adjustment on the losses (R and G) is negligible, see Figure 4.4.

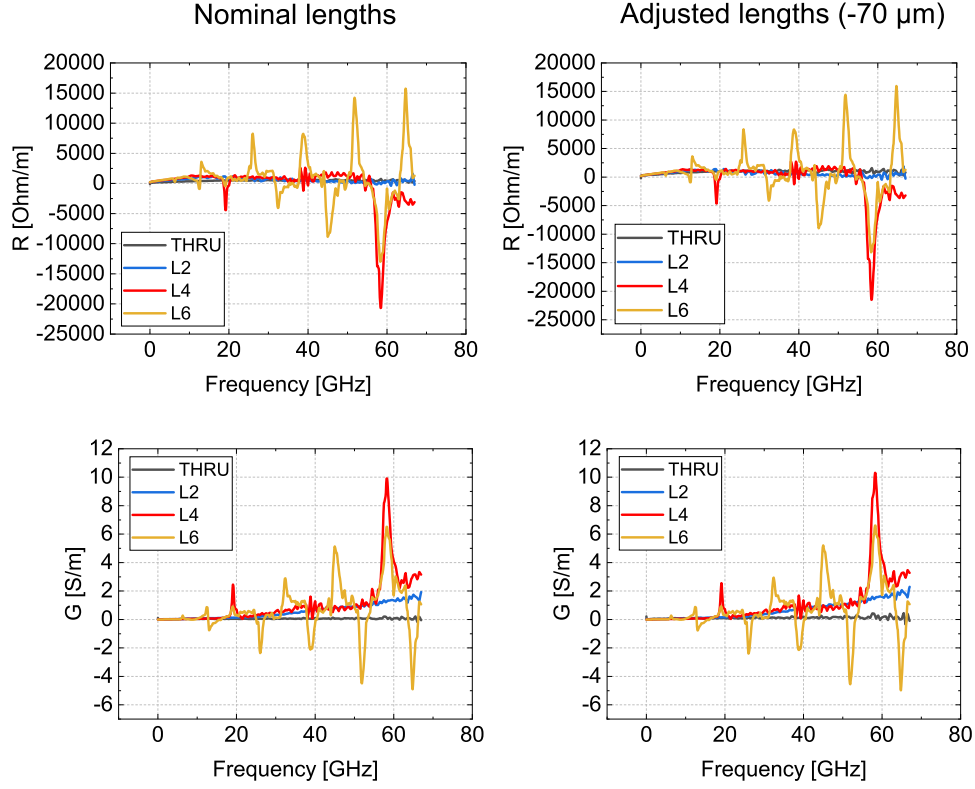


Figure 4.4: Losses (R and G) of 138-356 THRU, L2, L4 and L6 lines measurements: highlight of the effect of length adjustments.

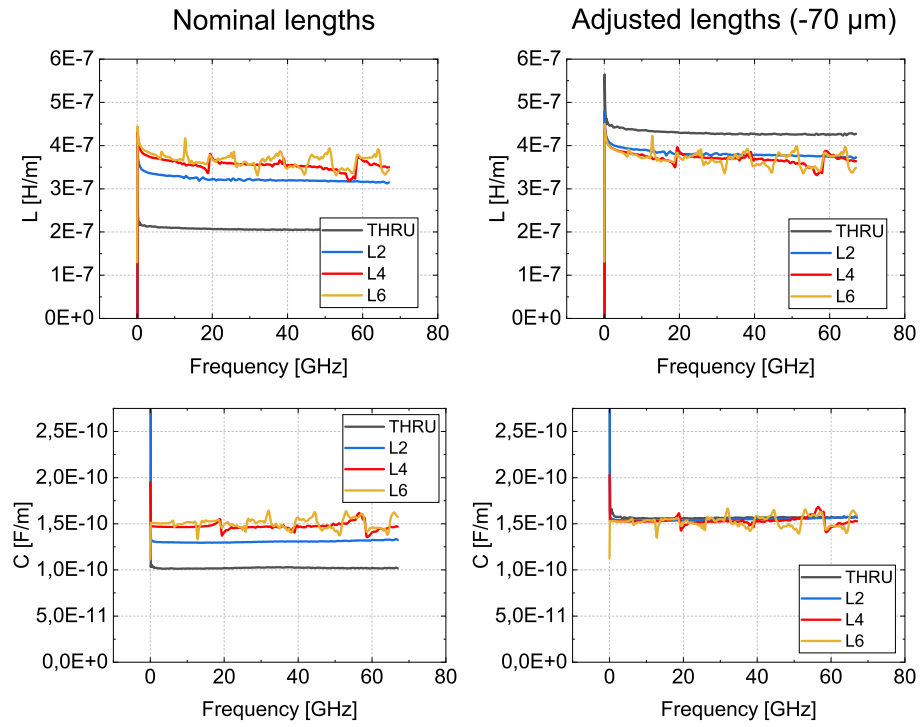


Figure 4.5: L and C of 138-356 THRU, L2, L4 and L6 lines measurements: highlight of the effect of length adjustments.

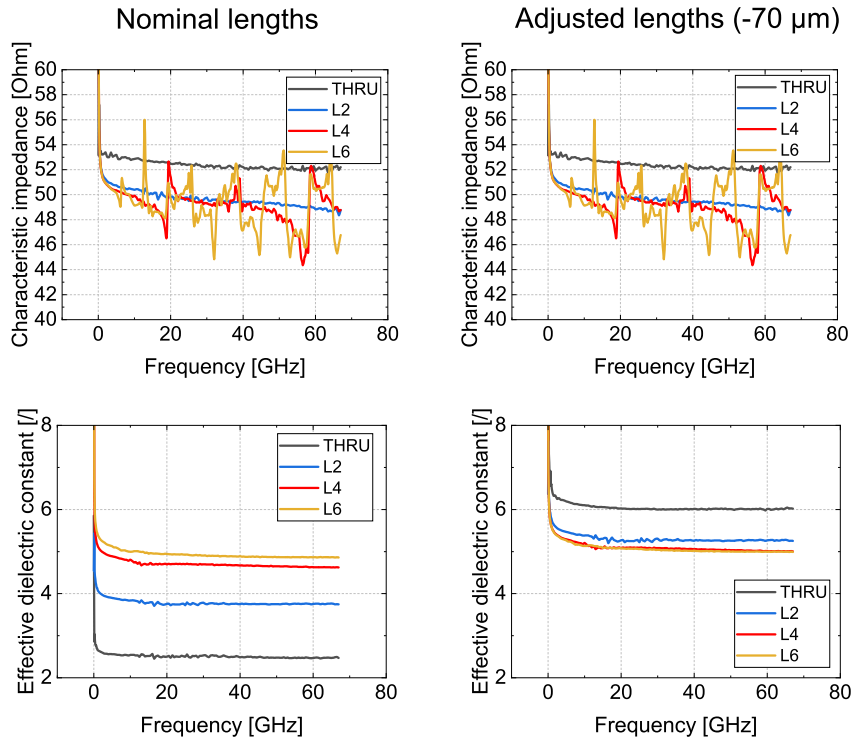


Figure 4.6: Z_c and ϵ_{eff} of 138-356 THRU, L2, L4 and L6 lines measurements: highlight of the effect of length adjustments.

Length adjustment is an easy operation on the length done when computing the $RLGC$ elements, the characteristic impedance, the effective dielectric constant and other transmission line parameters. It helps to enhance the measurements or the simulation results of the L , C and ϵ_{eff} . It can be used as a quick and easy way to have cleaner results when trying to extract these three parameters. This technique is simple but leaves something to be desired. Mangan de-embedding is more time-consuming but provides better enhancement of the data, as it treats the parasitics.

Mangan de-embedding

In Figures 4.7, 4.8 and 4.9, the benefits of the Mangan de-embedding are highlighted. The measurements go through length adjustment, Mangan de-embedding and Mangan de-embedding with length adjustment. The different results are compared for the $RLGC$, Z_c and ϵ_{eff} .

As already observed previously, the length adjustment does not impact the losses of the lines (R and G) and the characteristic impedance but leads to a slight improvement of the L , C and ϵ_{eff} . The Mangan de-embedding provides more significant improvements for all parameters as it de-embeds the parasitic effects of the pads. The length adjustment only accounts for the impact of the probe placement.

The Mangan de-embedding was also tested on measurements that were already

length-adjusted. As expected, the effect of the length adjustment is not visible because the Mangan de-embedding gets rid of the pad effects altogether.

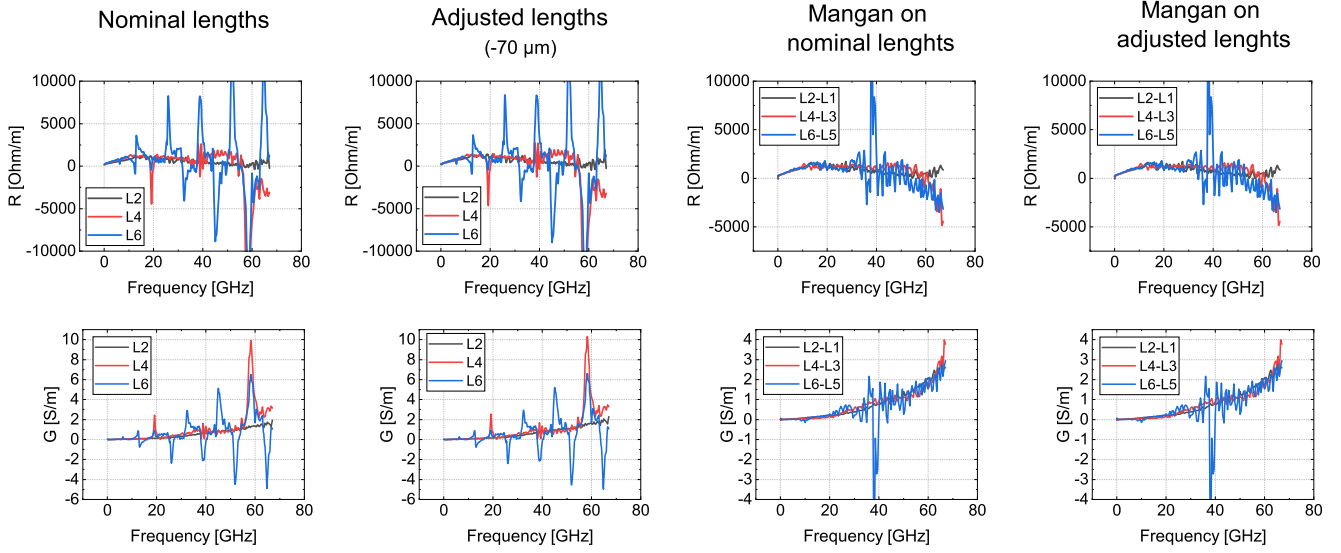


Figure 4.7: Losses (R and G) of 138-356 L2, L4 and L6 lines measurements: comparison of the effect of Mangan de-embedding with lengths adjustment.

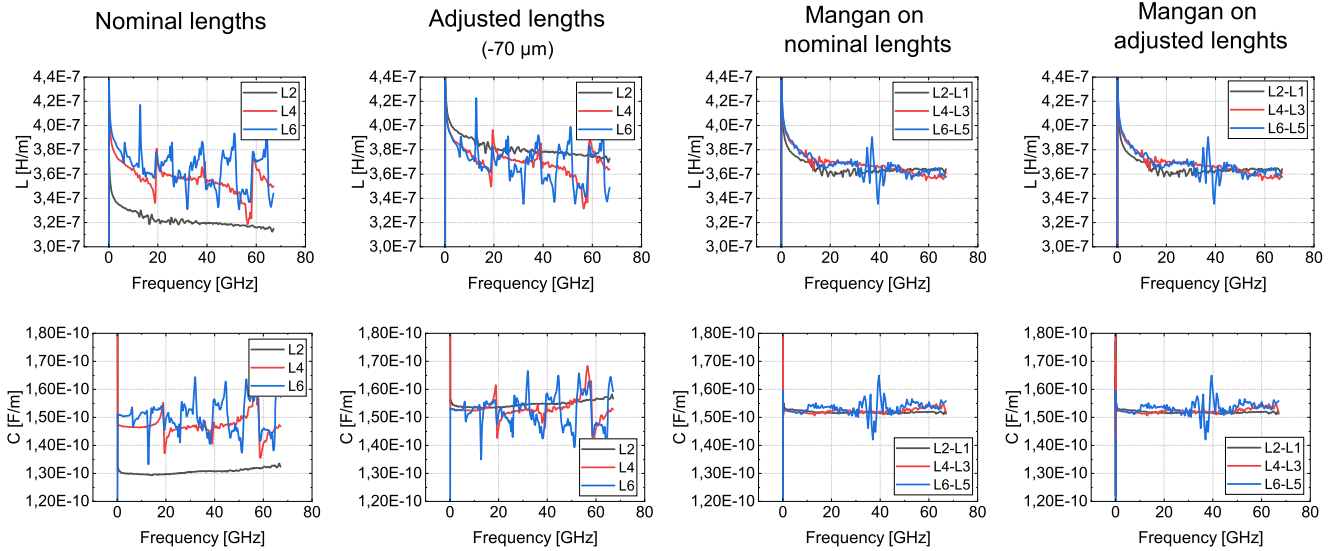


Figure 4.8: L and C of 138-356 L2, L4 and L6 lines measurements: comparison the effect of Mangan de-embedding with lengths adjustment.

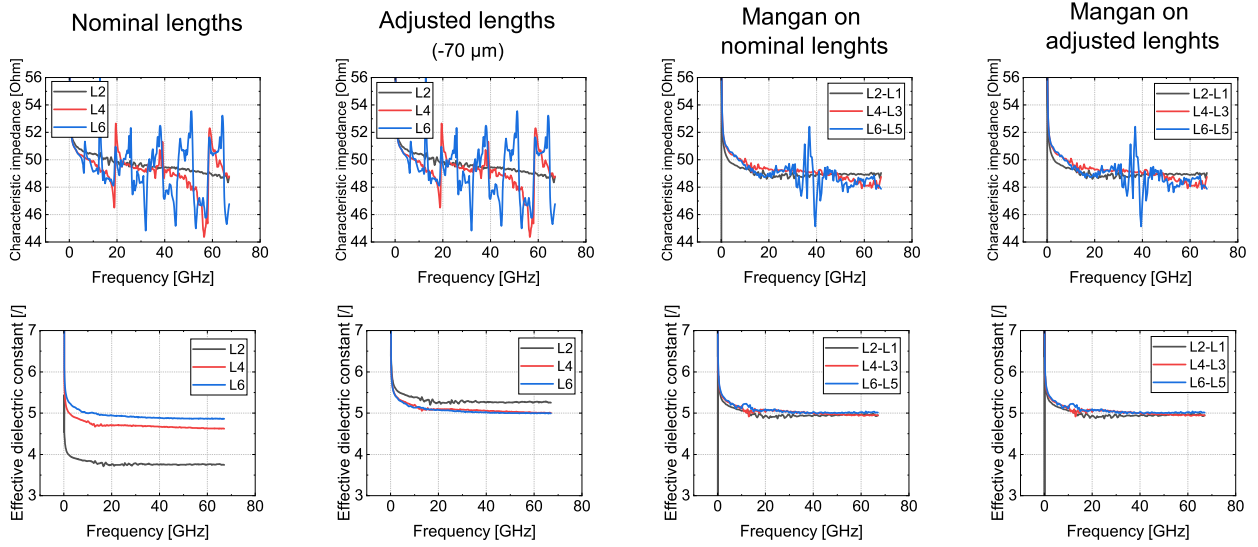


Figure 4.9: Z_c and ϵ_{eff} of 138-356 L2, L4 and L6 lines measurements: comparison the effect of Mangan de-embedding with lengths adjustment.

4.1.3 Analytic simulations: LineCalc and CILD

As seen in the previous sections, the Momentum simulation tool provides good predictions of the different parameters for the characterization of the 138-356 lines. However, EM simulations need the setting up of various parameters, the drawing of the layouts and the definition of the substrate. Precise knowledge of the stack and the dimensions is needed. LineCalc and Controlled Impedance Line Designer, also from Keysight ADS are less complex and quicker to set up analytical alternatives, with the price of a lessened accuracy.

The 138-356 ISS L4 line is simulated in both analytical simulators for a simulation setup as shown in Table 4.1. CILD can easily perform a sweep over a range of frequencies. The simulated $RLCG$ for L4 is plotted in Figure 4.10 and compared to the measurements to assess its accuracy. The losses (R and G) are correctly simulated at low frequency (until 10 GHz for R and until 20 GHz for G). At higher frequencies, the measured losses and the simulated ones start to deviate one from another. The lineic inductance L is underestimated by about 30 nH, which is 8.33% of its measured value. The lineic capacitance C is overestimated by about 10 pF, which is 6.67% of its measured value. The differences between the measured and simulated L and C directly impact the accuracy of the characteristic impedance that can be seen in Figure 4.11.

The characteristic impedance, the effective dielectric constant and the normalized attenuation are depicted in Figure 4.11 for both simulators and are again compared to the measurements. It can be observed that the overall trend can be predicted by the simulator though the values predicted are not the most accurate. Both simulators underestimate the characteristic impedance by a few Ohms. CILD performs better

for the effective dielectric constant and both simulators can predict the attenuation at low frequencies (up until around 10 GHz). It is also interesting to note that there is always a shift between the results from LineCalc and CILD. Overall, CILD is slightly better at predicting the line parameters as it is more sophisticated. For reliable results, provided that the user is willing to put in the work, it is still preferable to perform an EM simulation.

Parameter	Value	Unit
ϵ_r	9.9	/
Mur	1	/
t_{substr}	254	μm
t_{cond}	3.5	μm
ρ	4.1e+7	/
$TanD$	0.0003	/
Frequency	10	GHz
W	37.8	μm
G	16.2	μm
L	65	μm

Table 4.1: Parameters setting for the LineCalc and CILD simulation of 138-356 THRU.

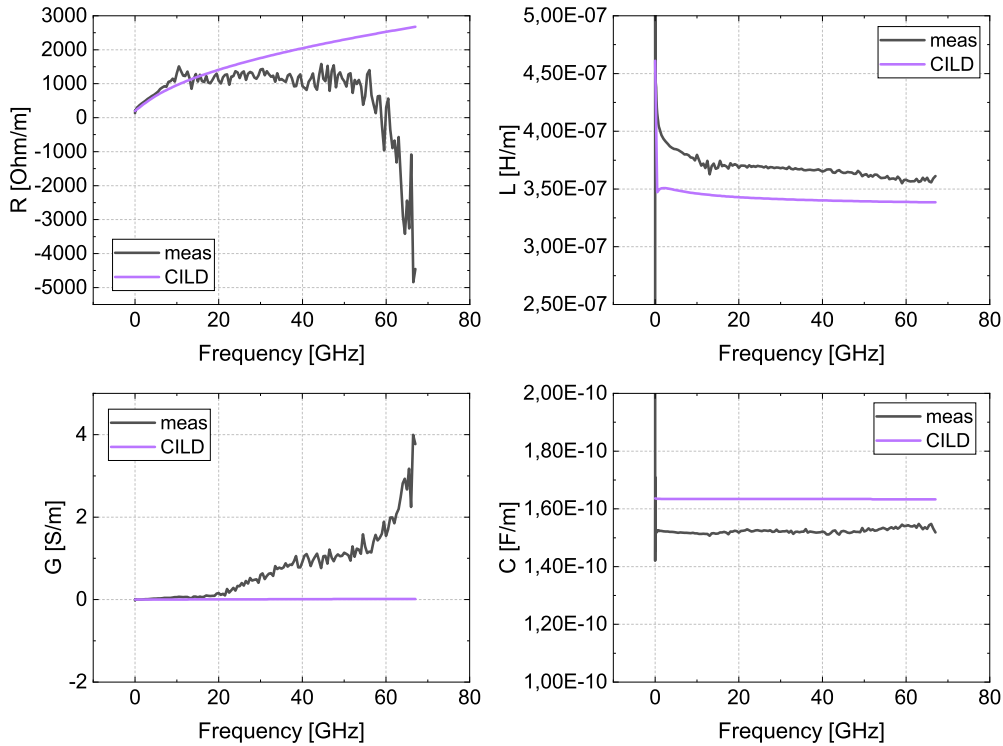


Figure 4.10: $RLGC$ of 138-356 L4 line: comparison between CILD results and measurements with Mangan de-embedding.

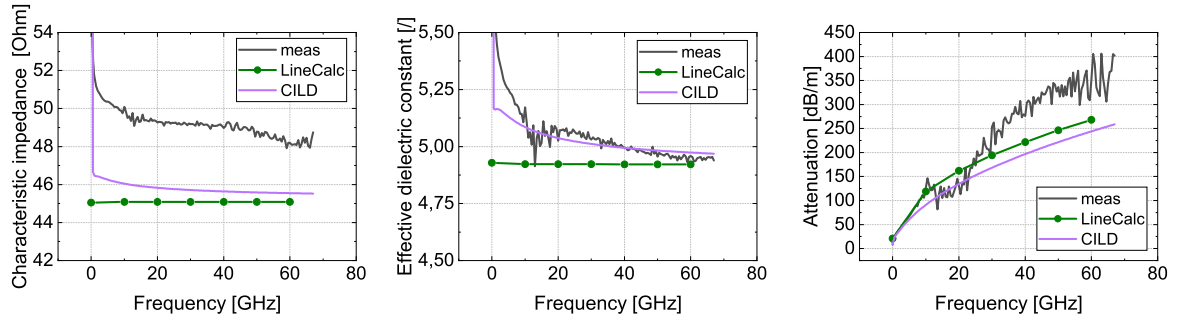


Figure 4.11: Z_c , ϵ_{eff} and normalized attenuation of 138-356 L4 line: comparison between LineCalc results, CILD results and measurements with Mangan de-embedding.

4.2 FD28 design: pad characterization

In this section, the pads of the two FD28 designs are characterized to observe the impact of the ground plane shielding. The different capacitances and inductances of the circuit elements available were extracted for the *STD* and *HR* wafers that were described in the previous chapter in Table 3.4.

4.2.1 Design without ground plane

For this design, no lines were available so we can only do a characterisation of the pads. For the FD28 with no ground plane design, there is a pad, an open, a short and an inductor available. The elements were measured by a VNA calibrated using the LRRM calibration technique. The measured S-parameters allowed the extraction of the capacitances of the pad and the open (Figure 4.12), as well as the inductances of the short and the inductor (Figure 4.13). Also, the latter figure is the inductor value after an open de-embedding and an open-short de-embedding.

By observing Figure 4.12, it can be seen that both the pad and the open capacitances, $C - open$ and $C - pad$, decrease with increasing frequencies. The open capacitance is bigger than the pad capacitance as it has more metal parts contributing to the overall capacitance. The *HR* wafer showcases lower $C - open$ and $C - pad$ compared to its *STD* counterparts. The difference between the two types of wafers is more significant at low frequencies and decreases at higher frequencies because the signal becomes too quick for the substrate carriers to follow.

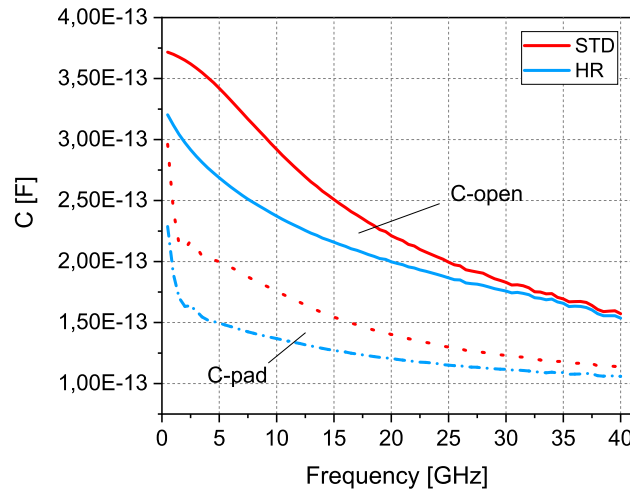


Figure 4.12: Capacitances of the pad and open in FD28 without ground plane, for the two wafer types.

In Figure 4.13 are plotted all the inductances for the no ground plane design. The short inductance is stable over the frequencies and its value is not impacted by the change in substrate resistivity. The inductor inductance resonates at around 13 GHz for the *STD* wafer and a bit higher in frequency at around 15 GHz for the *HR* wafer. After de-embedding, the effect of the substrate resistivity is not visible anymore. The open-short de-embedding results in an inductance of 400 pH, compared to an inductance of 500 pH when an open de-embedding is used. The open-short de-embedding is better than the open de-embedding because it uses an extra dummy circuit (short) to also get rid of the series parasitics.

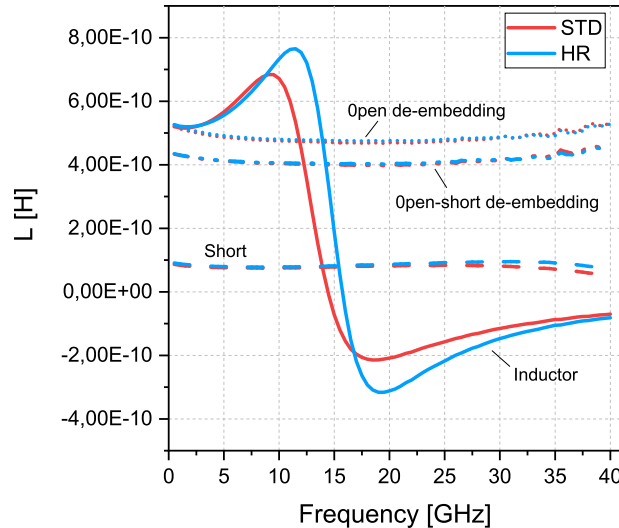


Figure 4.13: Inductances in FD28 without ground plane, for the two wafer types: inductances of the inductor, short and inductor after open and open-short de-embedding.

Finally, the quality factors are computed for the raw inductor from the measurements and after the two de-embedding techniques (Figure 4.14). It illustrates the benefit of performing a de-embedding and confirms that an open-short de-embedding is better than just an open de-embedding. Another aspect that is highlighted in the figure that is interesting to note, is that the *HR* wafer results in a better quality factor than the low resistivity *STD* wafer.

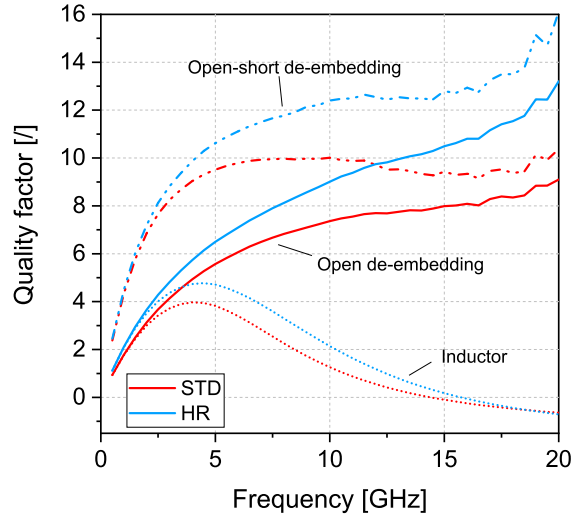


Figure 4.14: Quality factor of the inductances in FD28 without ground plane: for the raw inductor and after open and open-short de-embedding.

4.2.2 Design with ground plane

In the FD28 with ground plane design, a pad was available for measurements. The extracted capacitances for the two types of wafers are shown in Figure 4.15. Similarly to the design without ground plane, the higher resistivity wafer results in a smaller pad capacitance. The difference between the two wafers is around 10 fF (about 5-6% of C-pad). The pad capacitance here, unlike the other design, remains stable over the frequencies. That highlights the advantage of having a ground plane to shield the signal metal from the substrate. However, the addition of the ground plane increases the capacitive effect of the element. In fact, for the *STD* wafer, the pad capacitance when there is no ground plane is between 120 and 200 fF, stabilizing at high frequencies around 120 fF. Compared to this, the addition of the ground plane gives a constant capacitance of about 175 fF.

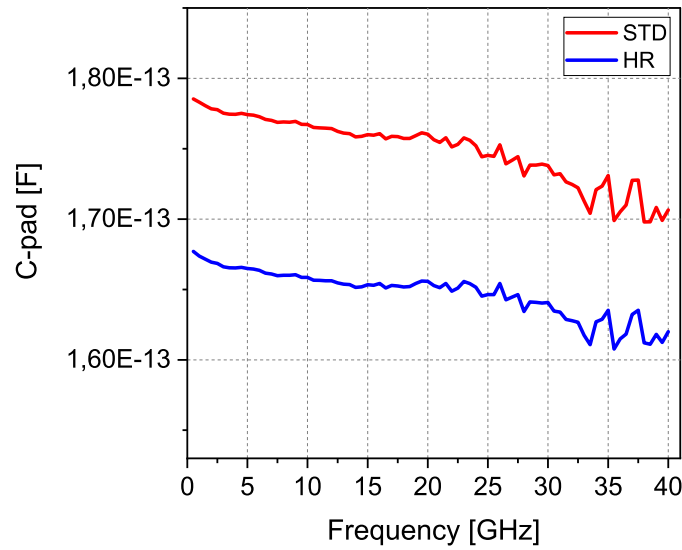


Figure 4.15: Capacitance of the pad for FD28 with ground plane, for the two wafer types.

4.3 FD28 design: lines and inductance characterization

4.3.1 EM simulations: Momentum

FD28 without ground plane: inductance

For the FD28 without ground plane, the inductor is simulated with Momentum. This design has a complex geometry, especially for pads. It was attempted to simplify the layouts to avoid an explosion in computational expenses. The pads were too complex to work with and resulted in incoherent results. Instead, the layout used for the simulations just ignored the pad, and focused on the inductor coil exclusively. The results of such simulation are expected to be close to the measurements after de-embedding. That is the case, as illustrated in Figure 4.16. The simulations and the measurements differ by less than 40 nH.

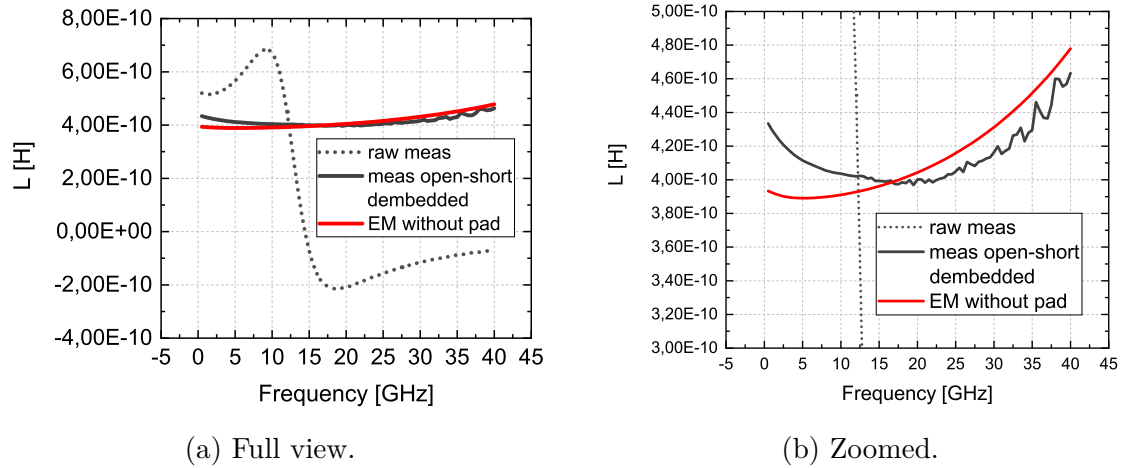


Figure 4.16: Inductances of the inductor in FD28 without ground plane: from the raw measurements, after open de-embedding and from EM simulations without the pad.

Lines with ground plane

There are three lines in the FD28 with ground plane design. In Figure 4.17, the *RLGC* of those lines from the measurements and from the EM simulations, both with a Mangan de-embedding, are depicted. The same is done for the characteristic impedance and the effective dielectric constant in Figure 4.18.

The EM simulation results are less close to measurements compared to how they performed for the ISS lines. The lineic resistance R is underestimated by up to 3.5 times. The G is also underestimated by up to 4 times. The simulated L is about 80 nH less than the measurements (deviation of about 40%) and the simulated C is greater than the measurements by 40 pF (deviation of about 10%).

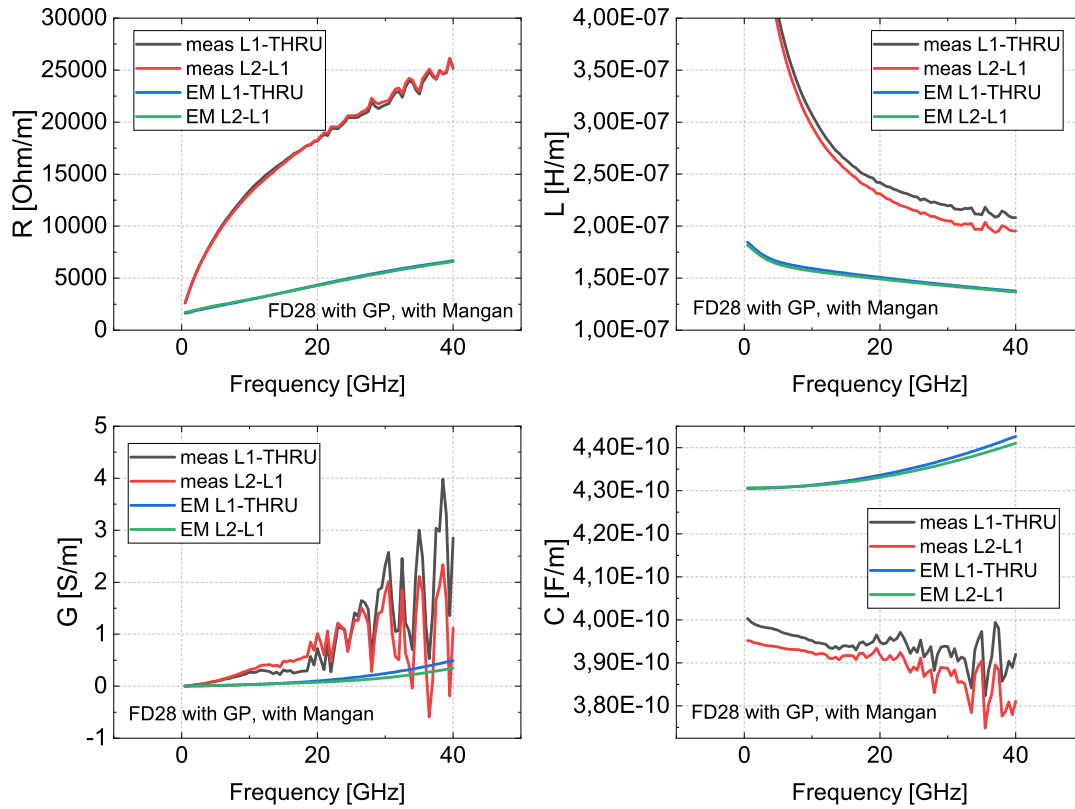


Figure 4.17: $RLCG$ for FD28 with ground plane L1 and L2 lines: measurements compared to EM simulations with Mangan de-embedding.

The difference in L and C between the measurements and the EM simulations results in the underestimation of the characteristic impedance, as observed in Figure 4.18. The simulated Z_c is between 17 and 20 Ohm. The measured Z_c is located between 25 to 30 Ohm. These lines were not very good lines, its characteristic impedance is way off the desired 50 Ohm. The real Z_c is about 8 to 10 Ohm bigger than the simulated one (deviation of 25 to 30 %). The effective dielectric constant is also underestimated. There is a difference of about 2 to 4.

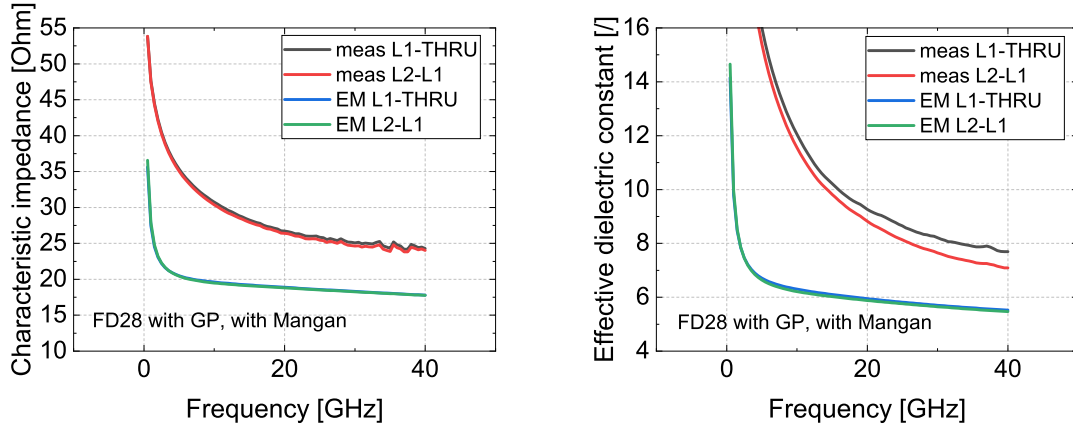


Figure 4.18: Z_c and ϵ_{eff} for FD28 with ground plane L1 and L2 lines: measurements compared to EM simulations with Mangan de-embedding.

The EM simulations of these lines are not as precise as those of the ISS lines. This is probably due to the uncertainties on the stack configurations. The knowledge of the different layers present is available but the thicknesses are nominal or target values and physical thicknesses are not always known and may be significantly different. There is also no definite knowledge of the dielectric materials used. To be able to launch EM simulations, it is necessary to provide the simulator with a substrate stack. To be able to do that, assumptions were made. It was not possible to recreate the setting mimicking the reality due to the lack of data on the stack. This leads to the big deviations observed in the figures above. Better knowledge and configuration of the stack parameters will certainly enhance the EM simulation results, bringing them closer to the measurements.

4.3.2 Analytical simulations: LineCalc and CILD

Parameter	Value	Unit
ϵ_r	3.83	/
Mur	1	/
t_{substr}	0.55	μm
t_{cond}	0.75	μm
ρ	5.96e+7	/
$TanD$	0.001	/
Frequency	10	GHz
W	4.5	μm
L	108	μm

Table 4.2: Parameters setting for the LineCalc and CILD simulation of FD28 with ground plane THRU.

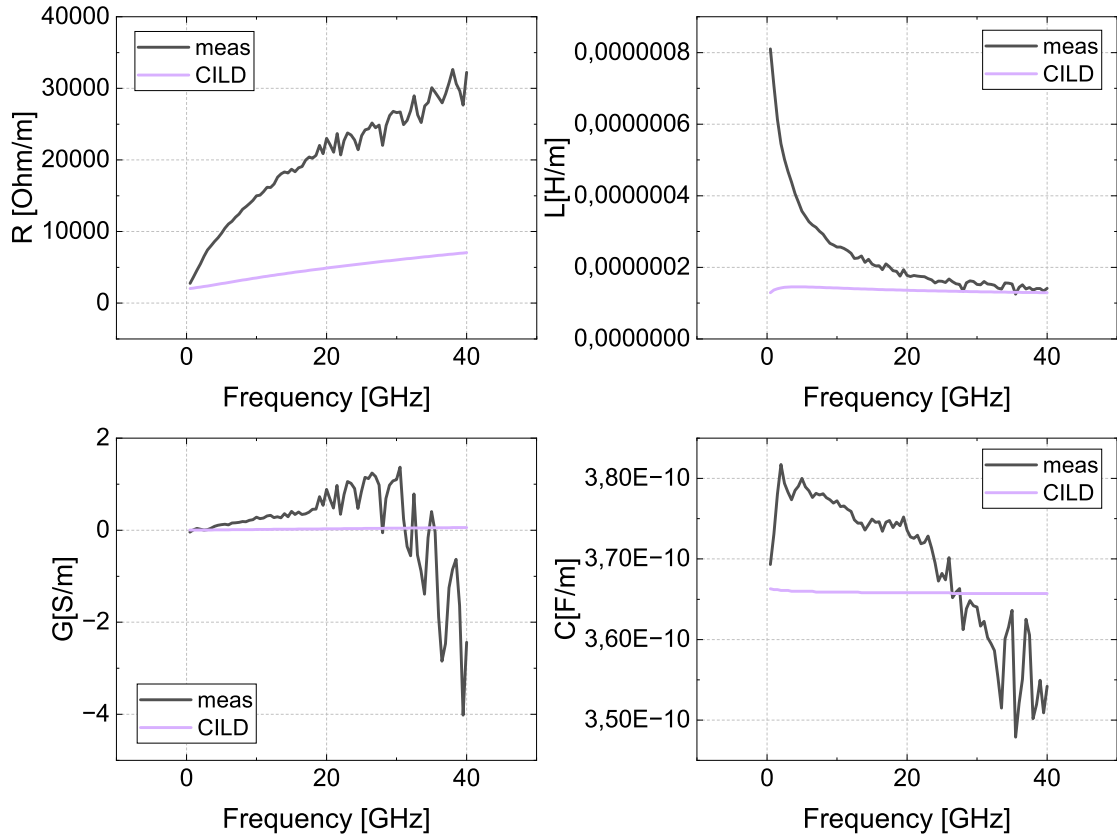


Figure 4.19: $RLGC$ in FD28 with ground plane THRU: comparison between CILD results and measurements with Mangan de-embedding?.

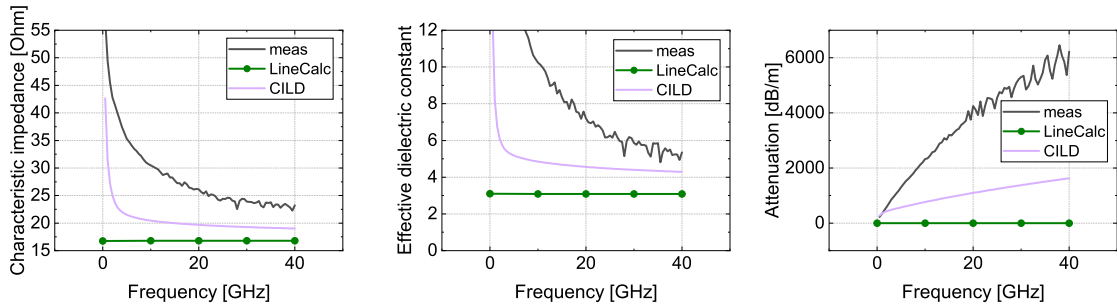


Figure 4.20: Z_c and ϵ_{eff} in FD28 with ground plane THRU: comparison between LineCalc results, CILD results and measurements with Mangan de-embedding.

The same conclusion can be drawn for the analytical simulations. With the uncertainty of the stack configuration, the EM simulations have trouble correctly predicting the behavior of the lines. The analytical simulators will logically have even more trouble mirroring reality.

Chapter 5

Discussion

In the previous section, the EM and analytical simulators were tested on known elements of an Impedance Standard Substrate (ISS) and of an experiment on FD28. The simulators (mainly the EM simulator) showcased a good capability to predict the line behaviors for the ISS case, based on the knowledge of the stack configuration and the layout. The simulations for the FD28 case were less successful because there was some missing or unclear information on the stack. Now it is time to reuse those tools on the real design of interest: the first test mask in 10-nm FD-SOI in the context of the NextGen project.

In this chapter, the stack for the first test mask is described, as well as the different line configurations that were tested. Then, the simulation results will be shown. The layouts were drawn by Dr. Luca Lucci, my industrial supervisor at CEA.

5.1 Design for the first FD10 test mask (TV0)

The BEOL stack for the first test mask in 10-nm is depicted in Figure 5.1. Similarly to the FD28 experiment, some elements will have a ground plane shielding at M1 while others do not have the shield. There are at most 4 metal layers connected by vias, set on top of a Silicon substrate. The different layers are described more in detail in Table 5.1.

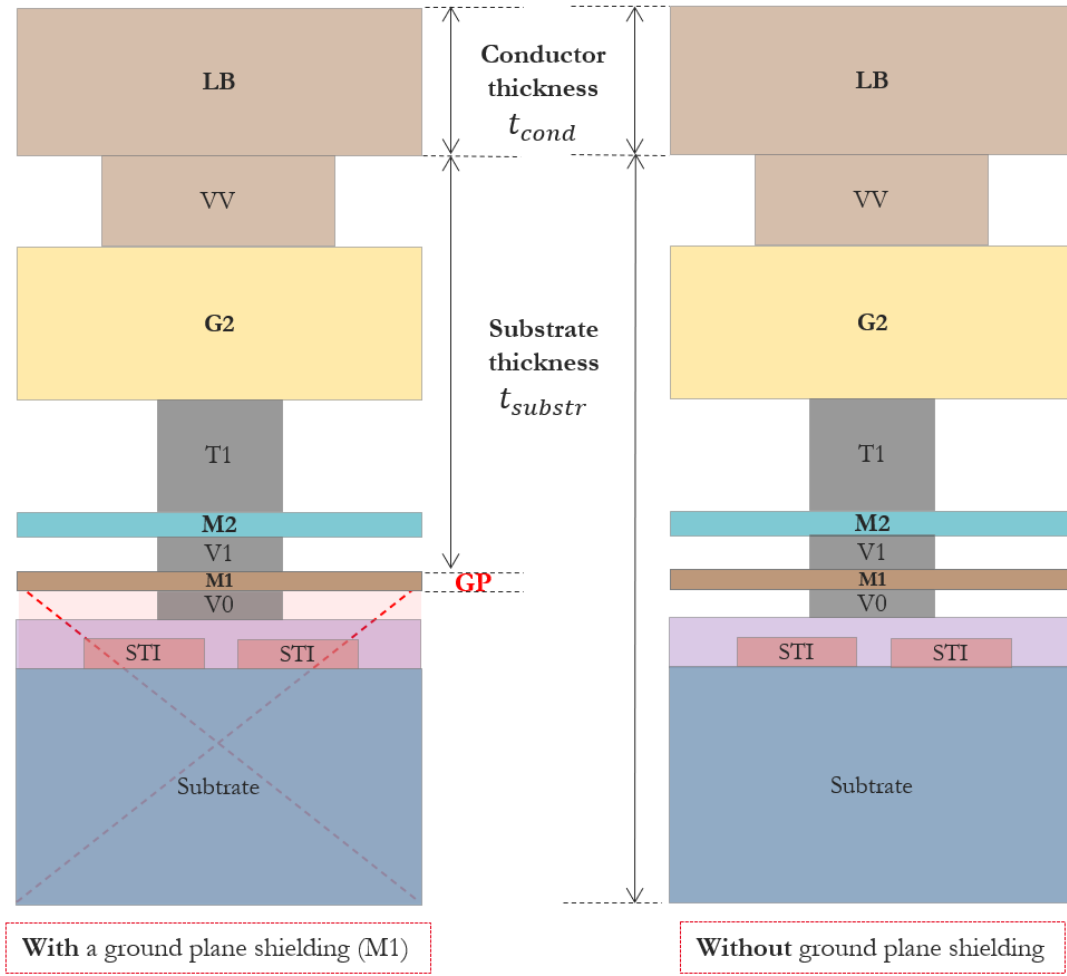


Figure 5.1: Substrate stackup and BEOL for the first FD10 test mask (TV0).

Layer name	Type	Material	Thickness
LB	Metal	Aluminium	2.8 μm
VV	Via	Aluminium	640 nm
G2	Metal	Copper	880 nm
T1	Via	Copper	600 nm
M2	Metal	Copper	63 nm
V1	Via	Copper	62 nm
M1	Metal	Copper	81 nm
V0	Via	Tungsten	68 nm
STI & dielectric	Dielectric	Unknown	290 nm
Substrate	Dielectric	Silicon	1 mm

Table 5.1: Description of the BEOL for TV0

Five lines in total were designed for each line configuration. They are described in Table 5.2.

Line name	Lengths	Units
L07EM	850.62	μm
L10EM	1180.79	μm
L14EM	1619.81	μm
L20EM	2291.07	μm
L30EM	3403.12	μm

Table 5.2: Lines for TV0

5.1.1 Different types of lines tested

The characterization of the FD28 experiment allows the observation of the impact of having a ground plane shielding. The addition of the ground plane reduces the effect of the substrate in a microstrip line, which is desired. The CPW lines can remain unshielded due to the closeness of the grounds on both sides of the signal strip. Based on that, three different line configurations were investigated for the first test mask: two CPW lines with the signal travelling at different metal layers and a ground-shielded microstrip line design.

Before beginning to describe the different lines tested, it is important to mention that real line layouts have complex meshed metal layers and vias that are not simple pillars. That is to satisfy very specific and strict design rules. The line layouts were simplified in order to decrease the computational time and complexity. The meshed metals are unmeshed and the vias are simplified into big single pillars, as can be seen in the example given in Figure 5.2. The layouts that are shown below to describe the different types of lines are the simplified versions.

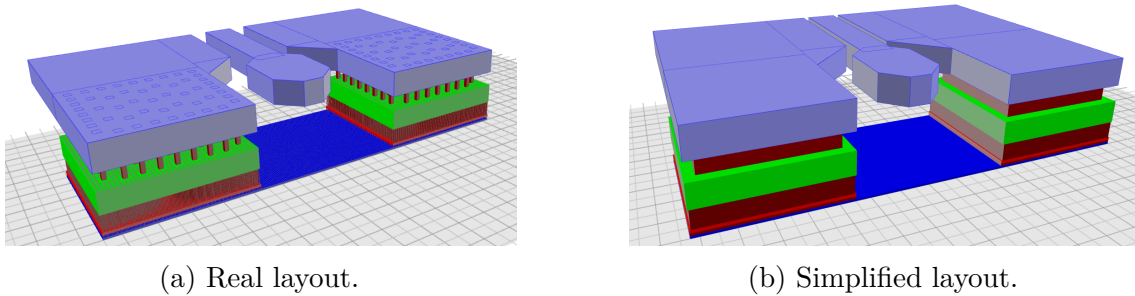


Figure 5.2: Comparison between the real pad layout and the simplified layout for TV0 used in the simulations.

CPW line at LB

For this design, the more 'conventional' one, the signal travels in the LB metal layer. There is no other metal underneath the line itself. The line is directly exposed to the substrate. The signal pads are shielded and the ground pads have all the metal layers connected with vias. A view of the layout of one of those lines is shown in Figure 5.3. It shows the location of the different metals. A three-dimensional view is provided in Figure 5.4 to help visualize the geometry of the line.

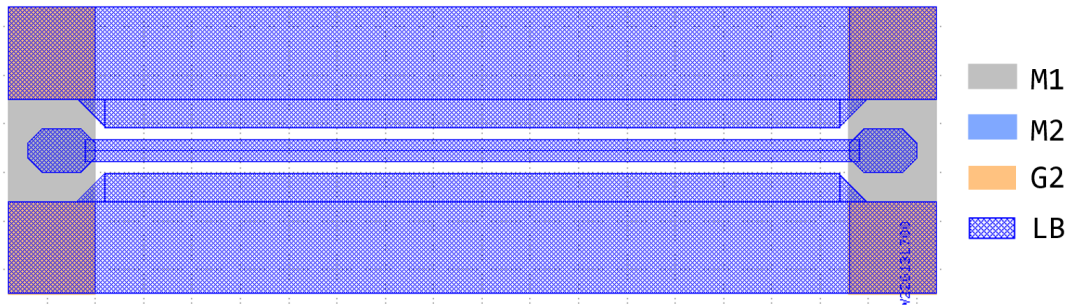


Figure 5.3: Layout of a CPW at LB line for TV0.

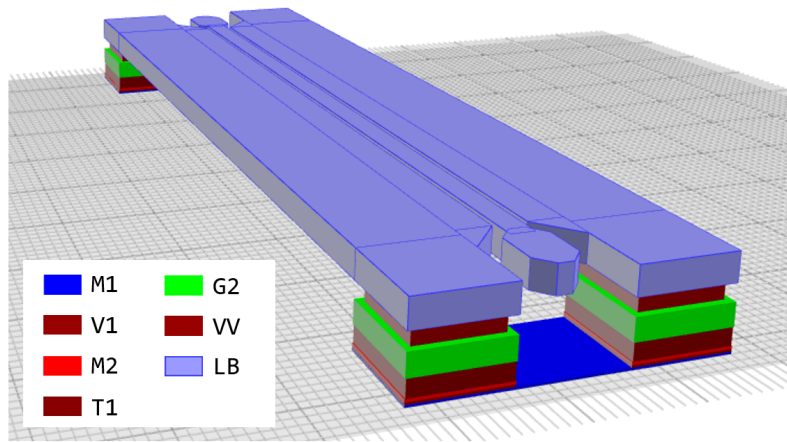


Figure 5.4: 3D view of the layout of a CPW at LB line for TV0.

CPW line at M1

The second type of lines are also CPWs but the signal travels at M1 instead of LB. The lines have only M1 directly exposed to the substrate. The pads go up to LB to keep them accessible for measurements. The signal is brought down the metal layers by the vias. Figure 5.5 shows the layout of such a line and Figure 5.6 shows the three-dimensional view.

It must be pointed out the necessity of this unconventional line layout. During process development, to contain expenses and reduce cycle time, non-essential process steps are frequently skipped. For this reason, the vast majority of the wafers in process development have a BEOL that stops at Metal 1 or Metal 2. Having transmission lines testable directly at M1, and corresponding RF test structures testable at M1 is very important to ensure that RF characterizations can be performed on each and every processed wafer from the very beginning of the technology development.



Figure 5.5: Layout of a CPW at M1 line for TV0.

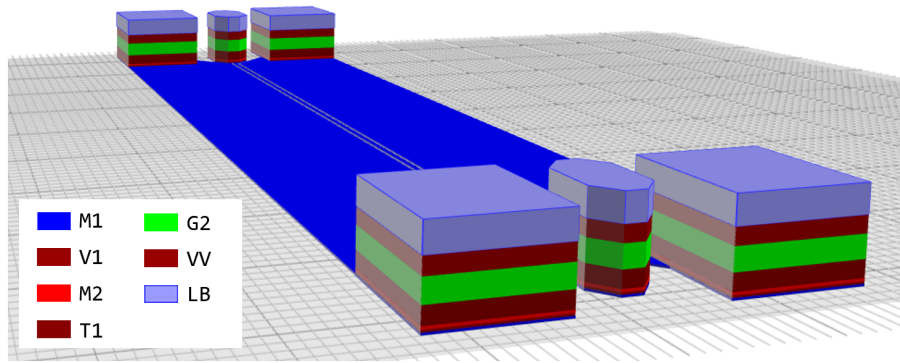


Figure 5.6: 3D view of the layouts of a CPW at M1 line for TV0.

Microstrip line at LB

The last type of line investigated for TV0 is a ground-shielded microstrip line with the signal travelling in the LB layer. M1 is present everywhere acting as the ground plane. Figure 5.7 shows the layout view and Figure 5.8 shows the 3D view.



Figure 5.7: Layout of a microstrip at LB line for the design for the TV0.

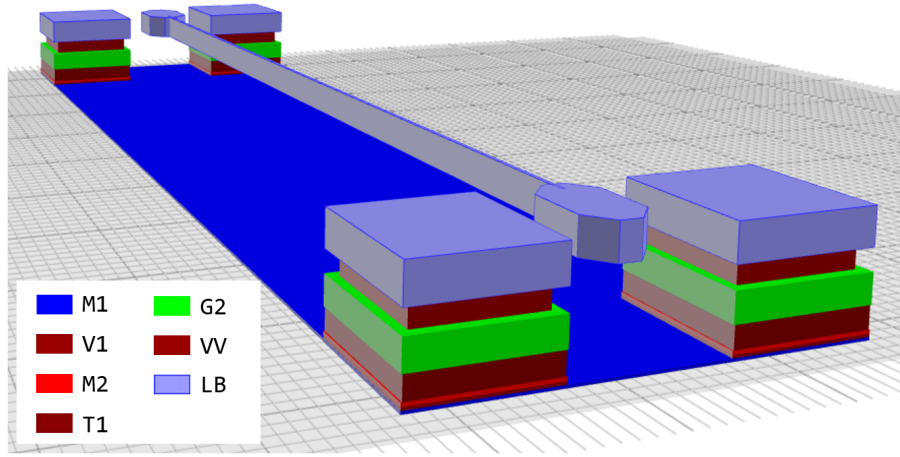


Figure 5.8: 3D view of the layouts of a microstrip at LB line for TV0.

5.2 Simulation results

For the first 10-nm test mask, the analytical simulation tools LineCalc and CILD are used to simulate the three line types. A characteristic impedance of 50 Ohm is set as the goal and the simulators can provide the line dimensions needed to achieve that impedance, with the known stack and line parameters. In LineCalc, this is done by setting Z_0 to 50 Ohms and by using the *Synthesis* mode. On the other hand, CILD has the *Optimize* mode that allows the optimization of one chosen parameter with a set goal, that is $Z_c = 50$ Ohms in this case.

5.2.1 Analytic simulations: LineCalc and CILD

Here are the results from both simulators for the three different line configurations. For CPW lines, the width (or the gap) needs to be set in order to optimize the gap (or the width). Arbitrary width (or gap) is fixed to find the corresponding gap (or width).

These simulated dimensions will help with the preliminary design of the transmission lines meant for TV0. They give an idea of the line dimensions needed to have a transmission line that minimizes power reflection. Using those dimensions to draw line layouts will allow for further EM simulations to confirm the behavior of the lines and determine whether they meet the requirements.

CPW line at LB

Tables 5.3 and 5.4 respectively list the simulation settings and two options of dimensions to achieve the best characteristic impedance, for a CPW line with the signal propagating in the LB layer.

Parameter	Value	Unit
ϵ_r	11.68	/
Mur	1	/
t_{substr}	1002.684	μm
t_{cond}	2.8	μm
ρ	3.538e+7	/
$TanD$	0.001	/
Frequency	10	GHz
L	150	μm

Table 5.3: Parameters setting for the LineCalc and CILD simulation of a CPW at LB line for TV0.

Fixed	Parameter	LineCalc	CILD	Unit
$W = 24 \mu\text{m}$	G	18.412	12.94	μm
	Z_c	50	50	Ohm
	ϵ_{eff}	5.811	4.971	/
	l_{eff}	4.209	4.016	degree
	Attenuation	153.333	132.69	dB/m
$G = 8 \mu\text{m}$	W	7.674	12.547	μm
	Z_c	50	50	Ohm
	ϵ_{eff}	5.201	4.937	/
	l_{eff}	4.209	4.002	degree
	Attenuation	406.667	204.516	dB/m

Table 5.4: Results for the LineCalc and CILD simulation of a CPW line at LB for TV0, with fixed width or fixed gap.

CPW line at M1

Tables 5.5 and 5.6 respectively list the simulation settings and two options of dimensions to achieve the best characteristic impedance, for a CPW line with the signal propagating in the M1 layer.

Parameter	Value	Unit
ϵ_r	11.68	/
Mur	1	/
t_{substr}	1000.358	μm
t_{cond}	0.081	μm
ρ	5.96e+7	/
$TanD$	0.015	/
Frequency	10	GHz
L	50	μm

Table 5.5: Parameters setting for the LineCalc and CILD simulation of a CPW at M1 line for TV0.

Fixed	Parameter	LineCalc	CILD	Unit
$W = 5 \mu\text{m}$	G	3	2.849	μm
	Z_c	50	78.512	Ohm
	ϵ_{eff}	6.127	7.741	/
	l_{eff}	1.492	1.671	degree
	Attenuation	4280	464.038	dB/m
$G = 8 \mu\text{m}$	W	13.818	30.381	μm
	Z_c	50	43.012	Ohm
	ϵ_{eff}	6.185	5.923	/
	l_{eff}	1.491	1.461	degree
	Attenuation	1580	808.143	dB/m

Table 5.6: Results for the LineCalc and CILD simulation of a CPW line at M1 for TV0, with fixed width or fixed gap.

Microstrip line at LB

Finally, tables 5.7 and 5.8 respectively list the simulation settings and the dimension required to achieve the best characteristic impedance, for a microstrip line with the signal propagating in the LB layer.

Parameter	Value	Unit
ϵ_r	4.088	/
Mur	1	/
t_{substr}	2.245	μm
t_{cond}	2.8	μm
ρ	3.538e+7	/
$TanD$	0.001	/
Frequency	10	GHz
L	100	μm

Table 5.7: Parameters setting for the LineCalc and CILD simulation of a microstrip at LB line for TV0.

Parameter	LineCalc	CILD	Unit
W	3.2	2.5	μm
Z_c	50	50	Ohm
ϵ_{eff}	2.670	4.732	/
l_{eff}	1.789	2.612	degree
Attenuation	530	442.477	dB/m

Table 5.8: Results for the LineCalc and CILD simulation of microstrip at LB line for TV0.

5.2.2 EM simulations: Momentum

Based on the dimensions provided by LineCalc and CILD summarized in Table 5.9, lines were drawn to be simulated by Momentum. CILD is more trustworthy than LineCalc, thus, the line dimensions highlighted in Table 5.9 are used for the EM simulations. This part will show the EM simulation results for the three types of lines with those dimensions, with an analysis of the sensitivity of the line parameters to a variation in the line dimensions.

	CPW at LB		CPW at M1		MS at LB
	W [μm]	G [μm]	W [μm]	G [μm]	W [μm]
LineCalc	24 7.674	18.412 8	5 13.818	3 8	3.2
CILD	24	12.94	2.849	5	2.5
	12.547	8	30.381	8	

Table 5.9: Summary of the dimensions predicted by LineCalc and CILD for all line configurations to achieve $Z_c = 50$ Ohms.

CPW line at LB

Figure 5.9 shows EM simulations results of the *RLGC* and 5.10 shows the Z_c and ϵ_{eff} for the CPW *L20EM* line at LB. The default dimensions are the ones given by CILD (Table 5.9): $W = 24 \mu m$ and $G = 13 \mu m$. It is plotted in solid green in the figures. It showcases a characteristic impedance that decreases with frequency and hits 50 Ohms at around 35 GHz, with an effective dielectric constant of about 5.1.

The sensibility of the line parameters is analyzed by performing a variation of $2 \mu m$ on the width (short dotted) and on the gap (dash-dotted) respectively. The line losses (R and G) and the effective dielectric constant are not greatly impacted by the width or gap variations. A wider line or a line with a smaller gap leads to a decrease in the lineic inductance (of 20 to 40 nH/m) and an increase in the lineic capacitance (of 5 to 10 pF/m). That translates into a decrease in the characteristic impedance (of 1.2 to 2.5 Ohms).

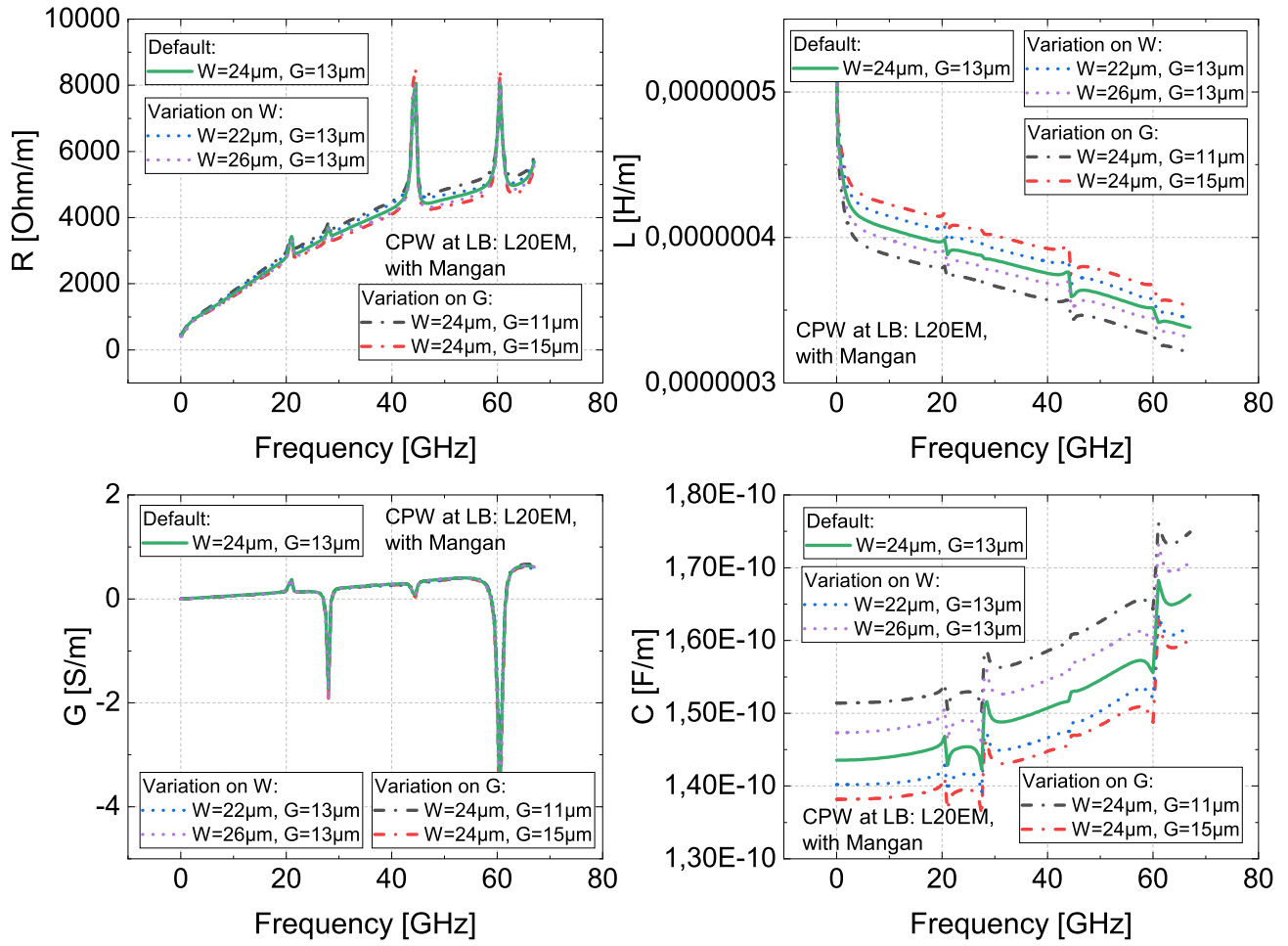


Figure 5.9: $RLGC$ of TV0 CPW at LB L20EM line: with default dimensions and with variations of line width and gap, Mangan de-embedded.

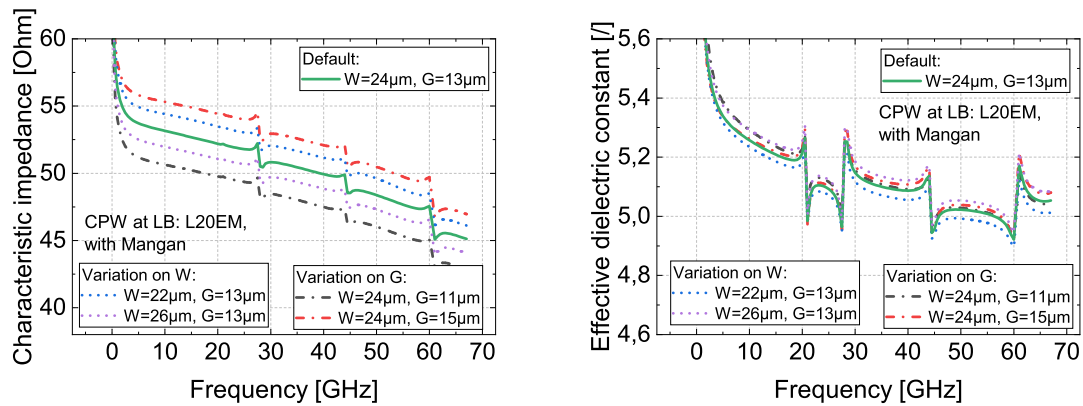


Figure 5.10: Z_c and ϵ_{eff} of TV0 CPW at LB L20EM line: with default dimensions and with variations of line width and gap, Mangan de-embedded.

CPW line at M1

Just like the CPW at LB, the default dimensions, $W = 30 \mu\text{m}$ and $G = 8 \mu\text{m}$ (Table 5.9, for the CPW at M1 was tested, alongside with a variation of $2 \mu\text{m}$ on the width and the gap. The $RLGC$ are plotted in Figure 5.11. The Z_c and ϵ_{eff} are shown in Figure 5.12. This time, the impact of the fluctuation in the gap size on the lineic resistance is visible. The R sees a shift of about 2000 Ohm/m with a gap bigger or smaller by $2 \mu\text{m}$. the G remain not that sensitive to width and gap variations. The value of the lineic inductance decreases (for 10 to 15 nH/m) and the lineic capacitance increases (for 50 to 150 pF/m) for a wider line or more narrow gap, just like the CPW at LB line. In term, that leads to a characteristic impedance that shifts by 1 to 2 Ohms. The effective dielectric constant can vary up to 0.1.

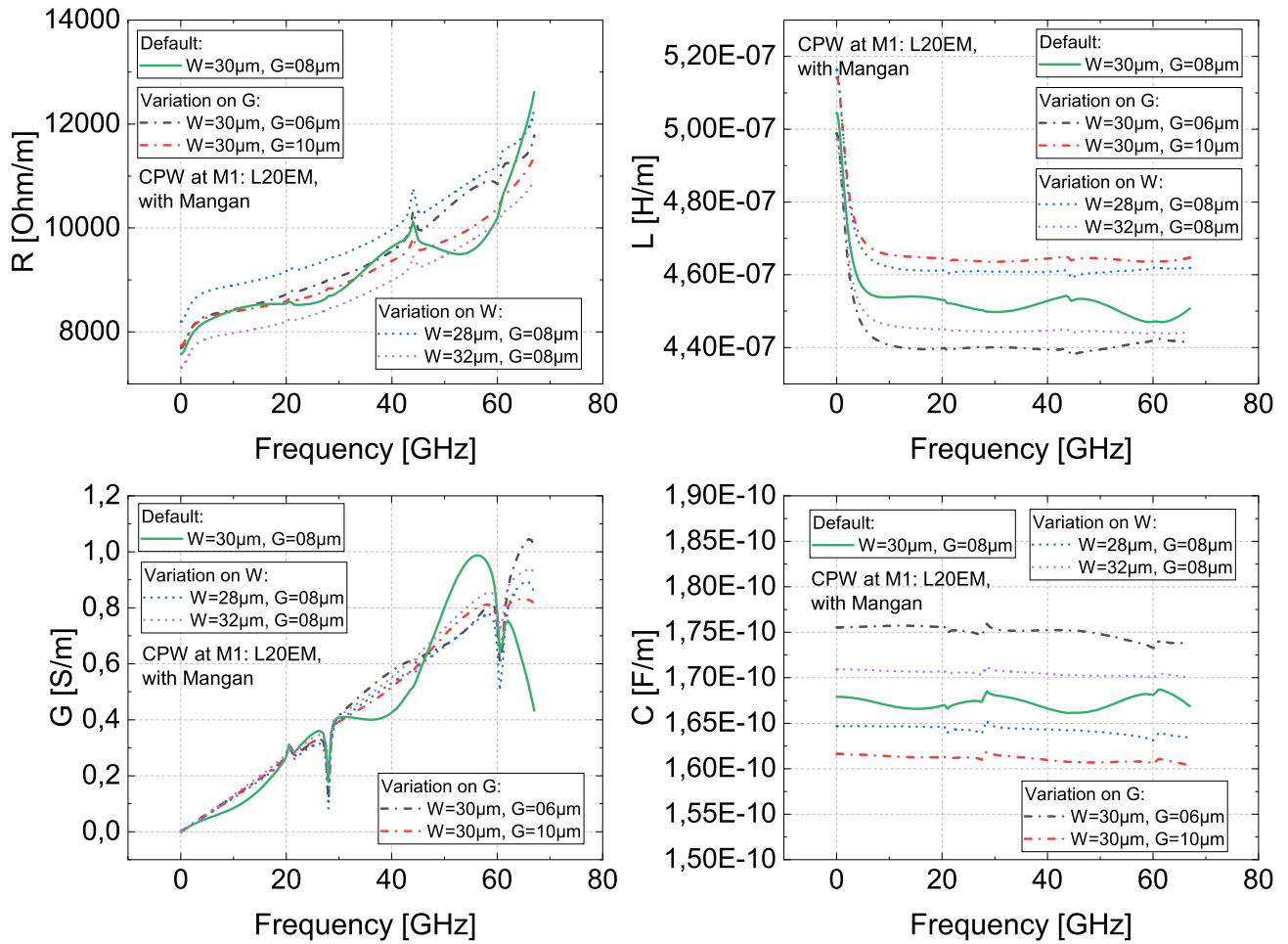


Figure 5.11: $RLGC$ of TV0 CPW at M1 L20EM: line with default dimensions and with variations of line width and gap, Mangan de-embedded.

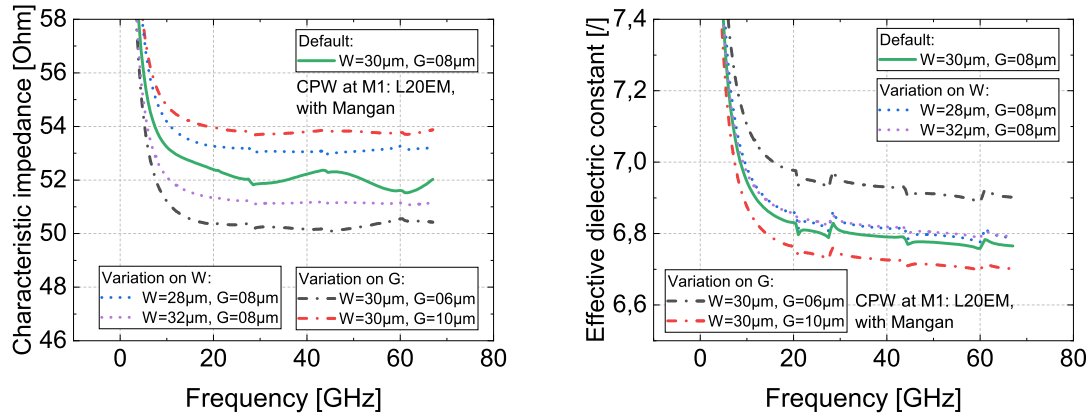


Figure 5.12: Z_c and ϵ_{eff} of TV0 CPW at M1 L20EM: line with default dimensions and with variations of line width and gap, Mangan de-embedded.

Microstrip at LB

For the microstrip at LB, both LineCalc and CILD have given widths that are not manufacturable. According to the design-rules manual, any LB line needs to be at least $3.6 \mu\text{m}$ wide to be able to be put into production. A microstrip line at LB with the narrowest line manufacturable is simulated in Momentum to monitor its behavior, see Figures 5.13 and 5.14. As expected, the characteristic impedance is near but not exactly at 50 Ohms. It decreases from about 45 to 42 over the frequencies. Though it could be acceptable, further investigations are done to try to continue optimizing this line.

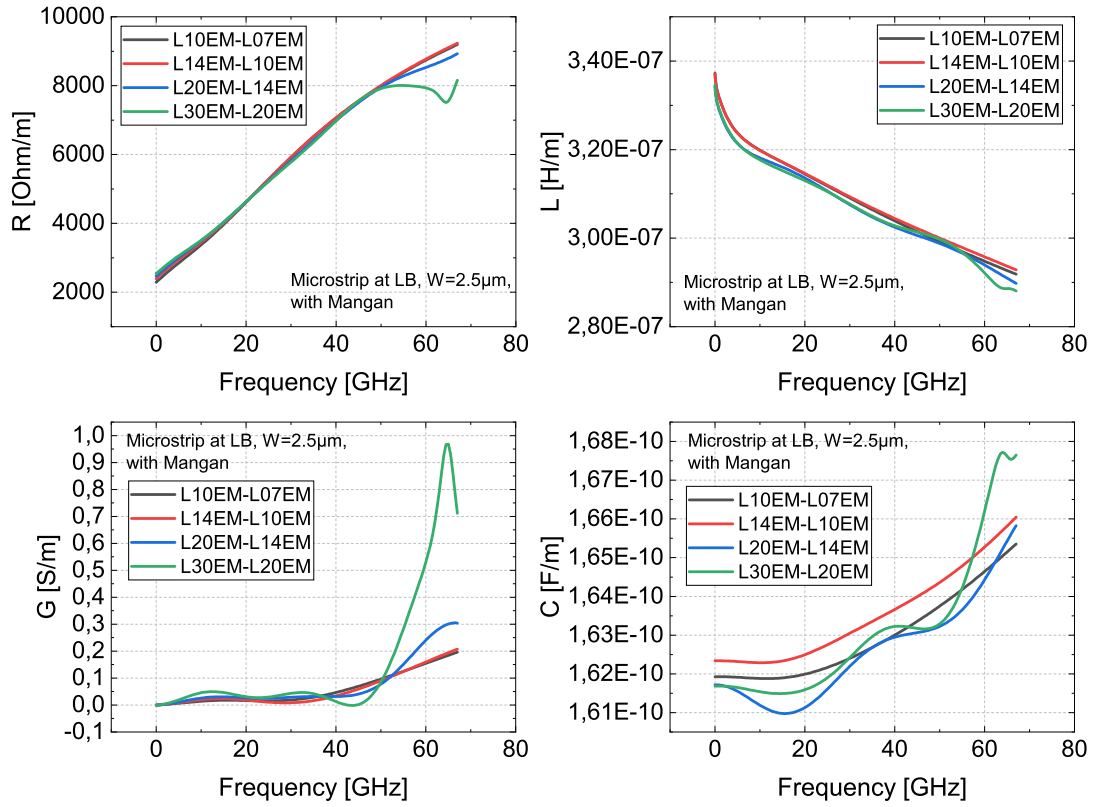


Figure 5.13: $RLGC$ of TV0 microstrip at LB lines: with $W = 3.6 \mu\text{m}$, Mangan de-embedded.

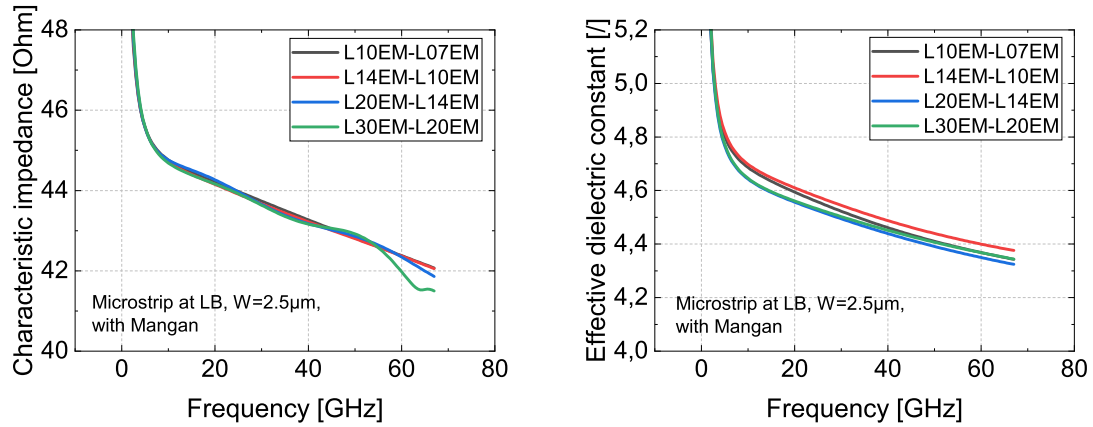


Figure 5.14: Z_c and ϵ_{eff} of TV0 microstrip at LB lines: with $W = 3.6 \mu\text{m}$, Mangan de-embedded.

M1 unlike LB is a layer that is very well controlled in the manufacturing process. The line dimensions can have a deviation in the order of the nanometers, which is negligible in the micrometre scale of the lines. It is seen that the width needs to be at least $3.6 \mu\text{m}$ and can not be further tuned. A play on the conductor thickness

can compensate for the inflexibility of the line width to get a line that is closer to 50 Ohms. Another option would be to fine-tune the thickness of the VV via that can also modify the line parameters and bring the line closer to the desired characteristic impedance.

Variation of LB

The nominal thickness for the LB metal is $2.8 \mu\text{m}$. The line is tested with a conductor thickness that decreases down to $1 \mu\text{m}$. A thinner conductor increases the losses in the overall. The lineic inductance sees an increase, whereas the lineic conductance perceives a decrease. Overall, the characteristic impedance increases with a thinner LB, which is the desired effect. The best LB thickness would be at $2 \mu\text{m}$, as it gives a characteristic impedance very close to 50 Ohms.

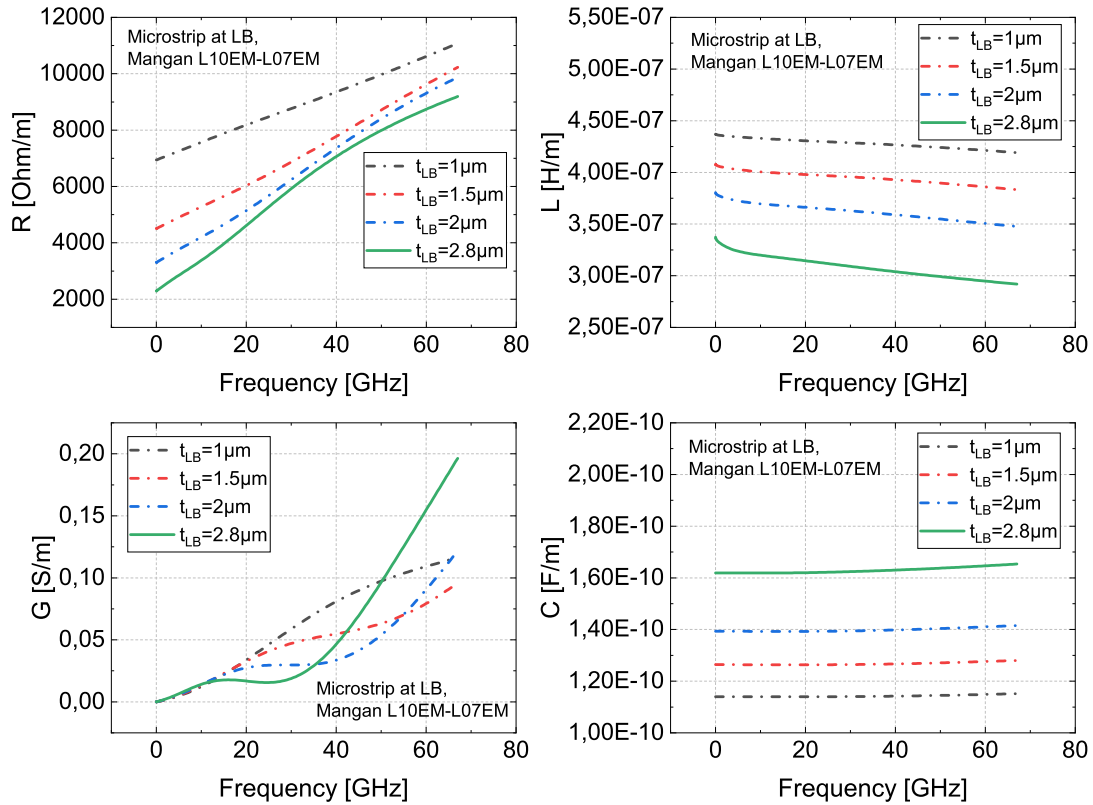


Figure 5.15: $RLGC$ of TV0 microstrip at LB L10EM line: with $W = 3.6 \mu\text{m}$ and a variation LB thickness, Mangan de-embedded.

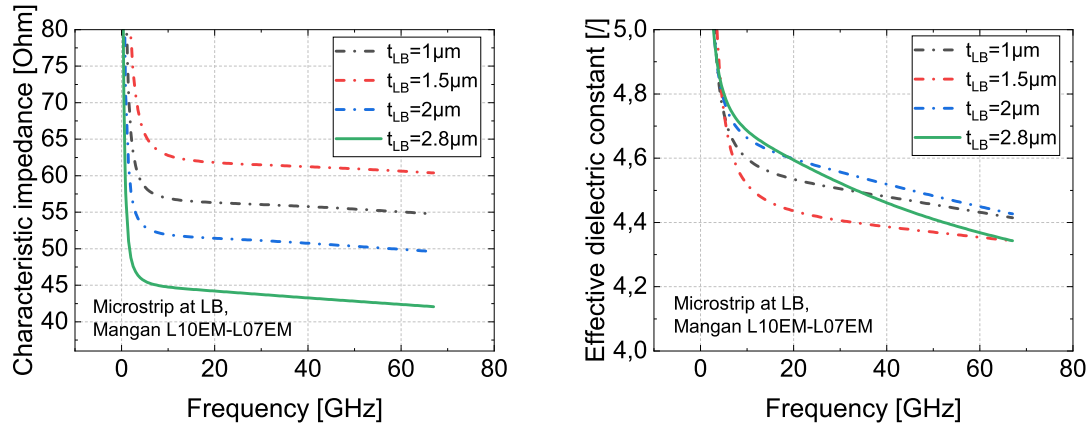


Figure 5.16: Z_c and ϵ_{eff} of TV0 microstrip at LB L10EM line: with $W = 3.6 \mu m$ and a variation LB thickness, Mangan de-embedded.

Variation of VV

The impact of the VV via thickness is investigated in Figure 5.17 and 5.18. The via thickness is doubled and tripled to again increase the value of the characteristic impedance. Varying the via thickness does not impact the lineic conductance at low frequencies and the lineic resistance until 67 GHz. Similar to the effect of decreasing the conductor thickness, increasing the VV via results in an upward shift of the lineic inductance and a downward shift of the lineic capacitance. The best choice of VV via thickness would be a bit thicker than $1.2 \mu m$.

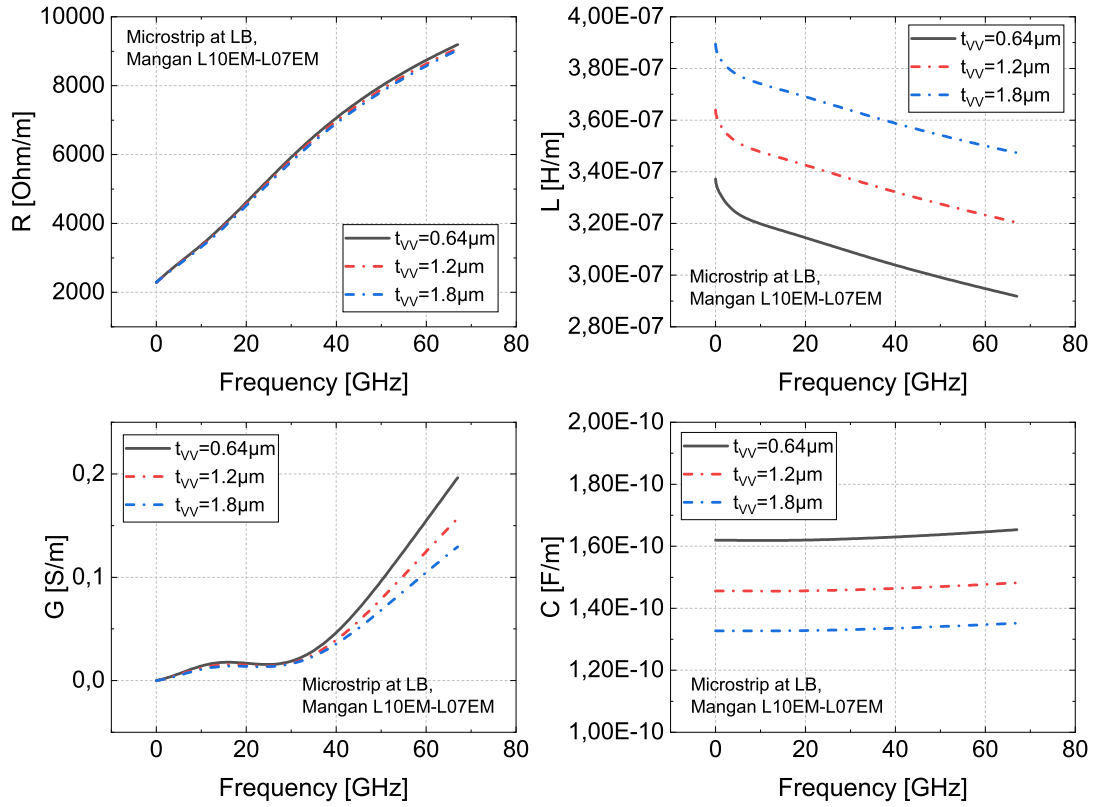


Figure 5.17: $RLGC$ of TV0 microstrip at LB L10EM line: with $W = 3.6 \mu\text{m}$ and a variation VV via thickness, Mangan de-embedded.

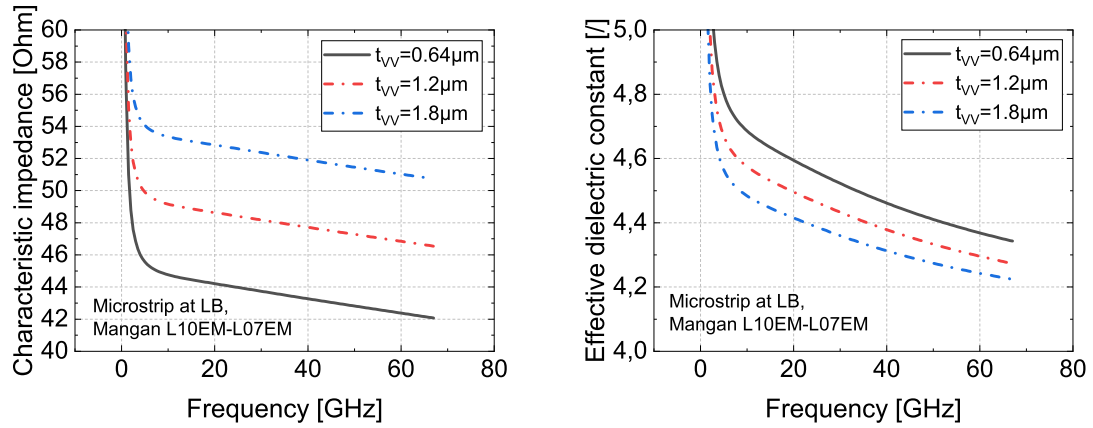


Figure 5.18: Z_c and ϵ_{eff} of TV0 microstrip at LB L10EM line: with $W = 3.6 \mu\text{m}$ and a variation VV via thickness, Mangan de-embedded.

5.3 Conclusion for TV0

Three line configurations of interest were investigated in this chapter. the LB metal layer is not as precisely controlled as the M1 metal layer. Therefore, there could be

a deviation in the line dimensions or conductor thickness during the manufacturing. Two types of lines have their signal propagating in this metal. The CPW line at LB showcases a good performance with a deviation of the characteristic impedance of 1 to 2.5 Ohms for 2 μm of error in the line width or gap. The microstrip at LB needs a change of conductor or via thickness to achieve minimum reflection because of the design rules limitations mentioned above. Opting for a thinner LB can give a flatter characteristic impedance over the frequencies but the control over the LB thickness is not very strict. Choosing to make a thicker via could seem like a better solution as the losses are less influenced by the change in via thickness but having a VV via that is too thick could lead to a discontinuity in the LB layer during the deposition.

Both options, thinner LB and thicker VV, are technologically feasible and not mutually exclusive and give good perspective for achieving good matching results in the TV0 test-structures.

Chapter 6

Conclusion

Europe and France have massively invested in the research and design of a new generation of Fully-Depleted-Silicon-on-Insulator (FD-SOI) to revive the design, R&D and manufacturing of microelectronics to reestablish their competitiveness in future markets and their sovereignty. In this context, CEA, in collaboration with many industrial and academic partners, are working on a project called *NextGen*. The project is still at an early stage and the first milestone will be the design of the first FD10 test mask to be sent for manufacturing to allow on-wafer measurements and testing later on in the project.

This work takes part in this large-scale project and focuses on the design RF test structures. Theoretical closed-forme approximation by W. Heinrich [12] and multiple analytical and EM simulation tools: LineCalc, Controlled Impedance Line Designer (CILD) and Momentum from Advance Design System (ADS), are investigated to try to establish a routine to support the design of future test structures or other devices still in the design phase.

These techniques were first tested on two types of test structure designs before being used to support the design of test structures in view of the first FD10 test mask in the NextGen project.

Transmission lines are the main focus of this work. Therefore, the characteristic impedance is the most important parameter that needs to reach the targeted 50 Ohms. For lossless transmission lines or lines that can be considered as nearly lossless, the value of the characteristic impedance comes from the lineic inductance and the lineic capacitance of the *RLGC* equivalent circuit. According to Mongia, Bahl and Bhartia [10], the determination of the characteristic impedance of a transmission line ultimately reduces to the determination of two capacitances of the structure. This highlights the importance of achieving a good accuracy in the prediction of the lineic inductance and especially capacitances when characterizing a transmission line.

First, analytical and EM simulations were done on 138-356 ISS lines. Measurements of its verification lines were available and can be used to appreciate the accuracy and quality of the different techniques used in their characterisation. The EM results

showed an ability to bound the measured lineic inductance from both sides, with an error of at most 10nH. The performance of the EM simulations on the lineic capacitance meets a deviation of up to 15 pF, (10%). The deviation of the simulated characteristic impedance compared to the measurements reflects the ones seen in the lineic inductance and capacitance. The EM simulations make an error of 1 to 2 Ohms.

A de-embedding technique introduced by Mangan and his colleagues was used on the measurements and EM simulations to clean these data from the parasitic effects of the pads. The EM simulations have more trouble predicting the effective dielectric constant and the losses of the lines, i.e. the lineic resistance and conductance.

For the analytical simulators, LineCalc and CILD, an error of 3 to 5 Ohms is seen on the value of the characteristic impedance. Errors of 10nH and 15 pF were respectively observed for the lineic inductance and capacitance between the results from CILD and the measurements. This means that the analytical simulators are able to get close to the real parameter values of the lines with an accuracy that is similar to the maximum error done by the EM simulator.

Similarly, lines in a FD28 design, with a similar stack configuration as what is intended for the FD10 test mask, were tested. The simulation results showed less accuracy in predicting the measured values of the important parameters with a simulated characteristic impedance that is off by 8 to 10 Ohms. This is due to uncertainties in the stack configuration and physical parameters. Assumptions were made, resulting in the deviations observed. The interesting conclusions that can be drawn from that experiment are that the simulation methods are still able to give an idea of the behavior of the lines despite missing information and the impact of the Mangan de-embedding is even better than for the ISS lines because the pad configuration in the FD28 experiment corresponds more to the assumption made in this particular de-embedding technique (i.e. the pad is assumed to be a lumped admittance [20]).

Finally, the interest in using such simulation tools in the design process of test structures is demonstrated on the first FD10 test mask. The analytical simulators, especially CILD, which is more sophisticated and thus accurate than LineCalc, are used to get an idea of the line dimensions to use for specified stack and line configurations. The corresponding layouts are then drawn and simulated using Momentum to verify their behaviors.

If one wants to have an insight into the behavior of a transmission line or other types of structures, one should rely on EM simulations. However, those types of simulations are lengthy to set up and need extensive knowledge of the structure's physical parameters and layout. At the beginning of the design process, the engineer can use the analytical simulation tools to form a perspective on how the design choices impact the structure's behavior. Analytical simulators allow him to easily test different parameters to help him decide on the first set of parameter choices. Then, he can use Momentum or equivalent EM simulation tools to confirm whether

or not the chosen parameters give out the desired device behavior. Fine-tuning is then possible to achieve the best results under the design rule set.

The mix and match of the characterization techniques used in this work can support the engineer's design choices and help reduce the likelihood of testing and redesigning which are expensive and time-consuming. The final EM simulation results provide the engineer with a tangent proof of the behavior that is expected from the designed structures.

This work focused on transmission line test structures. Looking ahead, an investigation into more sophisticated test structures is of interest to provide the future users of the developed calibration kit with an extensive set of test structures that allows them to perform a variety of calibrations, de-embeddings and characterizations. The work will continue onto the full electrical characterization of the in-development RF test structures and the real on-wafer characterization of the first test mask, once it has been manufactured. Investigation into the environmental implications and impacts of the development and manufacturing of the new generation of FD-SOI could also be interesting.

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Appendices

Appendix A

RLGC extraction model used by Keysight ADS

$$\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \quad (\text{A.1})$$

$$\omega = 2\pi f \quad (\text{A.2})$$

$$Z_c = \sqrt{\frac{Z_{11}}{Y_{11}}} \quad (\text{A.3})$$

$$\gamma_{wrapped} = \arctan\left(\frac{1}{Z_c Y_{11}}\right) / Length \quad (\text{A.4})$$

$$\gamma = \alpha + j\beta \quad (\text{A.5})$$

$$R = \Re(\gamma Z_c) \quad (\text{A.6})$$

$$L = \Im(\gamma Z_c) / \omega \quad (\text{A.7})$$

$$G = \Re(\gamma / Z_c) \quad (\text{A.8})$$

$$C = \Im(\gamma / Z_c) / \omega \quad (\text{A.9})$$

$$\alpha = \Re(\gamma_{wrapped}) \quad (\text{A.10})$$

$$\beta_{wrapped} = \Im(\gamma_{wrapped}) \quad (\text{A.11})$$

$$\beta = \frac{\text{unwrap}\left(\frac{\beta_{wrapped} * Length * 180}{\pi}, 90\right) * \pi}{180 * Length} \quad (\text{A.12})$$

$$att[dB/m] = 20\alpha * \log e \quad (A.13)$$

$$velocity = \frac{\omega}{\beta} \quad (A.14)$$

$$= \frac{1}{\beta} \quad (A.15)$$

$$\epsilon_{eff} = \sqrt{\frac{c}{velocity}} \quad (A.16)$$

$$delay[ps/m] = \frac{1e12}{velocity} \quad (A.17)$$

$$phaseShift = \beta * Length * \frac{180}{\pi} \quad (A.18)$$

Appendix B

Selection of short line for the Mangan de-embedding

Mangan de-embedding, as described in [20], uses a shorter line of length l_1 to de-embed a longer line of length l_2 . It gets rid of the parasitic effects of the pad to only keep the characteristics of the line segment of length l_2-l_1 . Here, two different choices of the shorter line are investigated. The goal is to determine whether it is preferable to use the thru to de-embed all the longer lines or if the next shorter line would be a better candidate. The next figures showcase the comparison between the two choices of shorter lines for some 138-356 ISS lines from the measurements and from the EM simulations. The conclusion drawn is that the next shorter line is the best candidate to perform the de-embedding because, in our tests, it gives out cleaner results.

B.1 ISS Measurements

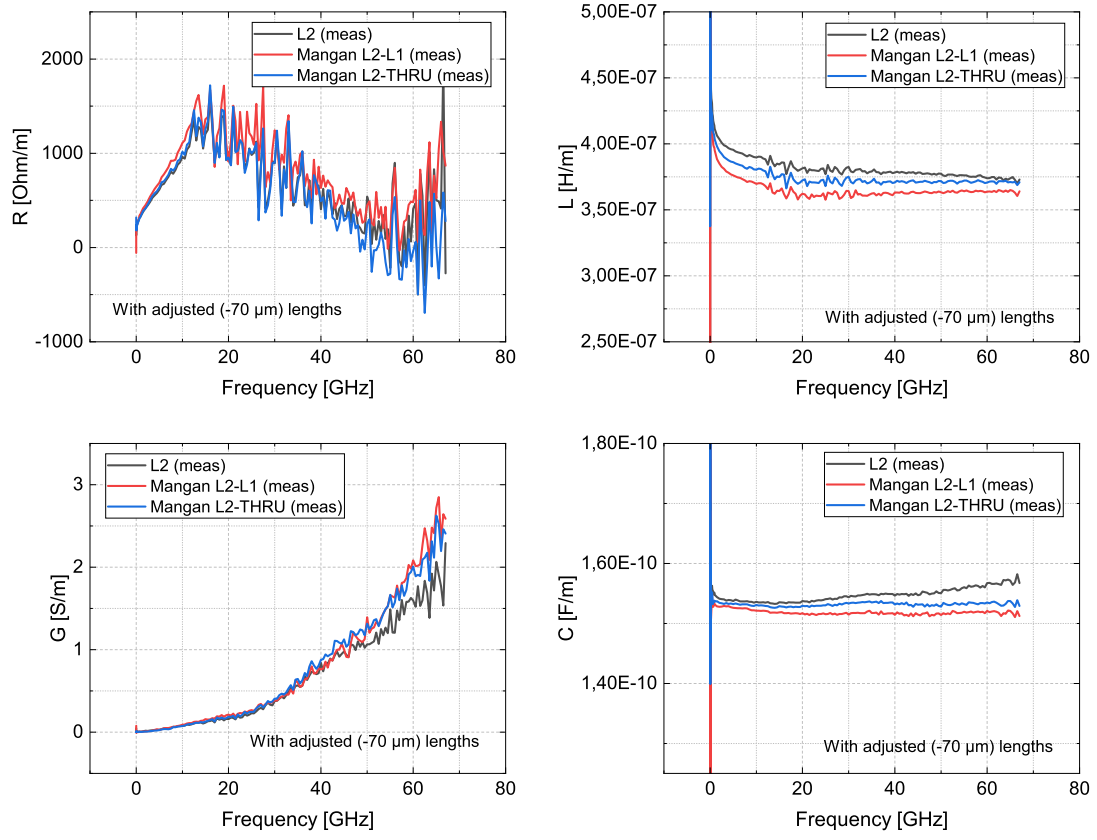


Figure B.1: Effect of Mangan applied to 138-356 L2 measurements, using L1 or THRU as the shorter line in the operation.

APPENDIX B. SELECTION OF SHORT LINE FOR THE MANGAN DE-EMBEDDING

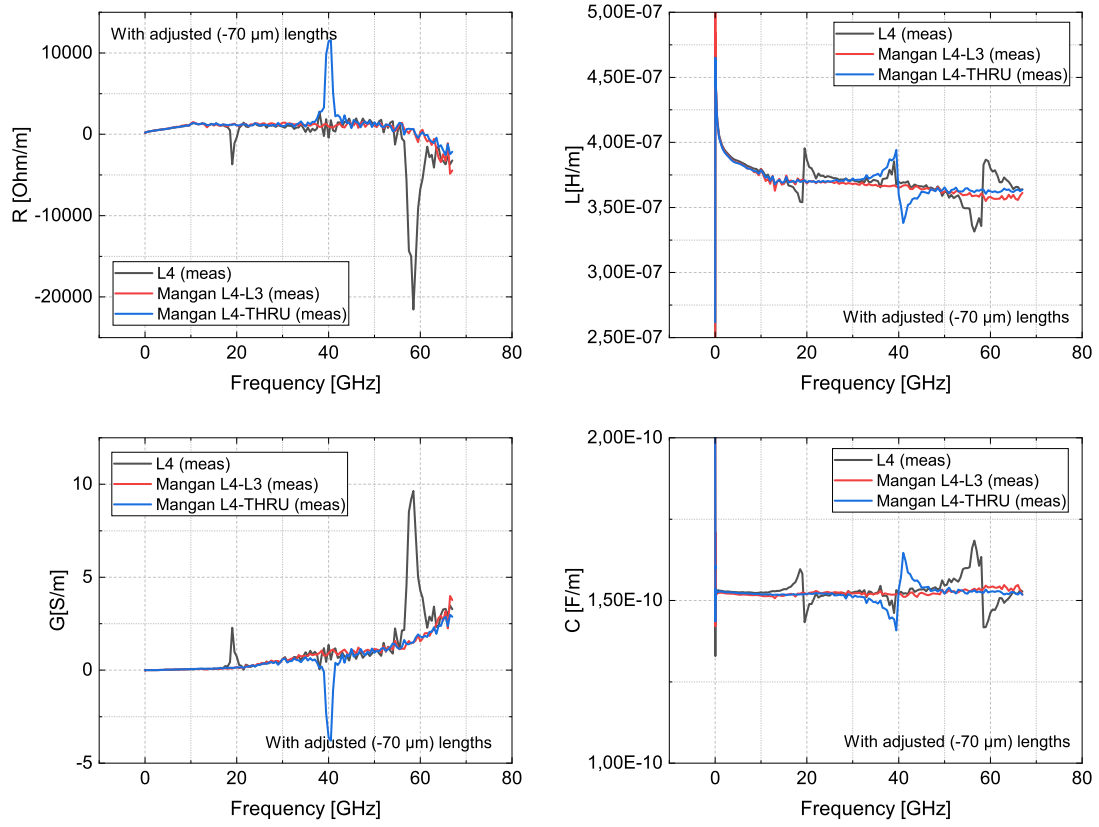


Figure B.2: Effect of Mangan applied to 138-356 L4 measurements, using L3 or THRU as the shorter line in the operation.

APPENDIX B. SELECTION OF SHORT LINE FOR THE MANGAN DE-EMBEDDING

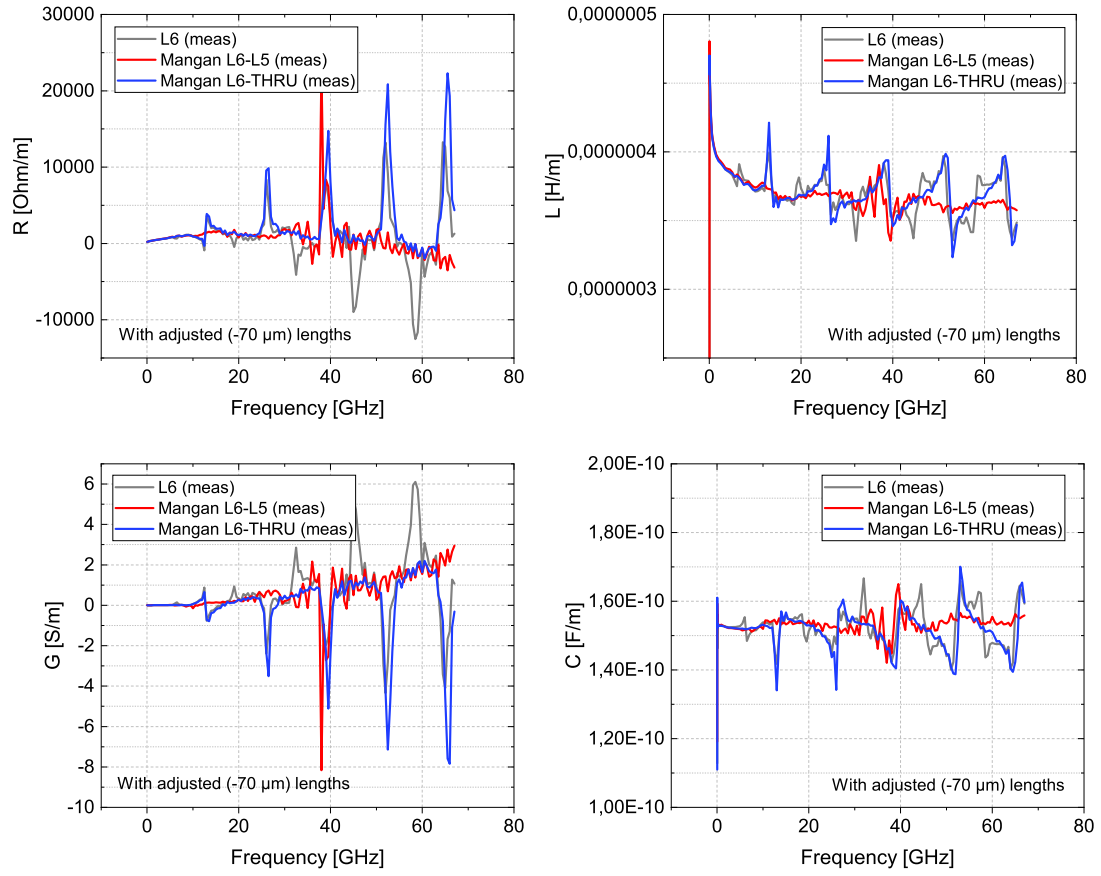


Figure B.3: Effect of Mangan applied to 138-356 L6 measurements, using L5 or THRU as the shorter line in the operation.

B.2 ISS EM simulations

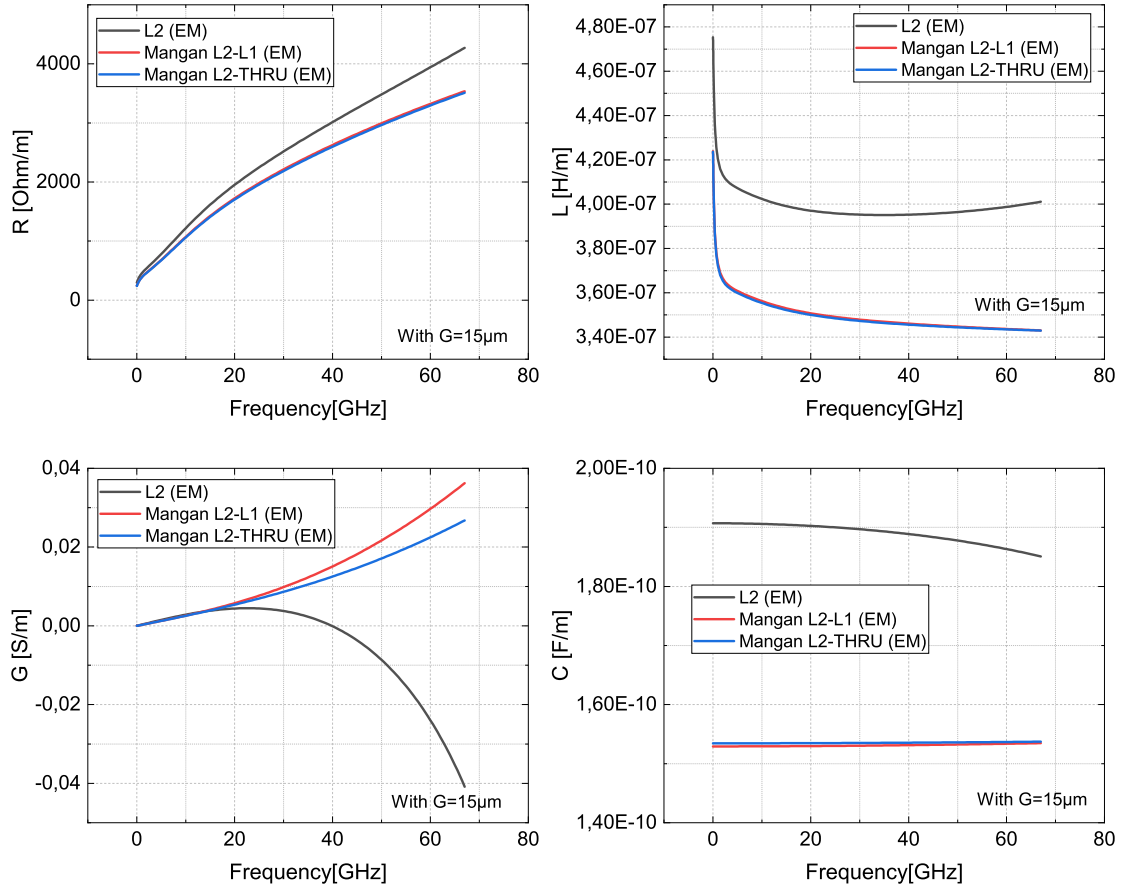


Figure B.4: Effect of Mangan applied to 138-356 L2 Momentum EM simulations ($G=15\mu\text{m}$), using L1 or THRU as the shorter line in the operation.

APPENDIX B. SELECTION OF SHORT LINE FOR THE MANGAN DE-EMBEDDING

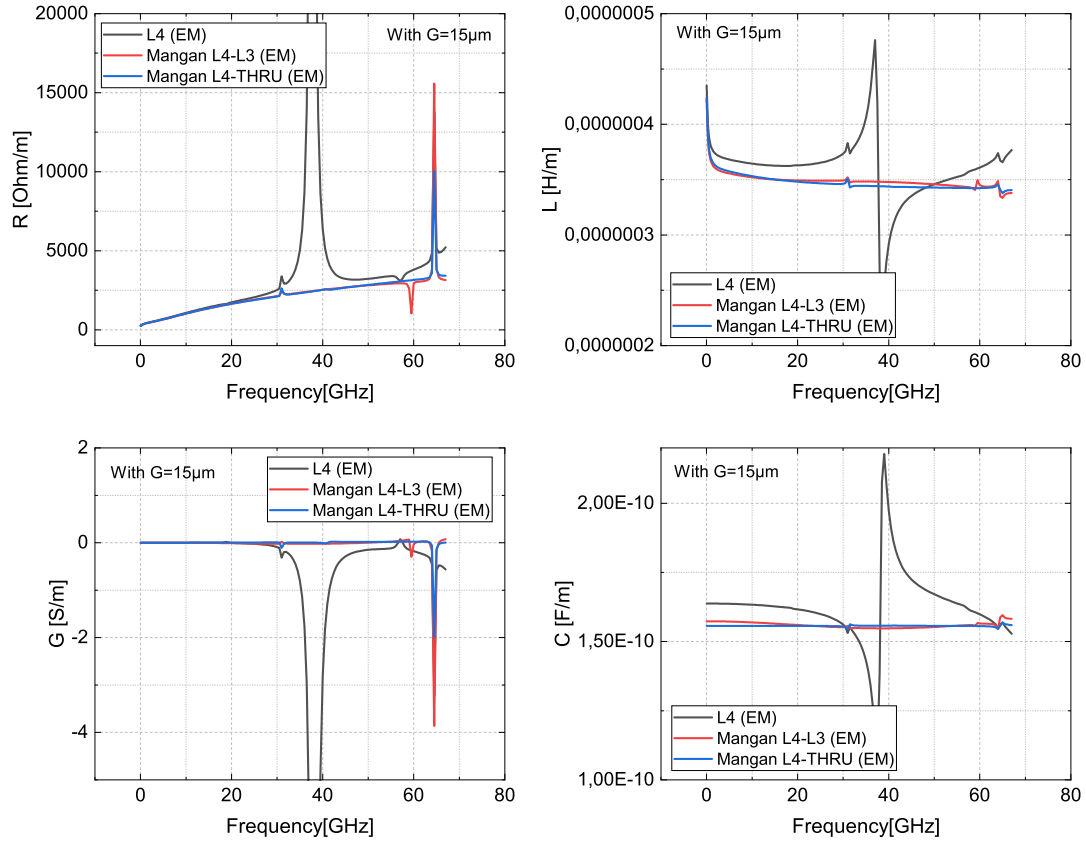


Figure B.5: Effect of Mangan applied to 138-356 L4 Momentum EM simulations ($G=15\mu\text{m}$), using L3 or THRU as the shorter line in the operation.

APPENDIX B. SELECTION OF SHORT LINE FOR THE MANGAN DE-EMBEDDING

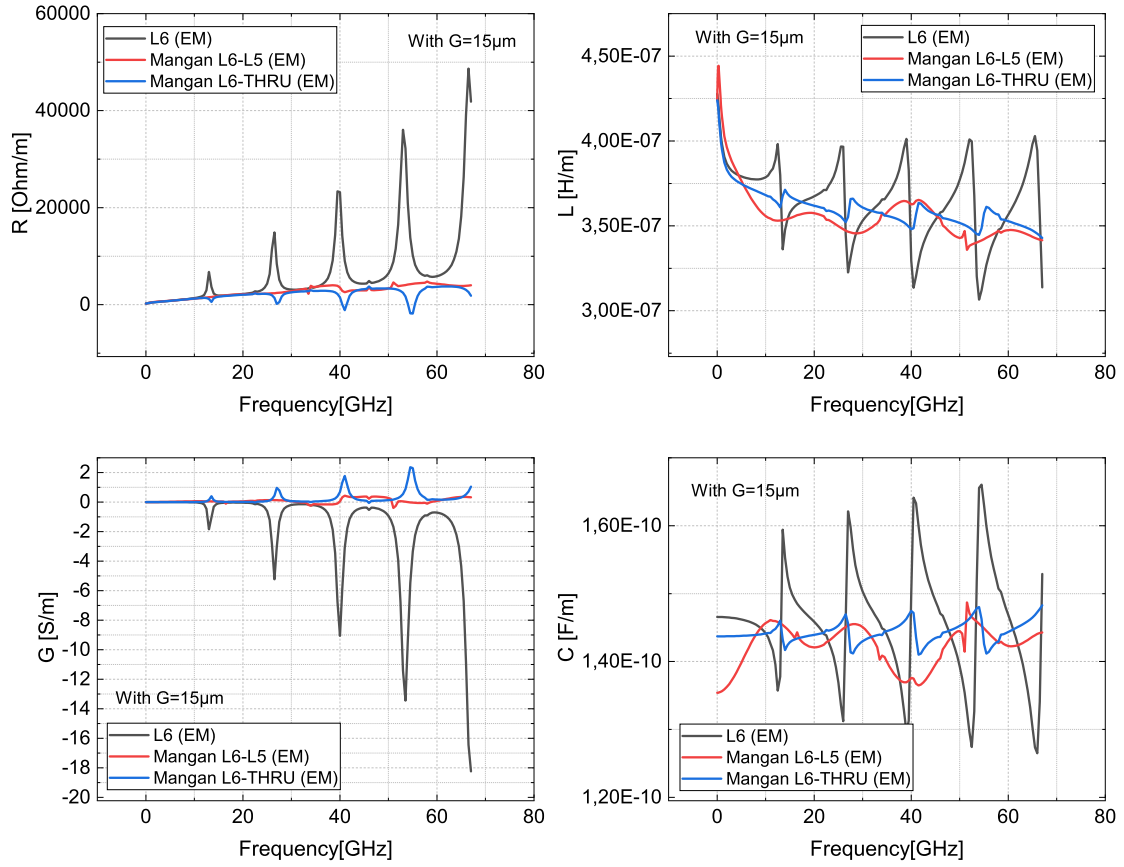


Figure B.6: Effect of Mangan applied to 138-356 L6, using L5 or THRU as the shorter line in the operation.

Appendix C

LineCalc and CILD sensibility to material parameters and line dimensions

The following figures reproduce the sensibility of the characteristic impedance, the dielectric constant and the normalized attenuation to different stack or line parameters for the 135-356 ISS.

C.1 138-356 ISS

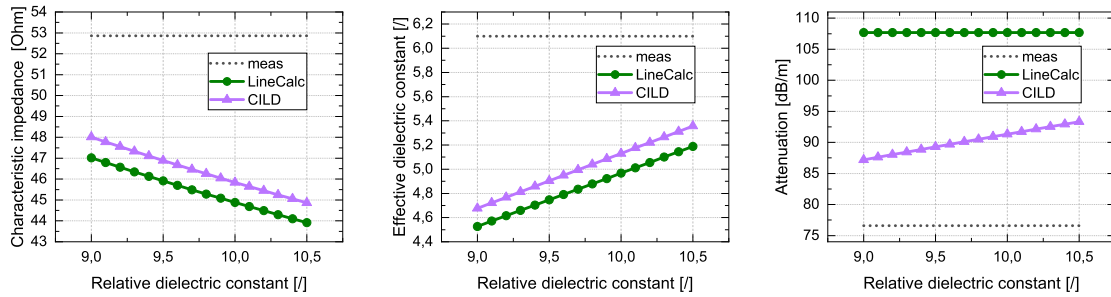


Figure C.1: Sweep of relative dielectric constant.

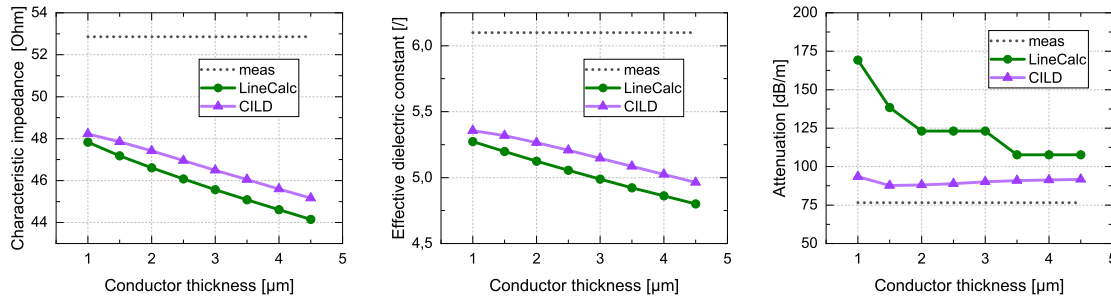


Figure C.2: 138-356 THRU Z_c , ϵ_{eff} and normalized attenuation sensibility to conductor thickness.

APPENDIX C. LINECALC AND CILD SENSIBILITY TO MATERIAL PARAMETERS AND LINE DIMENSIONS

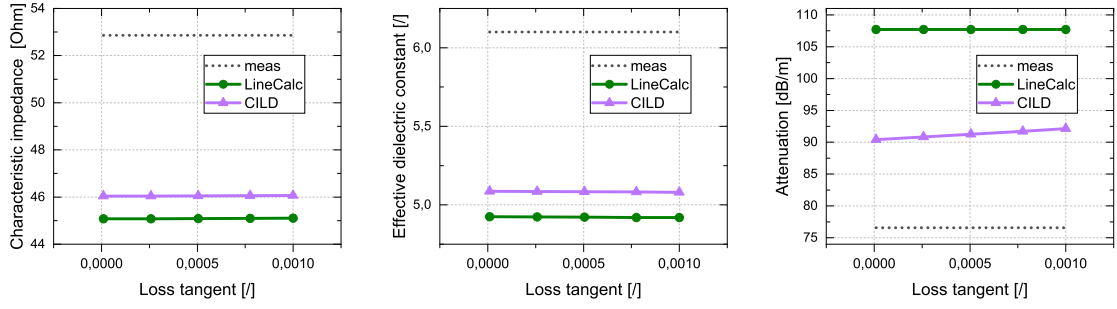


Figure C.3: 138-356 THRU Z_c , ϵ_{eff} and normalized attenuation sensibility to loss tangent.

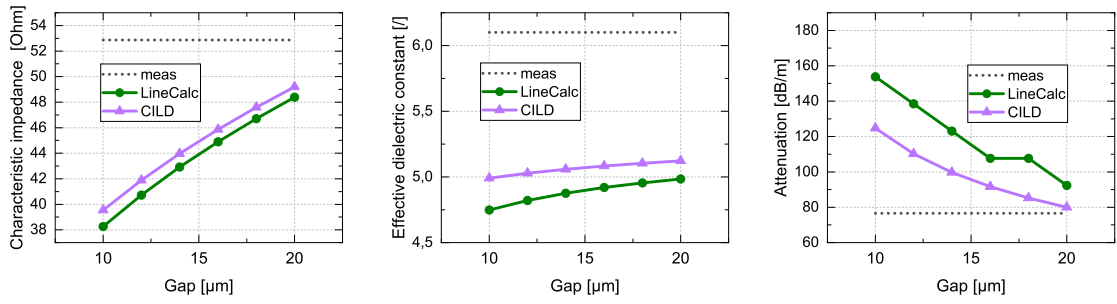


Figure C.4: 138-356 THRU Z_c , ϵ_{eff} and normalized attenuation sensibility to line gap.

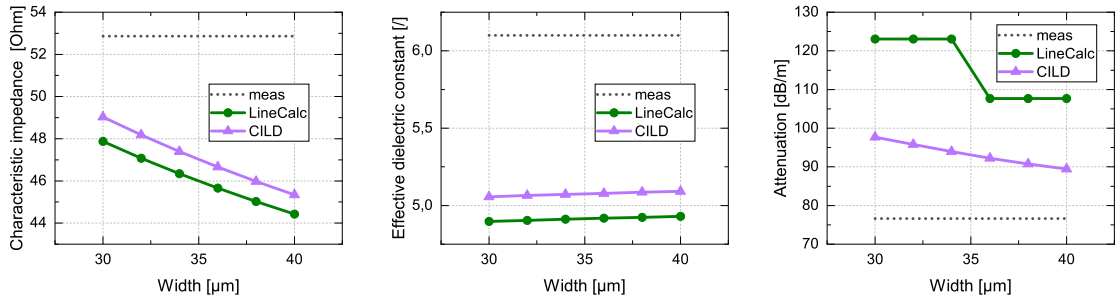


Figure C.5: 138-356 THRU Z_c , ϵ_{eff} and normalized attenuation sensibility to line width.