

École polytechnique de Louvain

Design of a Capacitance-to-Digital Converter Integrated Circuit

A Time-Domain Approach

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Acronyms

ADC Analog-to-Digital Converter. 15, 20, 24, 26, 27, 92

BBPLL Bang-Bang Phase-Locked-Loop. 22, 27, 97, 102, 104

CCO Capacitance-Controlled-Oscillator. 7, 22, 24, 25, 27, 29, 63, 64, 66, 67, 73, 74, 78, 80, 83, 84, 89, 90, 92, 95–104

CDC Capacitance-to-Digital Converter. 5, 12, 13, 15, 18–20, 22–24, 26, 27, 63, 72, 100, 101, 103, 104

CMOS Complementary Metal Oxide Semiconductor. 39, 103

CPU Central Processing Unit. 11, 12

CTC Capacitance-to-Time Converter. 5, 15, 18, 22, 27, 101, 103

CVC Capacitance-to-Voltage Converter. 5, 15, 18, 19, 26

DAC Digital-to-Analog Converter. 20

DJ Deterministic Jitter. 30, 31

DNL Differential Non-Linearity. 92, 99

ENOB Effective Number Of Bits. 18, 19, 25, 26, 63, 83, 99, 101, 102, 104

FoM Figure-of-Merit. 16, 18, 19, 26, 63, 72, 83, 99, 102, 104

GBW Unity-Gain Bandwidth. 76, 77, 79, 81, 102

GP General-Purpose. 39

HVT High Voltage Threshold. 39

- IC** Integrated Circuit. 39, 48, 100, 104
- INL** Integral Non-Linearity. 99
- IoT** Internet-of-Things. 11, 103
- KCL** Kirchhoff's Current Law. 78
- LP** Low-Power. 39
- LVT** Low Voltage Threshold. 39
- MCU** Micro-Controller Unit. 12, 27, 99–101, 104
- PCB** Printed-Circuit-Board. 100, 102
- PDF** Probability Density Function. 30, 31
- PSD** Power Spectral Density. 34, 36, 69, 70
- PVT** Process-Voltage-Temperature. 21, 85, 102, 104
- RJ** Random Jitter. 30
- RO** Ring-Oscillator. 21, 39, 41–44, 49, 50, 54, 56–58, 61–63, 103
- SAR** Successive Approximation Register. 20
- SNQR** Signal-to-Quantization-Noise Ratio. 25, 26
- SNR** Signal-to-Noise Ratio. 25, 26, 99
- SoA** State-of-the-Art. 13, 15, 26, 63, 101, 103, 104
- SoC** System-on-Chip. 11, 12, 26, 103
- Sub- V_t** Subthreshold. 42
- SVT** Standard Voltage Threshold. 39
- TDC** Time-to-Digital Converter. 5, 24, 25, 63, 73, 77, 99, 103
- ULP** Ultra-Low-Power. 11
- VCO** Voltage-Controlled Oscillator. 13, 29, 30, 37, 39, 103

Introduction

1

1.1 Context

The emergence of the Internet-of-Things (IoT) field has brought many challenges to the electronic industry. An IoT network is composed of multiple nodes that acquire, process and exchange data at the image of a communication network. An IoT node is a device that can be in charge of sensing a physical information and transmit it to the network. The challenges come from several constraints that surround IoT devices. As a matter of fact, these devices must be small, energy autonomous, they must embed processing capabilities for reducing data size and ensure security, and they must include communication systems for transmitting these data [1] [33].

The requirements for processing and size limitation tend to push electronic designers to integrate more and more peripherals on-chip. The need for energy autonomy boosts the field of Ultra-Low-Power (ULP) devices and energy harvesting. Fig. 1.1 shows an illustration of a typical System-on-Chip (SoC) in the context of IoT, which embeds a Central Processing Unit (CPU), interfaces for communicating with other devices and interfaces for analog sensors and actuators. IoT nodes that are in charge of acquiring data involve a sensor. Some IoT SoCs directly embed one or more sensors on-chip while some can only embed **interfaces** for communicating with various sensors [1]. In both cases, there is always an interface between sensors that work in the analog domain, and the processing units that work in the digital domain.

This work is focused on the interface part of the typical SoC in an IoT context. Specifically, we will work on interfaces for *capacitive* sensors as many sensors used for pressure sensing, acceleration sensing and humidity sensing are of this type [8] [7] [2].

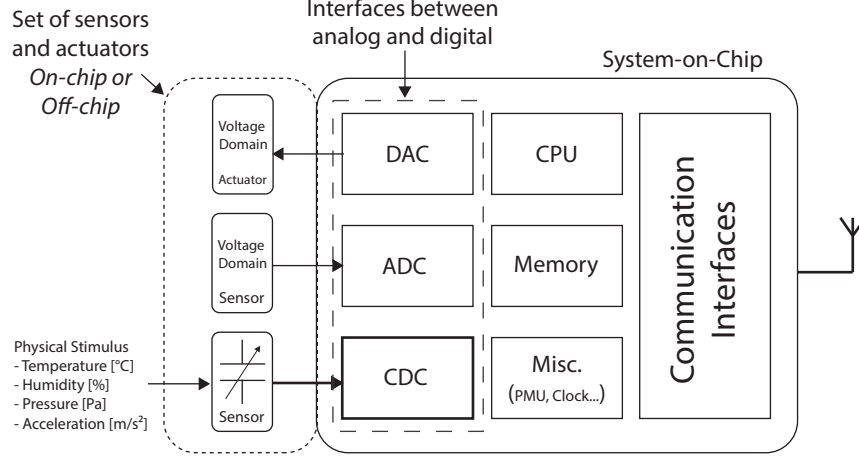


Figure 1.1: System-on-Chip - Illustration inspired from [4]

A capacitive sensor is a device which maps a physical stimulus variation into a capacitance variation. In a digital context, it is required to have an interface for translating this capacitance into a digital word as illustrated in Fig. 1.2. This circuit is usually called Capacitance-to-Digital Converter (CDC).

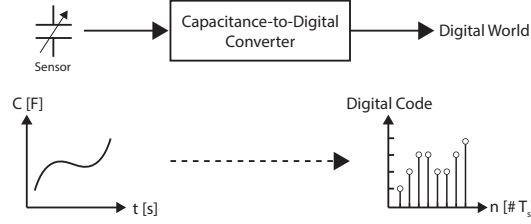


Figure 1.2: Capacitance-to-Digital Converter - Illustration

Objectives Our main goal is to design a CDC that can be integrated in a SoC and answers to the low-power challenge. Also, we are exploring the possibility to use existing blocks available in the SoC to simplify the design and gain in area and power. In addition, we consider the presence of a CPU or a Micro-Controller Unit (MCU) in the SoC to improve the performances of the converter by post-processing data. Finally, the designed interface needs to be as universal and compatible as possible with various kinds of capacitive sensors.

As this is a first design, we decided to constraint it to *low specifications*. This work will be a first step with primary focus on the jitter aspect of CDC as it will be explained later. It will allow us to elaborate a design methodology for future development of a more advanced converter.

1.2 Organization of the Work

Chapter 2 We will start this work by exploring the State-of-the-Art of Capacitance-to-Digital Converters. We will analyze the different types of CDCs, namely voltage domain CDCs and time-domain CDCs, and we will compare them based on their characteristics. We will present two designs from the literature, we will explain their principle and we will evaluate their advantages and disadvantages. Finally, we will motivate our decision to focus this work on time-domain converters and we will describe their structure and their characteristics.

Chapter 3 Then, we will present the theory of jitter in the context of time-domain converters. We will present a methodology for measuring the jitter of an oscillator in time domain. We will describe tools for the time-domain analysis of jitter. These principles and tools will be the basis of our work as we will design a time-domain interface.

Chapter 4 In the next chapter, we will analyze measurements performed on Voltage-Controlled Oscillators, we will compare them to simulation results. We will explain the differences observed between the measurements and the simulation results and we will show how to evaluate the robustness of an oscillator against supply-voltage variations. It will allow us to evaluate our methodology for jitter analysis in practice as this will be the next step after the design of the time-domain converter.

Chapter 5 Finally, we will choose a circuit topology for the design of our time-domain converter, we will justify our choice, we will explain the theory of operation of this circuit and we will detail the design methodology followed. After, we will present techniques for improving the performances of the converter and we will show the testing methodology planned.

State-of-the-Art

2

In this chapter, we will present the multiple techniques used in the field of sensor interfaces for capacitance-to-digital conversion, we will also present some techniques for performance enhancement of sensor interfaces. Finally, we will focus on the state-of-the-art of time-domain capacitance-to-digital conversion.

2.1 General Overview

There are two main types of CDCs linked to the type of conversion technique which is used. On one hand, time-domain CDCs convert the capacitance variation into a series of time events, the digital conversion is performed in time-domain using a time-to-digital converter (e.g. a frequency counter). On the other hand, voltage-domain CDCs transform the capacitance variation into a voltage amplitude which is translated to digital using an Analog-to-Digital Converter (ADC). These types are illustrated in Fig. 2.1. Table 2.1 summarizes the State-of-the-Art (SoA) of CDCs compared based on their input capacitance range, their resolution, their conversion time, their power, their area and their type of converter.

Note 1 - Table 2.1 Values noted with (*) were calculated from the article data using (2.1) and values noted with (**) were computed using (2.2).

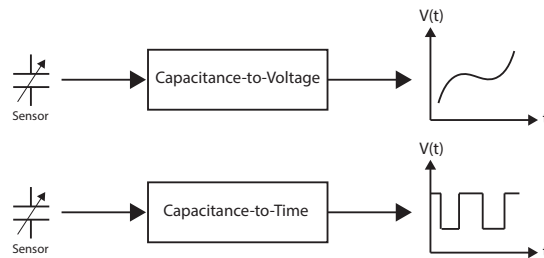


Figure 2.1: CTC and CVC illustration

$$ENOB = \frac{SNR[dB] - 1.76}{6.02} \quad (2.1)$$

$$FoM = \frac{\text{Power} \cdot \text{Conversion time}}{2^{ENOB}} \quad (2.2)$$

Note - FoM The computed Figure-of-Merit (FoM) corresponds to the energy required for one conversion step (i.e. one LSB conversion). It allows comparing converters that have different power consumption and conversion time.

Reference	[23]	[18]	[13]	[22]	[10]	[35]	[36]	[42]	[41]	[24]	[37]	[39]	[25]
Cap range (pF)	0.7 - 10000	8	3.36	2000000	0.15-15	0.9	1	2.97-7.67	1.5-20	12.6	0-5	0-388	20
Resolution (bits)	12 (*)	13.1	8.9 (*)	15	8.6 (*)	13	15.7 (*)	8.6 (*)	7.46	16	10.4 (*)	13	14.4
Resolution (fF)	12.3	0.91 (*)	2.05	1.5	11.4	0.09	0.0054	4.07	105 (*)	0.2 (*)	1.1	47.36 (*)	0.92 (*)
Conversion time (μ s)	19.06	6860	17500	10000	1	3200	20000	40	1000	1125	1	800	120000
Power (μ W)	1.84	14	18.4	12500	20	52.8	220	0.242	0.8	0.254	75	305	376
FoM (pj/c-step) (**)	0.009	10.93	680.5	3814.7	0.052	20.62	82.41	0.024	4.54	0.00436	0.0566	29.78	2087.07
Area (mm ²)	0.0017	0.05	0.1	-	0.0016	0.1482	0.317	0.08	-	0.63	0.033	0.57	0.66
Process (nm)	40	160	180	700	130	130	130	65	350	180	40	180	180
Type	T	T	T	T	T	V	V	V	V	V	V	V	V

Table 2.1: General Overview of the State-of-the-Art - See note 1 for (**) and (*)

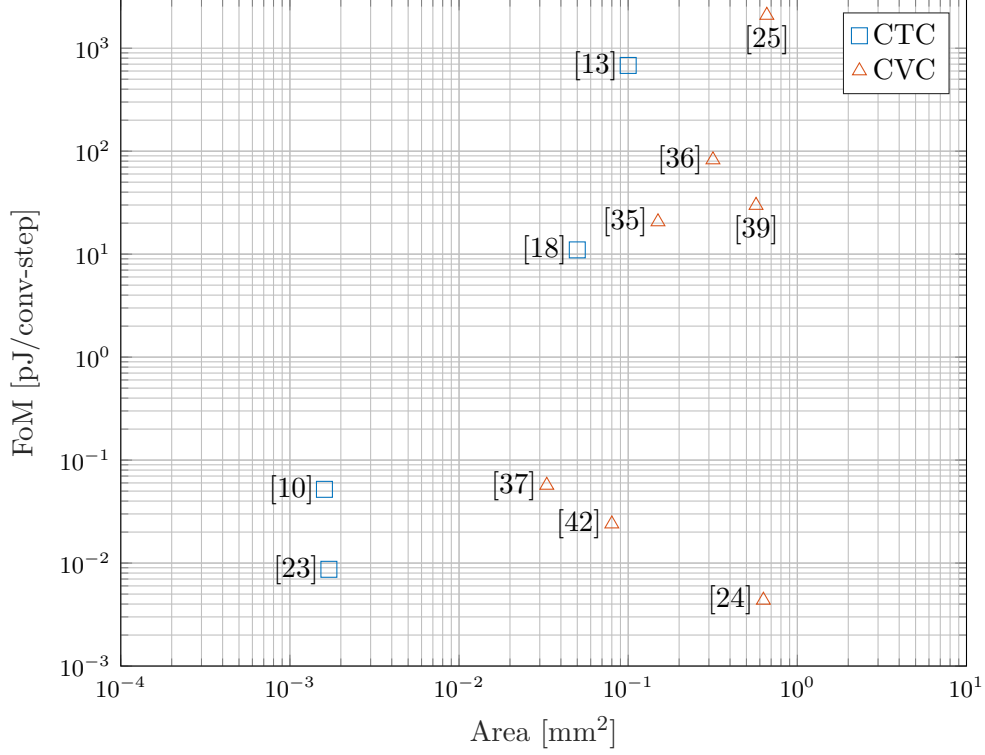


Figure 2.2: Comparison of CDC types - Area vs. FoM

A first comparison of these two categories can be made on the basis of the constraints defined for this work, namely low-power design and low area for simple integration. The evaluation of the low-power aspect is made using the FoM defined previously instead of using power, to avoid biased comparison. The plot in Fig. 2.2 shows several state-of-the-art results classified in two categories (CTC and CVC) and comparing these results in terms of FoM and area. While some voltage-domain converters allow ultra-low-energy designs ([24], [42] and [37]), time-domain converters fit in 10-100 times smaller area than their voltage-domain counterparts ([10], [23]). The design from [23] was made in 40 nm technology and shows the best results in this comparison for time-domain CDCs. Looking at CVCs only, the design presented in [37] shows the best compromise in 40 nm technology. The one from [42] exhibits the best compromise, using a 65 nm technology. For both types of converters, the best results are obtained with the most advanced technologies.

A second comparison can be made considering the Effective Number Of Bits (ENOB) and the FoM. The objective of this work was set to consider a low-specification design as a first attempt but it is still interesting to observe the capabilities of the two types of converters in the state-of-the art. In Fig. 2.3, voltage-domain converters seem to offer better resolution performances compared to their time-domain counterparts, especially

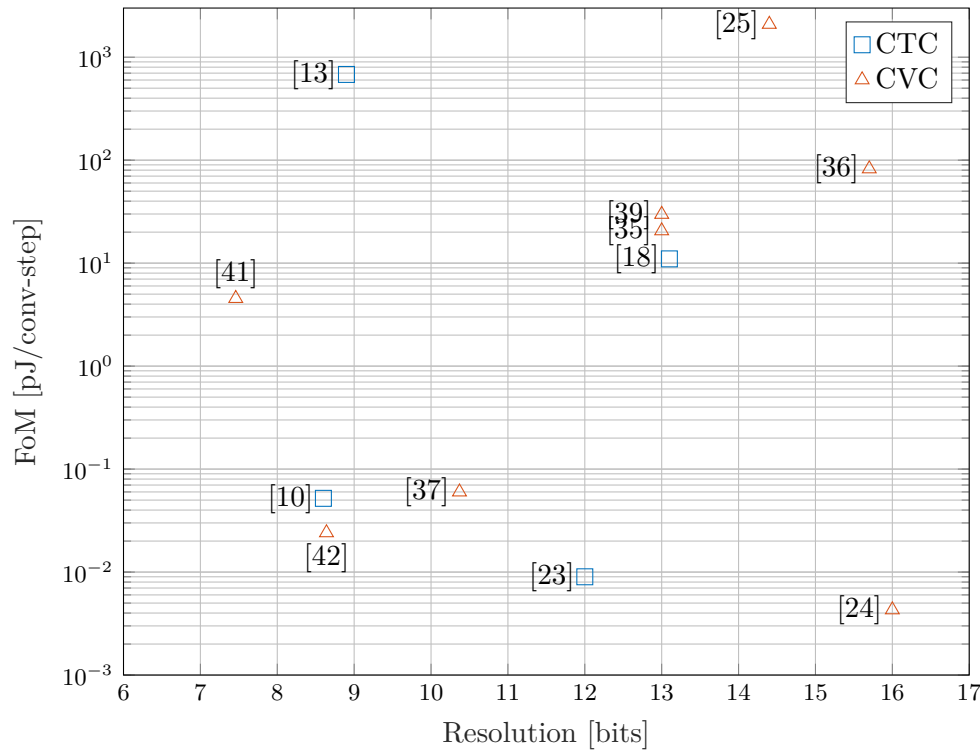


Figure 2.3: Comparison of CDC types - Resolution vs. FoM

the design from [24] which shows an ENOB of 16 bits with the lowest FoM while the low-area design from [42] has an ENOB of 8.6 bits. The time-domain converter from [18] shows an ENOB of 13.1 bits with a poor FoM while the converter from [23] presents an ENOB of 12 bits with the best FoM of its family.

2.1.1 Capacitance Conversion

2.1.1.1 Analysis of a Voltage-Domain Converter

Among the many voltage-domain CDCs presented in Table 2.1, the designs from [37] and [42] present the best compromise in terms of FoM and area. However, the one from [37] uses a $\Sigma\Delta$ technique to reach a better resolution, which makes the design more complex. The design from [42] is simpler, even if it has a lower ENOB, it is interesting to review briefly the circuit of this CVC.

Voltage Conversion and General Behaviour This design is shown in Fig. 2.4. It uses a switched capacitive bridge for capacitance-to-voltage conversion. The conversion works in two phases: phase 1 is the sampling of the sense capacitor C_s after a first reset (all capacitors are short-circuited), phase 2 is the sampling of the reference capacitor C_r after a second reset. The voltage at the sampling node for phase 1 is expressed in

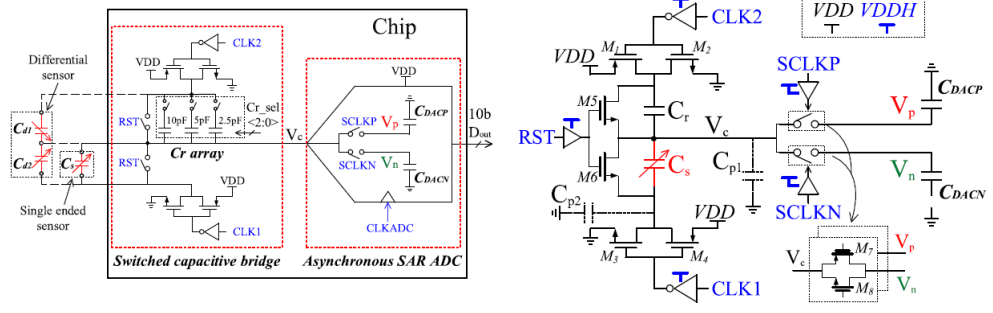


Figure 2.4: Architecture of the CVC and Switched Capacitive Bridge from [42]

Eq. 2.3, the expression for phase 2 is given in Eq. 2.4. This design uses a Successive Approximation Register (SAR) ADC for voltage-to-digital conversion in the two phases [42].

$$V_p = \frac{C_s}{C_s + C_r + C_{DACP} + C_{p1}} \quad (2.3)$$

$$V_n = \frac{C_r}{C_s + C_r + C_{DACN} + C_{p1}} \quad (2.4)$$

This structure presents the advantage of using only a few capacitors for relative measurements, in the context of the integration into an existing SoC, thus limiting the associated area overhead. Also, it consumes energy only during the sampling phases. Nonetheless, this structure requires the use of a reference capacitor value C_r close to the nominal value of the measured capacitor C_s for high-sensitivity of the bridge. Consequently, a bank of capacitors is required for measurement of a wide capacitance range, also, the Digital-to-Analog Converter (DAC) capacitance C_{DAC} should be small compared to other capacitors for keeping the bridge sensitivity high enough. Thus, the use of this structure may require a specific ADC design to meet this requirement [42]. It should be noted that this circuit allows differential measurement and non-grounded capacitor measurement.

2.1.1.2 Analysis of a Time-Domain Converter

The design proposed in [23] shows the best compromise in terms of energy and area results in the state-of-the-art of time-domain CDC. Its basic structure is shown in Fig. 2.5.

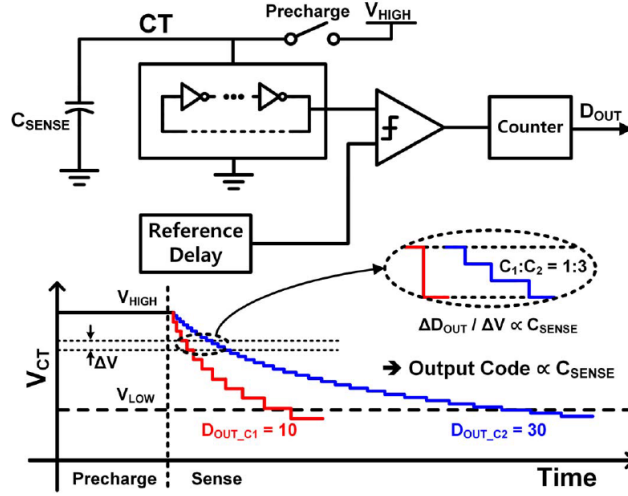


Figure 2.5: Architecture of the CTC from [23]

Time Conversion and General Behaviour The main idea of this design is the connection of the sensing capacitor to the supply node of a Ring-Oscillator (RO). At the beginning of the measurement, the sensing capacitor C_{SENSE} is pre-charged to a voltage V_{HIGH} , after this phase, the RO is directly supplied by the sensing capacitor only. As the RO oscillates, it gradually discharges the capacitor to a voltage V_{LOW} , the time-domain signal of the oscillator is compared to a constant reference delay generated by a chain of inverters so that a counter produces a digital output proportional to the number of transitions during the reference delay period. The RO delay is proportional to the capacitor voltage, thus, the digital output is proportional to the capacitance [23].

This structure has the advantage of being universal in the sense that, as long as the counter is large enough (in terms of counting capability), the measurement range is only limited by the measurement time allowing a wide measurement range without design changes. This advantage is usually common to time-domain interfaces. This system uses only digital blocks allowing more scaling capabilities. Finally, the energy used to charge the capacitor is used for powering the RO which limits the power consumption [23].

2.1.2 Performances Enhancement

All the designs presented previously or cited in Table 2.1 use circuit-level or system-level techniques for reducing the effect of non-idealities such as Process-Voltage-Temperature (PVT) variations, noise and errors (offset, drift). Also, some interesting system-level techniques were found outside the frame of these designs. We will briefly present some of these techniques as they may be useful for this work.

2.1.2.1 Three signal approach [6]

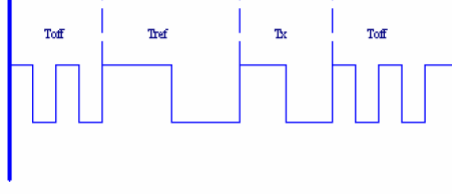


Figure 2.6: Example of a period-modulated output signal from [6]

The three signal measurement method consists in performing three times the same measurement with a given interface for a short period but with different sensing conditions at the input of the converter. For example, in the case of a time domain interface, the first measurement could be done with no capacitor ($Toff$), the second measurement with a reference capacitor ($Tref$) and the last one with the sensing capacitor of interest (Tx) as illustrated in Fig. 2.6. A micro-controller can then be used for post-processing calculation of Eq. 2.5 [6].

$$C_x = \frac{T_x - T_{off}}{T_{ref} - T_{off}} C_{ref} \quad (2.5)$$

This method allows reducing additive and multiplicative errors such as offset due to parasitic capacitors (in the case of capacitive sensors), drift (temperature variations or long-time variations), low-frequency noise and interferences. Also, this method only requires the addition of a reference capacitor which is not a problem for off-chip capacitive sensor measurement. Finally, it exploits the micro-controller capability for improving the measurements of the interface. Consequently, this method represents a good candidate in this work, nonetheless, it should be noted that the use of multiple measurements increases the measurement time.

2.1.2.2 BBPLL-based time-domain interface [14]

The Bang-Bang Phase-Locked-Loop (BBPLL) is a general structure from [14] shown in Fig. 2.7 for a time-domain CDC. It uses 2 units of the same CTC, or Capacitance-Controlled-Oscillator (CCO), connected to a capacitor multiplexer to which the sensing capacitor and a variable capacitor are connected on a given input while a reference (fixed) capacitor is connected to the remaining input.

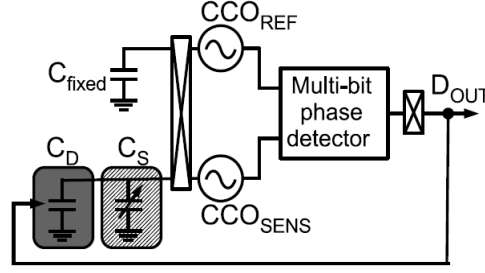


Figure 2.7: BBPLL architecture for CDC from [14]

The variable capacitor allows the use of feedback which is one of the main functionalities of this structure. The operation is based on phase-locking of the loop with the reference path. If the nominal sensing capacitance C_S is equal to the reference capacitance C_R and the oscillators are assumed to be linear and matched, the average sensor variation is related to the digital output of the interface as expressed in Eq. 2.6. The locking of the loop allows rejection of common-mode perturbations as the output is only function of relative deviations, it should be noted that this operation requires a calibration phase [14].

$$(\Delta C_S)_{avg} = -LSB \cdot (D_{out})_{avg} \quad (2.6)$$

The two oscillator units produce time-domain signals that are converted to a digital output using a multi-bit phase detector. A time-domain chopping technique is used for removing $1/f$ noise (low-frequency) by inverting the connection of the oscillators units using the capacitor multiplexer. This method also allows limiting common-mode perturbations, offset, low-frequency perturbations, noise and interference [14]. This is also a good candidate in this work. However, it requires the use of two units, thus doubling the area compared to the previous method. It also requires a variable capacitor while not requiring multiple measurements as in the previous method. This technique is less universal as it requires the reference capacitor to be equal to the nominal capacitance of the sensor but this may not be problematic if off-chip capacitors are used.

2.2 Time-Domain Conversion

As explained in Section 2.1.1.2, time-domain interfaces usually have a theoretical unlimited input capacitance range as they convert the capacitance variation into a time-event. In the context of a universal CDC, this represents an important advantage. Also, it was shown in Table 2.1 that time-domain converters usually present better results in terms of power and area than their voltage-domain counterparts for an equivalent technology. On this basis, it was decided to focus this work on the study and design of time-domain converters.

2.2.1 Parameters of Time-Domain Converters

The conversion in time-domain is always performed with a Capacitance-Controlled-Oscillator (CCO), which is an oscillator whose period is a function of the capacitance value (Eq. 2.7) as shown in the design from [23]. The digital conversion is then performed using a *counter* which counts the number of periods with respect to a reference clock as illustrated in Fig. 2.8.

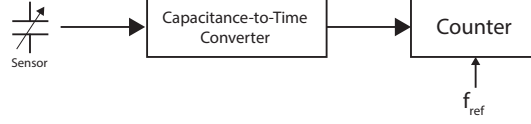


Figure 2.8: Time-Domain CDC general structure

Full Range From this general statement, a parallelism can be made with the usual parameters used in the field of standard ADCs. The full range of a sensor is defined as the difference between the maximum analog output and the minimum analog output [11]. In the case of time-domain conversion, this full range can be expressed as the period range corresponding to the capacitance range, it is shown in Eq. 2.8.

Resolution The resolution of a sensor is the smallest increment of a stimulus that can be sensed [11], in the case of a converter, it is the smallest increment of an input signal that can be converted. If we define a resolution in the time domain for a given converter, it represents the minimum period that can be detected. The resolution expressed in the time domain represents the period increment corresponding to an LSB increment of the period counter given in Eq. 2.9.

$$T_{CCO} = f_{CCO}(C_S) \quad (2.7)$$

$$T_{FR,CCO} = f_{CCO}(C_{S,max}) - f_{CCO}(C_{S,min}) \quad (2.8)$$

$$T_{R,CCO} = f_{CCO}(\Delta[C_S]_{min}) \quad (2.9)$$

2.2.2 Parameters of Time-to-Digital Converters

The quantization of the time-domain signal is performed by a Time-to-Digital Converter (TDC). This operation can be performed using various types of circuits where all-digital systems are usually preferred as they allow to benefit from technology scaling [19].

The basic counter-based TDC uses a reference clock period T_{CP} higher than the measured period and counts the number of reference clock cycles in a cycle of the measured clock as illustrated in Fig. 2.9. The quantization error performed on the input period can be expressed as in Eq. 2.12 [19].

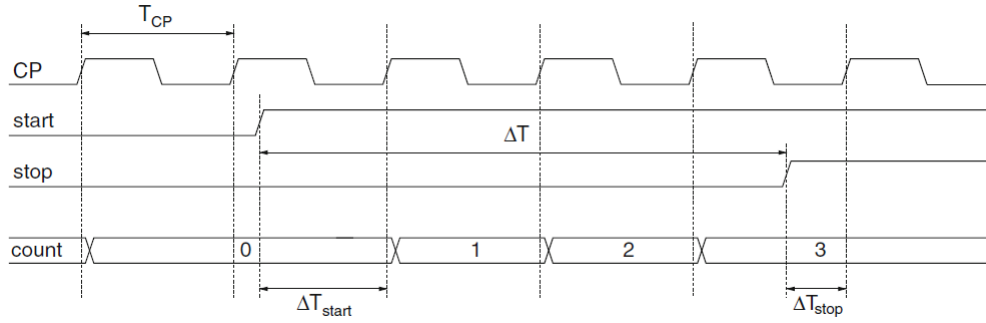


Figure 2.9: Timing diagram of a counter-based TDC from [19]

$$\Delta T_{start} \in [0; T_{CP}] \quad (2.10)$$

$$\Delta T_{stop} \in [0; T_{CP}] \quad (2.11)$$

$$\epsilon_T = \Delta T_{start} - \Delta T_{stop} \in [-T_{CP}; T_{CP}] \quad (2.12)$$

Reference clock frequency Referring to the previous section, the minimum clock period of the CCO is the resolution expressed in time-domain T_{LSB} . Thus, to avoid missing a bit in the quantization process, the interval error should be smaller than half of T_{LSB} [19].

$$\epsilon_T = 2 \cdot T_{CP} \quad (2.13)$$

$$T_{CP} \leq \frac{T_{LSB}}{2} \quad (2.14)$$

2.2.3 Effective Resolution of Time-Domain Converters

For any type of converter, we define the Effective Number Of Bits (ENOB) as the resolution of a hypothetical noise free converter that has the same SNR as the studied converter [19]. It is a function of the Signal-to-Noise Ratio (SNR) and is expressed in Eq. 2.18.

Any quantizer will generate an error due to the discretization effect. This error is usually considered as a uniformly distributed random noise in $[-\frac{q_s}{2}; \frac{q_s}{2}]$ (q_s is the quantization step) and leads to the definition of the Signal-to-Quantization-Noise Ratio (SNQR) which is the ratio of the quantization noise power to the signal power as shown in Eq. 2.16.

The maximum output signal SNQR of an ideal N-bits quantizer is given in Eq. 2.17. Consequently, any non-ideal quantizer adding noise to the signal such that the output

SNR is greater than the ideal SNQR loses one or more bits of resolution. The ENOB expressed in Eq. 2.18 is a measurement of the effective resolution considering the actual SNR of a quantizer. The signal power is considered for a sine wave of full-scale peak-to-peak amplitude [32].

$$A_{rms} = \frac{2^n \cdot q_s}{2\sqrt{2}} \quad e_{rms} = \frac{q_s}{\sqrt{12}} \quad (2.15)$$

$$SNQR = \frac{A_{rms}}{e_{rms}} = 2^n \cdot \sqrt{1.5} \quad (2.16)$$

$$SNQR[dB] = 1.76dB + N \cdot 6.02dB \quad (2.17)$$

$$ENOB = \frac{SNR[dB] - 1.76dB}{6.02dB} \quad (2.18)$$

In order to achieve N bits of effective resolution, the SNR should be as high as the SNQR of Eq. 2.17. Thus, the output signal of the time-domain converter should respect the same constraint in time domain, which is expressed as the RMS period jitter of the CCO at the full-scale capacitance considering a random Gaussian distributed jitter [10].

Given a full-scale capacitance C_{FS} , we can derive the resolution capacitance using Eq. 2.19. From this, we can derive the output RMS period shown in Eq. 2.21. It is the upper bound of the period jitter σ_{pj} given in Eq. 2.22.

$$C_R = \frac{C_{FR}}{2^N} \quad (2.19)$$

$$C_{R,rms} = \frac{C_R}{\sqrt{12}} \quad (2.20)$$

$$T_{R,rms} = f_{CCO}(C_{R,rms}) \quad (2.21)$$

$$\sigma_{pj} \leq T_{R,rms} \quad (2.22)$$

2.3 Summary

In this chapter, we explored the SoA of Capacitance-to-Digital Converters, we distinguished time-domain and voltage-domain converters. We compared all the designs based on their performances and characteristics. We emphasized the fact that advanced technologies resulted in better FoM and area.

Then, we reviewed briefly the circuits of the best designs for each category of converter. We showed that the CVC from [42] was interesting for its low area and its low power consumption. We also noted that it required a specific ADC design for proper sensitivity, which is less interesting for the integration into an existing SoC.

We analyzed the CTC from [23], we showed that the time-domain operation allows the use with a wide range of capacitance. We pointed out the fact that the major use of digital blocks in the circuit allowed the use of scaling which is an advantage when area reduction is required. We explained that the advantage of time-domain concerning the capacitance range led us to choose this type of converter for the design of our CDC.

After, we presented two techniques for reducing errors and low-frequency noise in time-domain converters. We showed the three signal approach which allows reducing additive and multiplicative errors by exploiting post-processing capabilities of a MCU while requiring an increase of the conversion time. We showed the BBPLL structure which is capable of reducing low-frequency noise and perturbation as well as common-mode interference by using a feedback loop with two CCOs.

Finally, we reviewed the parameters of time-domain converters by making a parallelism with standard ADC parameters. We explained briefly the requirements of the counter and we showed the link with the effective resolution. In the end, we presented the jitter constraint which is necessary for reaching the effective resolution in a time-domain converter.

As the design of a time-domain CDC is constrained by the jitter, we will review the theory of jitter in the next chapter.

Jitter Concerns and Tools for Analysis

3

In this chapter, we will introduce important definitions related to jitter, we will mainly focus on jitter in the context of square wave oscillators as the goal of this work will be to design such an oscillator as CCO of our converter. We will also show a technique for measuring the jitter of a Voltage-Controlled Oscillator (VCO). We will present a tool called Allan Variance that can be useful in the analysis of oscillators. All these concerns are the basis of the methodology followed for VCO analysis and time-domain interface design that will be detailed later on.

3.1 Jitter Definitions

General definition In the context of clock signals, jitter can be defined as the deviation of the time instant at which a clock edge occurs compared to its ideal time instant [9]. This definition encompasses a variety of specific notions related to the various faces of jitter, let us review these before going further.

Absolute jitter Let us consider two oscillators, an ideal oscillator with a period T and a non-ideal oscillator with an average period T . The absolute jitter is defined as the deviation of the k -th edge of the non-ideal clock compared to the k -th edge of the reference ideal clock. Mathematically, it can be described as in Eq. 3.1 [9]. It is illustrated as a_k in Fig. 3.1.

$$a_k = t_k - KT \quad (3.1)$$

Period jitter The period jitter, also called cycle jitter, of an oscillator is defined as the variation of the clock period with respect to its nominal value. The period jitter of the cycle k can be viewed as the difference between the period T_k and the nominal one T as in Eq. 3.2 [9]. It is illustrated in Fig. 3.1.

$$p_k = T_k - T \quad (3.2)$$

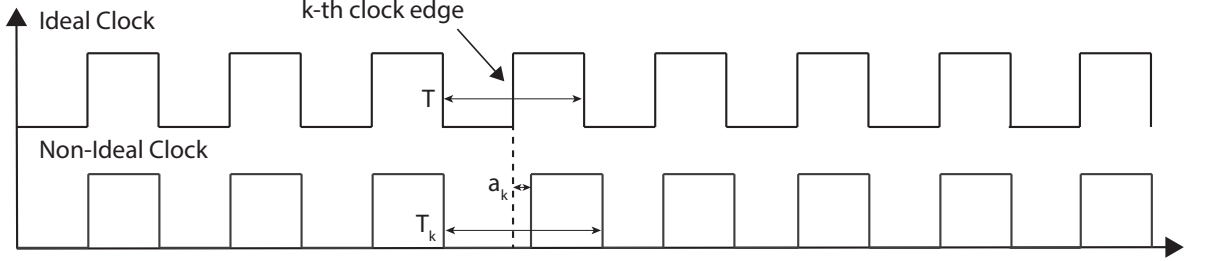


Figure 3.1: Absolute jitter and period jitter - Illustration inspired from [9]

N-Period Jitter The period jitter can also be considered on a given number N of cycles which leads to the definition of the N -period jitter. In this case, it is defined as the difference between N cycles of the oscillator and N nominal periods T as expressed in Eq. 3.3 for cycle k [9].

$$p_k(N) = \sum_{i=k}^{i=k+N-1} T_i - NT \quad (3.3)$$

Cycle-to-cycle Jitter By considering a free-running oscillator of unknown period, we can define the cycle-to-cycle jitter as the difference between two consecutive clock periods. The k -th realization of the cycle-to-cycle jitter is the difference between period T_{k+1} and period T_k [9]. It is expressed in Eq. 3.4.

$$cc_k = T_{k+1} - T_k \quad (3.4)$$

Accumulated Jitter - Long-Term Jitter In autonomous systems as VCOs, jitter accumulates over time, thus, we define the long-term jitter as the jitter accumulated on a large number of periods, it can be seen as the N -period jitter for large N [9].

3.1.1 Jitter Contributors

Jitter classification In a non-ideal system, multiple sources of jitter can be present. These jitter components are classified in two categories called Deterministic Jitter (DJ) and Random Jitter (RJ). The DJ is defined as all components having a bounded Probability Density Function (PDF). The RJ is defined as all components having an unbounded PDF, it is due to random noise sources and, following the central limit theorem, usually

presents a Gaussian distribution[43]. Multiple jitter components can combine into the total jitter. If these components are independent, the resulting jitter can be computed using the sum of all the jitter components as in Eq. 3.5.

While the jitter contribution from each component are simply summed, the PDF of the resulting jitter is the convolution of the PDF of each component expressed in Eq. 3.6. Still considering the independence hypothesis, we can deduce that the variance of the resulting random jitter is the sum of the variance of all individual random jitter components given in Eq. 3.7. Also, the resulting DJ is the sum of all the DJ components [9].

$$j_k = \sum_{i=1}^n j_{i,k} \quad (3.5)$$

$$f_j(t) = f_{j1}(t) * \dots * f_{jn}(t) \quad (3.6)$$

$$\sigma_j^2 = \sum_{i=1}^n \sigma_{i,j}^2 \quad (3.7)$$

Standard deviation - RMS When evaluating jitter on a given system, the root mean square is usually used as it represents how wide the jitter spreads around the average. The RMS value of the jitter is also the standard deviation of its distribution. For a Gaussian distribution the σ value represents the range $[\mu - \sigma; \mu + \sigma]$ around the mean inside which 68% of samples can be. For a set of discrete jitter samples, an estimator of the standard deviation is given in Eq. 3.8 where σ_j is the jitter standard deviation, j_i is the i -th jitter sample and μ_j is the mean of the jitter¹ [9].

$$\sigma_j^2 = \frac{1}{N-1} \sum_{i=1}^N (j_i - \mu_j)^2 \quad (3.8)$$

Non-Gaussian behaviour When designing a circuit based on a strict jitter constraint, it is necessary to define objective metrics that will ensure proper evaluation of the jitter constraint as well as its measurement. If the total jitter is only random and presents a Gaussian distribution, the standard deviation can be used with a probability $P(Q)$ constraint. Nonetheless, if the distribution is not Gaussian, the RMS or the standard deviation does not properly represent the spread. Consequently, it is necessary to define a metrics that will be used for non-Gaussian jitter distributions.

Dual Dirac and non-Gaussian PDFs As an example, we measured the histogram of Fig. 3.2 which results from the convolution of random and deterministic jitter components PDFs. A technique for separating these two contributions consists in considering the

¹Usually also computed from a statistical estimator of the mean.

histogram as the convolution of a Dual-Dirac jitter and a Gaussian jitter and trying to apply a tail fitting algorithm to identify the two Dirac impulses.

The two Dirac positions correspond to the means (μ_R and μ_L) of the Gaussians, their difference is called the Dual-Dirac *deterministic jitter* and represents the **deterministic contribution** to total jitter. The two sigma represents the contribution of random jitter. The total jitter (peak-to-peak) $\rho\rho$ can be expressed as in Eq. 3.9 where Q represents the probability of finding a jitter sample outside of the total jitter range. The total jitter can be used as a metrics for defining a stronger jitter constraint in the presence of various jitter contributors [9].

$$\rho\rho = \mu_R - \mu_L + Q(\sigma_R + \sigma_L) \quad (3.9)$$

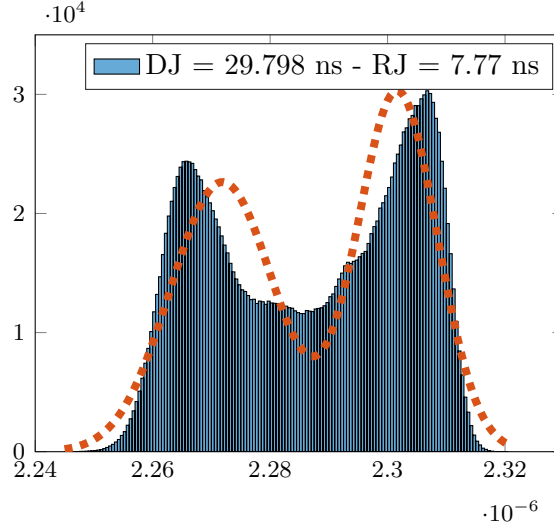


Figure 3.2: Histogram of periods - Tail fitting - VDDRO = 750 mV - Ts = 80 ns

3.2 Jitter Measurement Methodology

As time-domain interfaces are controlled-oscillators, a measurement technique was put in place and evaluated on the basis of ring oscillators measurements. This technique will be described here, the results of the measurement and the comparison with simulation results will be given later on.

Jitter histogram and estimation As explained in Section 3.1.1, multiple sources may lead to deterministic and random jitter contributions, consequently, the estimation of the jitter metrics (RMS, total jitter peak-peak) require the acquisition of a lot of samples for proper evaluation and reduced error. If one wants to evaluate the standard deviation of a Gaussian random variable with a relative error ϵ_r for a confidence interval

$1 - 2 \cdot P(Q)$, the minimum number of samples is given by Eq. 3.10. As an example, a confidence level of 99.7% and a relative error would require at least 45,000 samples.

$$n \geq 0.5 \cdot \left(\frac{Q}{\epsilon_r} \right)^2 \quad (3.10)$$

Measurement setup The VCOs that were measured had a frequency range going from the kHz up to the MHz. The square waveform of the output signal presents a high-frequency content that requires the use of a high sampling rate oscilloscope for proper measurement. The requirement for huge number of periods also leads to the need of a high capacity buffer. The measured VCOs can be supplied and controlled between 0.2 V and 1.2 V. These low values of supply voltage require the use of a precise and stable voltage source to avoid undesired frequency variations due to supply voltage variations.

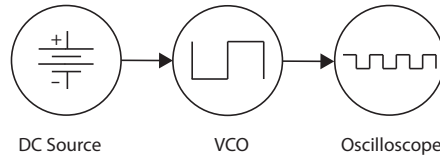


Figure 3.3: Measurement setup - VCO measured at UCLouvain

As it is required to properly setup the oscilloscope to acquire enough periods at the highest sampling rate, there is a trade-off to find between buffer capacity and sampling rate. It was decided to evaluate the fundamental frequency of the signal before performing the acquisition using the proper function offered by the device. Then, the sampling rate was chosen to be at least 10 times higher than the fundamental frequency, this value was adjusted so that a minimum of 50,000 periods were acquired.

Post-processing and statistics The data acquired by the oscilloscope represent the output voltage of the VCO over time, the useful information in our case are the transitions that are time events. The data were processed on computer to extract these transition events in the form of a vector of periods. The histogram of Fig. 3.2 was built on the basis of one of the vectors.

Period Jitter calculation As explained in Section 3.1, the period jitter is the deviation of the period from its nominal value. As shown in Eq. 3.12, the standard deviation of the periods on a vector of periods is actually the root mean square of the period jitter considering a random jitter of Gaussian distribution.

$$p_k = T_k - T \quad (3.11)$$

$$\sigma_T = \sqrt{\frac{1}{N} \sum_{i=0}^{N-1} (T_i - T_{avg})^2} = p_{j,RMS} \quad (3.12)$$

N-Period Jitter calculation It can be interesting to evaluate the N-period jitter when a great amount of periods is available. Let's consider we have a vector of M periods and we want to evaluate the N-period jitter ($N < M$), we can cut the main vector in sub-groups of N periods, we will end up with $\frac{M}{N}$ sub-vectors as shown in Fig. 3.4. We can then evaluate the standard deviation of the i-th period of each vector, this operation ends with a unique vector of size N, the N-period jitter is the sum of all the components.

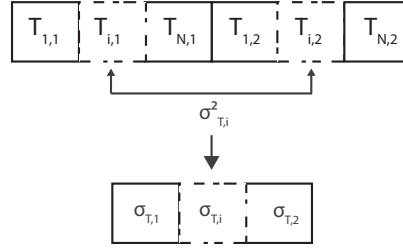


Figure 3.4: Illustration of sub-vectors

$$p_k(N) = \sum_{i=k}^{i=k+N-1} T_i - NT \quad (3.13)$$

$$\sigma_{T,i} = \sqrt{\frac{N}{M} \sum_{k=0}^{\frac{M}{N}-1} (T_{k,i} - T_{i,avg})^2} = p_{i,RMS} \quad (3.14)$$

$$p_j(N) = \sum_{i=1}^{i=N} p_{i,RMS} \quad (3.15)$$

3.3 Allan Variance: A Time-Domain Analysis Tool

In this part, we will present the Allan Variance which is a useful tool for characterizing noise in sensing systems. Usually, when we talk about noise, we tend to present its manifestation by using spectral representation (deterministic noise) or Power Spectral Density (PSD) (random noise). However, it can be interesting to stay in the time-domain, we will present the interest of this method with the measurements performed on VCOs.

Definition of Allan Variance The standard expression of Allan Variance is given in Eq. 3.16, it represents the variance on a given timescale τ . In practice, it can be seen as the variance or noise of the signal when observed at a specific time scale, it allows capturing different noise sources on their typical timescale. As noise analysis is usually performed in frequency domain, there is a direct link between Allan variance and PSD as expressed in Eq. 3.17 for a given noise PSD $S_x(f)$ [21]. The Allan Deviation $\sigma_A(\tau)$ is also usually used, it is the square-root of the Allan Variance $\sigma_A^2(\tau)$.

$$\sigma_A^2(\tau) = \frac{1}{2} \mathbb{E}[(x(t+\tau) - x(t))^2] \quad (3.16)$$

$$\sigma_A^2(\tau) = 4 \int_0^\infty S_x(f) \cdot \frac{\sin^4(\pi f \tau)}{(\pi f \tau)^2} df \quad (3.17)$$

3.3.1 Allan Variance of common noise sources

White Noise - Thermal Noise The first typical type of noise in sensing systems is white Gaussian noise. In electronic circuit, the main noise source called **thermal noise** is one of a kind [34]. The particularity of white noise is that its PSD is constant over all the frequency spectrum, consequently, it is usually characterized by its constant spectral density expressed in Eq. 3.18. In the case of thermal noise, it is expressed in V^2/Hz . In the time-domain, the Allan Variance of white Gaussian noise is a straight line of negative slope -1 given in Eq. 3.19 [38]. The Allan Deviation of white Gaussian noise is a straight line of negative slope $-\frac{1}{2}$.

$$S_x(f) = N^2 \quad (3.18)$$

$$\sigma_{A,wn}^2(\tau) = \frac{N^2}{\tau} \quad (3.19)$$

Quantization noise Quantization noise is a type of noise frequently met in data-converters, it is due to the discretization errors performed during the quantization process. It is modelled as a uniformly distributed white noise with a bounded bandwidth if the quantization step is small enough. The PSD of quantization noise is given in Eq. 3.21 for a signal sampled at period τ_s and quantization step q . The Allan Variance of quantization noise is described in Eq. 3.22. Its Allan Deviation is a straight line of negative slope -1 [38].

$$Q = \sqrt{\frac{q^2}{12}} \quad (3.20)$$

$$S_x(f) = \begin{cases} \frac{4Q^2}{\tau_s} \sin^2(\pi f \tau_s) & f \geq \frac{1}{2\tau_s} \\ (2\pi f)^2 \cdot \tau_s Q^2 & f < \frac{1}{2\tau_s} \end{cases} \quad (3.21)$$

$$\sigma_{A,q}^2(\tau) = \frac{3Q^2}{\tau^2} \quad (3.22)$$

Flicker noise - 1/f noise Flicker noise, also called 1/f noise is typically in lower frequency ranges. In electronic circuits, it is a phenomenon present as noise current in transistors. The characteristic of this type of noise is its negative slope PSD, it is often characterized by its corner frequency delimiting the low frequency range and the constant PSD in higher frequency range where it is usually dominated by thermal noise [34]. The Allan Variance of 1/f noise is a constant as shown in Eq. 3.24 [38]. For a given system, the flicker noise represents the minimum achievable variance after averaging, this fact may be exploited in post-processing sensor measurements for resolution enhancement but it is not in the scope of this chapter.

$$S_x(f) = \begin{cases} \frac{B^2}{2\pi} \frac{1}{f} & f \leq f_0 \\ 0 & f > f_0 \end{cases} \quad (3.23)$$

$$\sigma_{A,f}^2(\tau) = \frac{2B^2}{\pi} \ln 2 \quad (3.24)$$

Sinusoidal noise A sensing system in a non-ideal environment can be subject to interferences generated by other systems. This perturbation can be sinusoidal (e.g. interferences from the electrical grid [11]). The PSD of such an interference is characterized by a Dirac function located at the fundamental frequency of the perturbation as in Eq. 3.25. The resolution of Eq. 3.17 with the PSD of Eq. 3.25 results in Eq. 3.26 which expresses the Allan Variance of a sinusoidal signal.

$$S_x(f) = \delta(f - f_0) \quad (3.25)$$

$$\sigma_A^2(\tau) = 4 \frac{\sin^4(\pi f_0 \tau)}{(\pi f_0 \tau)^2} \quad (3.26)$$

These four noise sources are of particular interest in the case of this work, other types of noise could be studied but are outside of the scope. Fig. 3.5 shows the Allan Deviation of the four noise sources, it will be the basis of the analysis performed on the VCOs measurements.

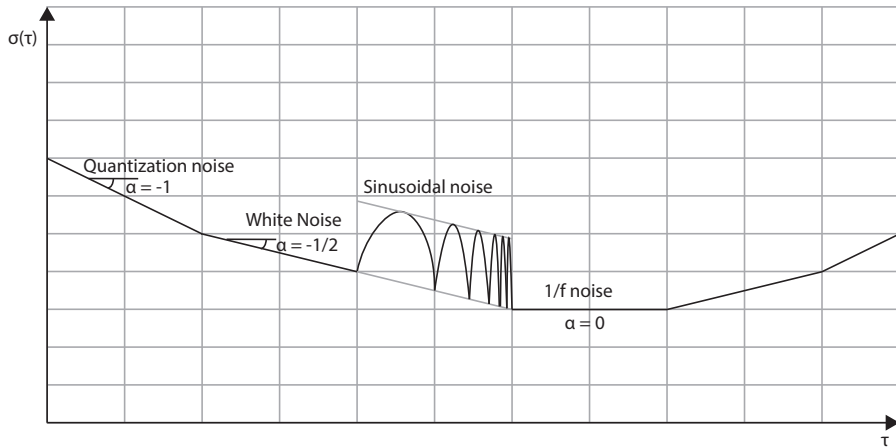


Figure 3.5: Allan Deviation of noise sources - Illustration

3.3.2 Estimator of Allan Variance for Frequency Stability

In practice, the numerical estimation of the Allan Variance is performed on the basis of the estimator given in Eq. 3.27. For a given time-domain dataset of measurements, the average on the timescale τ is computed, the result is a vector of n_i averages. The Allan Variance at timescale τ is thus the application of the estimator on this vector of averages [21]. In the case of clock frequency stability, the dataset is based on the relative frequency deviation expressed in 3.28.

$$\sigma_A^2(\tau) = \frac{1}{2 \cdot (n_i - 1)} \sum_{k=1}^{n_i-1} (x_{avg,k} - x_{avg,k+1})^2 \quad (3.27)$$

$$x_{avg,k} = \frac{f_0 - f_{avg,k}}{f_0} \quad (3.28)$$

3.4 Summary

We presented the basic definitions of jitter as well as methods for evaluating these ones using samples of measured periods. We also presented the methodology and precautions followed for performing period measurement of VCOs. We introduced a tool called *Allan Variance* for time-domain noise analysis. We will now present the VCO measurements, the results obtained following the defined methodology and the results obtained using the tools of this chapter.

Ring-Oscillator Measurements Analysis

4

Several measurements were performed on Voltage-Controlled Oscillator (VCO) designed by UCLouvain in bulk 65 nm CMOS technology from ST-Microelectronics. We will start by reviewing the general structure of the circuit, then, we will explore the results using the Allan Variance and we will finally develop jitter analysis for comparing the experimental results to computer-aided simulation.

4.1 Circuit Overview

The Integrated Circuit (IC) contains 25 ROs built with Low-Power (LP) and General-Purpose (GP) transistors¹ and using Standard Voltage Threshold (SVT), Low Voltage Threshold (LVT) and High Voltage Threshold (HVT). 24 are using 251 stages of inverters, the last one contains 53 stages. This design is arranged in 6 groups (A,B,C,D,E and F) connected to separate supply rails depending on their transistor type which allows independent measurements. Inside a block, each RO includes an **ENABLE** pin for independent activation in one group, each RO is also connected to a pre-level shifting block for shifting output voltage from the RO control voltage (VDDRO) to the fixed output voltage VDDL_P or VDDG_P. The values of these voltages are summarized in Table 4.1.

¹LP transistors usually have a lower leakage current by using thicker gate oxide.

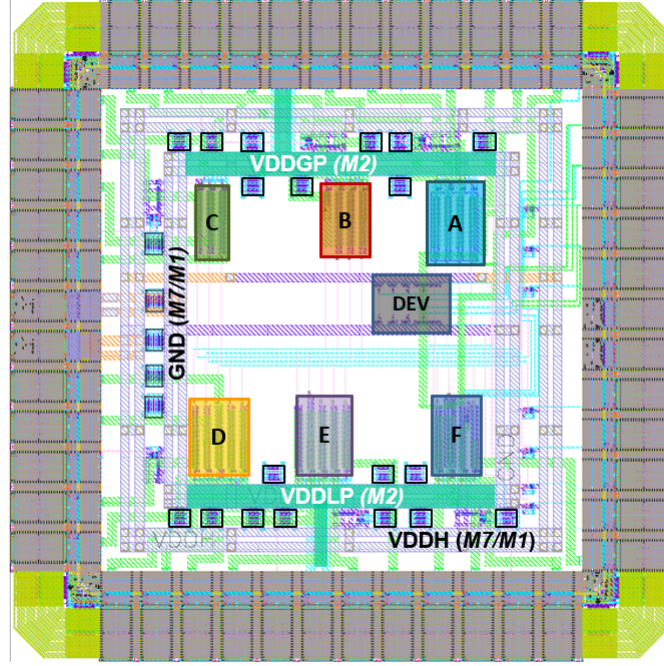


Figure 4.1: General view of the UCL0309 Chip - Image from UCLouvain

After pre-level shifting, each RO output signal of a given group is connected to a common NORING block from which a unique output (for the group) is connected to a main level shifting circuit, a frequency divider and an output buffer as illustrated in Fig. 4.2.

VDDRO	<0.2 V	>0.2 V & <0.5 V	<0.5 V
VDDH	0.65 V	0.65 V	1 V
VDDL/VP	VDDRO + 50 mV	VDDRO + 100 mV	VDDRO

Table 4.1

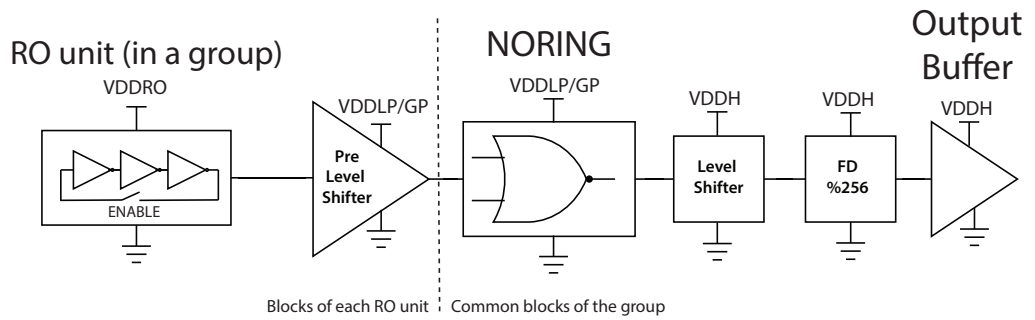


Figure 4.2: Schematic view of the UCL0309 Chip

Ring-Oscillator measurements For the purpose of this work, the measurements were focused on a specific unit of the block B containing a 53 stages ring-oscillator with LPSVT transistors. Both PMOS and NMOS transistors of this unit have length of 60 nm and width of 200 nm. The voltage thresholds of LPSVT PMOS in this technology is -425 mV , it is 442 mV for LPSVT NMOS.

4.1.1 Theory of Operation

CMOS Inverter The basic building block of the ring-oscillator is the CMOS inverter. The basic CMOS inverter is composed of a NMOS and a PMOS with both gates and drains connected together while body and source contacts of the PMOS (resp. NMOS) are tied to VDD (resp. GND) as shown in Fig. 4.3. This circuit implements the logic inversion function.

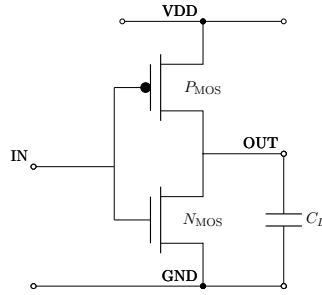


Figure 4.3: Circuit diagram - Basic CMOS Inverter

Dynamic Behaviour Considering a capacitive output load, the charge/discharge of this load will induce a decay between input and output nodes as illustrated in Fig. 4.4. This *stage delay* is the basis of the RO, it can be computed as in Eq. 4.1 where Δt is the stage delay and considering an ideal inverter switching at $0.5 \cdot V_{DD}$.

$$\Delta t = C_L \cdot \frac{\frac{1}{2} \cdot V_{DD}}{I_D} \quad (4.1)$$

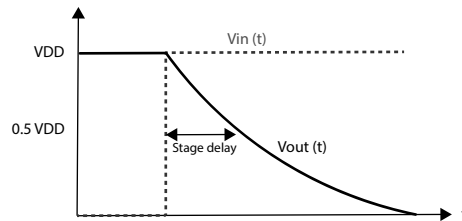


Figure 4.4: Voltage vs. time curve - Basic CMOS Inverter

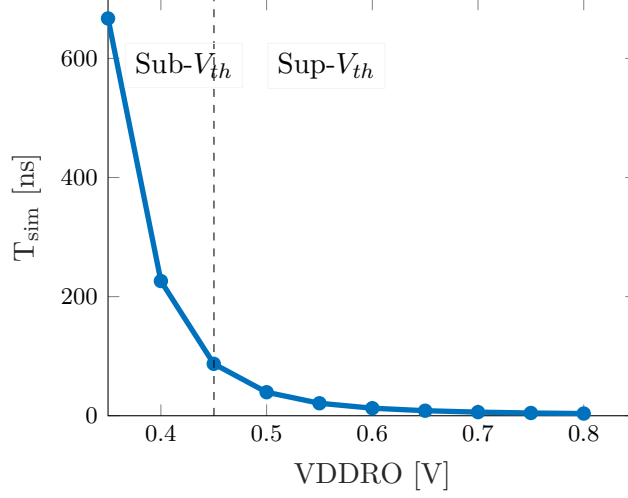


Figure 4.5: Simulated period vs. VDDRO - Standard Transient Simulation

N-Stage RO A Ring-Oscillator is built by looping N inverters, each of them being loaded by the previous one. The output period of a RO composed of N identical inverters is computed following Eq. 4.2 [28].

$$T_{RO} = 2 \cdot N \cdot \Delta t \quad (4.2)$$

$$T_{RO} = N \cdot C_L \cdot \frac{VDD}{I_D} \quad (4.3)$$

MOS Transistor Current As one can see in Eq. 4.3, the output period of the RO is inversely proportional to the drain current of MOS transistor switched on. As a first approximation, if we consider an NMOS transistor operating in saturation region ($V_{ds} > V_{gs} - V_{th}$) during all the switching phase, the drain current discharging the load capacitor in an inverter can be expressed as in Eq. 4.4. For an NMOS operating in sub-threshold regime ($V_{gs} < V_{th}$), the drain current discharging the load capacitor can be expressed as in Eq. 4.5 [3].

$$I_D = \frac{1}{2} \cdot \mu C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 \quad V_{ds} > V_{gs} - V_{th} \quad \text{Saturation} \quad (4.4)$$

$$I_D = I_0 \cdot 10^{\frac{V_{gs} + \nu V_{ds}}{\ln 10 \cdot n \cdot U_{th}}} \cdot (1 - e^{\frac{-V_{ds}}{U_{th}}}) \quad V_{gs} < V_{th} \quad \text{Subthreshold} \quad (4.5)$$

Considering Eq. 4.3 with Eq. 4.4 and Eq. 4.5, we can expect the period the RO to be proportional to $\frac{VDD}{(VDD - V_{th})^2}$ when $VDD > V_{th}$ and proportional to $\frac{VDD}{10^{VDD}}$ when $VDD < V_{th}$. The curve in Fig. 4.5 shows the period of the ring-oscillator simulated for multiple values of VDDRO, the exponential-like behaviour below 500 mV could be due to the MOS current behaviour in Sub- V_t and in saturation.

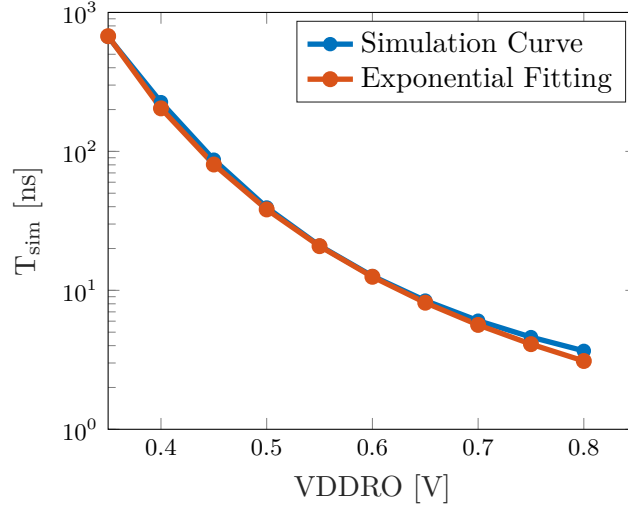


Figure 4.6: Simulated period vs. VDDRO - Exponential Approximation - Standard Transient Simulation

4.1.2 Supply-Voltage Noise Sensitivity

To quantify the influence of a voltage change in the output period, a fitting was performed on the curve in Fig. 4.5 using an exponential approximation, the function and estimated parameters are given in Eqs. 4.6 and 4.7. A comparison between the simulated curve and the exponential fitting is shown in Fig. 4.6.

$$T_{RO}(V_{DD}) = \alpha \cdot \exp\left(\frac{\beta}{V_{DD}}\right) \quad (4.6)$$

$$\alpha = 4.715 \cdot 10^{-11} \quad \beta = 3.349 \quad (4.7)$$

The effect of a relative voltage supply variation can be evaluated considering the sensitivity of the period to the voltage $S_V^{T^2}$ expressed in Eq. 4.9. For a given relative voltage variation, the resulting period variation is given by Eq. 4.10.

$$S_V^T(V) = \lim_{\Delta V \rightarrow 0} \frac{\Delta T}{\Delta V} \cdot \frac{V}{T} = \frac{\delta T}{\delta V} \frac{V}{T} \quad (4.8)$$

$$S_V^T(V) = \frac{-\beta}{V} \quad (4.9)$$

$$\delta T = \left(\frac{\Delta V}{V}\right) \cdot S_V^T(V) \cdot T \quad (4.10)$$

This period variation was computed for voltage variations of 10 mV, 25 mV and 50 mV at each supply voltage. The curve in Fig. 4.7 shows the absolute value of the

²This is a first order approximation.

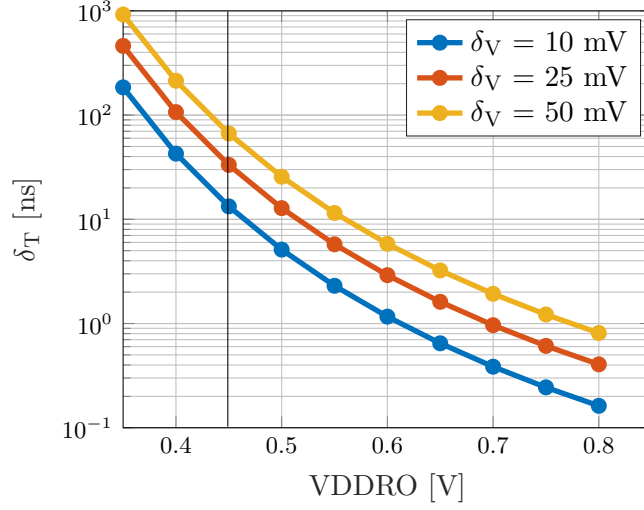


Figure 4.7: Period variation vs. VDDRO - Exponential Approximation

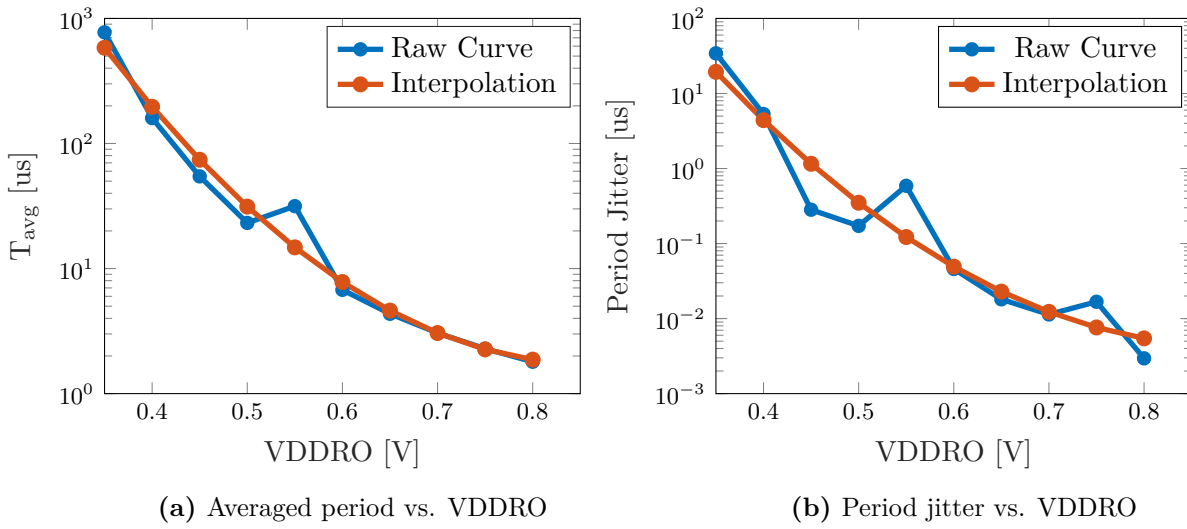
period variation for the three mentioned voltage variations. Below 450 mV the period variation is between 10 ns and 1 μ s, above this voltage, it is between 0.1 ns and 10 ns. This approximation will be useful to investigate the contribution of supply voltage noise in the measurements.

4.2 General Statistical Analysis

The data extracted from the oscilloscope are waveforms corresponding to the output voltage over time, as our analysis focus on timing behaviour of the VCOs, it was decided to directly extract the periods from these raw data.

Average period and jitter The instantaneous periods over time for each DC step were evaluated by finding the time instant of each rising edge considering the transition occurring when the instantaneous amplitude reaches 50% of the output signal full range. The average period of the RO was then estimated for each DC voltage by computing the average of the instantaneous periods over all the samples. The RMS period jitter was estimated by computing the standard deviation of the instantaneous periods using Eq. 3.8. The graphs in Fig. 4.8 represent these estimations in a semi-log manner, the averaged period at 550 mV seems to be an outlier when considering the smooth behaviour of the curve. The period jitter curve shows a decreasing period jitter with increasing voltage. An interpolation was performed on the raw curve to observe its general behaviour³. A quantitative analysis is required and will be presented later with respect to the simulation results.

³This interpolation curve will be used in all the chapter for comparison with simulation results.

Figure 4.8: Average T and σ_T estimation

4.3 Jitter Results and Simulations

Histogram analysis A first analysis was performed looking at the period histograms. The period histogram at 800 mV (Fig. 4.9a) presents a Gaussian-like shape. The period histogram at 350 mV (Fig. 4.9b) presents a non-Gaussian shape which shows the presence of non-random jitter contributions. The histograms for other voltages present similar behaviour which suggests that the measured jitter is not purely random. This is an important point for the comparison with basic noise simulation results as these only take random noise effect into account. **Note:** The sampling period of the oscilloscope during measurement operation is noted T_s for each measurement shown.

4.3.1 Ideal Ring-Oscillator Simulation

Simulated circuit The simulations were performed using Mentor Graphics ELDO simulator with Noisetran and SSTNOISE functionalities. The circuit simulated did not include post-layout RC extraction. As the measured circuit presents many blocks (RO, level shifter, frequency divider), these circuits were simulated separately so that their respective effects could be evaluated properly.

Noisetran - SSTNOISE It is important to notice the difference between the simulation tools used in this work. On one hand Noisetran is an ELDO functionality which performs several transient simulations that are usually called traces, each trace represents a *realization* of the process under investigation with instantaneous noise values based on the noise models defined for the technology, consequently, the higher the number of traces, the better the noise statistical distribution is evaluated which means the quality of simulation results is highly dependent on this parameter [29]. On the other hand,

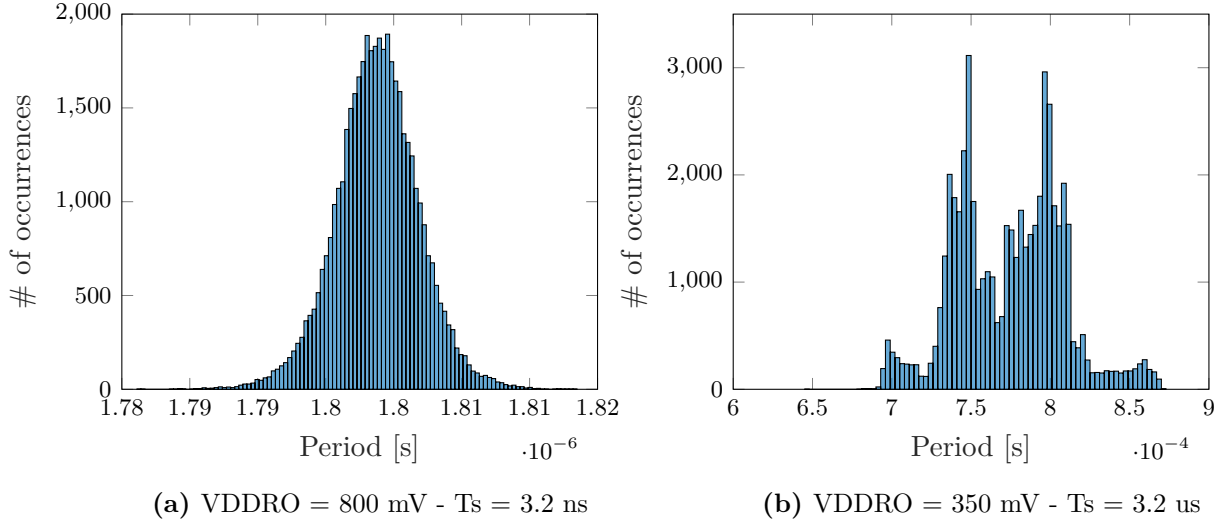


Figure 4.9: Histograms of measured periods

SST simulations are *steady-state transient*, the SST tools uses the harmonic balance for solving differential equations in the frequency-domain. The SSTNOISE function is a part of SST tools for performing noise analysis on oscillators, PLLs, frequency divider or related oscillator circuits. The main parameters are the frequency range of analysis, the fundamental frequency, the number of harmonics and the number of points per sub-range of frequency (decade, octave, etc) [30]. Usually, SSTNOISE results are similar to those of Noisetran but requiring a smaller simulation time⁴.

Period jitter The first simulation was performed using the jitter analysis tool SST-NOISE. The simulated circuit was the 53-stages ring-oscillator without post-layout RC. As the measured circuit contains a frequency divider with a factor of 256, it is required to look at the N-Period jitter ($N = 256$) for the simulated period jitter as it represents the effect of the jitter accumulation inside the frequency divider [9].

The results plotted in Fig. 4.10a represent the RMS N-Period jitter simulated for the basic 53-stages RO with SSTNOISE and the RMS period jitter estimated with the fitting on the measurements results.

This first analysis shows that there are multiple order of differences between the results of simulation and the measurements.

The average periods obtained in simulation do not fit perfectly with the measurements consequently, it is more convenient to compare the normalized period jitters as shown in Fig. 4.10b. These values are computed by dividing each period jitter by the corresponding average period.

⁴Empirical estimation: a few hours on Noisetran is equivalent to a few minutes with SSTNOISE.

Finally, the Fig. 4.11 represents the ratio of the normalized period jitter obtained from measurements and the one obtained in simulation, the order of magnitude is between 60 and 12. These order of magnitudes between measurements and simulation are particular of interest as in the framework of a design it is necessary to have simulation results close to reality.

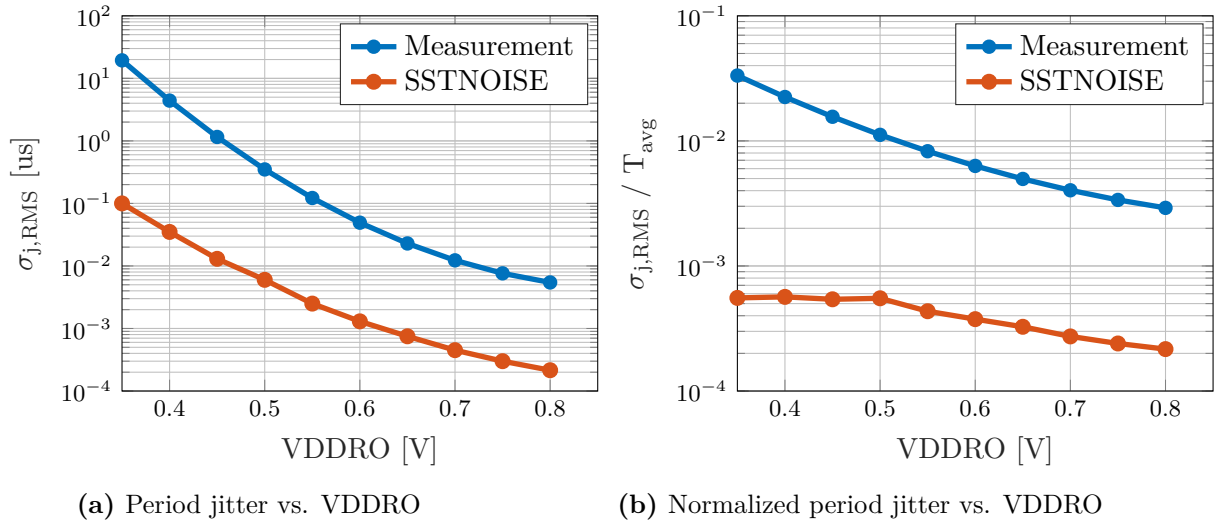


Figure 4.10: Period jitter comparison

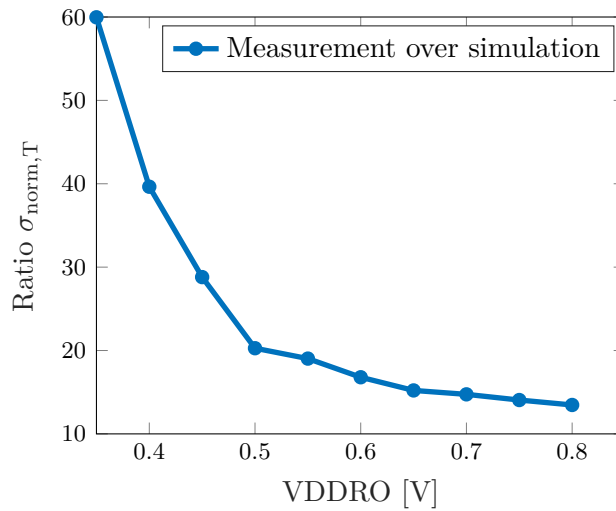


Figure 4.11: Ratio of normalized period jitter vs. VDDRO

4.3.2 Frequency Divider and Level Shifter

If the frequency divider is ideal, it will only integrate the jitter of the divided clock source but, as it is not an ideal circuit in practice, it may also introduce additional jitter to the output divided periodic signal [9]. Also, as shown in Fig. 4.2, the measured circuit contains several blocks between the RO and the frequency divider, especially the level shifters. The effect of a sub-threshold signal ($V_{th} \sim 400\text{ mV}$) may disturb the behaviour of the pre-level shifter.

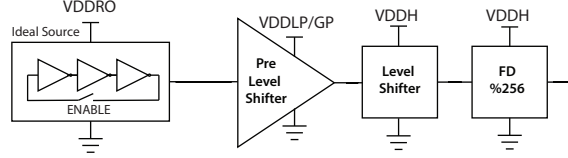


Figure 4.12: FD and LS Block Diagram - Simulation Setup

In order to evaluate the frequency divider and level shifters jitter contribution, simulations were run using Noisetran by feeding the frequency divider transistor level circuit and the level shifters (no post-layout RC) with an ideal jitter-free signal source at 350 mV and measuring the output signal to perform jitter analysis as shown in Fig. 4.12. The period of the ideal source was fixed at the mean period of the measurement at 350 mV (774 μs) divided by 256. This simulation resulted in a RMS period jitter of 24 ps at the output of the frequency divider. The resulting RMS period jitter was calculated following Eq. 3.7 and is given in Table 4.2, the effect of these blocks is negligible.

Jitter Budget	
Jitter RO (350 mV) [ns]	100
Jitter LS & FD (350 mV) [ns]	0.024
Resulting jitter [ns]	100

Table 4.2

4.3.3 Ring-Oscillator Simulation with Package Parasitics

The IC used for the measurements was inside a CQFP64 package. IC packages introduce parasitics RLC that may lead to supply/ground bounces [5]. To counteract these supply bounces, the usage of decoupling capacitors is required. In the measured IC, decoupling capacitors are present on all supply rails **VDDH** and **VDDLPGP**. The supply rails of ring oscillators control voltage **VDDRO** are not decoupled even if traces parasitic capacitance may be present.

Package Model In order to simulate these effects, the T-equivalent circuit of National Semiconductor was used. It models the leads by defining a **source** and a **sink** for each

end. This model defines inter-lead capacitance, capacitance to ground, mutual inductance between leads and lead resistance [20]. A circuit diagram for three leads is represented in Fig. 4.13. In the context of the ring-oscillator simulation, only the VDD RO supply lead was considered, thus, lead 1 and lead 2 were considered to be ground⁵.

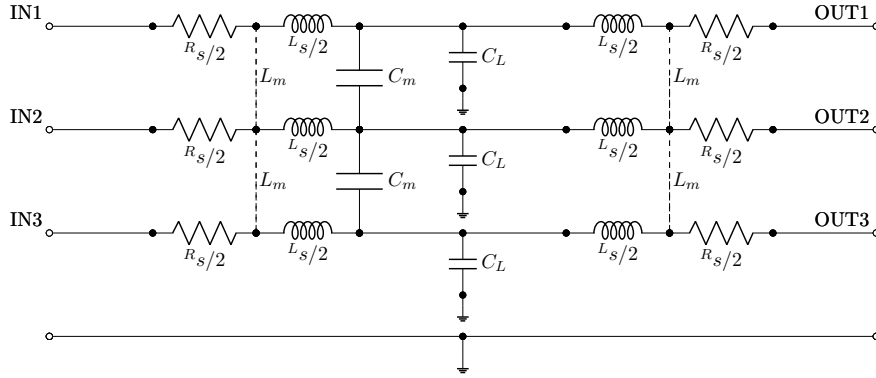


Figure 4.13: T-Equivalent circuit - Texas Instrument [20]

CQFP64 - Model values As it was not possible to measure the RLC parasitics of the package used in practice, it was decided to use typical values provided in the literature for QFP packages. The goal is to have a qualitative estimation of the influence of the package on the jitter. The values used are given in Table 4.3.

Lead Count	R_s [m Ω]	L_s [nH]	L_m [nH]	C_L [pF]	C_m [pF]
52	18	2.2	1.1	0.55	0.19

Table 4.3: Typical model values - QFP Model [17]

4.3.3.1 Transient Simulation

A transient simulation of the package parasitics was performed to evaluate the voltage variations on the RO supply rail. This simulation was performed at two extremes voltages (350 mV and 750 mV).

The graph in Fig. 4.14 shows the supply voltage of the RO at a nominal DC voltage of 750 mV, we can observe the voltage variation due to the package parasitics. The peak-to-peak voltage variation is 165 μ V which represents **0.06%** of the nominal voltage. The RMS period jitter measured due to these voltage variations is 66 fs which is negligible.

⁵In practice, all supply leads of all ROs are on the same side of the package. Only the RO being measured was supplied, all the others were grounded.

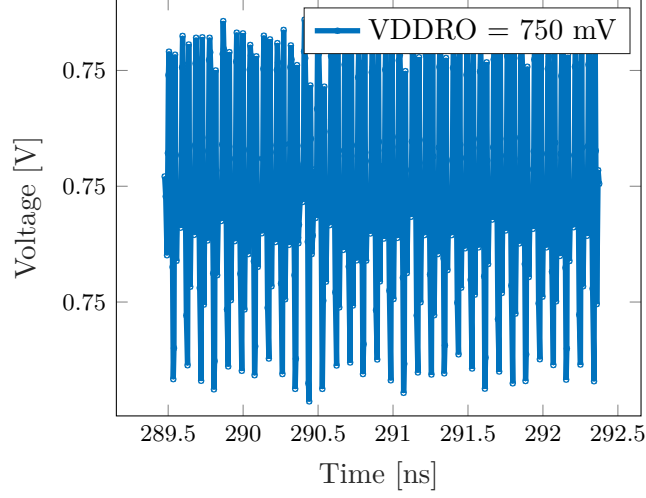


Figure 4.14: VDDRO vs. Time - QFP Model - VDDRO = 750 mV

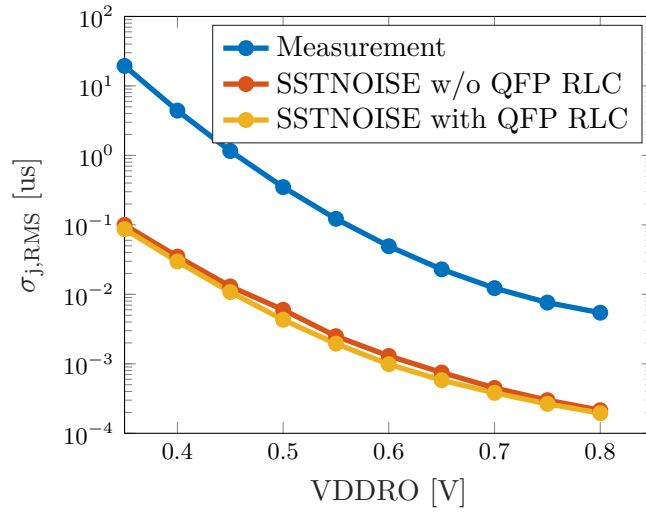
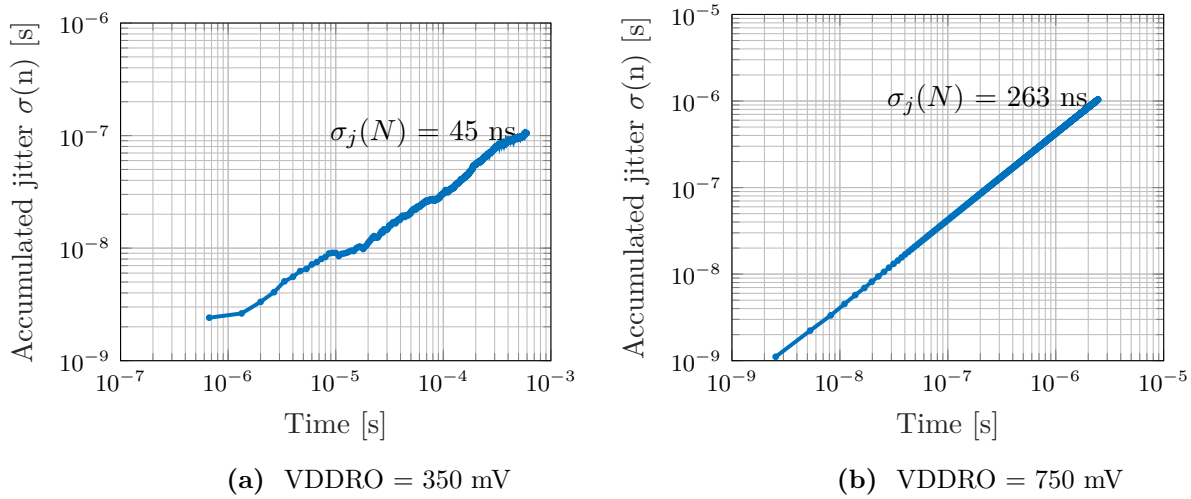
The same simulation performed at 350 mV results in a peak-to-peak voltage variation $0.2 \mu\text{V}$. The RMS period jitter resulting from this voltage variation is also negligible.

4.3.3.2 Noise Simulation

SSTNOISE Results A simulation was performed using SSTNOISE for all voltages with the RLC package model of Fig. 4.13 and the parameters from Table 4.3. The results are shown in Fig. 4.15 with the results previously obtained with ideal RO and with the measurement curve. As suggested with the transient simulation, the package parasitics do not seem to add more jitter.

Noisetran Results The Noisetran simulation was performed on two voltages (350 mV and 750 mV) due to the high simulation time required (~ 10 hours). It was performed using 50 traces with at least 256 cycles to evaluate the **256-period jitter**. The accumulated jitter extracted from the simulation results is shown in Fig. 4.16a for VDDRO = 350 mV. The **256-period jitter** computed for this voltage is 45 ns which is smaller than the result of 100 ns obtained previously with SSTNOISE. As the number of traces is limited, this number is interesting in terms of order of magnitude, we can conclude that the package parasitic do not seem to affect the period jitter at 350 mV in Noisetran.

The accumulated jitter extracted for a supply voltage of 750 mV is plotted in Fig. 4.16b. The resulting **256-period jitter** is 263 ns which is higher than the result of 300 ps obtained in SSTNOISE with parasitics. This disparity between SSTNOISE and Noisetran does not allow to conclude and requires an analysis of the simulation results from Noisetran.

**Figure 4.15:** Period jitter vs. VDD - Comparison**Figure 4.16:** Noisetran Simulation - 50 Traces - QFP Parasitics

An additional simulation with 100 traces was performed at 750 mV. The graph in Fig. 4.17 shows the period obtained in Noisetran over time for the trace 20 at 750 mV and for a small time range. As one can see, the period seems to oscillate periodically between 1.2 ns and 1.9 ns. The theoretical period at this voltage is supposed to be 4.62 ns, the behaviour observed in trace 20 is far from what we would expect on the basis of the standard transient simulation. The histogram of this trace is shown in Fig. 4.18a in comparison with the one of trace 4. The histogram of trace 4 presents a Gaussian distribution centered around 4.62 ns which is closer to what we would expect while the histogram of trace 20 presents a non-Gaussian distribution with a lot of occurrences

between 1.2 ns and 2 ns.

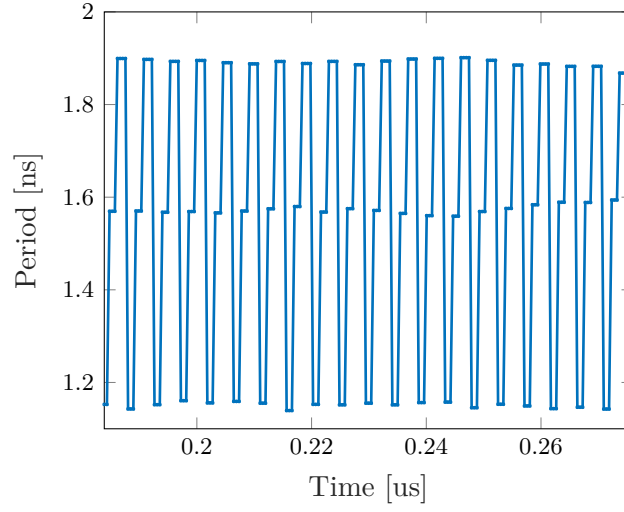


Figure 4.17: Period vs. Time for trace 20 - QFP Model - VDDRO = 750 mV

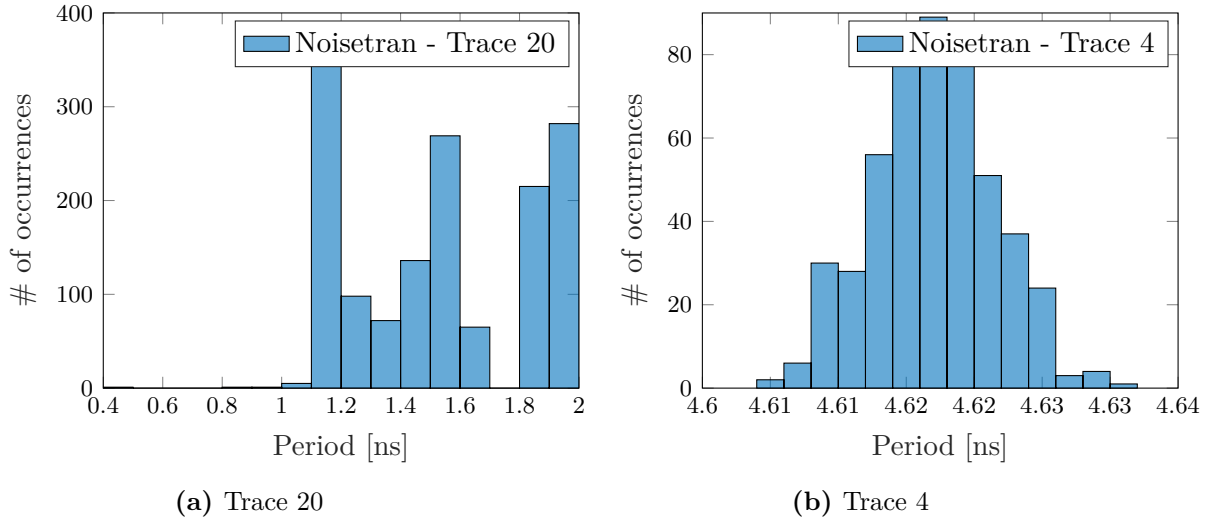


Figure 4.18: Noisetran - Histogram - QFP Parasitics Model - VDDRO = 750 mV

To have a broader view of the phenomenon, the histogram of all traces is shown in Fig. 4.19 with a bin width of 0.1 ns. We can notice 3 main parts, a non-Gaussian distribution between 1 ns and 2 ns, a non-Gaussian distribution between 2.5 ns and 3 ns, and a Gaussian distribution which is not clear considering the bin width.

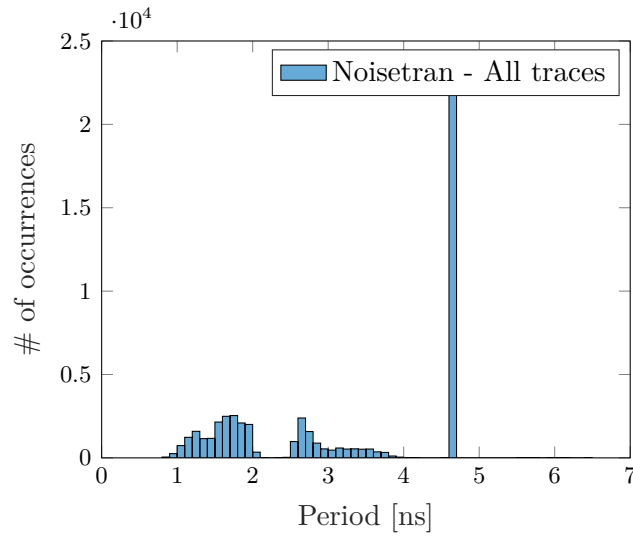


Figure 4.19: Noisetran - Histogram of 100 traces - QFP Parasitics Model - VDDRO = 750 mV

Additional simulations were performed at 600 mV and 800 mV in Noisetran with 100 traces. The histograms of these two simulations are shown in Fig. 4.20. The two histograms show a Gaussian distribution and do not show the phenomenon observed at 750 mV. Thus, it seems that this phenomenon is specific to this last supply voltage.

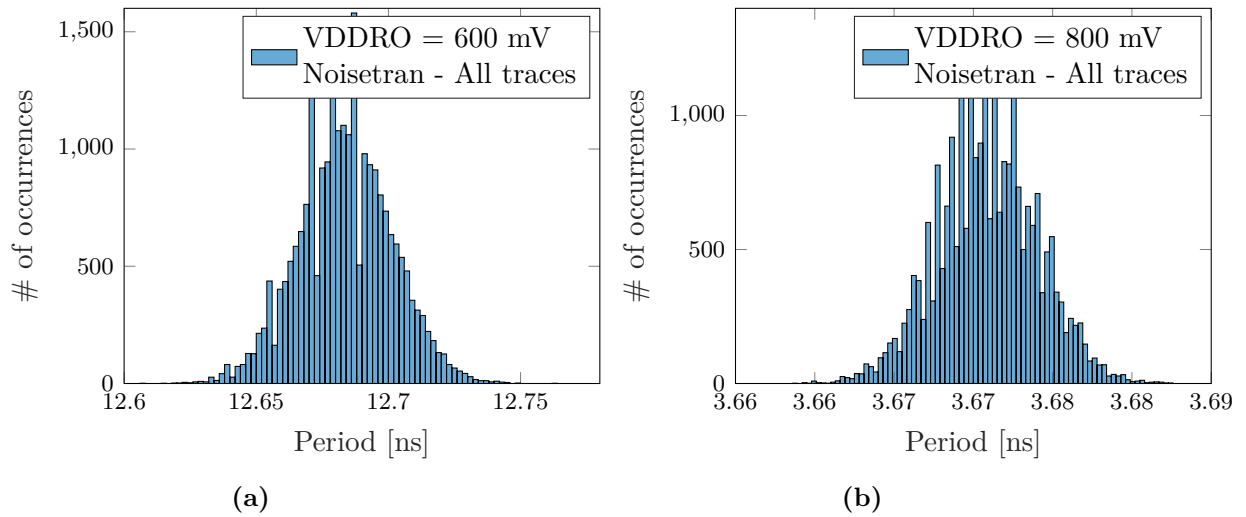


Figure 4.20: Noisetran - Histogram of 100 traces - QFP Parasitics Model

4.3.3.3 Conclusion on package parasitics

The transient simulation performed with the package parasitics results in a negligible supply voltage variation for all the voltage range. Consequently, it seems that supply voltage variation from package parasitics contributes weakly in the high jitter measured with ring oscillators.

The results obtained with package parasitics in SSTNOISE also seem to conclude that this is not a strong contribution in the RO jitter. The results of the transient noise simulation for 350 mV, 600 mV and 800 mV lead to the same conclusion. Nonetheless, the results obtained with Noisetran present an unexpected behaviour at 750 mV which cannot be explained for now, consequently, in absence of a better understanding of this phenomenon, we will not consider these results in the analysis⁶.

4.3.4 Measurement Analysis through Allan Variance

The Allan Variance was computed on the measured periods to have a better idea of the possible components affecting the output signal. The application of the estimator described in Section 3.3.2 allows observing the variability of the N-period jitter over consecutive N-periods of observations [9]. Based on the typical noise behaviour in Allan Variance presented, it is possible to observe how the RMS N-period jitter is affected by these sources.

The plot in Fig. 4.21a represents the Allan Deviation computed on the measured periods at 350 mV. The τ -range starts at 1 ms because the mean period at this voltage is 774.2 μ s. The most obvious component we can observe is the correlated sinusoidal noise characterized by the round peaks, the starting dip is located at $\tau = 20$ ms which means the frequency of this sinusoidal noise is 50 Hz [38]. We can notice how the Allan Deviation **converges** progressively to a minimum when the averaging time window is around 20 ms as low-frequency noise components become more dominant.

⁶The QFP model values used for the simulation are not those of the real package. These are typical values.

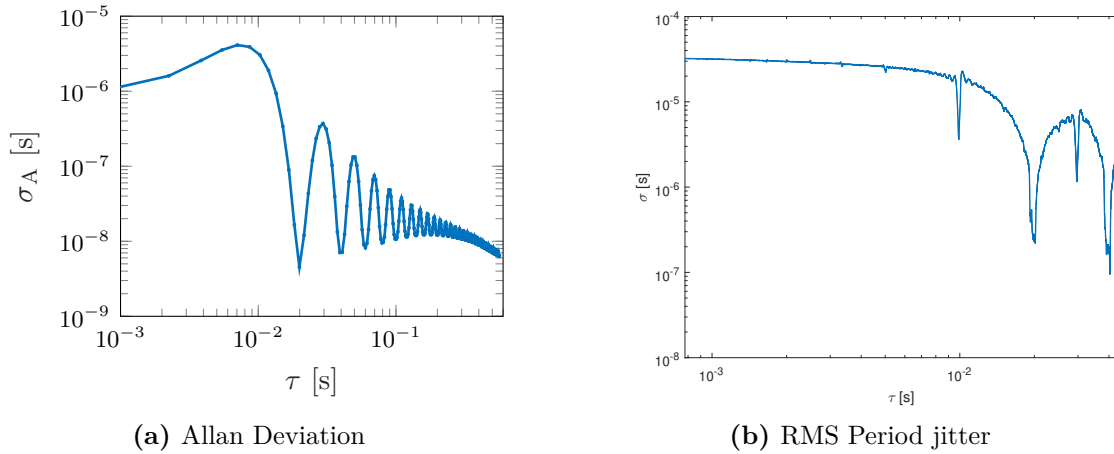


Figure 4.21: VDDRO = 350 mV - Ts = 3.2 μ s

The plot in Fig. 4.21b represents the standard deviation of the periods computed for various averaging time ranges⁷. While the Allan Variance represents the variability of the N-period jitter for various N-period averaging time ranges, this graph represents the absolute RMS period jitter for these time ranges. Consequently, we can see that the RMS period jitter after averaging over 20 ms is 524 ns, this represents the RMS period jitter for which the effect of the correlated sinusoidal noise is attenuated. An averaging of the periods with a time window of 20 ms was performed at 350 mV using **all** the samples measured and the RMS period jitter resulting from this operation is 2.93 μ s, this is **10 times smaller** than without averaging.

Histograms after averaging The effect of averaging on cycles of 20 ms can also be observed in the histograms. Fig. 4.22 shows the histograms of the periods at 350 mV with no averaging and with averaging, the first effect we can notice is absence of some of the peaks. As a matter of fact, the histogram 4.22a has 4 distinct peaks while the histogram 4.22b has only two peaks. In theory, if the only deterministic jitter contribution is the sinusoidal noise, we should get a perfect Gaussian-like histogram but it should be noted that the averaging operation loses some information as we decrease the number of samples. Also, there may be another deterministic contribution producing the second peak.

Finally, the same operation was performed at 450 mV, the histograms are shown in Fig. 4.23. The histogram with no averaging has 2 distinct peaks while the histogram after averaging seems to have only one distinct peak. Again, these histograms are not extremely accurate due to the loss of information with reduction of the number of samples. This averaging operation at 450 mV results in an RMS period jitter of 28.5 ns which is

⁷This plot was computed with a reduced number of samples for limiting computation time.

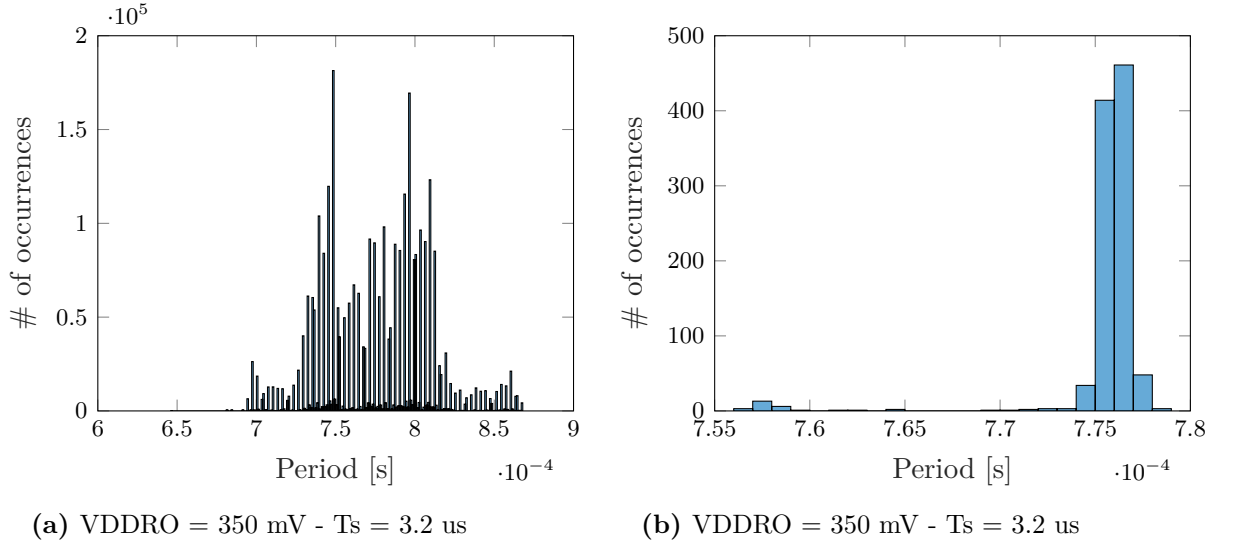


Figure 4.22: Period histograms - No averaging (left) - 20 ms cycles averaging (right)

closer to the 10 ns RMS period jitter obtained in SSTNOISE with the simulation of the ideal RO circuit.

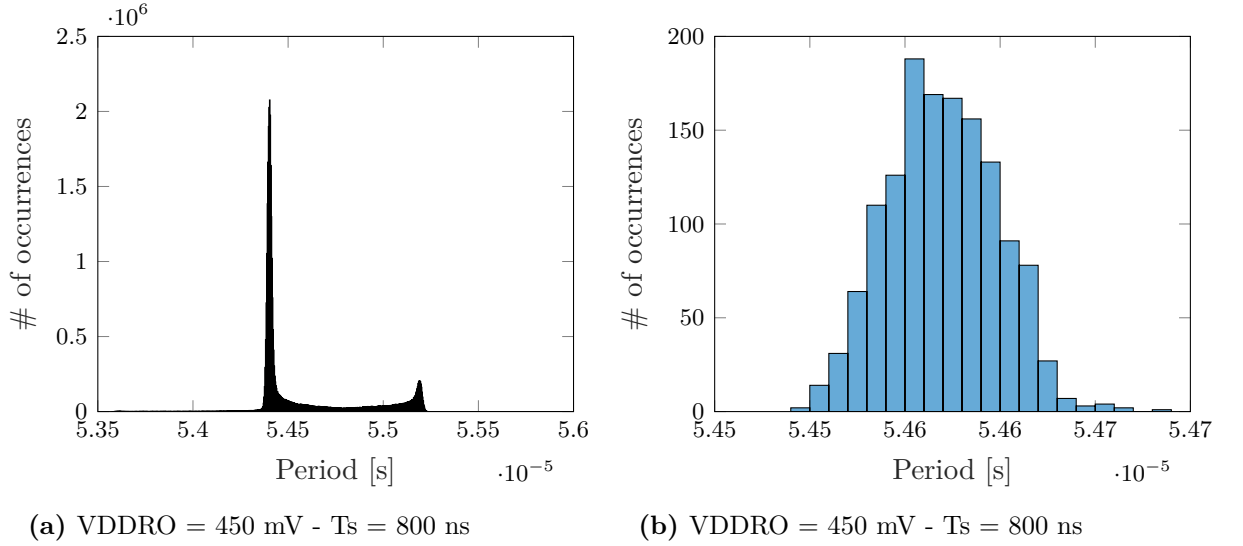


Figure 4.23: Period histograms - No averaging (left) - 20 ms cycles averaging (right)

We repeated this operation for all voltages excluding 800 mV as the number of samples available at this voltage after averaging was too small (2 samples). The plot in Fig. 4.24 shows the RMS period jitter of the measurements without averaging, the RMS period jitter with averaging and the jitter extracted from SSTNOISE for all voltages. We can

see that this operation highly reduces the difference observed between simulation and measurements.

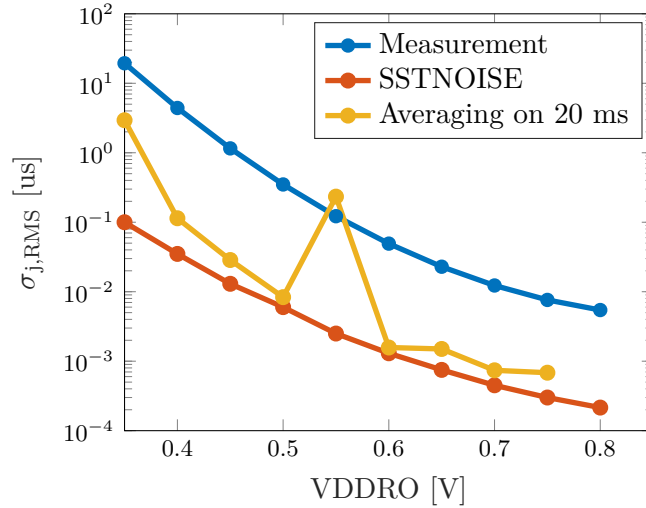


Figure 4.24: Period jitter vs. VDD - Measurement - SSTNOISE - Measurement after averaging

4.3.5 Supply-Voltage Noise Simulation

The Allan Variance was used to identify the noise sources that affect the period jitter of the measured ring-oscillators. It allowed us to notice the presence of a deterministic sinusoidal noise affecting the circuit as supply-voltage noise. Also, by performing an averaging over cycles of 20 ms, we were able to mitigate the effect of this noise. Nonetheless, it is interesting to analyze the effect of this kind of noise in simulation to evaluate the sensitivity of the circuit and effect of this one.

4.3.5.1 Sinusoidal Noise Estimation

Considering an ideal RO⁸ affected by a sinusoidal supply noise, the supply voltage can be expressed as in Eq. 4.11. Then using the approximation of Eq. 4.6 with Eq. 4.10, the period jitter resulting from a sinusoidal noise can be expressed as in Eq. 4.15. The RMS period jitter can be estimated using Eq. 4.16.

⁸In the sense that it is not affected by random noise.

$$\text{VDD}(t) = \text{VDD} + A \cdot \sin\left(\frac{2\pi}{T_g} \cdot t\right) \quad (4.11)$$

$$T_{out}(t) = f_{RO}(\text{VDD}(t)) \approx \alpha \cdot \exp\left(\frac{\beta}{\text{VDD}(t)}\right) \quad (4.12)$$

$$T_{out}(t) = \alpha \cdot \exp\left(\frac{\beta}{\text{VDD} + A \cdot \sin\left(\frac{2\pi}{T_g} \cdot t\right)}\right) \quad (4.13)$$

$$T_{out}(t) \approx T_{out,0} + \left(\frac{\Delta V(t)}{\text{VDD}}\right) \cdot S_V^T(V) \cdot T_{out,0} \quad (4.14)$$

$$p_j(t) = \Delta T = \left(\frac{\Delta V(t)}{\text{VDD}}\right) \cdot S_V^T(V) \cdot T_{out,0} \quad (4.15)$$

$$p_{j,\text{RMS}} = \sqrt{\frac{1}{T} \int_0^T (p_j(t))^2 dt} \approx \frac{A}{\sqrt{2}} \cdot S_V^T(V) \cdot \frac{T_{out,0}}{\text{VDD}} \quad (4.16)$$

Simulation and Approximation To verify the accuracy of this approximation, a transient simulation was made with the RO being supplied by a DC source with a sinusoidal perturbation. Due to the huge simulation time (≈ 10 hours), the simulation was made for few voltages (350 mV, 450 mV, 650 mV and 750 mV) and few perturbations amplitudes (10 mV, 25 mV and 50 mV), the sinusoidal noise at the two higher voltages was set to a frequency of 10 kHz while it was set at 50 Hz for the two other voltages. The curves in Fig. 4.25 show the estimation in *dashed lines* and the results of the simulation in *solid lines*, the estimation being close to the simulation.

Measurement fitting In Section 3.1.1 from Chapter 3, we explained that the presence of random jitter and deterministic jitter contributors leads to non-Gaussian distributions. A technique based on the dual-Dirac approximation and tail fitting was introduced for separating these two jitter components. We applied this method by using a tail fitting algorithm in MATLAB [27] to identify the two Gaussian means μ_L and μ_R that correspond to the position of the two Dirac impulses. The difference $\mu_R - \mu_L$ of these two means corresponds to the deterministic jitter **DJ**.

The results of the application of this method are shown in Fig. 4.26 where the original histograms measured at 650 mV and 750 mV are shown with the distribution estimated from the tail fitting algorithm. Unfortunately, the dual-Dirac approximation only works when the distribution is characterized by a dual-Gaussian shape, which is not the case for all histograms as shown in the example of Fig. 4.27 which corresponds to VDDRO of 550 mV.

Considering only the histograms that show a dual-Gaussian shape, we evaluated the **DJ** using the methodology of tail fitting with the dual-Dirac approximation. For the

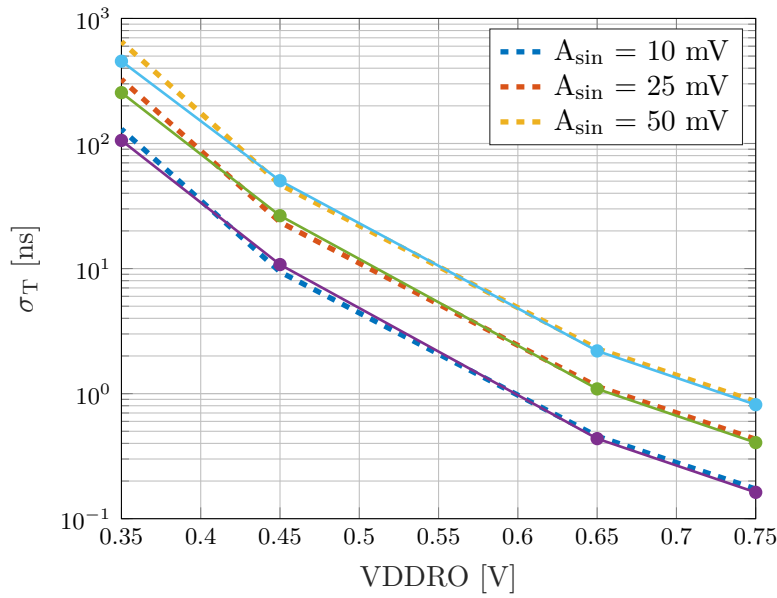


Figure 4.25: Sinusoidal noise - *Dashed line: Approximation - Solid line: Simulation* - The values of the y-axis represent the RMS period jitter evaluated on a sinusoidal period

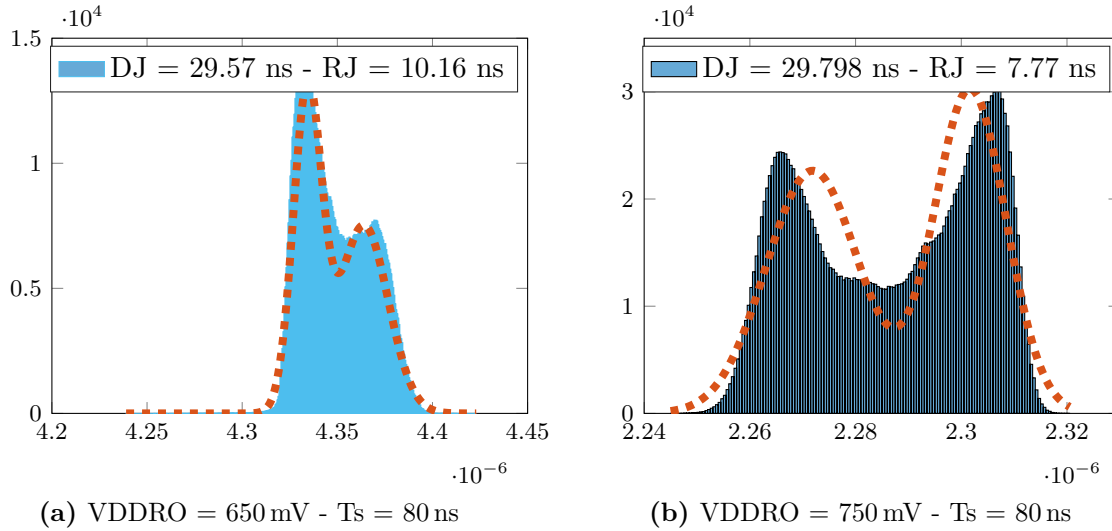


Figure 4.26: Period histograms - Tail fitting

histograms presenting more complex shapes, we noticed that some of them contained more than two Gaussian-like shapes as in Fig. 4.27, consequently, we manually measured the distance between the individual peaks thus evaluating the **DJ** manually. Finally, we compared the curve of **DJ** to the results obtained with the sinusoidal jitter estimator described previously. The plot in Fig. 4.28 shows the result obtained with the estimation

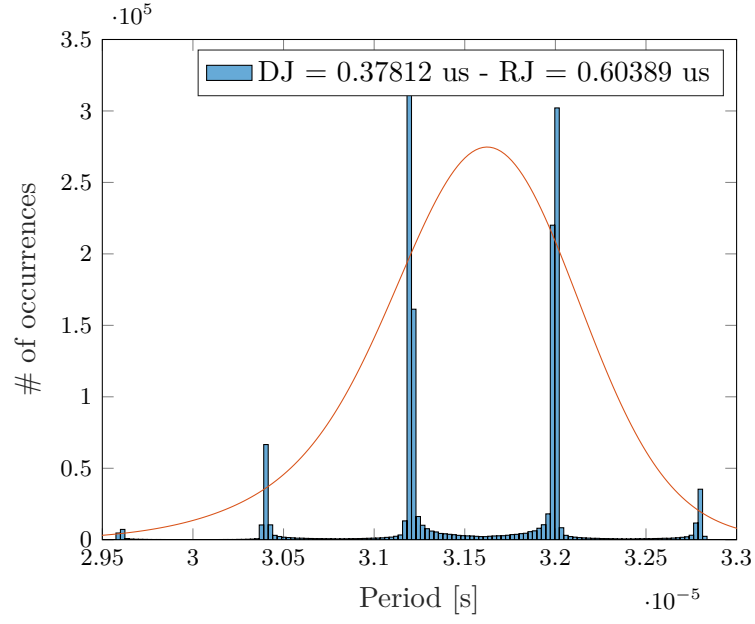


Figure 4.27: Period histograms - Tail fitting - VDDRO = 550 mV - $T_s = 800$ ns

for sinusoidal noise of two amplitudes (1 mV and 20 mV) compared to the **DJ** jitter curve extracted from the measurements.

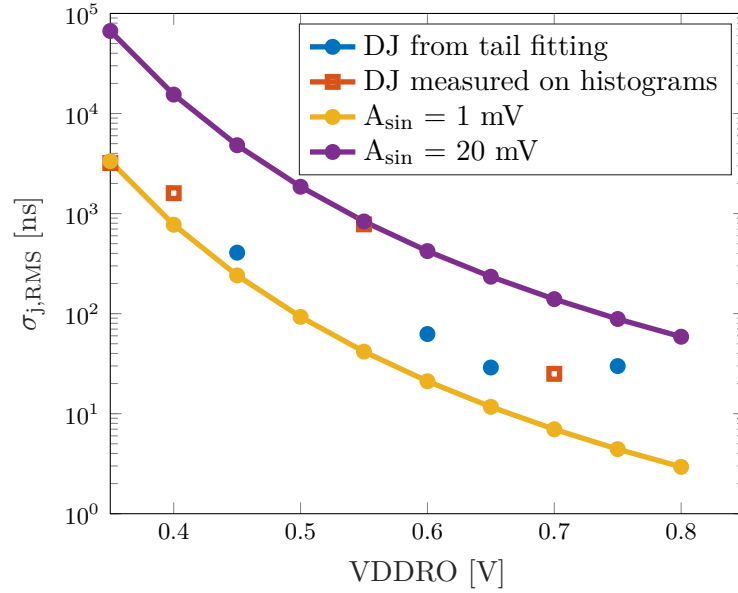


Figure 4.28: Sinusoidal noise estimation and DJ from tail fitting vs. VDDRO

4.4 Summary

In this chapter, we analyzed the time-domain performances of an RO built in bulk 65 nm technology from ST-Microelectronics.

We started by analyzing theoretically the behaviour of the RO based on circuit theory and we extracted a mathematical relationship between output period and supply voltage from simulation. From that relationship, we were able to build an approximation to evaluate the sensitivity of the RO against supply-voltage noise.

After that, we started our jitter analysis on measurements of a fabricated unit of this oscillator by extracting general statistics from the measurements shown in Fig. 4.8a and 4.8b. The period jitter curve extracted from the measurements was then first compared to the period jitter obtained in simulation of the RO ideal circuit with SSTNOISE. This comparison was made based on absolute values and then on normalized values with respect to the nominal period to take into account the nominal period offsets between simulation and fabricated unit. Finally, we could see that the ratio between the normalized period jitter in measurements and simulation was situated between **60** for the smallest voltage (350 mV) and **10** for the highest voltage (800 mV) as shown in Fig. 4.11.

In order to explain the gap between measurements and simulation, we explored multiple possibilities of jitter contributors that were not in the ideal simulation of the RO. We first studied the effect of the frequency divider and the two level shifters. This was done by simulating these blocks with their ideal circuit fed by an ideal clock source at the smallest supply voltage in Noisetran. We could see that these blocks were adding an **RMS period jitter** of 24 ps which was **negligible** compared to the 100 ns **RMS period jitter** of the RO alone in simulation.

Next, we investigated the possible effect of the CQFP64 package parasitics on the RO in terms of period jitter. To do so, we decided to use a T-equivalent circuit which models the package leads as a combination of resistances, capacitors and inductors. The parameters found in the literature for this model were for a typical QFP package.

We first performed a standard transient simulation of the ideal RO circuit with the model to evaluate the supply-voltage variation due to these parasitics, this simulation showed us that the voltage variation at 750 mV had a **peak-to-peak value** of 165 μ V and at 350 mV, the peak-to-peak voltage variation was 0.2 μ V. The RMS period jitter measured in the classic transient simulation with this model was 66 fs at 750 mV which corresponds to an RMS period jitter of 16.9 ps after accumulation in the frequency divider and is small compared to the 300 ps RMS period jitter of the RO obtained in simulation.

To evaluate accurately the effect on the jitter, simulations of the RO circuit with the package parasitics model were performed in SSTNOISE resulting in a period jitter similar

to the one that was obtained in the simulation without this model. Similar simulations performed in Noisetran showed the same results for nearly all voltages. However, we noted an unexpected behaviour of the Noisetran simulation at 750 mV we decided to discard as the other tools did not show this behaviour. It will still be required to study this phenomenon deeper to identify its cause as it may happen in reality. In the end, we concluded that the package parasitics were not the major reason of the gap between the simulation and the measurements.

After that, we analyzed the measurements using the **Allan Variance**. This time-domain tool based on successive sample averaging allowed us to identify precisely the presence (at 350 mV) of a correlated noise which was in fact sinusoidal noise with a period of 20 ms. On the basis of this analysis, an averaging was performed on samples subsets of 20 ms for the period data at 350 mV, we showed that this operation allowed us to attenuate the influence of the sinusoidal noise leading to a calculated RMS period jitter of 2.93 μ s (after averaging) which is smaller than the RMS period jitter 30 μ s computed without averaging. This value is closer to the RMS period jitter of 100 ns obtained in SSTNOISE. We also showed that this operation resulted in a Gaussian distribution at 450 mV and a general reduction of the RMS period jitter for voltages up to 750 mV.

Finally, we elaborated a way to estimate the RMS period jitter resulting from a sinusoidal noise for a given amplitude and supply voltage. We used the tail-fitting method with dual-Dirac approximation to compute the deterministic jitter contribution at each voltage and we used it to evaluate the possible sinusoidal noise amplitude affecting the circuit during measurements. We saw that a sinusoidal noise of amplitude between 1 mV and 20 mV could explain the **DJ** curve.

To conclude, we must note that the histograms of measurements did not all present perfect Gaussian distribution, some histograms even showed more than two Gaussian-like shapes, which could be due to a modulated correlated noise. We verified that the gap between simulation and measurements was not due to the effect of other blocks surrounding the RO, we also verified that this was not due to the package parasitics, we can only conclude with certitude that a sinusoidal noise was affecting the measurements.

To go further, we can note that, in the context of a strong jitter constraint, the robustness of an oscillator upon supply voltage noise variation is a major point and this will be the basis of our choice in the next chapter. This analysis was useful as it allowed us to put in practice the use of multiple jitter analysis tools as the simulation tools, the Allan Variance and the tail fitting method. This set of tools will be necessary for the evaluation of the time-domain interface which will have a strong jitter constraint.

Time-Domain Capacitance-to-Digital Converter

5

In Chapter 2, we explored the State-of-the-Art of CDCs. We briefly reviewed the two types of converters and explained the decision of designing a time-domain CDC. This topology offers better capabilities in terms of versatility with the range of capacitance, it also usually results in lower FoM and area. In Chapter 3, we introduced all the tools required for performing jitter analysis. We applied these tools to a study case (RO) in Chapter 4 allowing us to develop a methodology for time-domain analysis and also identify jitter contributors that could disturb the function of a time-domain converter.

Note As explained in Chapter 2, time-domain CDCs contain two high-level blocks, the CCO for converting the capacitance variation to time-domain and the TDC for converting the time-event into a digital signal. In this work, we decided to focus on the design of the CCO. Consequently, this chapter will only treat the design of this block.

In this chapter, we will present the circuit we designed in UMC-RF 0.18 μm technology, we will motivate this choice and we will detail the *top-down* design methodology we followed. Finally, we will review all the results obtained in simulation and we will describe the measurement methodology developed for evaluating the real performances of the fabricated circuit.

5.1 Relaxation Oscillator

The design from [22] is a time-domain CDC built on the basis of a relaxation oscillator. The FoM of this design reaches 3.8 nJ per conversion step, it is 300 times higher than the time-domain CDC from [18], but this design reaches an ENOB of 15 bits and it was built in 700 nm technology. It was decided to design a CDC based on this article with the goal of reaching a lower FoM in the range of the state-of-the-art. As explained in Chapter 4,

the robustness against supply-voltage noise is an important point for the CCO and we will show that the relaxation oscillator is better than the ring-oscillator for this point. Also, relaxation oscillators theoretically perform better than ring-oscillators in terms of jitter for a given technology [9].

5.1.1 Theory of Operation

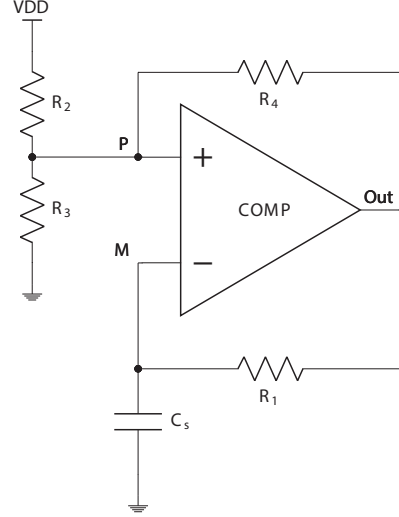


Figure 5.1: Circuit diagram - Relaxation Oscillator [22]

The circuit from [22] is shown in Fig. 5.1 with the sensing capacitance noted C_s . The operation of this circuit can be divided in two phases, a charging phase and a discharging phase, we will see the theory of operation considering an ideal comparator.

Let's consider the beginning of the charging phase for which the output of the comparator is **high**, then, the voltage at node **P** can be expressed as in Eq. 5.1. At the beginning of the discharging phase, the voltage at node **M** is smaller than the voltage at node **P** during previous phase, thus the output of the comparator is **low**. The voltage at node **P** in the actual phase can be calculated as in Eq. 5.3.

$$V_{Out}(t_0) = VDD, V_{C_s}(t_0) = 0 \quad V_P(t_0) = VDD \cdot \frac{R_3}{R_3 + R_2 \parallel R_4} \quad (5.1)$$

$$\implies V_{TH} = V_P(t_0) \quad (5.2)$$

$$V_{C_s}(t_1) > V_P(t_0), V_{Out}(t_1) = 0 \quad V_P(t_1) = VDD \cdot \frac{R_3 \parallel R_4}{R_2 + R_3 \parallel R_4} \quad (5.3)$$

$$\implies V_{TL} = V_P(t_1) \quad (5.4)$$

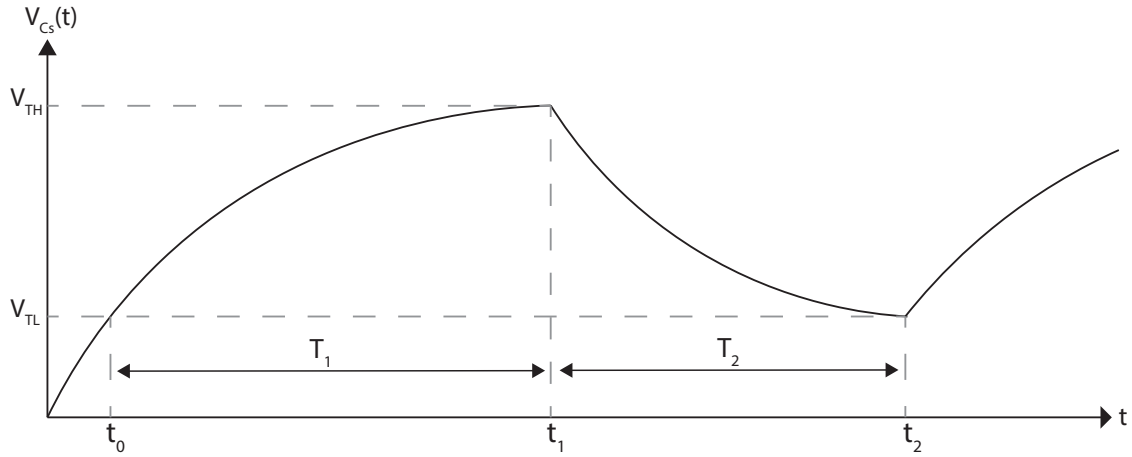


Figure 5.2: Voltage vs. time curve - Capacitor - Relaxation Oscillator

Each phase can be seen as an ideal RC circuit operating either in charge or in discharge. Thus, the voltage on capacitor C_s can be expressed as in Eqs. 5.6 and 5.7. The two phases are illustrated in Fig. 5.2.

$$\tau = R_1 \cdot C_s \quad (5.5)$$

$$V_{C_s}(t) = VDD \cdot \left(1 - \exp\left(\frac{-t}{\tau}\right)\right) \quad \text{During charging phase} \quad (5.6)$$

$$V_{C_s}(t) = V_{C_s}(0) \cdot \exp\left(\frac{-t}{\tau}\right) \quad \text{During discharging phase} \quad (5.7)$$

The duration of the charging phase T_1 is the difference of the two time instants corresponding to the switching of the comparator as shown in Eq. 5.8. The time instant t_0 is the one at which the capacitor voltage reaches the low threshold voltage V_{TL} . The instant t_1 is the time at which the capacitor voltage reaches the high voltage threshold V_{TH} . As we know each voltage, we can deduce the corresponding time instants using Eqs. 5.9 and 5.10. The charging phase duration is given in Eq. 5.11.

$$T_1 = t_1 - t_0 \quad (5.8)$$

$$V_{TL} = VDD \cdot \left(1 - \exp\left(\frac{-t_0}{\tau}\right)\right) \quad (5.9)$$

$$V_{TH} = VDD \cdot \left(1 - \exp\left(\frac{-t_1}{\tau}\right)\right) \quad (5.10)$$

$$T_1 = \tau \cdot \ln\left(\frac{V_{TL} - VDD}{V_{TH} - VDD}\right) \quad (5.11)$$

Following the same reasoning, the duration of the discharging phase can be evaluated using Eq. 5.13. The duration T_2 is given in Eq. 5.14.

$$T_2 = t_2 - t_1 \quad (5.12)$$

$$V_{TL} = V_{TH} \cdot \exp\left(\frac{-(t_2 - t_1)}{\tau}\right) \quad (5.13)$$

$$T_2 = \tau \cdot \ln\left(\frac{V_{TH}}{V_{TL}}\right) \quad (5.14)$$

$$(5.15)$$

The complete period of the relaxation oscillator is simply the sum of the two phases duration as expressed in Eq. 5.16.

$$T = T_1 + T_2 = \tau \cdot \ln\left(\frac{V_{TH}}{V_{TL}} \cdot \frac{V_{TL} - VDD}{V_{TH} - VDD}\right) \quad (5.16)$$

We can also highlight the fact that, in order to obtain an output square wave with a duty-cycle of 50%, the two phases should have the same duration as shown in Eq. 5.17. Using the same value for resistors R_2 , R_3 and R_4 allows satisfying this condition as shown in Eqs. 5.19 and 5.20.

$$\frac{V_{TL} - VDD}{V_{TH} - VDD} = \frac{V_{TH}}{V_{TL}} \quad (5.17)$$

$$R_2 = R_3 = R_4 = R_0 \quad (5.18)$$

$$\frac{0.5 \cdot R_0 - (R_0 + 0.5 \cdot R_0)}{R_0 + 0.5 \cdot R_0} \cdot \frac{R_0 + 0.5 \cdot R_0}{R_0 - (R_0 + 0.5 \cdot R_0)} = \frac{R_0}{R_0 + 0.5 \cdot R_0} \cdot \frac{R_0 + 0.5 \cdot R_0}{0.5 \cdot R_0} \quad (5.19)$$

$$\frac{1}{0.5} = \frac{1}{0.5} \quad (5.20)$$

5.1.2 Supply-Voltage Noise Sensitivity

Considering an ideal comparator, the sensitivity of the circuit upon supply voltage noise or variation can be evaluated. The period expressed in Eq. 5.16 can be written in the form of Eq. 5.21 where the supply voltage is noted $\mathbf{U}$ and the dependence of parameters on supply voltage is specified in the form $f(U)$. After simplifications, the period can be expressed as in Eq. 5.23 where there is clearly no dependence upon supply voltage. Consequently, we can state that a relaxation oscillator with an **ideal** comparator should be **robust against supply voltage variation** making this structure very convenient for a CCO.

$$T = \tau \cdot \ln \left(\frac{V_{TH}(U)}{V_{TL}(U)} \cdot \frac{V_{TL}(U) - U}{V_{TH}(U) - U} \right) \quad (5.21)$$

$$= \tau \cdot \ln \left(\frac{U \cdot K_H}{U \cdot K_L} \cdot \frac{U \cdot K_L - U}{U \cdot K_H - U} \right) \quad (5.22)$$

$$= \tau \cdot \ln \left(\frac{K_H}{K_L} \cdot \frac{K_L - 1}{K_H - 1} \right) \quad (5.23)$$

$$= \tau \cdot \ln \left(\frac{1}{0.5} \cdot \frac{1}{0.5} \right) \quad \text{if Eq. 5.18 is respected.} \quad (5.24)$$

$$\frac{\delta T}{\delta V} = 0 \quad (5.25)$$

5.1.3 Noise Modeling and Jitter Estimation

It is necessary to evaluate the period jitter of the CCO from the noise sources of the circuit. This can be done by building a model which relates basic noise sources to a time-domain noise expressed as jitter.

Noisy operation of the relaxation oscillator As explained in Section 5.1.1, the relaxation oscillator operates in phases of charging and discharging a capacitor. The switching between these phases is achieved by the comparator based on the difference between the instantaneous capacitor voltage and voltage of the resistor divider. If there is noise on the resistor divider voltage, this will induce a small deviation of the switching time from its ideal instant [40]. This is illustrated in Fig. 5.3 where the noisy voltage thresholds V_{th} are shown and the capacitance voltage is approximated by a straight line.

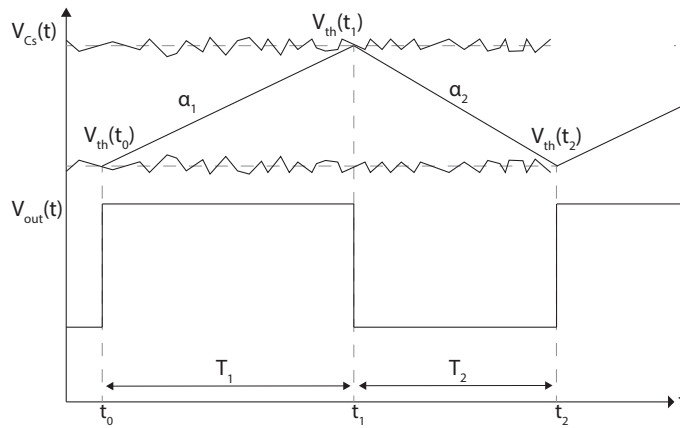


Figure 5.3: Noisy thresholds - Noise modeling of relaxation oscillator - Inspired from [40]

There are 3 switching time events t_0 , t_1 and t_2 in the operation of the oscillator. If there is noise on V_{th} , these time events will be affected by small time deviations $t_{n,0}$ and $t_{n,1}$ resulting in a period deviation t_n as expressed in Eq. 5.27.

$$T_0 = T_1 + T_2 \quad (5.26)$$

$$T_0 + t_n = T_1 + t_{n,1} + T_2 + t_{n,2} \quad (5.27)$$

$$\frac{t_n}{T_0} = \frac{t_{n,1} + t_{n,2}}{T_0} \quad (5.28)$$

$$(5.29)$$

Thanks to the first order approximation of the capacitor voltage, we can linearly relate the phases duration to $V_{th}(t)$.

$$T_i = \frac{V_{th}(t_i) - V_{th}(t_{i-1})}{\alpha_i} \quad (5.30)$$

Assuming that the noise voltages are relatively small compared to the voltage swing V_{hys} of the capacitor signal, we can consider that the transition time events in the noisy oscillator are approximately equal to the ones in a noise-free oscillator [40]. Consequently, the voltage thresholds are approximately equal in the noisy and noise-free oscillators. This is valid only if Eq. 5.32 is respected, which means that the frequency of noise components should be low compared to the maximum possible jitter [40].

$$V_{th}(t_{\text{noisy}}) \approx V_{th}(t_{\text{noise-free}}) \quad (5.31)$$

$$\frac{\delta V_{th}(t)}{\delta t} \cdot (t_{\text{noisy}} - t_{\text{noise-free}}) \ll V_{th}(t_1) - V_{th}(t_0) \quad (5.32)$$

The instantaneous value of the voltage thresholds in the noisy oscillator can be expressed as the ideal value with additive voltage noise. Consequently, the phase duration T_i can be expressed from Eq. 5.30 by introducing directly the additive noise resulting in Eq. 5.34. The relative variation of the two phases duration can then be evaluated as in Eqs. 5.36 and 5.37. The notation of the time-instant t_{nf} corresponds to the noise-free oscillator and the notation t_n corresponds to the noisy oscillator.

$$V_{th}(t_n) = V_{th}(t_{nf})_{ideal} + v_n(t_{nf}) \quad (5.33)$$

$$T_i + t_{n,i} = \frac{V_{th}(t_{i,nf})_{ideal} + v_n(t_{i,nf}) - V_{th}(t_{i-1,nf})_{ideal} - v_n(t_{i-1,nf})}{\alpha_i} \quad (5.34)$$

$$t_{n,i} = \frac{v_n(t_{i,nf}) - v_n(t_{i-1,nf})}{\alpha_i} \quad (5.35)$$

$$\frac{t_{n,1}}{T_1} = \frac{v_n(t_{1,nf}) - v_n(t_{0,nf})}{V_{hys}} \quad (5.36)$$

$$\frac{t_{n,2}}{T_2} = \frac{v_n(t_{2,nf}) - v_n(t_{1,nf})}{V_{hys}} \quad (5.37)$$

From Eq. 5.28, the relative total period variation can be expressed as a function of the instantaneous noise voltages leading to Eq. 5.38. By expressing the phase periods as functions of the duty cycle, we get Eq. 5.41 and replacing by 50%, we get Eq. 5.42.

$$\frac{t_n}{T_0} = \frac{1}{T_0} \cdot \left(T_1 \frac{v_n(t_{1,nf}) - v_n(t_{0,nf})}{V_{hys}} + T_2 \frac{v_n(t_{2,nf}) - v_n(t_{1,nf})}{V_{hys}} \right) \quad (5.38)$$

$$T_1 = \theta \cdot T_0 \quad (5.39)$$

$$T_2 = (1 - \theta) \cdot T_0 \quad (5.40)$$

$$\frac{t_n}{T_0} = \frac{1}{V_{hys}} \cdot (-\theta \cdot v_n(t_{0,nf}) + v_n(t_{1,nf}) - (1 - \theta) \cdot v_n(t_{2,nf})) \quad (5.41)$$

$$p_{j,norm} = \frac{t_n}{T_0} = \frac{1}{V_{hys}} \cdot \left(-\frac{v_n(t_{0,nf})}{2} + v_n(t_{1,nf}) - \frac{v_n(t_{2,nf})}{2} \right) \quad (5.42)$$

From Eq. 5.41, we see that the relative total period variation is a combination of noise samples at different time instants [40]. A continuous-time filter can be built around the last equation by shifting the samples to the back end of the system [40]. The filter resulting from this operation is expressed in Eq. 5.46. It allows evaluating the relative period jitter from the time-domain noise voltages samples.

$$t_{2,nf} \equiv t \quad (5.43)$$

$$t_{1,nf} \equiv t - T_2 = t - 0.5 \cdot T_0 \quad (5.44)$$

$$t_{0,nf} \equiv t - T_0 \quad (5.45)$$

$$p_{j,norm}(t) = \frac{t_n}{T_0}(t) = \frac{1}{V_{hys}} \cdot \left(-\frac{v_n(t - T_0)}{2} + v_n(t - 0.5 \cdot T_0) - \frac{v_n(t)}{2} \right) \quad (5.46)$$

Finally, the magnitude of the relative period jitter should be evaluated based on the noise frequency spectrum as noise sources are expressed in terms of Power Spectral

Density (PSD). This can be done by taking the Fourier transform of the continuous-time filter leading to Eq. 5.48.

$$|P_{j,norm}(j\omega_n)| = \frac{1}{V_{hys}} \cdot \left| -\frac{e^{-j\omega_n T_0}}{2} + e^{-j\omega_n \frac{T_0}{2}} - \frac{1}{2} \right| \quad (5.47)$$

$$= \frac{2}{V_{hys}} \cdot \sin\left(\frac{\pi \omega_n}{2 \omega_0}\right)^2 \quad (5.48)$$

For a noise source of PSD $S_v(f)$ at the input of the comparator, assuming a one-pole system of bandwidth BW , the RMS period jitter of the relaxation oscillator can be evaluated using Eq. 5.49 [12].

$$\sigma_{pj} = \sqrt{\int_0^{BW} |P_{j,norm}(jf)|^2 S_v(f) df} \quad (5.49)$$

Noise sources We now have a model allowing us to estimate the period jitter resulting from the operation of the relaxation oscillator with known noise sources. The circuit from [22] is re-drawn in Fig. 5.4 with the noise sources from the resistors noted $\overline{v_{n1}^2}, \overline{v_{n2}^2}, \overline{v_{n3}^2}$ and $\overline{v_{n4}^2}$, and the input-referred noise source of the comparator noted $\overline{v_{nc}^2}$. The voltage noise sources of the resistors are characterized by their RMS noise voltage which can be calculated using Eq. 5.50 [16].

$$\overline{v_R^2} = 4 \cdot k \cdot T \cdot R \cdot \Delta f \quad (5.50)$$

In order to exploit the elaborated model, we have to bring all the noise sources at the input node P of the comparator. As all the resistor noise sources are uncorrelated, we can use the superposition theorem to evaluate their individual contribution to the output signal [16]. These contributions are given in Eqs. 5.51 to 5.55. Finally, the noise sources can be referred at the input using Eq. 5.56.

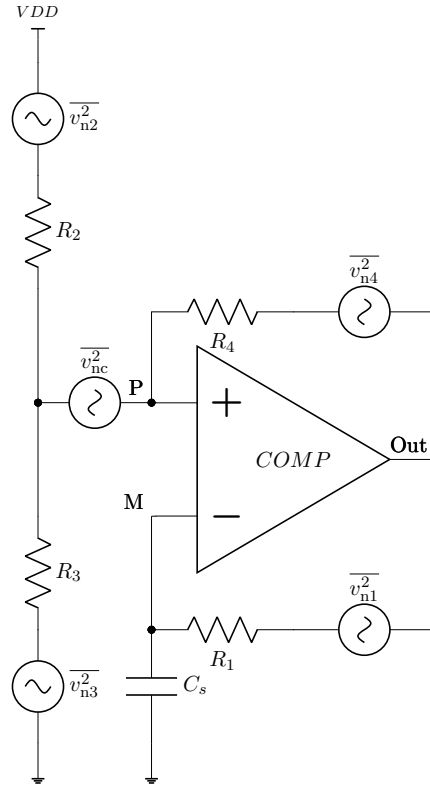


Figure 5.4: Circuit diagram - Relaxation Oscillator with noise sources

$$\frac{V_{out}}{\sqrt{v_{n1}^2}} = \frac{-R_3 \cdot R_4 - R_2 \cdot R_4 - R_2 \cdot R_3}{R_3 \cdot R_4 + R_2 \cdot R_4 - j\omega \cdot (R_1 \cdot R_2 \cdot R_3 \cdot C_s)} \quad (5.51)$$

$$\frac{V_{out}}{\sqrt{v_{n2}^2}} = \frac{R_3 \cdot R_4 + j\omega \cdot (R_1 \cdot R_3 \cdot R_4)}{R_3 \cdot R_4 + R_2 \cdot R_4 - j\omega \cdot (R_1 \cdot R_2 \cdot R_3 \cdot C_s)} \quad (5.52)$$

$$\frac{V_{out}}{\sqrt{v_{n3}^2}} = \frac{R_2 \cdot R_4 + j\omega \cdot (R_1 \cdot R_2 \cdot R_4)}{R_3 \cdot R_4 + R_2 \cdot R_4 - j\omega \cdot (R_1 \cdot R_2 \cdot R_3 \cdot C_s)} \quad (5.53)$$

$$\frac{V_{out}^2}{\sqrt{v_{n4}^2}} = \frac{-R_2 \cdot R_3 - j\omega \cdot (R_1 \cdot R_2 \cdot R_3)}{R_3 \cdot R_4 + R_2 \cdot R_4 - j\omega \cdot (R_1 \cdot R_2 \cdot R_3 \cdot C_s)} \quad (5.54)$$

$$\frac{V_{out}}{\bar{v}_n} = \frac{(R_2 \cdot R_3 + R_3 \cdot R_4 + R_2 \cdot R_4)}{R_3 \cdot R_4 + R_2 \cdot R_4 - j\omega \cdot (R_1 \cdot R_2 \cdot R_3 \cdot C_s)} \quad (5.55)$$

$$+ \frac{j\omega \cdot (C_s \cdot R_1 \cdot R_2 \cdot R_3 + C_s \cdot R_1 \cdot R_3 \cdot R_4 + C_s \cdot R_1 \cdot R_2 \cdot R_4)}{R_3 \cdot R_4 + R_2 \cdot R_4 - j\omega \cdot (R_1 \cdot R_2 \cdot R_3 \cdot C_s)} \quad (5.56)$$

The total input-referred noise due to the resistors $\overline{v_{ni,total}^2}$ in the relaxation oscillator is expressed using Eqs. 5.57 and 5.58.

$$\overline{V_{out,total}^2} = \overline{v_{n1}^2} \cdot \left(\frac{V_{out}^2}{v_{n1}^2} \right) + \overline{v_{n2}^2} \cdot \left(\frac{V_{out}^2}{v_{n2}^2} \right) + \overline{v_{n3}^2} \cdot \left(\frac{V_{out}^2}{v_{n3}^2} \right) + \overline{v_{n4}^2} \cdot \left(\frac{V_{out}^2}{v_{n4}^2} \right) \quad (5.57)$$

$$\overline{v_{ni,total}^2} = \overline{V_{out,total}^2} \cdot \frac{\overline{v_n^2}}{\overline{V_{out}^2}} \quad (5.58)$$

5.2 Circuit Design

As stated in Chapter 1, the goal of this work is to design a low-power CDC with relaxed specifications as it is a first design. The specifications of the CDC were set on the basis of the state-of-the-art and considering a typical capacitive sensor designed at UCLouvain [2].

5.2.1 System Specifications

The system specifications are the starting point of a top-down design, these characteristics define all the constraints of the building blocks of the system. These specifications were defined as a mix of ranges corresponding to results observed in the state-of-the-art of time-domain CDC.

The full range of the converter was set based on a humidity capacitive sensor from [2] designed at UCLouvain. The effective resolution was set to 8 bits, this represents a low specification according to the goal of this work. The measurement time was set to a range from 6.86 ms to 17.5 ms according to the maximum and minimum conversion times of time-domain CDCs in Table 2.1. The power consumption was set to a range from 1 μ W to 20 μ W also according the extremes of Table 2.1 excluding the design from [22]. Following the same methodology, the range for the FoM was set from 0.01 pJ to 680 pJ per conversion step and the area was set to a range from 0.002 mm² to 0.1 mm². Table 5.1 summarizes the ranges and the fixed system specifications.

Full Range [pF]	300	Maximize
ENOB [bits]	8	Maximize
Measurement Time [ms]	0.02 - 17.5	Minimize
VDD [V]	1.2 - 1.8	Low-power
Power [μ W]	1 - 20	Minimize
FoM [pJ/conv-step]	0.01 - 680	Minimize
Area [mm ²]	0.002 - 0.1	Minimize

Table 5.1: Specifications ranges - Based on state-of-the-art

5.2.2 Design Specifications

The design specifications are the next following key steps in a top-down methodology as they directly relate the system specifications into parameters and design rules for the building blocks of the system. These specifications comprise the conversion function of the relaxation oscillator from which results the jitter constraint of the oscillator, followed by the values of the resistors and the characteristics of the comparator.

5.2.2.1 Jitter Constraint and measurement time

In Section 2.2.3 of Chapter 2, we showed that the period jitter of a given CCO was bounded by the period at $C_{R,rms}$ in Eq. 2.22. In our design, this period is given by the relaxation oscillator, it is thus necessary to fix the measurement time for evaluating the jitter design constraint.

Measurement time As explained in Section 2.2 of Chapter 2 about time-domain conversion, the full-range of capacitance directly relates to the full-range time period of the CCO which is the minimum measurement time. Also, we showed in Section 2.2.2 of the same chapter that the minimum clock period of the CCO T_{LSB} leads to a constraint of maximum reference clock period of the TDC. Finally, the measurement time specification of our design was previously set to a range of typical state-of-the-art values. In order to fix the measurement time, we decided to start from a typical clock frequency of an IoT micro-controller family on the market, this is the PIC18-Q43 from Microchip. These micro-controllers work at a clock frequency of 64 MHz [31].

According to Eq. 2.14, this typical clock frequency value leads to a maximum boundary for the LSB frequency expressed in Eq. 5.60. Considering an effective resolution of 8 bits, it also gives the maximum frequency for the full-range as expressed in Eq. 5.61, the corresponding period is 8 μ s which is below the minimum measurement time of 20 μ s given in Table 5.1. This means that the range specified previously already provides margin for the system.

$$f_{LSB} \leq \frac{1}{2} \cdot f_{MCU} \quad (5.59)$$

$$f_{LSB} \leq 32 \text{ MHz} \quad (5.60)$$

$$f_{FR} \leq 125 \text{ kHz} \quad (5.61)$$

An important element for defining the measurement time is the bandwidth of the sensed signal. The application of the sensor from [2] uses a sampling time of 10 ms which corresponds to a frequency of 100 Hz. Also, in any sampling system, the Nyquist criterion imposes the sampling frequency to be at least twice the measurement bandwidth [32].

$$f_{FR} \geq 2 \cdot \text{BW} \quad (5.62)$$

Finally, the measurement time was set to 0.415 ms or 2.4 kHz. This value gives some margin in terms of signal bandwidth still being in the range defined in previous section, and respecting the constraint linked to the micro-controller reference clock frequency. As the period function of the relaxation oscillator is linear, the coefficient of conversion from capacitance to time, or gain of the CCO, can be evaluated as in Eq. 5.63.

$$T_{FR} = K_{CCO} \cdot C_{FR} \quad (5.63)$$

$$K_{CCO} = \frac{0.415 \text{ ms}}{300 \text{ pF}} = 1.4 \text{ } \mu\text{s pF}^{-1} \quad (5.64)$$

Jitter constraint As we know have the gain of the CCO, we can evaluate the jitter constraint. The resolution capacitance is given in Eq. 5.65 from which we get the RMS resolution capacitance in Eq. 5.66. The equivalent period is then evaluated using the CCO coefficient in Eq. 5.67. Finally, the RMS period jitter constraint is given in Eq. 5.68.

$$C_R = \frac{C_{FR}}{256} = 1.172 \text{ pF} \quad (5.65)$$

$$C_{R,rms} = \frac{C_R}{\sqrt{12}} = 338.3 \text{ fF} \quad (5.66)$$

$$T_{R,rms} = K_{CCO} \cdot C_{R,rms} = 473.6 \text{ ns} \quad (5.67)$$

$$\sigma_{pj,rms} \leq 473.6 \text{ ns} \quad (5.68)$$

We know have two important design specifications of the CCO, the conversion factor K_{CCO} of $1.4 \text{ } \mu\text{s pF}^{-1}$ from the measurement time and the maximum RMS period jitter of 473.6 ns.

5.2.2.2 Resistors of the CCO

Resistors values The values of the resistors are constrained by the rule of Eq. 5.18 to have a 50% duty-cycle output square-wave. Considering this rule, the value of R_1 is directly fixed from the previously defined conversion factor K_{CCO} as shown in Eq. 5.71.

$$K_{CCO} = R_1 \cdot \ln \left(\frac{K_H}{K_L} \cdot \frac{K_L - 1}{K_H - 1} \right) \quad (5.69)$$

$$= R_1 \cdot \ln(4) \quad (5.70)$$

$$R_1 = \frac{K_{CCO}}{\ln(4)} = 1 \text{ M}\Omega \quad (5.71)$$

The choice of the value of the other resistors is not as obvious. These resistors are constrained by the rule of Eq. 5.18 so their values should be the same which already removes some degrees of freedom. Their purpose is to provide two voltage thresholds

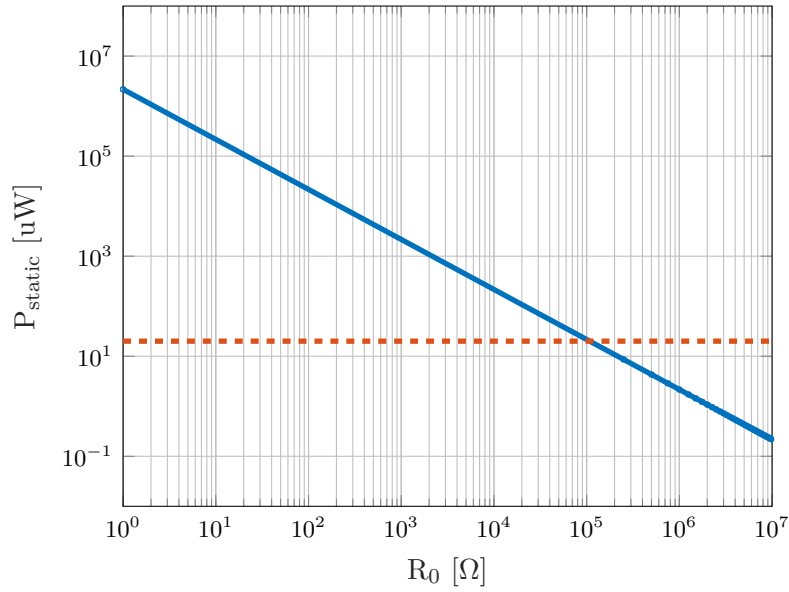


Figure 5.5: Static power vs. R_0 - $V_{DD} = 1.8$ V

allowing to add an hysteresis to the comparator thanks to the variable voltage divider formed. Consequently, these resistors dissipate a static power which should be limited to respect the power limitation defined previously (see Table 5.1). The plot in Fig. 5.5 shows the static power dissipated by the resistor divider depending on the R_0 value computed using Eq. 5.74. The orange dashed line represents 20 μW limitation. This allows use to further constrain R_0 to a minimum of 100 k Ω .

$$P_{static,divider} = \frac{U^2}{R_{eq}} \quad (5.72)$$

$$P_{static,divider} = \frac{V_{DD}^2}{R_0 + R_0 \parallel R_0} \quad (5.73)$$

$$P_{static,divider} = \frac{V_{DD}^2}{0.5 \cdot R_0} \quad (5.74)$$

Resistors Noise Following what was shown in Fig. 5.5, one would choose a maximum value for R_0 to limit the static power dissipated to a negligible constant. However, the jitter design constraint defined previously implies that noise sources of the system should be limited to reach the effective resolution. Thus, we will use the jitter constraint to define an upper boundary for the resistors values. The graph in Fig. 5.6 represents the RMS period jitter estimated from Eq. 5.49 considering an ideal noiseless comparator. The orange dashed line represents the period jitter constraint. As this result does not consider the input-referred noise of the comparator, it was decided to fix the value R_0 at 1 M Ω leaving some margin.

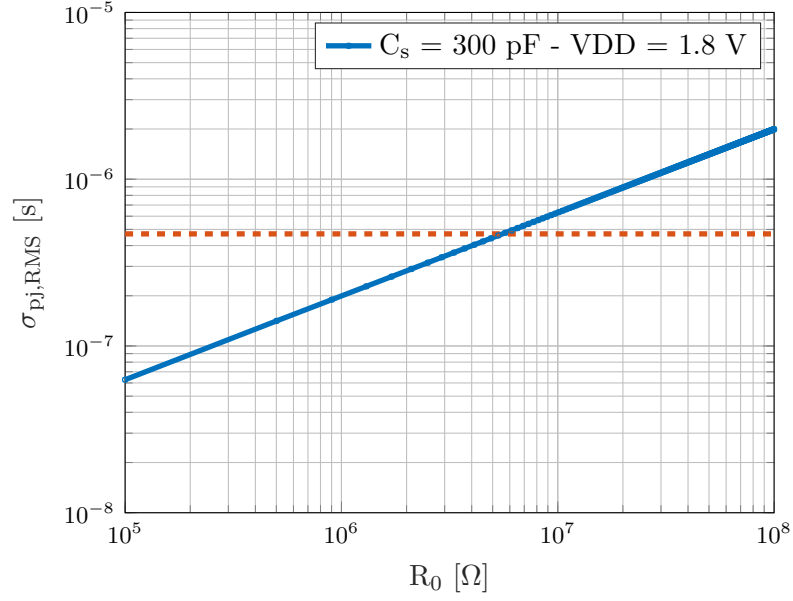


Figure 5.6: Period Jitter vs. R_0 - VDD = 1.8 V

5.2.2.3 Comparator Parameters

We defined the values of all the resistances based on the measurement time, the power consumption constraint and the jitter constraint. The last element we have to specify is the comparator. The parameters to specify for the comparator are the Unity-Gain Bandwidth (GBW), the input voltage offset and the driving capabilities.

Offset Voltage One of the advantage of the RC relaxation oscillator from [22] is that it is robust against offset voltage of the comparator. We explained in Section 5.1.3 that in first approximation, the phase duration T_i could be expressed as a function of the voltage thresholds as recalled in Eq. 5.75. A voltage offset V_{os} in the comparator will affect these voltage thresholds so that they will be shifted as expressed in Eq. 5.76. As the period duration is proportional to the difference of the voltage thresholds, the offset has no effect on the output period as shown in Eq. 5.77. This is illustrated in Fig. 5.7.

$$T_i = \frac{V_{th}(t_i) - V_{th}(t_{i-1})}{\alpha_i} \quad (5.75)$$

$$V_{th}(t) = V_d(t) + V_{os} \quad (5.76)$$

$$T_i = \frac{V_d(t_i) + V_{os} - V_d(t_{i-1}) - V_{os}}{\alpha_i} \quad (5.77)$$

Unity-Gain Bandwidth In order to estimate the required GBW of the comparator, we simulated the relaxation oscillator from Fig. 5.1 using a comparator model. This

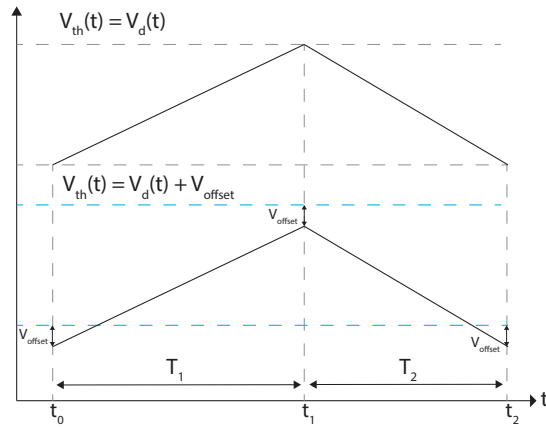


Figure 5.7: Offset voltage - Illustration

comparator model comprises an ideal comparator with infinite GBW, no offset and unlimited driving capabilities. At the output of this one, a pole was added to emulate a single pole system and finally, two ideal inverters were used at the output. The model is shown in Fig. 5.8.

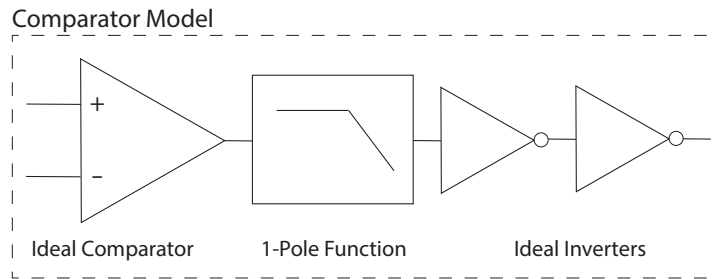


Figure 5.8: Comparator Model for GBW Evaluation

The plot in Fig. 5.9 shows the measured output frequency of the circuit simulated for a capacitor C_s fixed at the value of the LSB capacitance C_R . The yellow dashed line represents the target frequency. We decided to fix the GBW constraint to a minimum of 100 MHz to have some margin.

Driving Capabilities The output of the comparator is responsible of driving 2 elements of the circuit, the capacitor C_s through the resistor R_1 with current i_{C_s} and the resistor R_4 with current i_{R_4} . Also, the circuit will in practice be connected to a TDC, consequently there will be an additional parasitic capacitance C_p at the output node due to the routing tracks and the input capacitance of the TDC, this capacitance will have to be driven by a current i_{C_p} . The output stage of the comparator will be in the form of a buffer which switches between the two supply voltages, it can be modelled by two ideal switches.

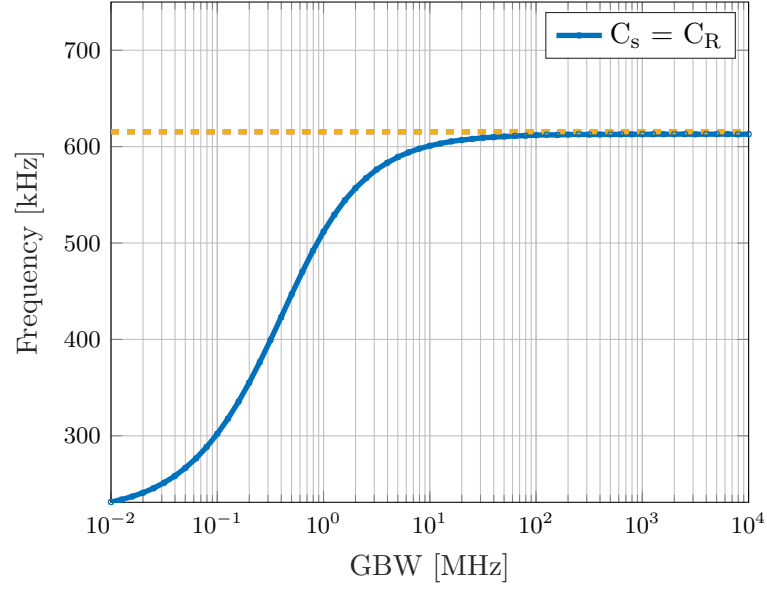


Figure 5.9: Output Frequency vs. GBW - $V_{DD} = 1.8\text{ V}$

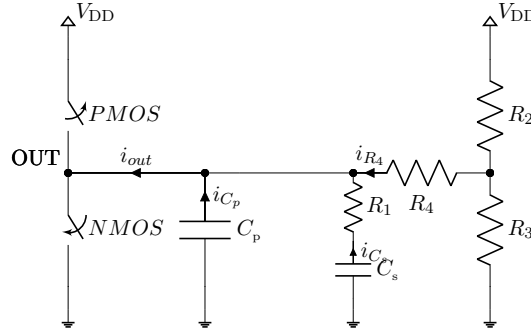


Figure 5.10: Circuit diagram - Model Output stage of Comparator

The total output current is expressed in Eq. 5.78 from Kirchhoff's Current Law (KCL). The average current i_{C_s} for the capacitance is computed from the basic capacitor relationship considering a voltage variation of $V_{hys} = V_{TH} - V_{TL}$ and a time variation of $\frac{T_0}{2}$. By simplifying the capacitance value, it results in Eq. 5.80. It represents the average current in the capacitance during one phase of charge or discharge¹. The charge/discharge current in the parasitic capacitance C_p is computed so that the charge/discharge time of this one is 1% of the smallest output period of the CCO as given in Eq. 5.81. Finally, the static current of resistors R_4 is computed from the basic voltage divider relationships resulting in Eq. 5.82.

¹This is a first order approximation as we consider a linear voltage curve.

$$i_{out} = i_{C_p} + i_{C_s} + i_{R_4} \quad (5.78)$$

$$i = C \cdot \frac{\delta V}{\delta T} \quad (5.79)$$

$$i_{C_s,avg} = C_s \frac{\Delta V}{\Delta T} = \frac{2 \cdot V_{hys}}{R_1 \ln(4)} \quad (5.80)$$

$$i_{C_p} = C_p \cdot \frac{VDD}{0.01 \cdot T_{min}} \quad (5.81)$$

$$i_{R_4} = \frac{VDD}{3 \cdot R_0} \quad (5.82)$$

The total output current was computed using all the parameters defined previously and considering a parasitic capacitance of 3 pF and is given in Table 5.2. The value of the parasitic capacitance was chosen to encompass various use cases like the PCB traces or IC layout parasitic capacitance.

$i_{C_s,avg}$ [uA]	0.86
i_{C_p} [uA]	332.4
i_{R_4} [uA]	0.6
i_{out} [uA]	334

Table 5.2: Total output current - $C_p = 3$ pF

5.2.2.4 Summary of the Design Specifications

All the design specifications evaluated are summarized in Table 5.3. The offset voltage is considered not relevant as the circuit functionality theoretically does not suffer from it, but it will have to be verified in simulation during design.

5.2.3 Design of the Comparator

The main analog block of the RC relaxation oscillator is the continuous-time voltage comparator which allows switching between the states of charge and discharge of the

Comparator Parameter	Value
Offset voltage	Not relevant
GBW [MHz]	100
Output Current [uA]	334
Resistors	Value
R_1 [MΩ]	1
R_2, R_3 and R_4 [MΩ]	1

Table 5.3: Design Specifications Summary

capacitor. This kind of comparator can be realized from a basic uncompensated CMOS operational amplifier [15].

The complete structure used for the design of this comparator is shown in Fig. 5.11 where the total capacitance of each node are represented. It comprises an input differential pair with active load followed by two CMOS inverters. The input differential pair serves at amplifying the voltage difference $V_{In+} - V_{In-}$, the inverters serve at driving the output load.

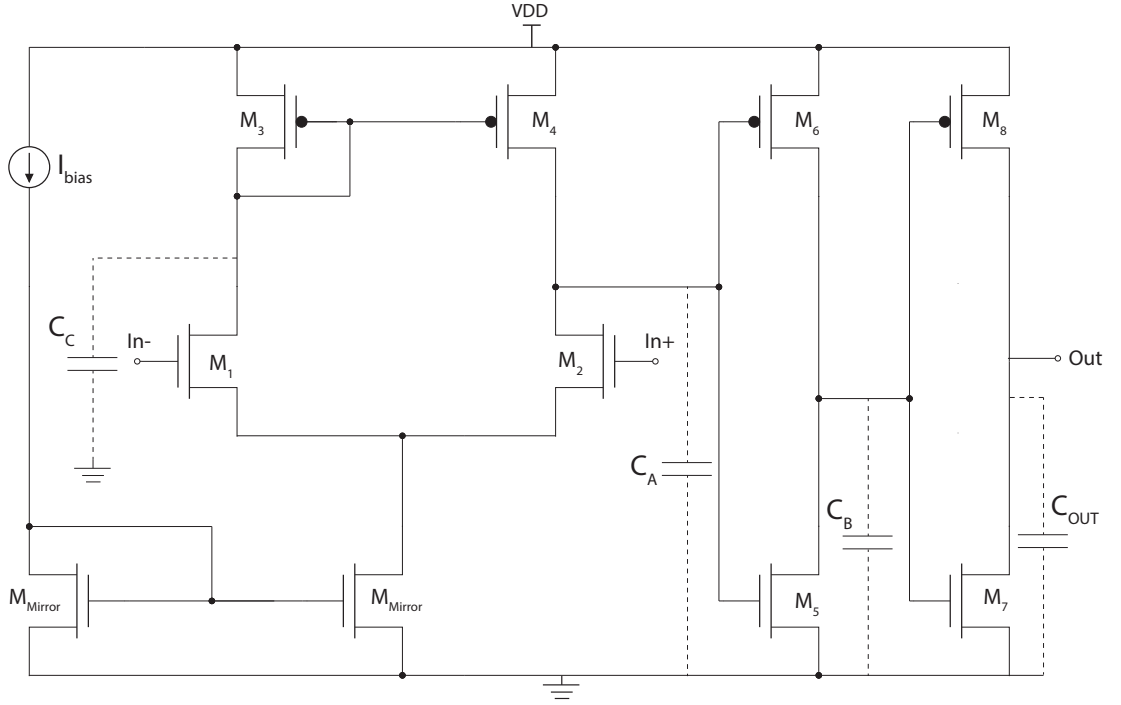


Figure 5.11: Circuit Diagram - Comparator

5.2.3.1 Design methodology

Output Current The output current specification constraints the design of the two inverters. Specifically, the last inverter has to be sized so that it can provides the output current specified. The intermediary inverter serves at providing a progressive driving strength to limit the load capacitance C_A . The sizing of the stages is performed using the current equation of MOS transistor in saturation leading to Eq. 5.84. The current for the intermediary inverter I_{int} is estimated from Eq. 5.85 where C_B is the equivalent load capacitor of the node and T_{min} is the minimum output period of the CCO.

$$I_D = \frac{1}{2} \cdot k_{n,p} \frac{W}{L} (V_{gs} - V_{th})^2 \quad V_{ds} > V_{gs} - V_{th} \quad \text{Saturation} \quad (5.83)$$

$$\frac{W}{L} = \frac{2 \cdot I_{out}}{k_{n,p} (V_{gs} - V_{th})^2} \quad (5.84)$$

$$I_{int} = C_B \cdot \frac{VDD}{0.01 \cdot T_{min}} \quad (5.85)$$

GBW The GBW specification defined in the previous section constraints the design of the input differential pair. This parameter is defined as the frequency at which the gain reaches 0 dB. The frequency response expression of the differential pair with active load is given in Eq. 5.86 [34].

$$A(f) = \frac{A_0}{1 + \frac{jf}{f_{p1}}} \cdot \left(\frac{1}{1 + \frac{jf}{f_{p2}}} + 1 \right) \quad f_{p1} = \frac{1}{2\pi \cdot r_{o4} \parallel r_{o2} C_A} \quad f_{p2} = \frac{g_{m4}}{2\pi \cdot C_C} \quad (5.86)$$

If the *mirror* capacitor C_C is small compared to the load capacitance C_A , the system can be approximated as a single pole system of frequency response given in Eq. 5.87. The GBW can be expressed as in Eq. 5.88 based on the stage trans-conductance and output node capacitance C_A .

$$A(f) \approx \frac{2 \cdot A_0}{1 + \frac{jf}{f_{p1}}} \quad \text{if } C_C \ll C_A \quad (5.87)$$

$$GBW = A_0 \cdot f_{p1} = \frac{g_{m1}}{\pi \cdot C_A} \quad (5.88)$$

This load capacitor is the combination of parasitic capacitors from the following inverter stage and differential pair itself as expressed in Eq. 5.89.

$$C_A = C_{DB4} + C_{DB2} + C_{GS5} + C_{GS6} + 2 \cdot C_{GD5} + 2 \cdot C_{GD6} + C_{GD2} \quad (5.89)$$

Finally, this constraint allows to estimate the required trans-conductance of the stage as expressed in Eq. 5.90. The sizing was optimized using simulations once the two inverters were sized and tested.

$$g_{m1} = GBW \cdot \pi \cdot C_A \quad (5.90)$$

Summary The design of the comparator with the final sizing for the UMC-RF 0.18 μm technology is shown in Fig. 5.12. The input differential pair was sized based on the GBW design specification using estimation and simulation, the output inverters were simulated based on the output current specification using estimation based on the technology parameters. The final gain obtained for the differential pair in simulation is shown in Fig. 5.13, the GBW reaches 148 MHz.

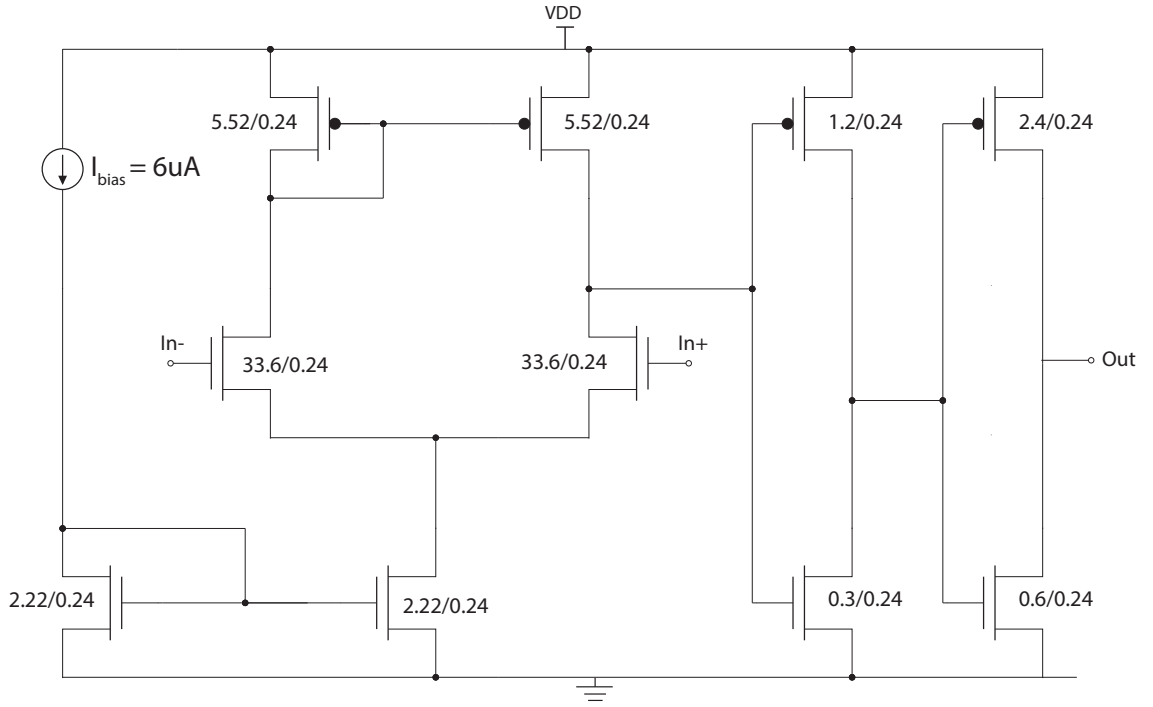


Figure 5.12: Circuit Diagram - Comparator with sizing - W/L in μm

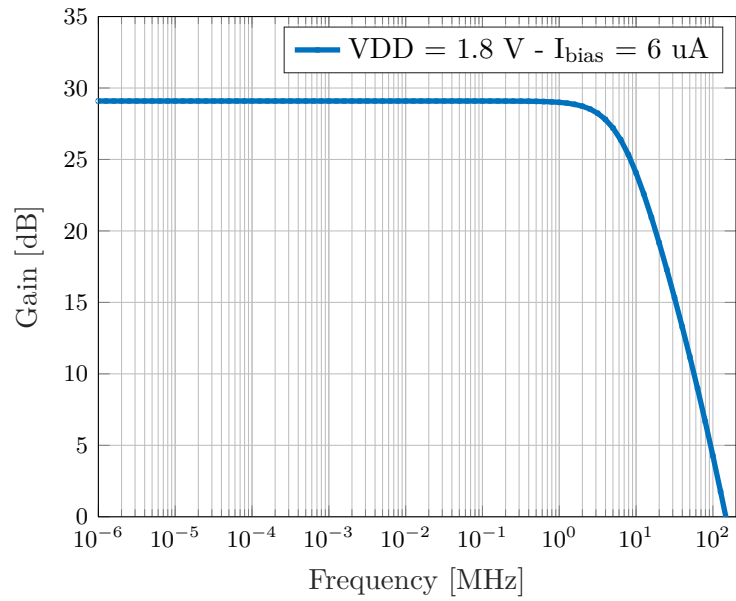


Figure 5.13: Gain vs. Frequency - Differential Pair - $VDD = 1.8 V$

5.2.4 Functionality under Ideal Conditions

5.2.4.1 Output frequency curve

The first simulation of the complete relaxation oscillator was performed in standard transient analysis by measuring the output frequency of the CCO for a sensing capacitor C_S varying between $C_R = 1.172\text{pF}$ and $C_{FR} = 300\text{pF}$. The circuit simulated did not include any noise or mismatch, it corresponds to ideal conditions². The result of the simulation is plotted in Fig. 5.14a with the theoretical estimation. We can observe a small deviation between the two curves, the relative deviation goes between 18% of the ideal output frequency at the minimum capacitance and 5% of the ideal output frequency at the maximum capacitance.

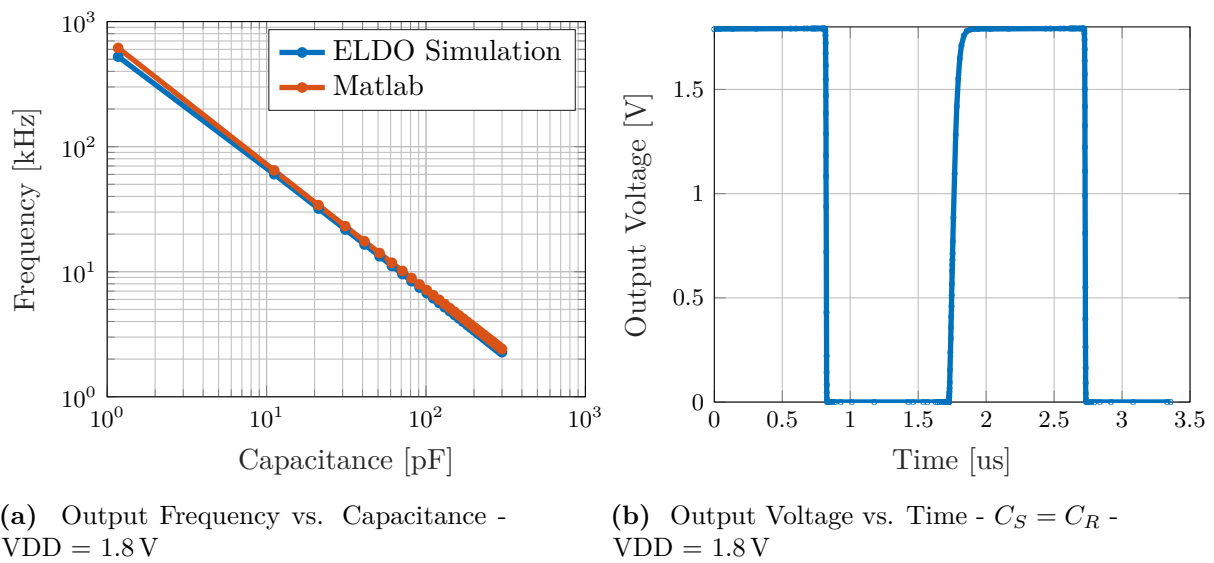


Figure 5.14: Standard Transient Simulation for Ideal Conditions

The graph in Fig. 5.14b represents the output signal of the CCO in the simulation for the minimum capacitance $C_s = C_R$. We can observe an asymmetry between the rising edges and the falling edges leading to the small deviation obtained. This is due to a small imbalance between PMOS and NMOS sizing leading to a small current difference.

Power consumption The simulation also allows us to evaluate the final power consumption of the circuit. The average current measured for the minimum capacitance C_R is 13.3 uA , the average power consumption in this case is $24\text{ }\mu\text{W}$ and the FoM corresponding is 38 pJ per conversion step considering an ENOB of 8 bits. The power consumption is a little bit above the specification of $20\text{ }\mu\text{W}$ but the FoM is well below the limit of 680 pJ per conversion step.

²T = 300 K - Ideal DC supply voltage - Typical process corner

5.2.4.2 Period jitter

The second type of simulation of the CCO was performed using SSTNOISE and Noisetran with ideal conditions of operation, the goal of this simulation is to verify that the system respects the RMS period jitter constraint defined in the specifications.

The graph in Fig. 5.15 represents the accumulated jitter of the CCO simulated with SSTNOISE when the sensing capacitance is at the resolution capacitance, the RMS period jitter is highlighted by the orange dashed line and reaches 2 ns.

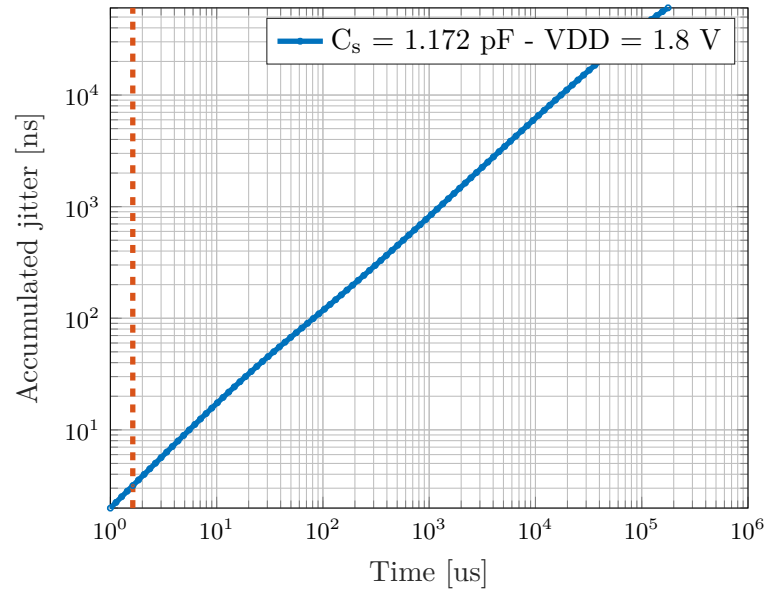


Figure 5.15: Accumulated Jitter vs. Time - $C_S = C_R$ - $V_{DD} = 1.8\text{ V}$

The accumulated jitter simulated for the full-range capacitance was simulated using Noisetran with 200 traces and is shown in Fig. 5.16, the RMS period jitter is the first data point on the graph and reaches 82.2 ns.

As the jitter specification is fixed at 473.6 ns, we can conclude that the circuit respects this limit for all the capacitance range.

5.2.5 Second Order Concerns

In previous section, we showed that the design performs well under ideal conditions. However, it is necessary to verify the functionality and the performance under multiple parameters variation that we call second order concerns.

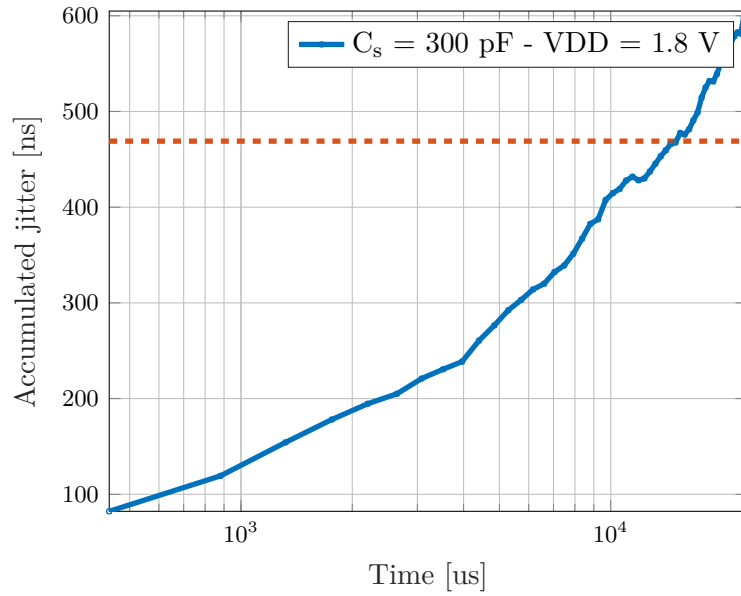


Figure 5.16: Accumulated Jitter vs. Time - $C_S = C_{FR}$ - $V_{DD} = 1.8\text{ V}$

5.2.5.1 Operation under PVT variations

The first variations simulated are the so-called Process-Voltage-Temperature (PVT) variations. The process corners represent the extreme parameters variations that can occur during semiconductor fabrication on a silicon wafer [5]. The design kit provided for the technology used in this design (UMC-RF $0.18\text{ }\mu\text{m}$) allows the simulation of 3 process corners namely *TT* for typical, *SS* for slow and *FF* for fast. The voltage variations were considered around 10% of the nominal supply voltage (1.8 V) and the temperatures were tested for -40°C , 25°C and 85°C .

The simulation was performed setting the sensing capacitance at the resolution capacitance. The goal is to ensure that the output period deviation is below half of the nominal output period which is $1.62\text{ }\mu\text{s}$ or 615.5 kHz , thus, the output frequency should remain between 410.3 kHz and 1.23 MHz . The graphs in Fig. 5.17, 5.18 and 5.19 show the results of the simulation. The output frequency remains in the boundaries for typical and fast process corners. The huge variations are mainly observed between the temperatures at each process and between all the processes, the variation due to the supply voltage is small as expected for a relaxation oscillator. The deviation obtained in slow corner can be reduced using calibration, we will see in Section 5.3 a calibration method that will allow us to do so.

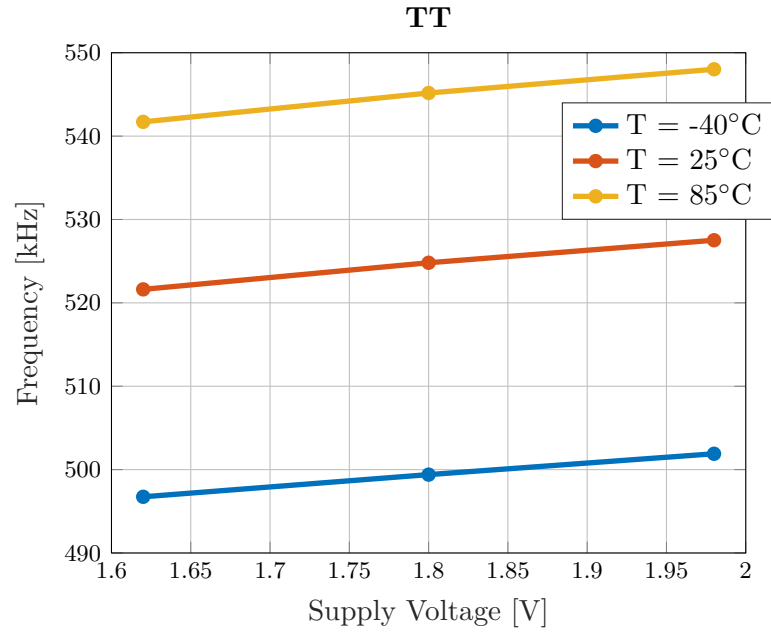


Figure 5.17: Output frequency vs. PVT - Process = TT - $C_S = C_R$ - VDD = 1.8 V

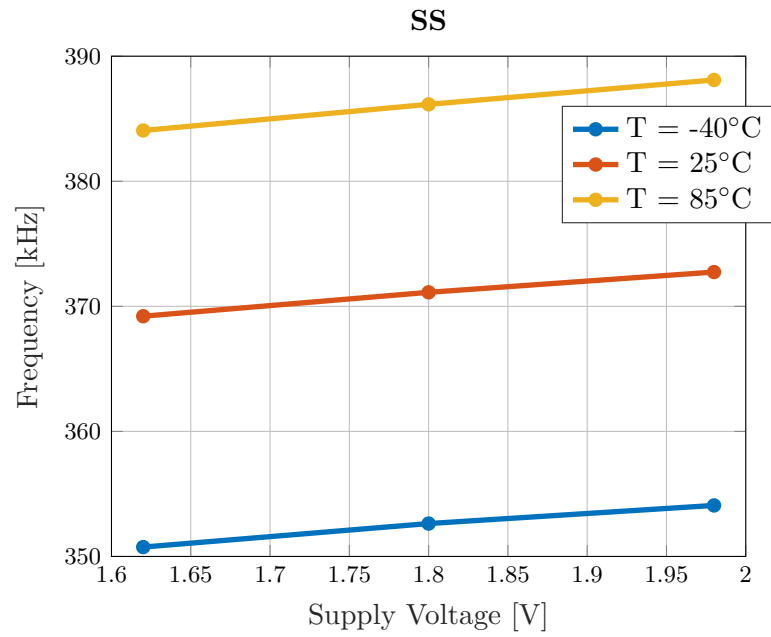


Figure 5.18: Output frequency vs. PVT - Process = SS - $C_S = C_R$ - VDD = 1.8 V

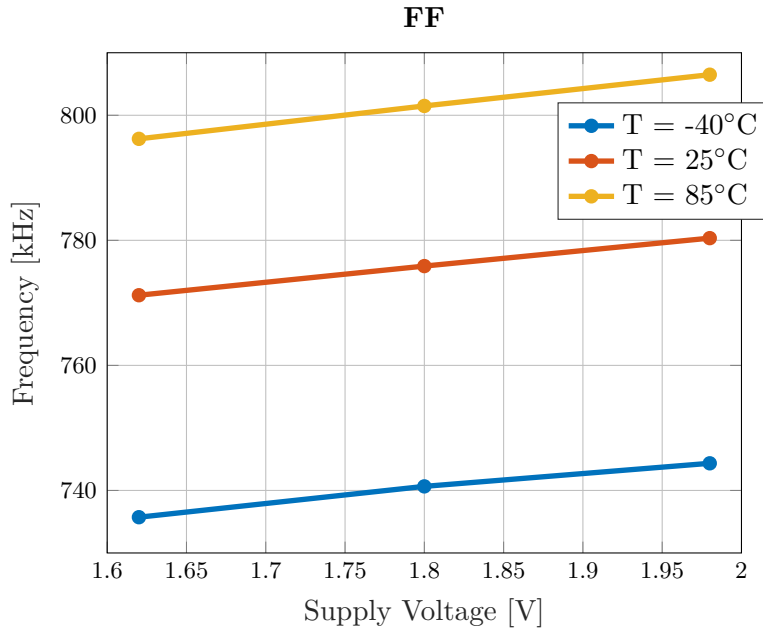


Figure 5.19: Output frequency vs. PVT - Process = FF - $C_S = C_R$ - VDD = 1.8 V

5.2.5.2 Device variations and mismatch

The last second order concerns we had to verify are device variations and mismatch. Indeed, the circuit from [22] comprises multiple resistors that serve at fixing the switching voltage thresholds and the output period, thus, variations in the value of these ones may disturb the performance of the system. Also, the comparator is based on a differential pair with active load and mismatch in this stage lead to input voltage offset [34]. Even if we showed that this circuit is robust against this non-ideality in theory, it is still necessary to verify this robustness in simulation.

These non-idealities are evaluated using Monte-Carlo simulation, this kind of simulation is based on statistical models provided by the foundry in the design kit of the technology. These models represent the distribution of device physical parameters allowing the simulator to generate sets of samples for each device that are then simulated multiple times. These multiple simulations of the circuit are similar to the *traces* used in transient noise simulations as they represent a *realization* of a random process.

Frequency variation A first Monte-Carlo simulation was performed at the resolution capacitance. This simulation was performed using 500 realizations in classic transient. The histogram of output frequency is plotted in Fig. 5.20, the average output frequency is 525.32 kHz, the standard deviation is 14.92 kHz, the minimum frequency is 484.71 kHz and the maximum frequency is 568.63 kHz. The theoretical frequency for the resolution capacitance being 615.5 kHz, the same verification is done as for PVT variations to ensure

that the output frequency stays between 410.3 kHz and 1.23 MHz. We can conclude that the output frequency respects this constraint at the resolution capacitance.

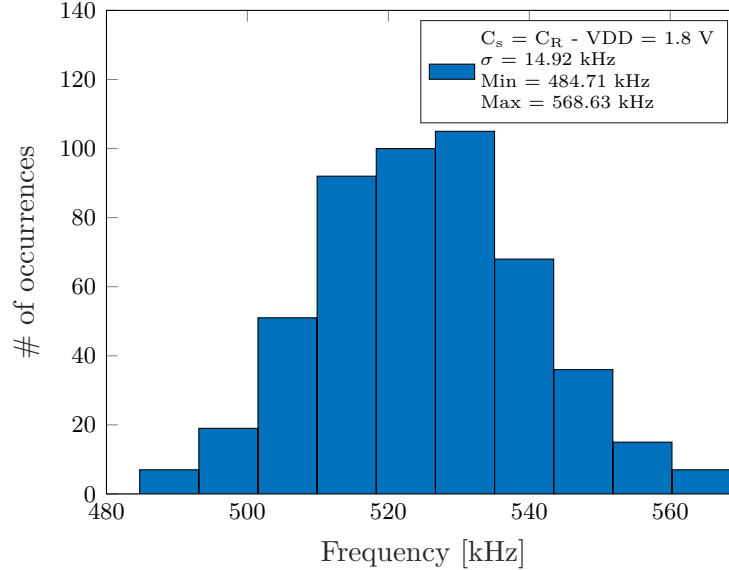


Figure 5.20: Histogram of frequency - Monte-Carlo Simulation

Period jitter Finally, a Monte-Carlo simulation of 100 realizations was performed using SSTNOISE to evaluate the boundaries of the period jitter for the maximum capacitance. The accumulated jitter resulting from this simulation is shown in Fig. 5.21, the green dashed line represents the jitter constraint, the red line is the maximum jitter evaluated while the yellow line is the minimum. The maximum period jitter resulting from this simulation is 100 ns, it is still below the constraint.

5.2.6 Layout of the Circuit

We showed that the design operates properly in non-ideal conditions and is robust against device variations and mismatch. The next step in the top-down methodology we followed is to go from a transistor-level implementation to a physical implementation that can be fabricated, this requires the design of the *layout*. The layout of a semiconductor circuit is a multi-layer representation of the real circuit. Each layer corresponds to a physical element such as the substrate, the oxide, the doped regions but also the various metal layers that are used for interconnections. This step involves the realization of the circuit layout which should be performed by considering physical non-idealities that could be problematic for the design to function.

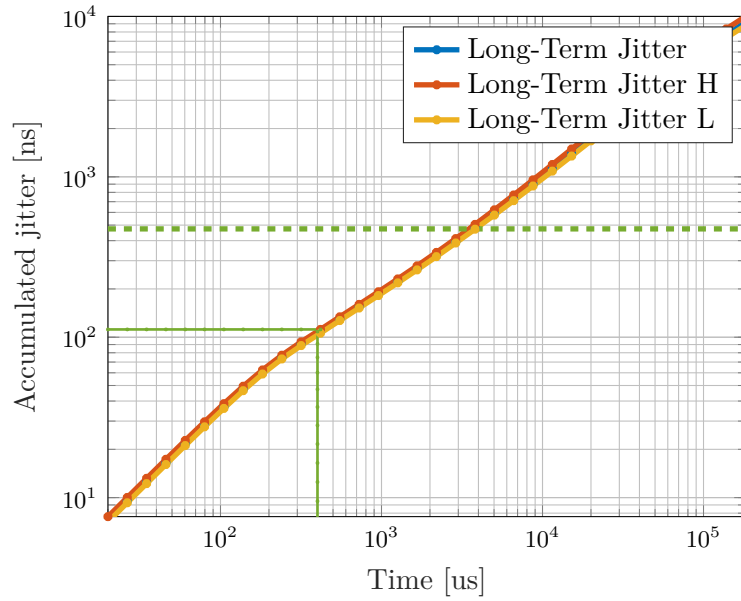


Figure 5.21: Accumulated Jitter vs. Time - $C_S = C_{FR}$ - VDD = 1.8 V - Monte-Carlo Simulation

5.2.6.1 Physical non-idealities

Several physical non-idealities were taken into account during layout design to limit their impact on the behaviour of the CCO.

Gate Noise and Multifinger transistors As our design has a jitter constraint which is linked to the noise generated by different components of the circuit, it is useful to reduce the influence of noise sources when possible. In the case of the transistors, the gate resistance can be seen as a source of thermal noise. A way to reduce the PSD of the gate thermal noise is to divide the transistor in multiple elements leading to a *multifinger* transistor. The use of multifinger transistor helps at reducing the gate thermal noise which is a good practice in low-noise applications [34].

Mismatch and symmetry The mismatch between different elements can lead to disparities in circuit parameters which in turn can lead to undesired non-idealities such as input voltage offset for a comparator. A good practice for reducing mismatch is to ensure symmetry in all related layout entities such as the transistors of the input differential pair or in a current mirror [34].

Well proximity effects and dummies During fabrication, **n-well** regions are formed by implant of **N-types** in areas of silicon, as this implant is not performed at 90 degrees angle, non-uniform doping can happen in n-well regions. The consequence is that

transistor units that are located near the edges of the n-well region will have different characteristics from the units that are in the middle [34]. A way to reduce this effect is to use *dummy* transistors at the ends of the region [26].

Parasitic capacitors and metal traces The metal layers are used for interconnection of various units, these traces combined together with the substrate lead to parasitic capacitors [5]. These unwanted capacitors may degrade the performance of the comparator by increasing the capacitive loads of the stages, but it can also induce an offset capacitance that adds up to the sensing capacitance. Nonetheless, these ones are not critical when they are situated on supply rails as they contribute to the decoupling. Consequently, we took care of limiting the overlapping area of traces and substrate when required to limit unwanted parasitic capacitors.

5.2.6.2 Decoupling capacitors

As explained in Section 4.3.3 of Chapter 4, the package and leads introduce parasitic RLC. The presence of parasitic inductors and resistors may lead to supply and ground bounce that may disturb the functioning of the circuit. In order to prevent this, the use of decoupling capacitors is required.

Evaluation of decoupling capacitors The plots in Fig. 5.22 show the output voltage of the CCO and the instantaneous total current against time, we can observe the peak current at each edge of the output signal. The quiescent current has a value of $12\mu\text{A}$ and is highlighted with the orange dashed line, the peak current has a value of $100\mu\text{A}$. The role of the decoupling capacitor is to provide the amount of charges required for the variation of current due to the peak. The amount of charges is calculated by integrating the peak current over its time duration, at first approximation, this can be done by considering the area of a triangle leading to Eq. 5.91. Considering a maximum voltage variation on the capacitor, the value C_{decoup} is calculated following Eq. 5.93.

$$Q_{\text{peak}} = \frac{1}{2} \Delta i_{\text{peak}} \cdot \Delta T_{\text{peak}} \quad (5.91)$$

$$Q_{\text{decoup}} = C_{\text{decoup}} \cdot \Delta V_{\text{max}} \quad (5.92)$$

$$C_{\text{decoup}} = \frac{\Delta i_{\text{peak}} \cdot \Delta T_{\text{peak}}}{2 \cdot \Delta V_{\text{max}}} \quad (5.93)$$

For a voltage variation of 10% (at 1.8 V), a current variation due to the peak of $88\mu\text{A}$ and a peak duration of 8 ns, the minimum decoupling capacitor is 3.9 pF.

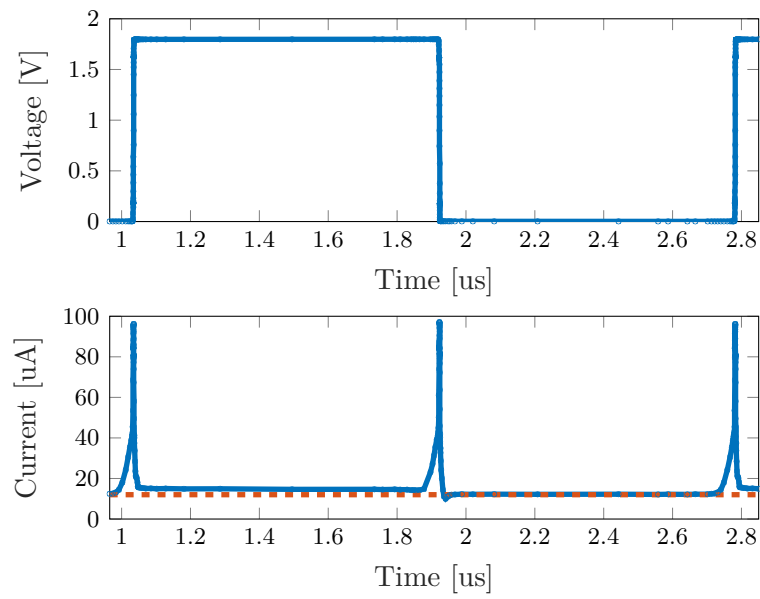


Figure 5.22: Output voltage and current vs. Time - $V_{DD} = 1.8\text{ V}$ - Post-Layout

5.2.6.3 Final layout

The final layout designed is shown in Fig. 5.23. The area of the circuit is 0.01 mm^2 . The final circuit does not integrate the bias current source required for the comparator, an external biasing circuit will be required.

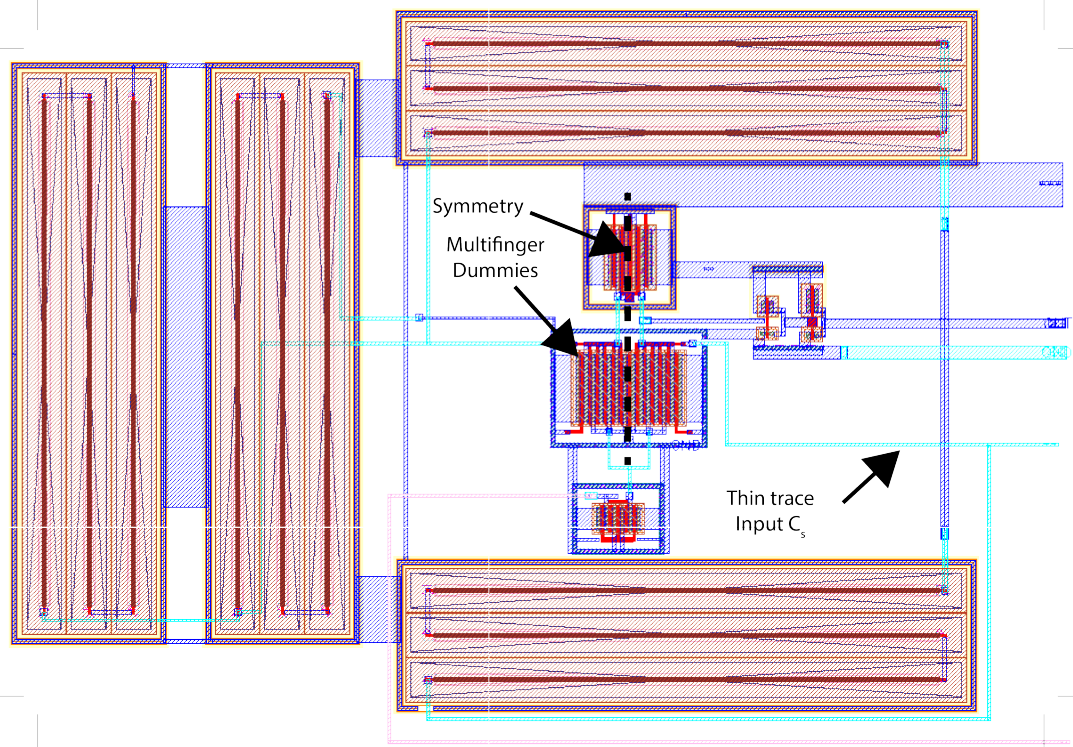


Figure 5.23: Final layout of the CCO

5.2.7 Post-Layout Simulation

As explained previously, the physical implementation is subject to non-idealities, the layout inherently introduces parasitic elements that were not necessarily considered during previous circuit design phase. The elements can be the parasitic resistance of the routing traces or the parasitic capacitors due to the multiple physical layers. In order to estimate these parasitics, the design kit is provided with tools allowing parasitic extraction. An extraction of RC parasitics was performed and simulations were realized with these extractions to ensure the functionality of the interface.

Output frequency curve The plot in Fig. 5.24 shows the output frequency curve simulated in standard transient analysis compared to the theoretical curve. There is a small deviation between the two curves as obtained previously with ideal circuit simulation. In order to determine if this deviation is problematic, we computed the difference in time periods between consecutive values of sensing capacitance which corresponds to the temporal resolution. This measure is similar to the Differential Non-Linearity (DNL) usually measured with ADC, but it is different as we are in the time domain. This

temporal resolution should remain between $0.5 \cdot T_R$ and $1.5 \cdot T_R$. The graph in Fig. 5.25 shows this temporal resolution measured in post-layout as a percentage of T_R and we can notice that it remains close to T_R with a relative deviation of maximum 17%. The resolution period T_R used for the normalization is the one measured in the same simulation for the resolution capacitance C_R , the Eq. 5.94 shows the computation performed.

$$\text{Temporal Resolution}[\%] = \frac{T_{out}(i+1) - T_{out}(i)}{T_{out}(1)} \quad T_{out}(1) = T_{R,\text{post-layout}} \quad (5.94)$$

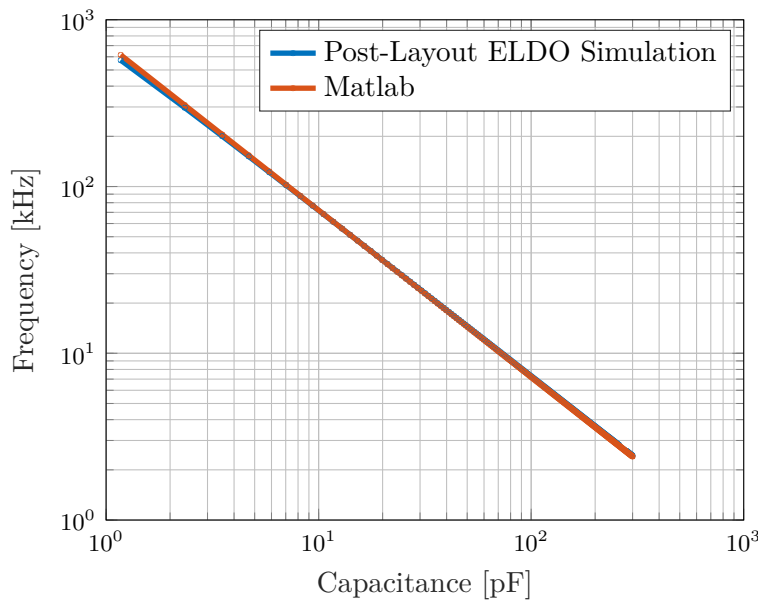


Figure 5.24: Output frequency vs. Capacitance - VDD = 1.8 V - Post-Layout

Period jitter The jitter constraint was also verified using Noisetran, a first simulation was performed using 200 traces at the maximum sensing capacitance. The accumulated jitter extracted from this simulation is shown in Fig. 5.26, the period jitter constraint is shown as an orange dashed line and the actual period jitter is at 70 ns. A second simulation was performed using 500 traces to ensure the reliability of the result, the period jitter extracted from this simulation is 123 ns which is still close to the results obtained in all previous simulations. In the end, we can conclude that the circuit is functional and respects the jitter constraint defined.

5.2.7.1 Supply-Voltage Noise Sensitivity

We motivated our choice of the relaxation oscillator for its theoretical robustness against supply-voltage variations, it is thus useful to verify this assumption using the post-layout

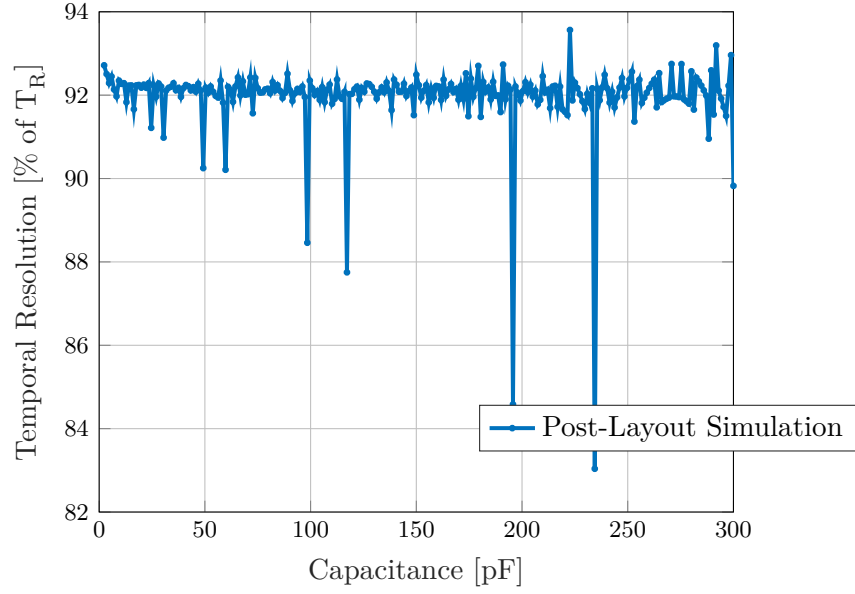


Figure 5.25: Temporal resolution vs. Capacitance - VDD = 1.8 V - Post-Layout

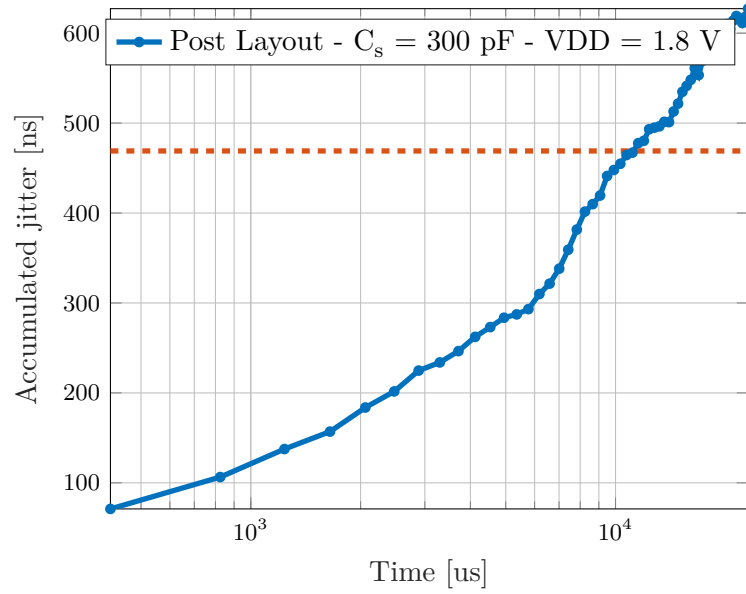


Figure 5.26: Accumulated Jitter vs. Time - $C_S = C_{FR}$ - VDD = 1.8 V - Post-Layout

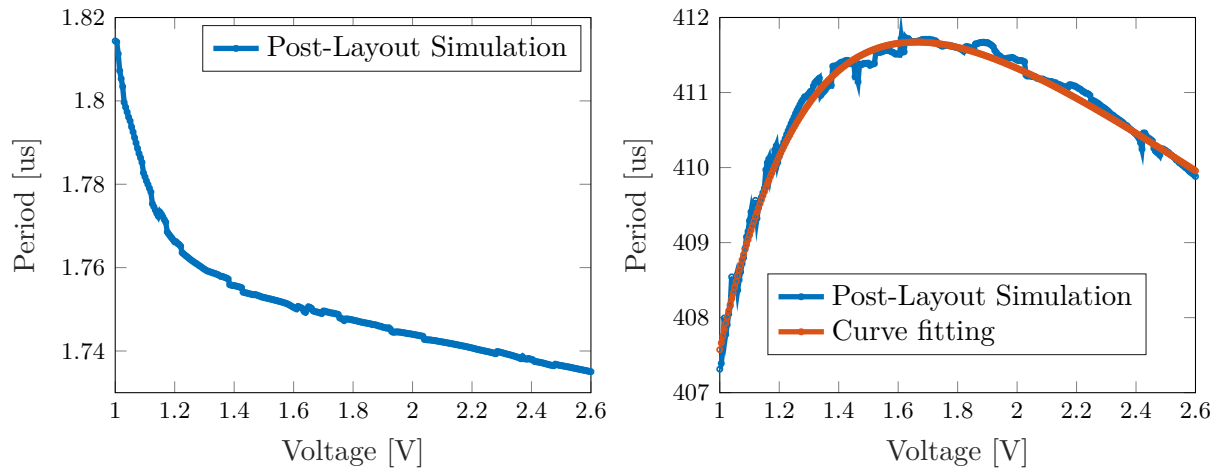
circuit.

In Chapter 4, we estimated the sensitivity of the ring-oscillator circuit against supply-voltage noise on the basis of the output period equation extracted from the simulation.

This sensitivity allowed us to evaluate the RMS period jitter caused by a supply voltage sinusoidal noise.

We simulated the post-layout circuit at the resolution capacitance and the full-range capacitance sweeping the supply-voltage between 1 V and 2.6 V. From these simulations, we extracted the voltage-to-period curves that are shown in Fig. 5.27a and 5.27b.

We can see that the period variation at the full-range capacitance is much higher for a given voltage variation than the period variation at the resolution capacitance. Based on this observation, it was decided to perform a curve fitting on the plot of the full-range capacitance. Following the method explained in Section 4.3.5.1, we built an estimator allowing us to evaluate the maximum allowable sinusoidal noise amplitude considering the jitter constraint.



(a) Period vs. Supply Voltage - $C_s = C_R$

(b) Period vs. Supply Voltage - $C_s = C_{FR}$

Figure 5.27: Standard Transient Simulation - Post-Layout

Assuming there is no noise in the circuit, a supply-voltage sinusoidal noise with an amplitude of 706 mV produces an RMS period jitter of 473.6 ns at the output of the CCO at the full-range capacitance. If we take into account the RMS period jitter of 70 ns produced by random noise that we evaluated on the post-layout circuit simulation at the full-range capacitance, the RMS period jitter due to the supply-voltage noise should remain below 403.6 ns which correspond to a sinusoidal amplitude of 602 mV.

In Section 4.3.5.1, we estimated that the sinusoidal noise affecting the measurements was between 1 mV and 20 mV resulting in a maximum RMS period jitter of 300 ps. In the case of the CCO designed, the estimation results in a maximum RMS period jitter of

13.4 ns. Consequently, we can conclude that the relaxation oscillator designed is at least more robust than the ring-oscillator tested against supply-voltage noise.

5.3 Prospects for Improvement

5.3.1 Additive and Multiplicative errors

We showed in section 5.2.7 that the designed CCO respects the jitter constraint and is robust against supply voltage noise. We also showed that the output frequency curve was slightly deviating from the ideal curve.

For any sensing system characterized by a linear transfer function, errors due to device to device variations or variation of environmental conditions can cause a deviation of the curve from its ideal position. These errors are usually distinguished as additive errors which result in a shift of the curve and multiplicative errors which result in a gain variation of the curve [11]. An illustration of these errors in the case of a CCO is given in Fig. 5.28.

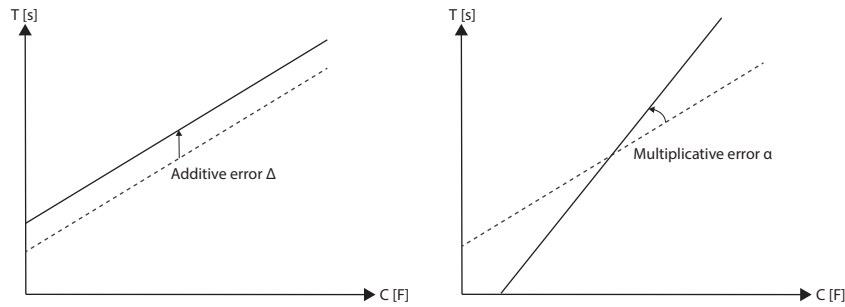


Figure 5.28: Illustration of errors in CCO transfer curve - Inspired from [11]

Three signal approach We presented the three signal approach in Chapter 2. This is a calibration method which allows removing the additive and multiplicative errors by performing three measurements. A first measurement with no sensing capacitor, a measurement with known reference capacitor and finally a measurement with the sensing capacitor. In absence of any error, the output period for a sensing capacitor C_s is given in Eq. 5.95. In presence of an additive error Δ and a multiplicative error α , the output period is given in Eq. 5.96. The output period for measurement without capacitor and with reference capacitor also follows the same transfer function. Consequently, we can remove these errors by applying Eq. 5.101 [6].

$$T_{s, \text{ ideal}} = K_{CCO} \cdot C_s \quad (5.95)$$

$$T_s = (K_{CCO} + \alpha) \cdot C_s + \Delta \quad (5.96)$$

$$T_{\text{off}} = (K_{CCO} + \alpha) \cdot 0 + \Delta \quad (5.97)$$

$$T_{\text{ref}} = K_{CCO} \cdot C_{\text{ref}} \quad (5.98)$$

$$T_s - T_{\text{off}} = (K_{CCO} + \alpha) \cdot C_s \quad (5.99)$$

$$T_{\text{ref}} - T_{\text{off}} = (K_{CCO} + \alpha) \cdot C_{\text{ref}} \quad (5.100)$$

$$\frac{T_s - T_{\text{off}}}{T_{\text{ref}} - T_{\text{off}}} \cdot C_{\text{ref}} = C_s \quad (5.101)$$

This operation can be repeated at each measurement, which increases the measurement time. It can also be simply done at the starting of the circuit which is useful for removing fixed errors (e.g due to offset capacitance) but it is not efficient for removing errors due to low-frequency variations such as temperature variation or slow supply voltage variation.

This solution will have to be evaluated in the testing process of the fabricated circuit, the possible implementation will be detailed later.

BBPLL architecture We also presented the technique of the BBPLL in Chapter 2. This architecture uses two CCOs units and a feedback loop controlling a variable capacitor. This system could be useful for removing low-frequency noise and variations, and limiting common-mode perturbations. This would be a solution for further improvement of the robustness against supply voltage noise and would also allow removing additive and multiplicative errors.

The implementation of this solution requires on-chip design as the two CCOs should be in the same conditions of operation. As the fabricated unit only includes one CCO, we will not be able to evaluate this solution directly. However, the analysis of the performances of the fabricated CCO will be useful for an improved design that may involve this architecture.

5.3.2 Noise Reduction

In Chapter 3, we explained that random jitter was caused by the presence of random noise sources, we showed that the Allan Variance was a tool allowing the analysis of these contributions in time-domain. Also, in Chapter 4, we used the Allan Variance as a tool to determine a proper averaging time slot for attenuating the effect of sinusoidal noise on the measurements resulting in a lower RMS period jitter.

Averaging In the context of noisy measurements, a solution for reducing the effect of noise is the use of averaging [6]. We showed in Chapter 3 that the variance of any sensing system is limited by flicker noise. In presence of thermal noise and flicker noise, averaging is useful for reducing thermal noise by reaching the flicker noise limit, this can be done using the Allan Variance. Consequently, a possible solution for noise reduction in a complete interface would be to use an averaging algorithm based on the Allan Variance for finding the flicker noise limit.

As an example, Fig. 5.29 shows the Allan Deviation computed on the basis of results obtained with Noisetran for the post-layout circuit of the CCO with the full-range capacitance. We can observe the decreasing straight line corresponding to the thermal noise. The Allan Deviation restarts increasing at after 400 ms. The goal of the algorithm would be to find the point at 400 ms for proper averaging.

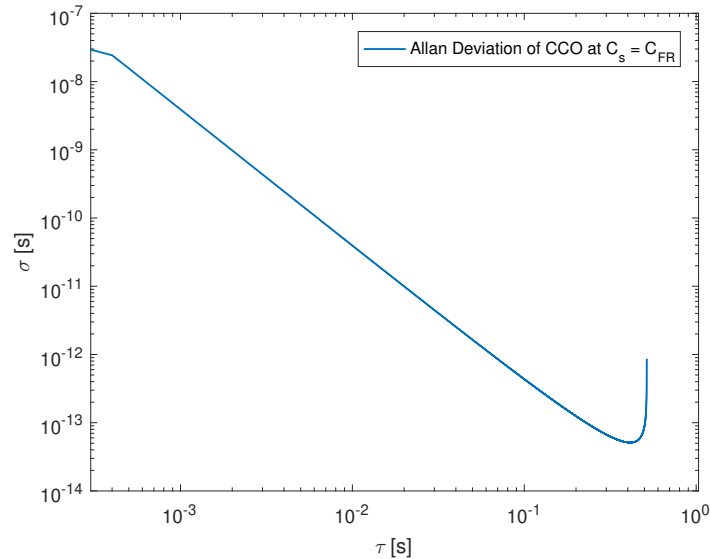


Figure 5.29: Allan Deviation of the CCO - Post-layout

5.4 Testing Methodology

We designed a CCO in UMC-RF 0.18 μ m technology which will be fabricated, we will thus be able to evaluate the real performance of the circuit. In view of what we presented in Chapters 3 and 4, we have a methodology allowing us to perform a jitter analysis that we will apply on the fabricated circuit.

5.4.1 Effective Resolution

In the framework of a sensor interface, our main goal will be to measure the ENOB of the final circuit. As the design does not include an on-chip counter, we will use an external Micro-Controller Unit (MCU) as a TDC.

As explained in Section 2.2, the ENOB can be characterized based on the SNR of the complete system which is expressed as jitter for a time-domain interface. We must notice that the MCU which performs the counting will also have its own jitter. The jitter measurement will thus be divided in two steps, a measurement of the RMS period jitter of the CCO and a measurement of the RMS period jitter of the MCU reference clock. The period jitter of the complete interface will be computed as in Eq. 5.102.

$$\sigma_{pj,measured}^2 = \sigma_{pj,cco}^2 + \sigma_{pj,MCU}^2 \quad (5.102)$$

The CCO period jitter measurement will be performed with a sensing capacitance fixed at the full-range specification C_{FR} . The measurement methodology presented in Chapter 3 will be followed. The ENOB will be calculated following Eq. 5.105.

$$T_{R,rms} = \sigma_{pj,measured} \quad (5.103)$$

$$T_{R,real} = \sqrt{12} \cdot T_{R,rms} \quad (5.104)$$

$$ENOB = \log_2 \frac{T_{FR,real}}{T_{R,real}} \quad (5.105)$$

5.4.2 Figure-of-Merit

We will also estimate the FoM which is expressed in terms of energy per conversion step. This step requires prior evaluation of the ENOB and the average power consumption of the circuit. The measurement of the power consumption will be performed for complete sensing capacitance range using a power supply with current monitoring. The FoM will be calculated following 5.106.

$$FoM = \frac{P_{measured} \cdot T_{FR,real}}{2^{ENOB}} \quad (5.106)$$

5.4.3 Linearity

The linearity of a data-converter is measured on the basis of two metrics, the Integral Non-Linearity (INL) and the Differential Non-Linearity (DNL). The INL shows the deviation of the conversion curve from the ideal conversion function and is given in Eq. 5.107 for any analog value A_i . The DNL shows the deviation of each conversion step

from the ideal conversion step and is given in Eq. 5.108 for any analog values $A(i+1)$ and $A(i)$ [32].

$$\text{INL}(i) = \frac{A(i) - i \cdot A_{\text{LSB}}}{A_{\text{LSB}}} \quad \forall i = 0 \rightarrow 2^N - 1 \quad (5.107)$$

$$\text{DNL}(i) = \frac{A(i+1) - A(i)}{A_{\text{LSB}}} \quad \forall i = 0 \rightarrow 2^N - 2 \quad (5.108)$$

The measurement of these two metrics will be performed using the micro-controller which will perform the time-to-digital conversion. The analog value $A(i)$ in the case of the CDC will be the input capacitance $C_s(i)$ in the sensing capacitance full-range.

5.4.4 Post-Processing Technique

We explained in Section 5.3 that two techniques will be tested for improving the performances of the system.

We will implement the **three signal technique** using the MCU, this will require the use of an off-chip capacitor and a digitally-controlled multiplexer for choosing between the three sensing capacitance cases. The control will be performed by the MCU. We will vary the measurement conditions (temperature and voltage) to verify the efficiency of the technique. The advantage of performing the three signals measurement at each measurement or at the starting of the circuit will also be evaluated.

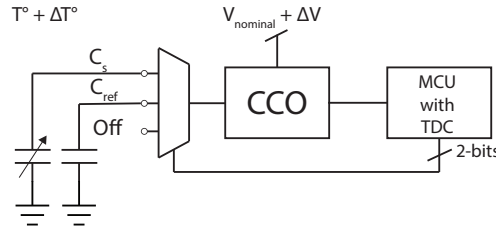


Figure 5.30: Three signal technique - Illustration - Inspired from [6]

5.4.5 Structure of the Evaluation Board

The IC will be placed on a PCB. The PCB will embed an output buffer which will also serve as a level shifter for the use of the CCO with an external MCU as shown in Fig. 5.31. A set of voltage regulators will be placed on the board with appropriate decoupling capacitors to supply the IC and the output buffer. All the voltage regulators will be supplied by an external DC source. An external current source will be used for proper biasing of the comparator. The capacitors for testing will be external to the board and will be connected using an on-board connector. As shown in Fig. 5.31, we will use

a laboratory period counter in addition to the oscilloscope and the MCU to have an additional accurate measure during testing.

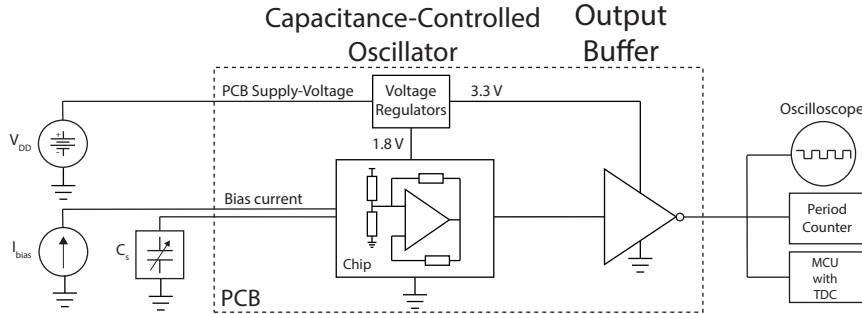


Figure 5.31: Illustration of the setup for testing the CCO

5.5 Summary

In this chapter, we presented the design flow followed for the conception of the Capacitance-Controlled-Oscillator that will be used as a Capacitance-to-Time Converter in our Capacitance-to-Digital Converter.

We presented the relaxation oscillator structure chosen, we explained the theory of operation of this structure and we motivated its choice by showing its theoretical robustness against supply voltage variation. We also developed a noise model based on the work from [40] to evaluate the jitter performance of the circuit as a design constraint.

After that, we started the design of the circuit by defining the system specifications of our interface using the results explored in the SoA of time-domain interfaces. We fixed the ENOB of the interface at 8 bits with respect to the relaxed specification defined for this work and we fixed the full-range capacitance at 300 pF based on a humidity sensor from [2]. We defined the other system specifications as ranges to respect in the design process.

Then, we derived the design specifications of the building blocks of the circuit using the system specifications. We fixed the measurement time based on a typical MCU reference clock from [31]. This allowed us to calculate the required gain of the CCO K_{CCO} resulting in a value of $1.4 \mu\text{s pF}^{-1}$. Using the gain of the CCO and the ENOB we derived the jitter constraint.

Afterwards, we used the power consumption specification to define a lower boundary for the resistor values of the voltage divider. We used the noise model and the jitter specification to define an upper boundary for all the resistors values. Then, we calculated the design specifications of the comparator. We showed that the relaxation oscillator

circuit chosen is theoretically insensitive to the offset voltage of the comparator, we evaluated the required GBW of this one using a model in simulation and we computed the output current specification using proper approximations. Finally, we motivated our choice for the structure of the comparator and we explained the design flow used for this block.

Next, we showed the results obtained in simulation for the circuit using the UMC-RF 0.18 μm CMOS technology design kit. We first verified the functionality of the circuit under ideal conditions, we verified the output frequency curve and the period jitter at the full-range capacitance. Then, we made the same verification taking into account PVT variations. We also ran Monte-Carlo simulations to evaluate the circuit functionality with device variations and mismatch.

We presented the layout process, we exposed the physical non-idealities inherent to this process as well as the techniques to limit their effects. We verified the circuit functionality using the post-layout model extracted which takes into account RC parasitics of the layout, we also verified the robustness of the circuit against supply-voltage variation.

Finally, we presented three techniques that we will evaluate for improving the performances of the system once the circuit will be fabricated. We showed the interest of the three signal technique for our interface to reduce linearity errors. We briefly discussed the usefulness of the BBPLL structure and we explained why it will require a new design for proper evaluation. We also briefly discussed the use of averaging as a noise reduction tool and we talked about the use of Allan Variance to make this technique efficient. Then, we discussed the testing methodology that will be followed for evaluating the fabricated circuit and we showed the structure of the PCB that will be made for this purpose.

The results obtained in simulation for this design are summarized in Table 5.4. These results do not include the counter that will add jitter and an additional power consumption. As there is not current source in this circuit, the power consumption related to it is not taken into account either. The CCO alone reaches an ENOB of 9.9 bits calculated using Eq. 5.105 from the simulation results. It reaches a FoM of 7.9 pJ per conversion step calculated following Eq. 5.106 with the simulation results.

Specification	Defined	Simulation
Full Range [pF]	300	300
ENOB [bits]	8	9.9
Measurement Time [ms]	0.02 - 17.5	0.412
VDD [V]	1.2 - 1.8	1.8
Power [μW]	1 - 20	18.5
FoM [pJ/conv-step]	0.01 - 680	7.9
Area [mm^2]	0.05 - 0.1	0.01

Table 5.4: System specifications obtained in simulation

Conclusion

6

In this work, we investigated several aspects surrounding the design of time-domain Capacitance-to-Digital Converters in an IoT context. We focused our interest on the jitter aspect, we developed a methodology for jitter analysis in time domain and we built a Capacitance-Controlled-Oscillator (CCO) as a first step in the design of a more advanced CDC answering to the challenges of the IoT field.

We explored the SoA of CDCs in which we distinguished voltage-domain converters and time-domain converters. We focused our work on time-domain interfaces as they allow larger input capacitance range and can easily integrate into a SoC. We showed the two main blocks composing a time-domain CDC: the CTC or CCO, and the TDC. We analyzed the main characteristics of these blocks and we concluded on the importance of the jitter aspect.

Then, we studied the theory behind jitter in time domain. We developed a measurement methodology for jitter analysis of oscillators and we presented the Allan Variance as a tool for this purpose.

After, we put these concepts in practice by analyzing measurements performed on Voltage-Controlled Oscillators designed previously by UCLouvain in bulk 65 nm CMOS technology from ST-Microelectronics. We observed the differences between the jitter extracted from the measurements and the results obtained in simulation. We evaluated several hypothesis concerning these differences.

We used simulation to estimate the influence of the level shifters and the frequency divider, resulting in a negligible influence. We used a circuit model of the package parasitics with typical values to evaluate their impact on the behaviour of the Ring-Oscillator resulting in a small influence on the jitter. Also, we used the Allan Variance to identify the presence of a sinusoidal noise affecting the oscillator. We exploited the technique of averaging to remove the effect of this perturbation. This operation resulted in jitter values closer to the simulation results. Finally, we estimated the amplitude of the sinusoidal interference as being between 1 mV and 20 mV.

We started the design of a CCO, which is the first block of the CDC, following a top-down methodology. We motivated our choice of the relaxation oscillator by its robustness against supply-voltage variation and its lower jitter compared to ring-oscillators. We analyzed the operation of this structure and we built a noise model to evaluate its jitter. Then, we defined the system specifications on the basis of the SoA.

From these system specifications, we defined the requirements of the building blocks of the circuit. We designed the CCO in UMC-RF 0.18 μm technology by analyzing its capacitance-to-time transfer characteristics under several constraints namely Process-Voltage-Temperature variations, device variations, mismatch and layout RC parasitics. We were able to reach a FoM of 7.9 pJ per conversion step with a measurement time of 412 μs for a capacitance range of 300 pF in simulation.

Finally, we exposed the testing methodology that will be followed for evaluating the fabricated CCO using a micro-controller for counting and using the methodology developed for jitter analysis. These tests will involve the estimation of ENOB, the possible linearity errors and the FoM.

Future work We also showed our interests for evaluating 3 performance enhancement techniques. We will be able to evaluate the three signal technique which is a calibration scheme for reducing additive and multiplicative errors using the MCU. It will also be possible to evaluate the interest of averaging coupled to an algorithm using the Allan Variance for noise reduction using the MCU. And finally, it will be possible to implement the BBPLL architecture in a future IC design for reducing low-frequency noise and common-mode perturbations.

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