UCLouvain

École polytechnique de Louvain

RF characterization of the back-gate contact on Fully Depleted SOI MOSFETs

Author: **Martin VANBRABANT**
Supervisor: **Jean-Pierre RASKIN**
Readers: **Denis FLANDRE, Valeriya KILCHYTSKA, Lucas NYSSENS, Martin RACK**
Academic year 2019–2020
Master [120] in Electrical Engineering

Abstract

Thanks to the thin buried-oxide, the UTBB FDSOI technology with a highly doped region under the BOX is one of the main candidates for future RF applications. One of the most interesting feature of this technology is the possibility to tune the threshold voltage, compensate variability issues and improve the overall device performance. In this work, the impact of the back-gate bias is mainly studied on the threshold voltage and RF FoMs of the front and back-gates.

Acknowledgments

The completion of this master thesis would not have been possible without the help and support of several people. In the following, I would like to thank them personally.

First of all, I would like to express my gratitude to my supervisor, Prof. Jean-Pierre Raskin, for his valuable guidance and also for giving me the opportunity to work within his research group. I met passionate people who were always available to help and give good advice. I also would like to thank Prof. Denis Flandre and Dr. Valeriya Kilchytska for their precious feedback all along the semester.

I also thank Lucas Nyssens and Martin Rack for accepting to be readers of this work and I am particularly grateful to Arka Halder for providing 4-Port measurements. Once again, I would like to thank Lucas Nyssens for the time he dedicated to help me and answer my questions.

Following this, I would like thank my parents, grandparents and little brother for their support and encouragements.

Next, I would also like to thank best friends with a special mention to Manuel Pace and Jules Poncin, aka "Le Trio".

Finally, I would like to thank my girlfriend Laetitia, for all the love and support I received throughout the realization of this work. I also gave you credit for trying to remember the meaning of the abbreviation "UTBB FDSOI MOSFET".

Martin Vanbrabant

Contents

Chapter 1

Introduction

1.1 Background and motivation

For more than four decades, the evolution of integrated circuits (ICs) has been mostly driven by the continuous down-scaling of the CMOS technology. Each new technology node has demonstrated an improvement of the circuit performances and a reduction of the cost per transistor. However, as the dimensions of the transistor decreased, a number of nonidealities, commonly referred as short-channel effects (SCE), appeared. Among them, one can cite channel length modulation, drain induced barrier lowering (DIBL) and velocity saturation. To overcome these detrimental effects and keep a good carrier mobility and electrostatic control, complex fabrication process and device doping profiles were introduced. However, most recently, reliability and yield issues have been encountered due to the increasing complexity of the doping profiles. Indeed, prohibitive variations in device properties such as the threshold voltage have been observed due to dopant fluctuations [1; 2].

Therefore, in order to continue the device down-scaling, alternative strategies such as new materials in both channel (GaAs and germanium) and gate oxide (high-k dielectrics) have been adopted [3]. New device architectures have also been investigated. Planar UTBB (ultra-thin body and ultra-thin buried oxide) FDSOI (fully depleted SOI) and FinFET appear to be the two main candidates satisfying ITRS requirements and thus, enabling continued CMOS scaling [2]. Both these devices rely on ultra-thin body instead of complex doping profile (as in bulk technology) in order to control short-channel effects [4]. However, most recently, the advent of widespread 5G wireless communication systems pushes RF performance requirements towards new limits. High gain-bandwidth product, high linearity, low power consumption and low noise can be cited among the high requirements of 5G communication systems. Therefore, advanced RF technologies are needed in order to satisfy these specifications. One of the devices which appears as a promising candidate is again the planar UTBB FDSOI with a highly doped region under the BOX (so-called ground plane GP) [5]. Currently, 28FDSOI from *ST-Microelectronics* and 22FDX from *GlobalFoundries* are the two main processes available.

One of the most unique features of UTBB FDSOI technology with GP is the possibility to use back-gate control schemes [6]. By dynamically modulating the threshold voltage, the transistor can thus be optimized for either performance or power consumption depending on the requirements. Furthermore, back-gate biasing can also be used to tune the main RF FoMs as demonstrated in [6].

In this context, the present work aims to characterize this very promising technology from DC

to RF operation. More specifically, the impact of the back-gate bias on the threshold voltage and the main RF Figures of Merit (FoMs) will be analyzed.

1.2 Structure of the document

This document is organized as follows:

The second chapter of this work, named *State of the art*, presents a quick overview of the UTBB FDSOI technology, especially from the structural point of view. The conventional-well and flip-well architectures are described.

The third chapter *DC characterization of UTBB FD-SOI with back-gate access* is mainly dedicated to the modulation of the threshold voltage with the back-gate bias. The dependence of the threshold voltage at one gate by the opposite gate bias is known as *coupling characteristics*. The analysis of the coupling characteristics is done for the analytical model proposed by Rudenko et al. [7], for TCAD simulations using Sentaurus Device [8] and finally for experimental measurements. The dependence of two other parameters (R_{SD} and $C_{well-sub}$) on the back-gate bias is also analyzed at the end of this chapter.

The fourth chapter *A wideband characterization of UTBB FD-SOI with back-gate access* studies a 3-Port and 4-Port small-signal equivalent circuit based on *ELDO* simulations. After that, the 3-Port small-signal model is applied to 22FDX RF measurements and the front and back-gate RF FoMs are extracted for various back-gate biases.

Finally, the last chapter *Conclusion* summarizes the main results of this work and gives future perspectives.

Chapter 2

State of the art

2.1 Introduction

As mentioned in the introductory chapter, UTBB FDSOI technology with a highly doped region under the BOX (ground plane) is recognized as a promising candidate for future low-power and RF applications [3; 6]. The aim of this short chapter is thus to give an overview of several advantages and design considerations of this technology.

2.2 UTBB FD-SOI MOSFETs and back-gate control schemes

Here is a non-exhaustive list of the advantages of the SOI technology over its bulk counterpart [9; 10]:

- Reduction of substrate parasitic capacitances due to use of the buried oxide.
- Small devices without latchup (PNPN thyristor) because the n- and p-well structures are isolated from each other. There is no current path through the substrate.
- Reduction of short channel effects.
- Better inverse subthreshold slope [11].

Since UTBB FDSOI transistors are based on the SOI technology, it inherits its advantages. Figure 2.1 shows a cross-section of an UTBB FDSOI transistor featuring a back-gate contact.

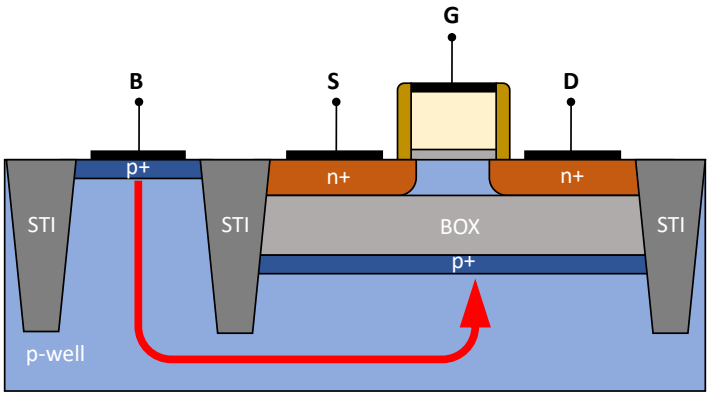


Figure 2.1: UTBB FDSOI nMOS transistor with back-gate access.

The so-call conventional-well and flip-well are presented in Figures 2.2 and 2.3. Due to the doping of the GP, the threshold voltage is different between the two architectures. It is an example of multi-V_T options. One can also bias the back-gate contact either with a static or with a dynamic voltage to tune on the fly the threshold voltage. This feature is possible thanks the ultra-thin BOX.

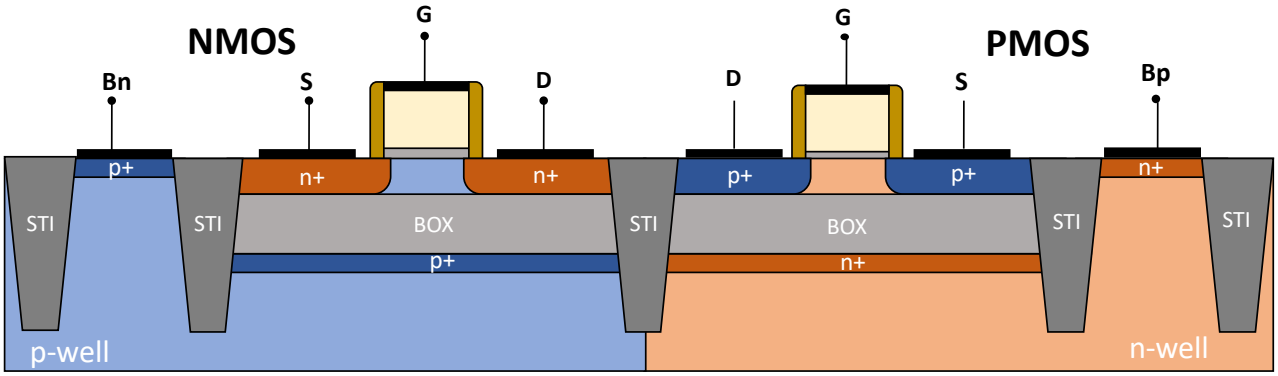


Figure 2.2: Conventional well architecture.

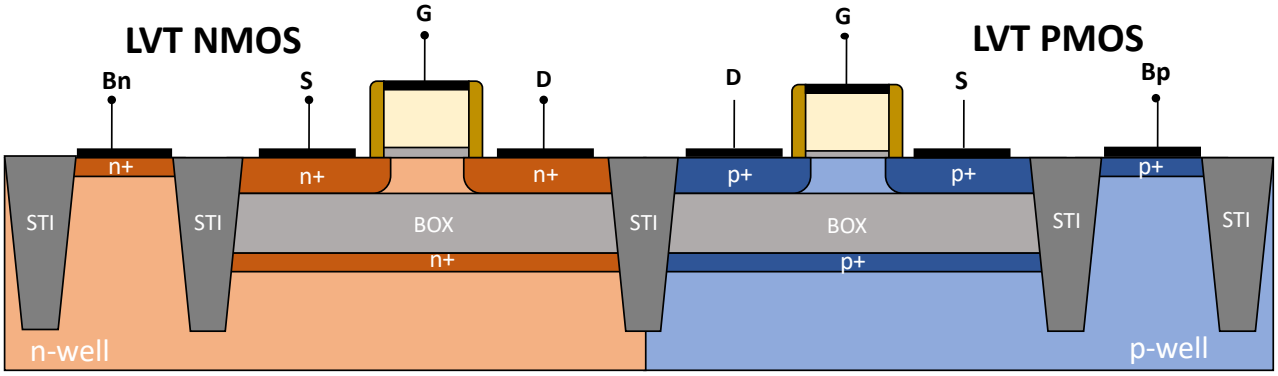


Figure 2.3: Flip well architecture.

First, it can be noticed that no channel doping is needed because the channel is fully depleted. Moreover, scaling the thickness of the silicon body has two major advantages. First, it reduces the subthreshold slope because $\alpha_{FDSOI} < \alpha_{Bulk}$ and then it also helps with DIBL since the thickness of the silicon film is directly in its equation. In order to limit short channel effect, the channel thickness must be approximately 1/4 of the channel length [4]. A highly-doped layer under the BOX (ground plane) is also a common solution to prevent the source-drain lateral coupling through the substrate since it has a high resistivity.

Finally, it can be said that with thin BOX and GP, the transistor acts like a DG transistor and the back-gate control scheme enables to easily tune the threshold voltage to find a balance between power/performance

In the next sections, the threshold voltage modulation with the back-gate bias will be studied.

Chapter 3

DC characterization of UTBB FD-SOI with back-gate access

As presented in Chapter 1, the semiconductor industry is earnestly researching new devices structures in order to be able to continue CMOS scaling down to the 20nm-node and beyond [2; 3]. Both FinFETs and planar fully depleted (FD) SOI MOSFETs with ultra-thin body and ultra-thin buried oxide (so-called UTBB) are considered to be the main candidates satisfying the International Technology Roadmap for Semiconductors (ITRS) requirements for device down-scaling.

This chapter focuses on the UTBB FDSOI technology with a heavily doped layer located just under the BOX, or so-called ground plane (GP). The realization of GP is primarily intended to prevent the lateral coupling between the source and drain through the substrate but is also a practical way to tune the threshold voltage depending on the nature of dopants. The well, which is isolated from the source and drain by the BOX, can be either n-type or p-type for both nFET and pFET. Classical transistor architecture is based on p-well for nFETs and n-well for pFETs (RVT transistors) and presents higher V_T than the flip-well architecture based on n-well for nFETs and p-well for pFETs (LVT transistors).

The next sections are dedicated to the possibility of back-gate biasing schemes of the UTBB FDSOI architecture with GP, which is one of the unique features of this technology [12]. To this end, TCAD simulations were performed using Sentaurus Device from Synopsys. Sentaurus Device is a numerical simulator capable of simulating electrical, thermal, and optical characteristics of silicon-based and compound semiconductor devices [8]. Thanks to CEA-Leti, an initial transistor structure with back-gate access was made available. This deck was calibrated to measurements on 28FDSOI transistors but as demonstrated by Morelle et al. [13] (who assess the same transistor structure), the initial constant carrier mobility must be modified in order to take into account other mobility degradation phenomena.

This chapter is organized as follows: Section 3.1 presents the TCAD simulation structure and its main parameters. In Section 3.2, the modifications applied to the carrier transport model are shortly described. The impact of the back-gate on the $I_D - V_{GS}$ characteristics as well as on V_{TH} is studied in Section 3.3. Then, different threshold voltage extraction methods are compared by means of TCAD simulations and experimental data in Section 3.4. Finally, the extraction of some common parameters and their dependence on the back-gate voltage is studied.

3.1 Device geometry

Figure 3.1 shows the TCAD simulation structure studied in this work. It can be noticed that the 28FDSOI transistor is designed as a 2D structure (assuming a default width of 1 µm), thus representing a cross-section of the real transistor. While 2D simulations are less numerically expensive than 3D simulations, one must keep in mind that some physical phenomena, such as the distributed aspect of the gate resistance, are not well modelled. The "Substrate" electrode, which will be referred as the "back-gate" electrode throughout this work, serves to bias the well under the BOX, enabling back-gate biasing schemes. This back-gate contact is isolated from the rest of the transistor by Shallow Trench Isolation (STI) made of silicon oxide. For both DC and AC simulations, the "Bulk" electrode is fixed at 0 V in this work.

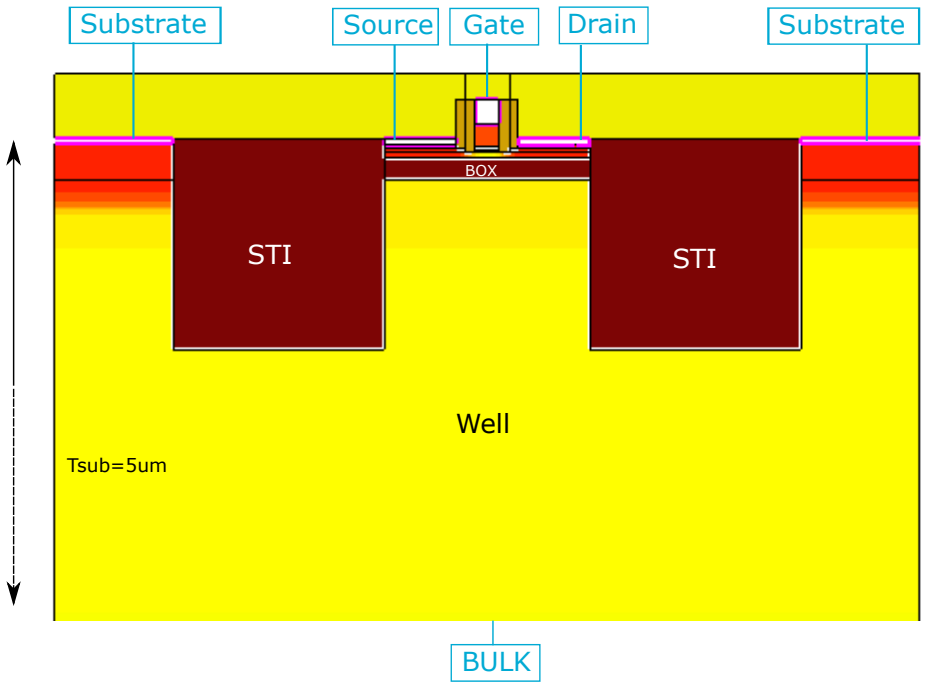


Figure 3.1: Sentaurus 2D structure provided by CEA-Leti.

As Figure 3.1 gives an overview of the transistor structure, a closer look centered around the channel is presented in Figure 3.2. One can observe that the gate stack is composed of several materials : polysilicon, titanium, HfO_2 and an interfacial layer of silicon oxide. Reduced gate leakage and improved drive current have been reported by introducing High-K/Metal Gate (HK/MG) technology (by means of a thin dielectric layer of HfO_2) [14]. The channel is made of a 6.7 nm thick silicon film separated from the well by a buried oxide. Important structural parameters with their default values are summarized in Table 3.1.

Parameter	Symbol	Value	Unit
Gate length	L_g	28	[nm]
Width	W	1	[µm]
Front oxide thickness SiO_2	t_{of,SiO_2}	1.3	[nm]
Front oxide thickness HK dielectric	$t_{of,HK}$	1.7	[nm]
Channel/body thickness	t_{Si}	6.7	[nm]
Back oxide thickness SiO_2	t_{ob}	25	[nm]

Table 3.1: List of structural parameters with their default values.

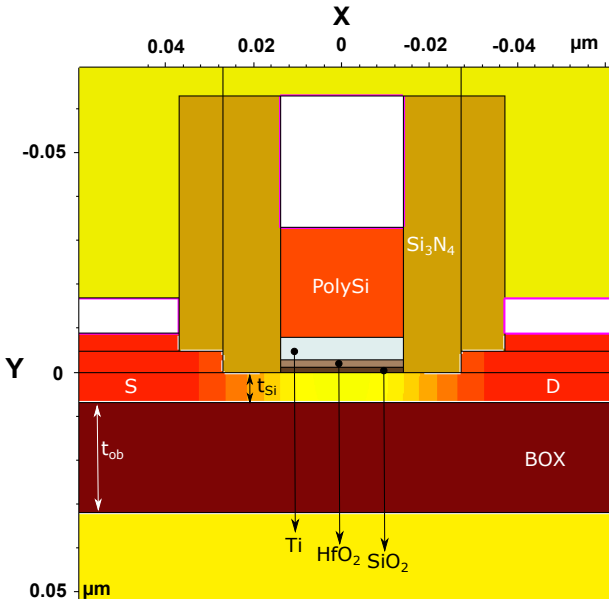


Figure 3.2: Sentaurus 2D structure provided by CEA-Leti. White regions delimited by pink boundaries correspond to electrodes (i.e. Source, Gate, Drain).

In this work, the description and modelling of the UTBB FDSOI transistors are mainly done on nMOS with N-type ground plane (LVT transistors) unless otherwise specified. Their phosphorus doping profile along the channel at $Y = 3\,\text{nm}$ is shown in Figure 3.3 for three different gate lengths. The doping profiles are normalized by the high doping concentration of source and drain. One can notice that for shorter gate lengths (i.e. 28 nm), the source and drain diffusion regions start merging together, resulting in a higher doping of the channel region. Although the channel doping is several orders of magnitude lower than the source and drain doping in the 150 nm case, its value is still non-negligible to be considered as undoped as it is traditionally done for UTBB FDSOI transistors. The "residual" channel doping is attributed to the N-well implementation. This hypothesis was verified by removing the command lines used to implement the N-well.

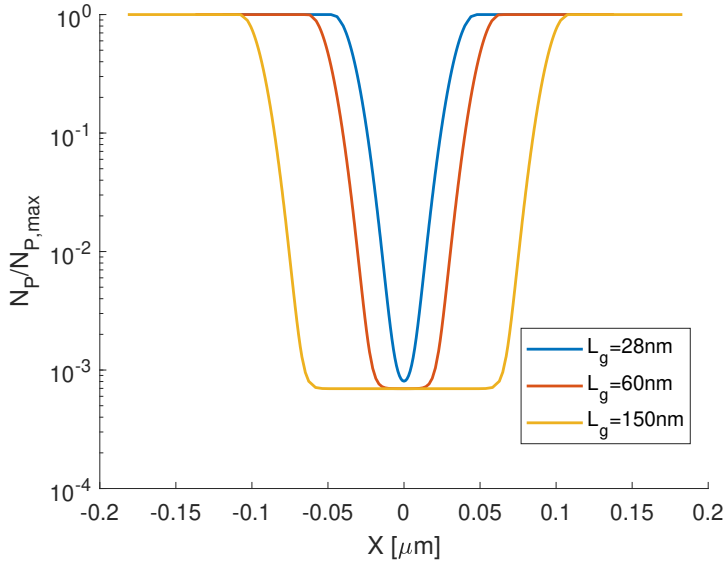


Figure 3.3: Normalized phosphorus doping profile for three different gate lengths, namely 28 nm, 60 nm and 150 nm.

3.2 Carrier transport model

This section introduces the physical models used to simulate the electrical behaviour of the device. By default, Sentaurus TCAD tool solves the Poisson and carrier continuity equations with the drift-diffusion model [8]. In addition to that, doping-dependent Shockley–Read–Hall (SRH) recombination and carrier quantization effects are also included. Indeed, since some features of current transistors (oxide thickness, channel width) have reached quantum mechanical length scales, the wave nature of electrons and holes can no longer be ignored. Quantization effects can cause tunneling, reduction of the gate capacity and a shift of threshold voltage [8] which is the subject of the next sections. Therefore, an accurate model of these effects must be added. In Sentaurus Device, quantization effects are taken into account by introducing a potential-like quantity Λ in the classical density formula. Several models of Λ are available but the "density gradient" model is selected because it is numerically robust and suitable for SOI structures. More detail about the definition of Λ can be found in Chapter 14 of [8].

Moreover, temperature is fixed to 300 K and is uniform over the whole structure. In order to take into account the self-heating effect, one must switch from the classical drift-diffusion model to a model that also solves the carrier and heat flow equations such as the hydrodynamic model [8]. Because of the longer simulation time needed for the hydrodynamic model and self-heating is not the main focus of this work, it was decided to not include it as a first approximation.

The default mobility model implemented in Sentaurus accounts only for phonon scattering and thus, is only temperature dependent:

$$\mu_{const} = \mu_L \left(\frac{T}{300\,\mathrm{K}} \right)^{-\zeta} \tag{3.1}$$

Where T is the lattice temperature and μ_L is the mobility due to bulk phonon scattering. The default values of μ_L coefficient were replaced by $150\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for electrons and $75\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for holes which are typical values in FDSOI transistors. Sentaurus Device also offers the option

to improve the modelling of tunneling through semiconductor barriers by modifying the mobility model:

$$\mu = \frac{\mu_{cl} + r\mu_{tunnel}}{1 + r} \tag{3.2}$$

Where μ_{cl} is the classical mobility, $\mu_{tunnel} = 0.05\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ is a fitting parameter and r is the percentage of carriers subjected to tunneling [8].

However, as pointed by Morelle et al. [13], the above constant mobility model is not physical and neglects many mobility degradation phenomena. It was demonstrated that replacing the constant mobility model by a more complex model that takes into account several mobility degradation phenomena shows good agreement between TCAD simulations and UTSOI2.2 compact model in strong inversion at $V_{DS} = 50\,\mathrm{mV}$. Therefore, it was decided to use the same complex mobility model in this work. Here is a brief list of these different mobility degradation models:

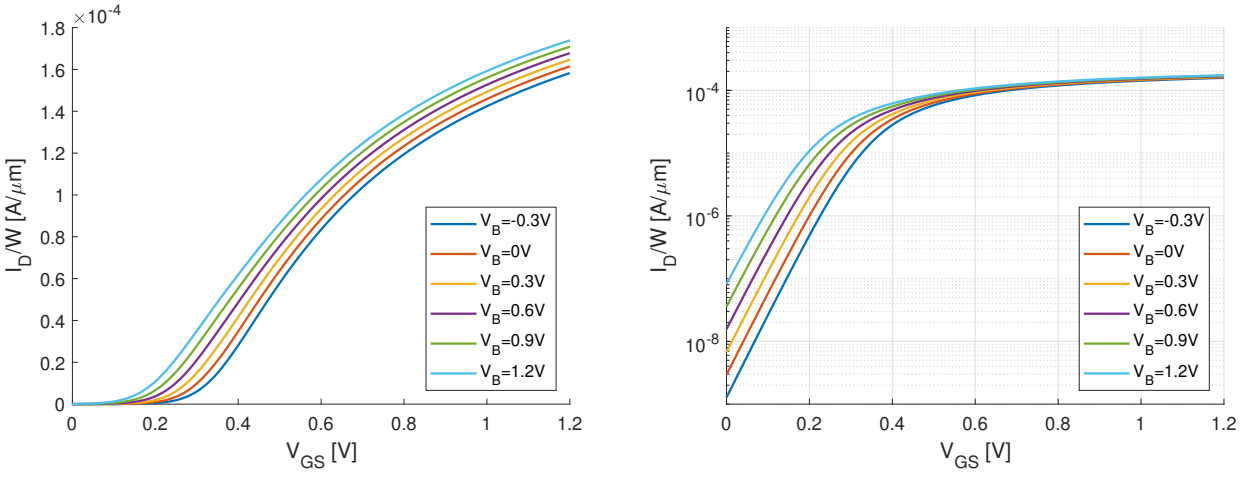
- Doping-dependent mobility in silicon is simulated with Masetti model [15] (default doping-dependent model used in Sentaurus Device): scattering of the carriers by charged ions leads to degradation of the mobility.
- Carrier velocity saturation for regions with high electric field is accounted for both electrons and holes by Canali model.
- A thin-layer mobility model is also added because of the very thin silicon layers used in the UTBB technology. It is based on the model proposed by S. Reggiani et al. [16] that accounts for thickness fluctuation scattering, surface phonon scattering, bulk phonon scattering in conjuction with the Lombardi model (mobility degradation at interfaces due to high transverse electric field forces) [8].

3.3 DC operation and theoretical study of $V_{TH} - V_B$ curves

Aside the excellent electrostatic integrity, the lower variability by using undoped channel [17] and the promising RF performance with high cut-off frequencies (f_T and f_{max}) [18] of UTBB FDSOI transistors, the possibility of back-gate control schemes is considered as one of the most interesting features of this technology. This section describes the fundamental theory of back-gate biasing and its effect on I-V and front-gate capacitance characteristics. The emphasis is on studying the modulation of the threshold voltage at one gate by the opposite-gate bias.

3.3.1 I-V characteristics

Figures 3.4a and 3.4b show the drain current versus front-gate voltage characteristics for various back-gate biases V_B. The simulated drain current is normalized by the default width ($W = 1\,\mu\mathrm{m}$) assumed by Sentaurus Device for 2D simulations. Increasing V_B is commonly called Forward Back Biasing (FBB) while lowering V_B is called Reverse Back Biasing (RBB).



(a) (b)

Figure 3.4: $I_D - V_{GS}$ characteristics in linear regime for various back-gate voltages V_B: (a) in linear scale and (b) in semi-logarithmic scale. $V_{DS} = 50\,\text{mV}$, $L_g = 30\,\text{nm}$ and $W = 1\,\mu\text{m}$.

As shown in Figures 3.4a and 3.4b, increasing the back-gate voltage V_B shifts I-V characteristics towards lower V_{GS}. This effect is of twofold origin. Firstly, a strong charge coupling between the front and back SOI interfaces is observed in FDSOI transistors [19]. Thus, an application of a back-gate bias results in the modulation of the threshold voltage, which leads to a shift of I-V curves to the left/right for FBB/RBB, respectively. This dependence of the threshold voltage at one gate on the opposite gate bias is known as coupling characteristics and is traditionally described by the classical Lim and Fossum (LF) model proposed in 1983 [20]. The validity of this model will be discussed in more detail in Section 3.3.2.

Secondly, a back-channel conduction appears at the Si film/BOX interface for positive back-gate biases. Figure 3.5 shows the electron density distribution across the 2D structure for three different V_B. At $V_B = 10\,\text{V}$, the back-channel is clearly visible at the Si film/BOX interface. In order to have a more insightful view of the electron density distribution, one can plot a cutline of Figure 3.5 at $X = 0\,\mu\text{m}$ along the Si film thickness, as presented in Figure 3.6. One can notice that for high V_B (i.e. $V_B = 10\,\text{V}$), the contribution of the back-channel is non-negligible with electron density at the back interface comparable with the one at the front interface. In DG UTB transistors, several authors [2; 21; 7] have also reported the concept of volume inversion. Indeed, the front and back channels are no longer independent in the case of thin boby. Therefore, specific front and back bias conditions can force most of the carriers to flow through the middle of the Si film. In these conditions, the inversion charge in the bulk (middle) of the body can be comparable to that near the interfaces and define much of the on-current [2].

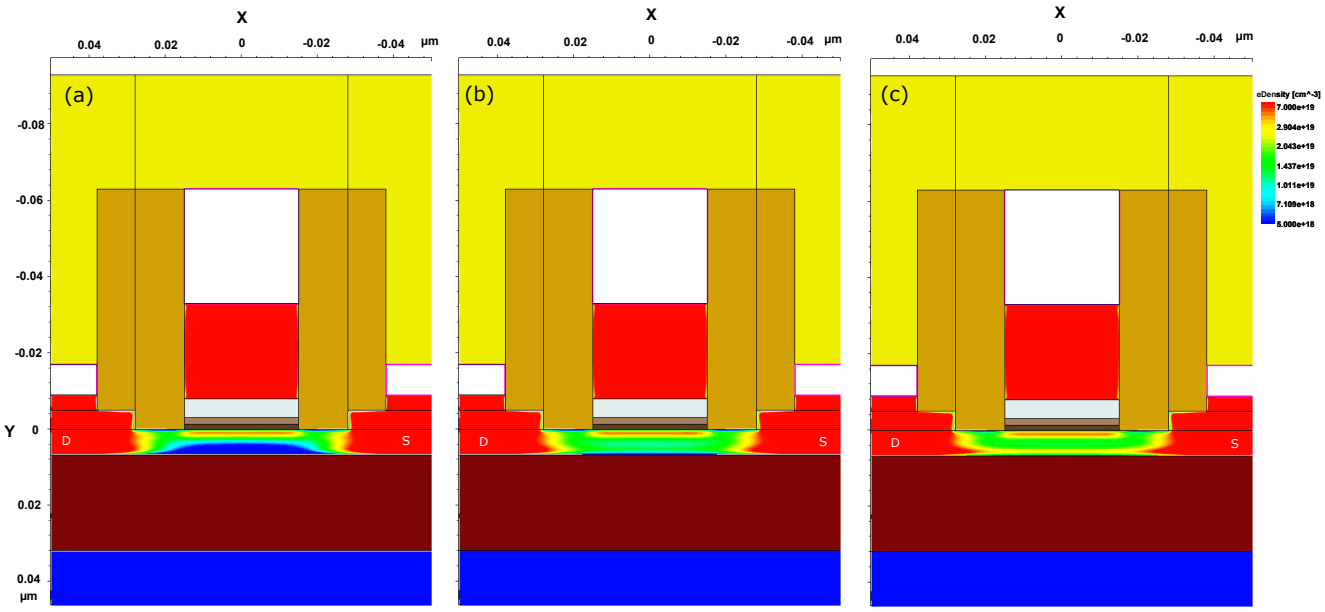


Figure 3.5: Electron density in linear regime for various back-gate biases: (a) $V_B = 0\,\mathrm{V}$, (b) $V_B = 5\,\mathrm{V}$ and (c) $V_B = 10\,\mathrm{V}$. $V_{DS} = 50\,\mathrm{mV}$ and $V_{GS} = 1\,\mathrm{V}$. $L_g = 30\,\mathrm{nm}$.

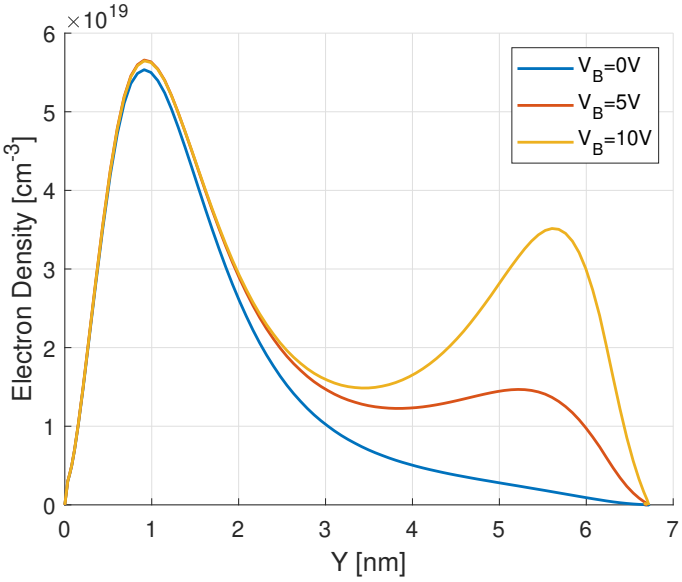


Figure 3.6: Electron density versus position in the silicon film for various back-gate biases at $X = 0\,\mu\mathrm{m}$ (cutline of Fig. 3.5). $L_g = 30\,\mathrm{nm}$, $V_{DS} = 50\,\mathrm{mV}$ and $V_{GS} = 1\,\mathrm{V}$.

3.3.2 Coupling characteristics

As mentioned in the previous section, interface coupling is widely used for understanding the modulation of the threshold voltage at one gate by the opposite gate bias. The BOX and Si body thicknesses can also be determined by using interface coupling [22] making it a suitable tool for characterization purposes. The well-known Lim and Fossum model [20] which describes the $V_{THf}(V_B)$ dependence is qualitatively pictured in Figure 3.7 and a schematic of a thin-film SOI

MOSFET is shown in Figure 3.8. As explained in their paper, the studied structure is a four-terminal device but in order to put emphasis on the charge coupling behaviour, a one-dimensional approach (Fig. 3.8b) was taken, neglecting small-geometry effects.

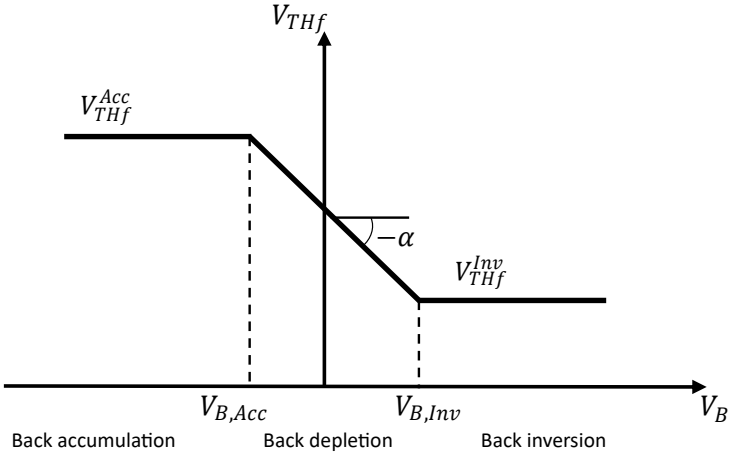


Figure 3.7: Qualitative representation of the classical Lim and Fossum model [20]. Dependence of the front-gate threshold voltage versus the back-gate voltage.

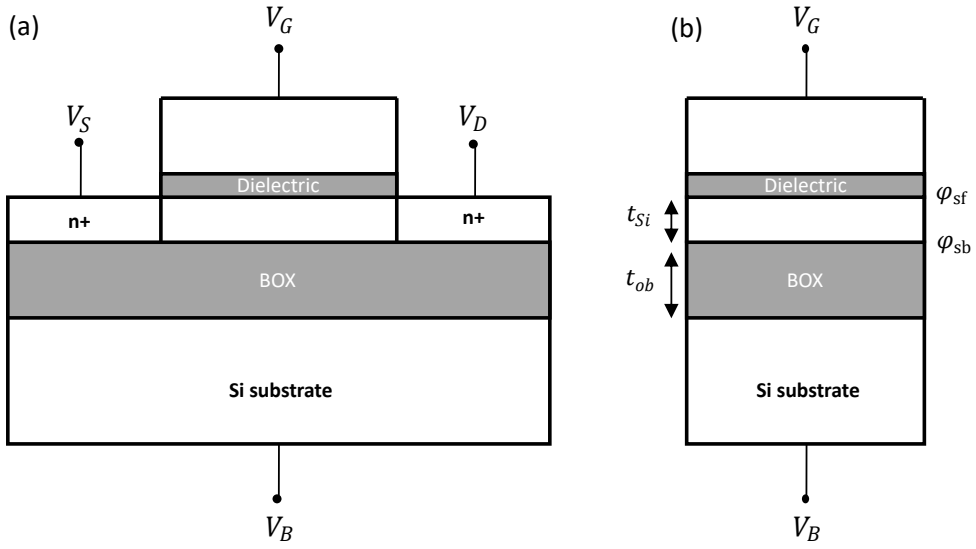


Figure 3.8: (a) Schematic of a thin-film SOI MOSFET. Front and back-gate voltages are noted V_G and V_B, respectively. (b) One-dimensional representation of the thin-film SOI MOSFET with the front φ_{sf} and the back φ_{sb} surface potentials.

According to this model, when the back surface is accumulated, φ_{sb} is approximately pinned to 0 V and the front threshold voltage $V_{THf}(V_B) = V_{THf}^{Acc}$ is independent of V_B. When the back surface is inverted, φ_{sb} is approximately pinned to $2\Phi_F$ (twice the Fermi potential) and $V_{THf}(V_B) = V_{THf}^{Inv}$ is also independent of V_B. Finally, when the back surface is depleted, φ_{sb} is strongly dependent on the back-gate voltage which gives

$$V_{THf}(V_B) = V_{THf}^{Acc} - \alpha(V_B - V_B^{Acc}) \qquad \text{when} \quad V_B^{Acc} < V_B < V_B^{Inv} \tag{3.3}$$

Where α is the slope of the front-gate coupling characteristic in depletion regime defined as

$$\alpha = \frac{\mathrm{d}V_{THf}}{\mathrm{d}V_B} = \frac{C_{Si}C_{ob}}{C_{of}(C_{Si} + C_{ob})} \tag{3.4}$$

Where C_{of} is the front-gate capacitance, $C_{ob} = \frac{\varepsilon_{SiO_2}}{t_{ob}}$ is the BOX capacitance and $C_{Si} = \frac{\varepsilon_{Si}}{t_{Si}}$ is the depletion capacitance.

Although this model provides a simple relationship between the front-gate threshold voltage and the back-gate bias, it fails to describe the non-classical effects in undoped UTB MOSFETs reported in [23; 24]. For example, the use of the conventional $2\Phi_F$ criterion is invalid in the case of undoped/lightly-doped SOI MOSFETs where the surface potential largely exceeds this value under threshold conditions [7]. Quantum-mechanical effects also enhance the modulation of V_{THf} (and V_{THb}) by the opposite-gate bias compared to classical simulations. Therefore, the analytical model derived by Rudenko et al. [7; 25] in order to study these non-classical effects is presented here and compared to the coupling characteristics obtained with TCAD simulations.

Analytical modelling Before presenting the analytical model of the modulation of the threshold voltage at one gate by the opposite gate bias, Table 3.2 summarizes some of the notations used in the following developments.

Parameter	Symbol
Dielectric permittivity of SiO_2	ε_{SiO_2}
Dielectric permittivity of HK dielectric	ε_{HK}
Front oxide thickness of SiO_2	t_{of,SiO_2}
Front oxide thickness of HK dielectric	$t_{of,HK}$
Channel/body thickness	t_{Si}
Back oxide thickness (BOX)	t_{ob}
Front-gate dielectric capacitance	C_{of}
Back-gate dielectric capacitance	C_{ob}
Capacitance of the depleted silicon film	C_{Si}
Body factor	n
Thermal potential	$\phi_T = \frac{kT}{q}$
Front surface potential	φ_{sf}
Back surface potential	φ_{sb}
Work function difference between front-gate and intrinsic Si	$\Delta\Phi_{fi}$
Work function difference between back-gate and intrinsic Si	$\Delta\Phi_{bi}$
Doping concentration	N_A

Table 3.2: Notation used for electrical and structural parameters.

Because the gate stack (Fig. 3.2) consists of a high-K dielectric layer on top of a silicon oxide layer, the front-gate dielectric capacitance is defined as the serie combination of the two individual

capacitances:

$$C_{of} = \frac{C_{of,SiO_2} C_{of,HK}}{C_{of,SiO_2} + C_{of,HK}} \tag{3.5}$$

Where $C_{of,SiO_2} = \frac{\varepsilon_{SiO_2'}}{t_{of,SiO_2}}$, $C_{of,HK} = \frac{\varepsilon_{HK}}{t_{of,HK}}$ and $C_{Si} = \frac{\varepsilon_{Si}}{t_{Si}}$. The apostrophe on ε_{SiO_2} means that the front SiO_2 layer, also known as interfacial layer, features a different dielectric permittivity from its bulk counterpart because its thickness (only 1.3 nm-thick).

Starting from the one-dimensional Poisson's equation and using the depletion approximation, one can derive the potential φ and the electric field F as a function of the depth x in the Si-film:

$$\varphi(x) = \varphi_{sf} + \left(\frac{\varphi_{sf} - \varphi_{sb}}{t_{Si}} - \frac{qN_A t_{Si}}{2\varepsilon_{Si}} \right) x + \frac{qN_A}{2\varepsilon_{Si}} \tag{3.6}$$

$$F(x) = \left(\frac{\varphi_{sf} - \varphi_{sb}}{t_{Si}} + \frac{qN_A t_{Si}}{2\varepsilon_{Si}} \right) x - \frac{qN_A}{\varepsilon_{Si}} x \tag{3.7}$$

In order to further simplify the above equations, the depletion charge can be neglected because its impact is negligible on the potential in ultra-thin low-doped Si films [24]. One thus obtains

$$\varphi(x) = \varphi_{sf} - Fx \tag{3.8}$$

$$F = \frac{\varphi_{sf} - \varphi_{sb}}{t_{Si}} \tag{3.9}$$

This result implies that the electric field is approximately independent of x. From Equations 3.8 and 3.9 and their related approximations, one finds by solving Gauss' law at the front and back interfaces the two well-known equations describing the charge coupling between the front and back gates in weakly inverted low-doped SOI MOSFETs [24]:

$$V_G = \Delta\Phi_{fi} + \left(1 + \frac{C_{Si}}{C_{of}} \right) \varphi_{sf} - \frac{C_{Si}}{C_{of}} \varphi_{sb} \tag{3.10}$$

$$V_B = \Delta\Phi_{bi} + \left(1 + \frac{C_{Si}}{C_{ob}} \right) \varphi_{sb} - \frac{C_{Si}}{C_{ob}} \varphi_{sf} \tag{3.11}$$

$$\tag{3.12}$$

If the inversion layer is predominantly formed near the the front surface, φ_{sf} will be set to φ_{sf_thresh} under threshold conditions. However, if the inversion layer is predominantly formed near the the back surface, φ_{sb} will be set to φ_{sb_thresh} under threshold conditions. Therefore, by rearranging Equations 3.9, 3.10 and 3.11, one can express the threshold electric field F_{thresh} and the front-gate threshold voltage V_{THf} for the front-channel (FC) and back-channel (BC) conduction as a function of V_B, φ_{sf_thresh} and φ_{sb_thresh}:

$$F_{thresh}^{FC}(V_B) = \frac{C_{Si} C_{ob}}{(C_{Si} + C_{ob})} \frac{\varphi_{sf\_thresh} - (V_B - \Delta\Phi_{bi})}{\varepsilon_{Si}} \tag{3.13}$$

$$F_{thresh}^{BC}(V_B) = C_{ob} \frac{\varphi_{sb\_thresh} - (V_B - \Delta\Phi_{bi})}{\varepsilon_{Si}} \tag{3.14}$$

$$V_{THf}^{FC}(V_B) = \Delta\Phi_{fi} + \left(1 + \frac{C_{Si}C_{ob}}{C_{of}(C_{Si}+C_{ob})}\right)\varphi_{sf\_thresh}(V_B) - \frac{C_{Si}C_{ob}}{C_{of}(C_{Si}+C_{ob})}(V_B - \Delta\Phi_{bi}) \tag{3.15}$$

$$V_{THf}^{BC}(V_B) = \Delta\Phi_{bi} + \left(1 + \frac{C_{ob}(C_{Si}+C_{of})}{C_{of}C_{Si}}\right)\varphi_{sb\_thresh}(V_B) - \frac{C_{ob}(C_{Si}+C_{of})}{C_{of}C_{Si}}(V_B - \Delta\Phi_{bi}) \tag{3.16}$$

In order to finalize the classical analytical model, one still needs to determine $\varphi_{sf\_thresh}(V_B)$ and $\varphi_{sb\_thresh}(V_B)$. For this purpose, the threshold voltage will be defined as the gate voltage corresponding to the maximum of the second derivative of the inversion carrier density $\frac{\mathrm{d}^2 N_{inv}}{\mathrm{d}V_G^2}$. A critical value of the inversion carrier density corresponding to this criterion (maximum of $\frac{\mathrm{d}^2 N_{inv}}{\mathrm{d}V_G^2}$) can be derived from the unified control charge model (UCCM) [26]:

$$N_{inv\_thresh} = \frac{n\phi_T C_{of}}{2q} \tag{3.17}$$

Where the body factor n is

$$n = 1 + \frac{C_{Si}C_{ob}}{C_{of}(C_{Si}+C_{ob})} \tag{3.18}$$

Using Equation 3.8 around threshold, the inversion carrier density can be expressed as

$$\begin{aligned} N_{inv}^{classic} &= \int_0^{t_{Si}} n(x)\mathrm{d}x \\ &= \phi_T n_i \frac{t_{Si}}{|\varphi_{sf} - \varphi_{sb}|}\left|\exp\left(\frac{\varphi_{sf}}{\phi_T}\right) - \exp\left(\frac{\varphi_{sb}}{\phi_T}\right)\right| \\ &= n_i \frac{\phi_T}{|F|}\exp\big(\varphi_{sf(b)}\big)\left[1 - \exp\left(-\frac{|F|t_{Si}}{\phi_T}\right)\right] \end{aligned} \tag{3.19}$$

The front φ_{sf_thresh} and back φ_{sb_thresh} threshold surface potentials are finally obtained by equating 3.17 to 3.19:

$$\varphi_{sf(b)\_thresh}(V_B) = \phi_T \ln\left[\frac{nC_{of}\big|F_{thresh}^{FC(BC)}(V_B)\big|}{2qn_i\Big(1 - \exp\Big(-\big|F_{thresh}^{FC(BC)}(V_B)\big|t_{Si}/\phi_T\Big)\Big)}\right] \tag{3.20}$$

One can notice that in order to solve Equation 3.20 in the front and back conduction regimes, one needs the threshold electric fields $F_{thresh}^{FC}(V_B)$ and $F_{thresh}^{BC}(V_B)$, which are dependent on the threshold surface potentials as described by Equations 3.13 and 3.14. This set of equations can be solved numerically and the values of $\varphi_{sf\_thresh}(V_B)$ and $\varphi_{sb\_thresh}(V_B)$ can be replaced in Equations 3.15 and 3.16 to obtain the coupling characteristics.

The modelling presented above is essentially a classical approach and does not take into account QM effects resulting from the structural confinement (thickness-induced confinement due to thin t_{Si}) and electrical confinement (field-induced confinement). Hence, using the approximations presented in [7], the field-induced QM effects can be introduced by expressing the threshold surface potential as

$$\varphi_{sf(b)\_thresh}^{QM} = \varphi_{sf(b)\_thresh}^{classic} + \frac{\Delta E_0(F_{thresh})}{q} - \phi_T \ln\left(\frac{\Delta E_0(F_{thresh})}{2\phi_T}\right) \tag{3.21}$$

Where $\Delta E_0(F)$ is the pseudo-bandgap widening given by

$$\Delta E_0(F) = \left(\frac{\hbar^2}{2m_x q}\right)^{\frac{1}{3}} \left(\frac{3}{2}\pi\left|F\right|\right)^{\frac{2}{3}} \tag{3.22}$$

Where $\hbar$ is the reduced Planck's constant and m_x is the carrier effective mass in the confinement direction.

Coupling characteristics In order to assess the quality of the analytical model and stress out the impact of QM effects in UTBB FDSOI transistors, the full model using the surface potential quantum correction (Equation 3.22) will be compared to TCAD simulations performed on the nMOSFET shown in Section 3.1. Since this study focuses on the vertical coupling characteristics, it was decided to increase the default gate length (28 nm) to 120 nm to avoid small-geometry effects. Although most of the experimental studies of the coupling characteristics are made on transistors with gate lengths larger than 1 µm (e.g. 10 µm in Rudenko et al. [7] or 100 µm in Ohata et al. [23]), larger structures greatly increases the simulation time and some convergence problems start appearing for high back-gate biases.

The next point to address is the threshold voltage extraction method used to obtain the coupling characteristics from TCAD simulations. The method selected for this purpose is the derivative of the gate-to-channel capacitance $\frac{\mathrm{d}C_{gc}}{\mathrm{d}V_G}$ as it originates from the unified charge control model and corresponds to the same V_{Th} criterion (maximum of $\frac{\mathrm{d}^2 N_{inv}}{\mathrm{d}V_G^2}$) used in the analytical model. However, since C_{gc} is not directly available, the coupling characteristics are computed based on the total gate capacitance C_{gg}. For rather long-channel transistors with no source-to-drain voltage, the channel under the gate is relatively uniform (see Figure A.1) and the contribution of parasitic gate capacitances is expected to be small compared to C_{gc}, thereby, the threshold voltage extraction method is directly applied to C_{gg} measurements instead. In [13], Morelle et al. used an "a posteriori" verification and confirmed that the values of the threshold voltage extracted from C_{gc} and C_{gg} were almost superimposed. Figure 3.9 shows the $C_{gg} - V_G$ curves for LVT transistors computed from a TCAD small signal AC analysis at $f = 100\,\mathrm{kHz}$. The $C_{gg} - V_G$ curves clearly exhibit a plateau for high positive back-gate biases (black curves) that is related to the creation of an inversion layer at the back interface.

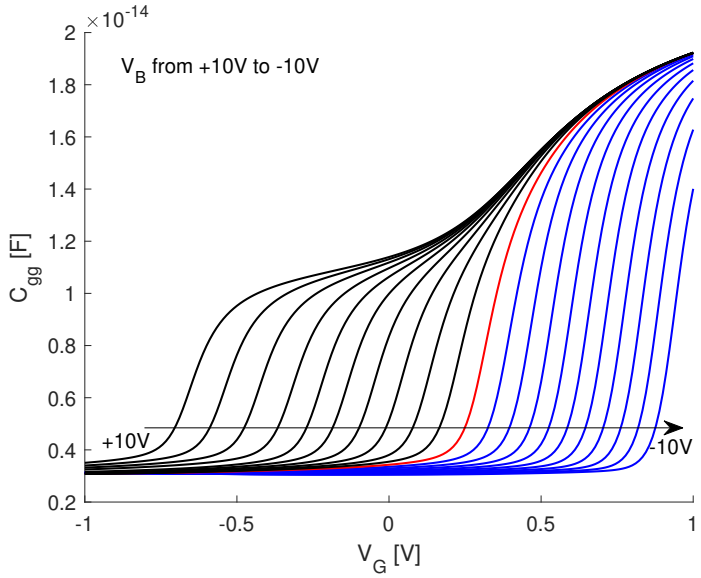


Figure 3.9: Gate capacitance C_{gg} versus front-gate voltage V_G for various back-gate voltages V_B for nMOSFETs with N-type ground plane at $V_{DS} = 0\,\mathrm{V}$. The AC analysis is performed at $f = 100\,\mathrm{kHz}$ ($L_g = 120\,\mathrm{nm}$ and $W = 1\,\mu\mathrm{m}$). Black curves correspond to positive back-gate biases while blue curves correspond to negative back-gate biases. The red curve is at $V_B = 0\,\mathrm{V}$.

The derivative of the $C_{gg} - V_G$ curves is shown in Figure 3.10 where two distinct peaks can be noticed. The position of these peaks mainly depends on the interface at which channel conduction takes place. The first peak observed for positive back-gate biases (black curves) is due to the activation of the back channel conduction. Its position varies with V_B and it corresponds to the modulation of front-gate threshold voltage in the back channel conduction regime $V_{THf}^{BC}(V_B)$. The second peak, whose position is independent of V_B, gives the front-gate threshold when the back interface is inverted $V_{THf}^{back,inv}$. In the front-channel conduction regime (negative back-gate biases represented by blue curves), only a single peak corresponding to the activation of the front channel is visible. Its dependence on V_B gives the coupling characteristics $V_{THf}^{FC}(V_B)$ in the front-channel conduction regime.

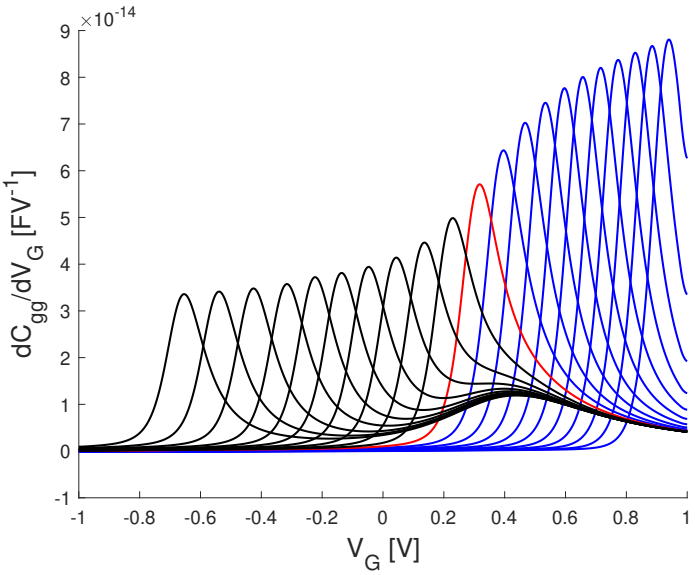


Figure 3.10: Derivative of the gate capacitance C_{gg} versus front-gate voltage V_G for various back-gate voltages V_B for nMOSFETs with N-type ground plane at $V_{DS} = 0\,\text{V}$. The AC analysis is performed at $f = 100\,\text{kHz}$ ($L_g = 120\,\text{nm}$ and $W = 1\,\mu\text{m}$). The same color notation as in Figure 3.9 is used here.

The coupling characteristics obtained from the maximum of C_{gg} derivative are shown in Figure 3.11 for two types of transistors (LVT and RVT transistors). The analytical model derived in the previous section is also depicted, showing a good agreement with TCAD simulations. One can note the difference between the classical (dashed lines) and QM (full lines) modelling. Indeed, the modulation of the threshold voltage at one gate by the opposite gate bias is seen to be enhanced by QM effects resulting in a larger (smaller) slope of the coupling curves in the front-channel (back-channel) conduction regime. However, the analytical model does not take into account the substrate impact on the threshold voltage. Knowing that the back-gate of UTBB FDSOI transistors is made of doped silicon, it is important to account its possible effect on the coupling characteristics. In [27], Burignat et al. investigated the influence of the space charge condition at the BOX/substrate interface on both the threshold voltage and the subthreshold slope. They observed a plateau between $V_B = 0\,\text{V}$ and $V_B = 1\,\text{V}$ in the coupling characteristics of UTBB transistors which was associated to a depletion layer formed at the BOX/substrate interface for these specific bias conditions. From an electrostatic point of view, this depletion layer can be associated to a thickening of the BOX. The GP doping level, its type as well as the back-gate bias define the thickness and existence of this depletion layer. In [28], Kushwaha et al. successfully tried to incorporate the substrate depletion effect in the surface-potential based BSIM-IMG model by computing the potential drop in the substrate due to the back-bias. They also show that the use of high doping levels for GP implementation reduces the substrate depletion effect. In our case, the doping just below the buried oxide is around 10^{18}cm^{-3} for both N-type GP and P-type GP which is consistent with the value found in [28] for highly-doped N-type ground plane.

In Figure 3.11, one can also note the higher threshold voltage featured by the RVT transistor (P-type GP) compared to the threshold voltage of the LVT transistor (N-type GP). This is due to the workfunction difference between the channel and BOX/substrate interface [29].

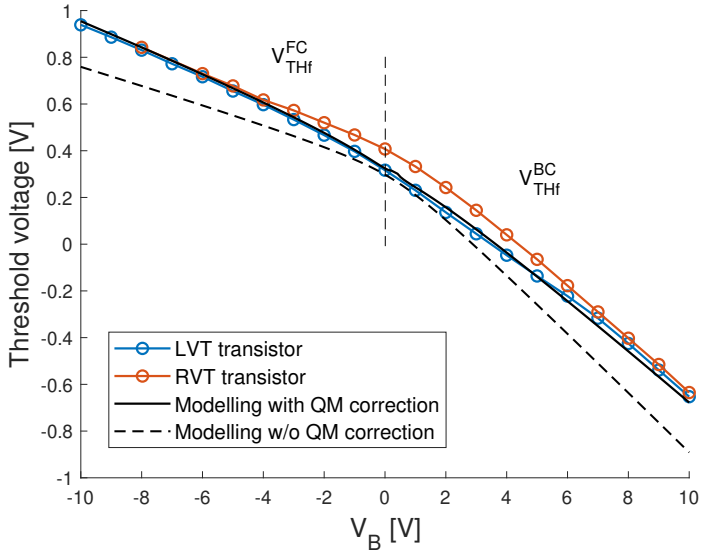


Figure 3.11: Coupling characteristics of UTBB FDSOI nMOSFETs with N-type (LVT) and P-type (RVT) ground plane ($L_g = 120\,\text{nm}$ and $W = 1\,\mu\text{m}$). Black curves indicate the classical (dashed) and QM (full) analytical model.

3.4 Comparison of different threshold voltage extraction methods

In this section, several threshold voltage extraction methods are compared in order to highlight their advantages and disadvantages. The following study is limited to back-gate biases ranging from $V_B = -3\,\text{V}$ to $V_B = 3\,\text{V}$ because the regular-well and flip-well architectures are designed for $V_B = [-3; V_{DD}/2 + 0.3]\text{V}$ (reverse back biasing) and $V_B = [-0.3; 3]\text{V}$ (forward back biasing), respectively [30].

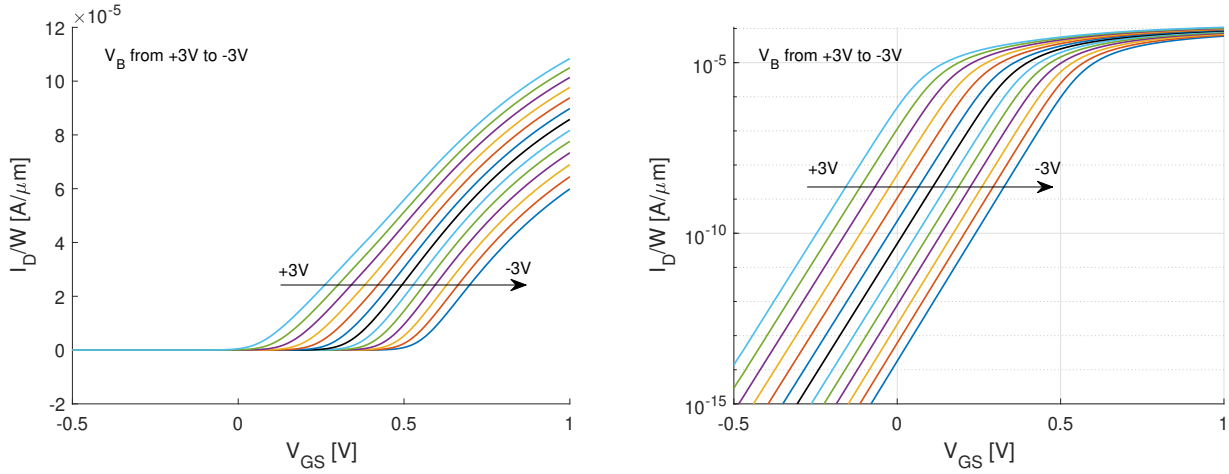
The maximum of the derivative of the gate capacitance C_{gg} (in all rigor, the gate-to-channel capacitance should be used) will be compared to some of the well-known threshold voltage extraction techniques based on $I_D - V_{GS}$ characteristics. The following threshold voltage extraction methods are thus considered:

- Linear extrapolation: The threshold voltage is found from the intercept of the $I_{DS} - V_{GS}$ curve extrapolation at its maximum first derivative point ($g_{m,max}$) with the gate-voltage axis ($I_{DS} = 0\,\text{V}$) in the linear regime.
- Second derivative method: V_{TH} is determined as the gate voltage at which the second derivative of the drain current with respect to the gate voltage is maximum.
- Derivative of g_m/I_D ratio: V_{TH} is determined as the gate voltage at which $-\frac{\mathrm{d}g_m/I_D}{\mathrm{d}V_G}$ is maximum [31].

3.4.1 TCAD Simulations

The simulated drain current I_D as a function of the front-gate voltage V_{GS} for various back-gate biases is plotted in Figure 3.12. The device considered here is an UTBB FDSOI nMOSFET with a N-type (LVT) ground plane. Its gate length is 120 nm while its width is still fixed to the default 1 µm-width assumed in 2D simulations. The simulations are performed in the linear regime at $V_{DS} = 50\,\text{mV}$. One can observe the impact of the back-gate bias on these $I_D - V_{GS}$

characteristics as explained in Section 3.3.1. For positive back-gate biases, the curve is shifted to the left (FBB) while for negative back-gate biases (RBB), the curve is shifted to the right. The black curve corresponds to $V_B = 0\,\mathrm{V}$.



(a) (b)

Figure 3.12: $I_D - V_{GS}$ characteristics of an UTBB FDSOI nMOSFET ($L_g = 120\,\mathrm{nm}$) with a N-type (LVT) ground plane for V_B ranging from $-3\,\mathrm{V}$ to $3\,\mathrm{V}$ by steps of $500\,\mathrm{mV}$: (a) in linear scale and (b) in semi-logarithmic scale. The TCAD simulations are performed in the linear regime at $V_{DS} = 50\,\mathrm{mV}$.

In order to gain some insight into the threshold voltage extraction procedure of each method, one can plot the transconductance g_m as a function of the front-gate voltage for various back-gate biases. The result is shown in Figure 3.13. Similar to the C_{gg} characteristics, a plateau in the transconductance curves is visible for positive back-gate biases.

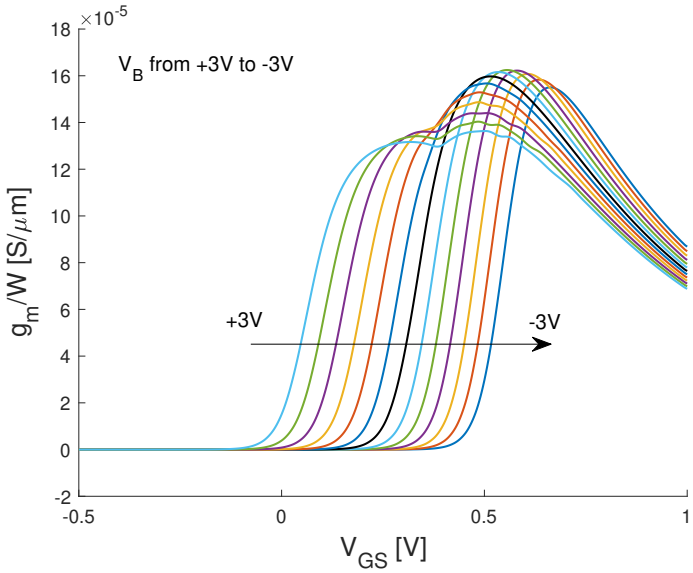


Figure 3.13: Transconductance g_m versus front-gate voltage V_G for various back-gate biases. The TCAD simulations are performed in the linear regime at $V_{DS} = 50\,\mathrm{mV}$. $L_g = 120\,\mathrm{nm}$

The different threshold voltage extraction methods based on the drain current measurements are compared to the maximum of C_{gg} derivative in Figure 3.14. The first thing that stands out is the huge offset for this technology node between the linear extrapolation method and the others methods. At $V_{GS} = 0\,\mathrm{V}$, a difference of 45 mV is observed between the linear extrapolation and the $\mathrm{d}C_{gg}/\mathrm{d}V_{GS}$ methods. It corresponds to an increase of 13%. This difference becomes even larger for positive back-gate biases. It can be explained by the fact that for positive back-gate biases, the maximum of the transconductance g_m is almost constant at around $V_G = 0.49\,\mathrm{V}$ (see Figure 3.13). Therefore, the point at which the extrapolation is performed (by drawing a tangent to $I_D - V_{GS}$ curve) is almost fixed. However, the current slope at $V_G|g_{m,max}$ becomes steeper when V_B is increased to more positive values which results in a larger gate-voltage intercept. This discrepancy can also be explained by the fact that the linear extrapolation technique assumed that the inversion charge varies linearly with V_G above threshold which is incorrect for UTBB transistors featuring very thin gate dielectrics [31].

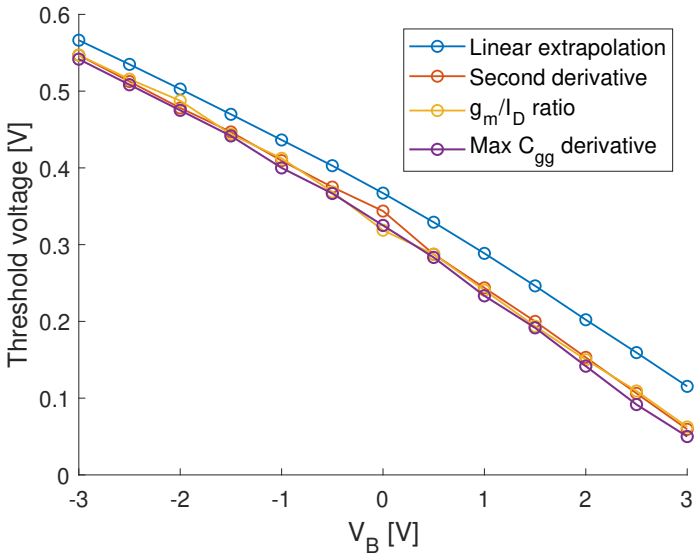


Figure 3.14: Comparison of the coupling characteristics of UTBB FDSOI nMOSFETs with N-type (LVT) ground plane obtained from different threshold voltage extraction methods ($L_g = 120\,\mathrm{nm}$).

On the other hand, the second derivative and g_m/I_D ratio methods show a good agreement with the maximum of C_{gg} derivative method. Indeed, these three methods are derived from the same V_{TH} criterion corresponding to the maximum of the second derivative of the inversion charge N_{inv}. Starting from the unified charge-control model [26], the derivative of the gate-to-channel capacitance is given by

$$\frac{\mathrm{d}C_{gc}}{\mathrm{d}V_G} = -C_{ox}\frac{\mathrm{d}^2\varphi_s}{\mathrm{d}V_G^2} \tag{3.23}$$

The g_m/I_D ratio method proposed by Flandre et al. [32] gives a similar expression which only differs by a factor $\frac{-C_{ox}q}{kT}$:

$$\frac{\mathrm{d}}{\mathrm{d}V_G}\left(\frac{g_m}{I_D}\right) = \frac{q}{kT}\frac{\mathrm{d}^2\varphi_s}{\mathrm{d}V_G^2} \tag{3.24}$$

Figures 3.15 and 3.16 show the peaks at which the threshold voltage is extracted for the second derivative and g_m/I_D ratio methods. It can be seen in Figure 3.16 that a second peak is present

around $V_G = 0.41\,\mathrm{V}$. Its position is constant with respect to V_B and it is associated to the front-threshold voltage when the back surface is inverted $V_{THf}^{Inv,back}$. However, compared to C_{gg} derivative measurements, this second peak is less pronounced for drain current measurements. In Figure 3.16, for g_m/I_D technique, only one peak remains which corresponds to the formation of an inversion layer at the back surface for positive V_B. This result showcases the difficulty to distinguish the front and back conduction channels from $I_D - V_{GS}$ characteristics.

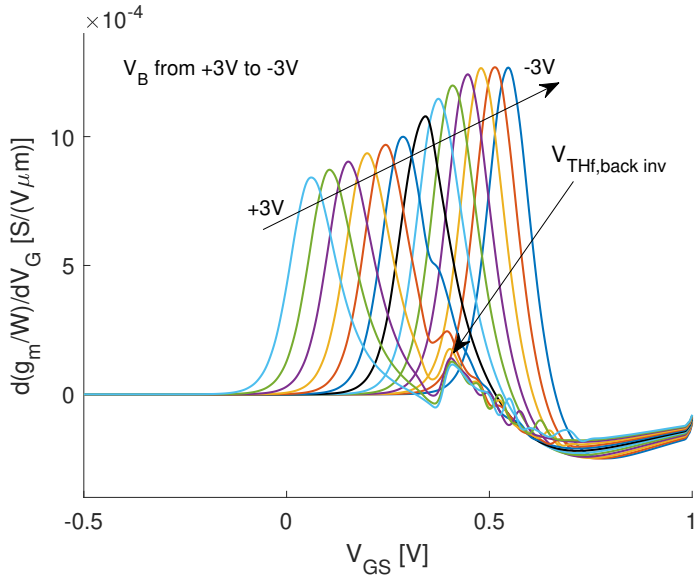


Figure 3.15: Second derivative of the drain current as a function of the front-gate voltage for various back-gate biases. ($L_g = 120\,\mathrm{nm}$).

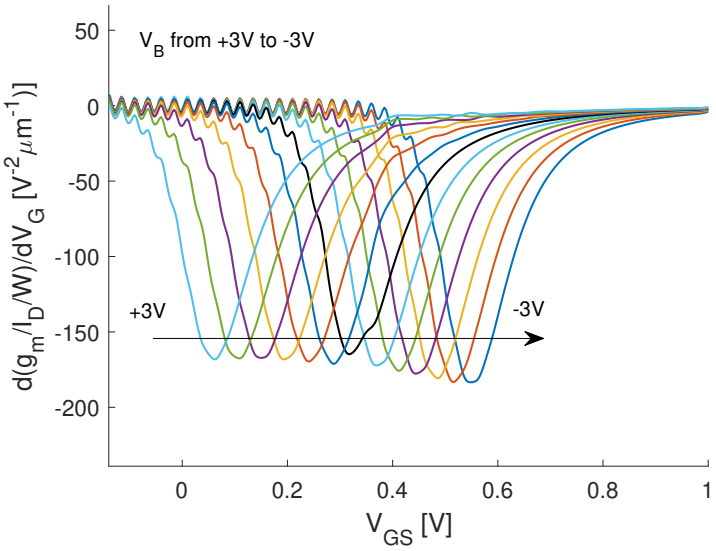


Figure 3.16: Derivative of the g_m/I_D ratio as a function of the front-gate voltage for various back-gate biases. ($L_g = 120\,\mathrm{nm}$).

Finally, the mismatch between the threshold voltage extracted from the C_{gg} derivative and g_m/I_D ratio methods is reported in Figure 3.17. The maximum mismatch is obtained for $V_B = 2.5\,\mathrm{V}$

with a value of 17.7 mV. In general, the C_{gg} derivative method appears to give better results for short transistors because on one hand, it enables front and back channel separation and on the other hand, it is unaffected by the gate-voltage-dependent mobility and series resistances effects unlike other current-based methods [7]. However, due to the low dimensions of these advanced devices, C_{gg} capacitance can become very small and thus extremely difficult to measure. In TCAD simulations, this is not an issue because it does not depend on any measurement setup but in reality, parasitic elements can dominate over C_{gg}, being below the measurement capabilities of the equipment. Moreover, RF transistors with dedicated RF pads are not always available in the early stages of characterization giving another reason to find new threshold voltage extraction techniques.

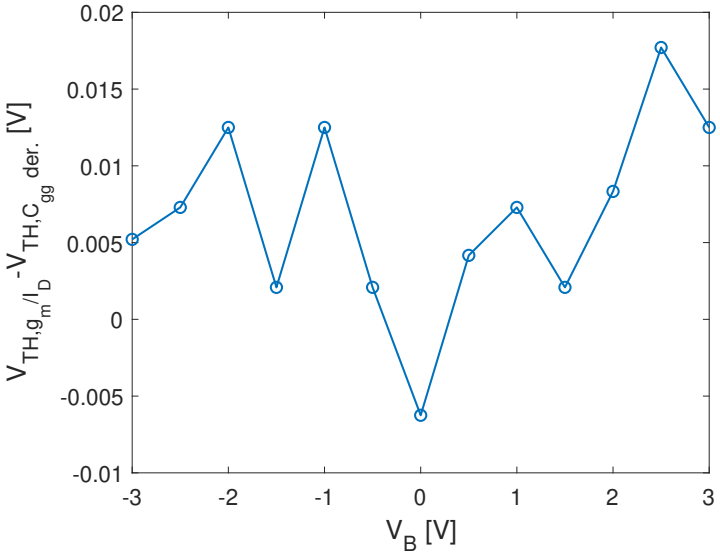


Figure 3.17: Mismatch between the threshold voltage extracted from the C_{gg} derivative and g_m/I_D ratio methods as a function of back-gate bias ($L_g = 120\,\text{nm}$).

The slopes for each method in FBB and RBB are summarized in Table 3.3.

Method	Slope (in mV/V) for $V_B < 0\,\text{V}$	Slope (in mV/V) for $V_B > 0\,\text{V}$
Linear extrapolation	-66	-84
Second derivative	-68	-93
g_m/I_D ratio	-75	-87
Max of C_{gg} derivative	-72	-93

Table 3.3: List of slopes of the coupling characteristics for each method ($L_g = 120\,\text{nm}$).

As a final comment regarding the current-based extraction methods, it should be noted that the transconductance g_m versus V_G graph only presents a single clearly visible peak for shorter-nodes. This is illustrated in Figure 3.18 for a short-channel transistor with a gate length of 30 nm. All other device/structural parameters are identical to those of the 120 nm UTBB FDSOI nFET previously studied. In [23], Ohata et al. reported the same behaviour for short-channel transistors

and concluded that the series resistance affects the transconductance curve. Therefore, as it can be seen in Figure 3.19, the linear extrapolation method gives threshold voltages closer to the other methods for $L_g = 30\,\text{nm}$ thanks to the disappearance of this second peak. Table 3.4 summarizes the slopes of the coupling characteristics for $L_g = 30\,\text{nm}$.

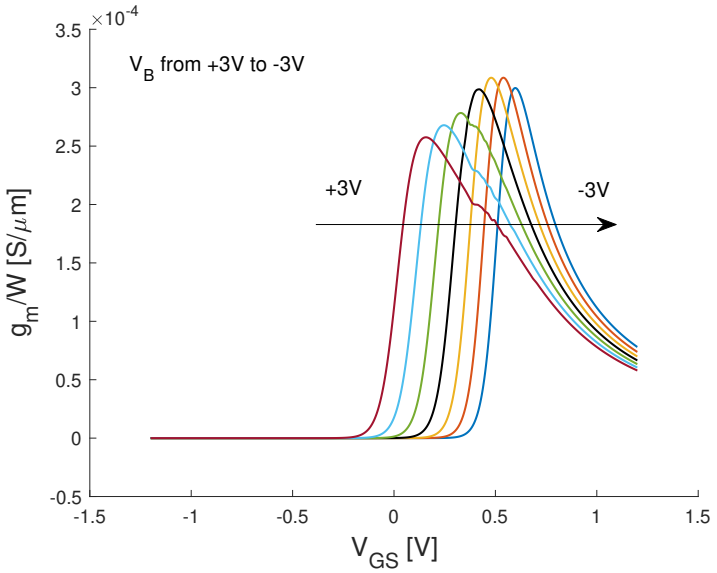


Figure 3.18: Transconductance g_m versus front-gate voltage V_G for V_B ranging from $-3\,\text{V}$ to $3\,\text{V}$ by steps of $1\,\text{V}$. The TCAD simulations are performed in the linear regime at $V_{DS} = 50\,\text{mV}$. $L_g = 30\,\text{nm}$.

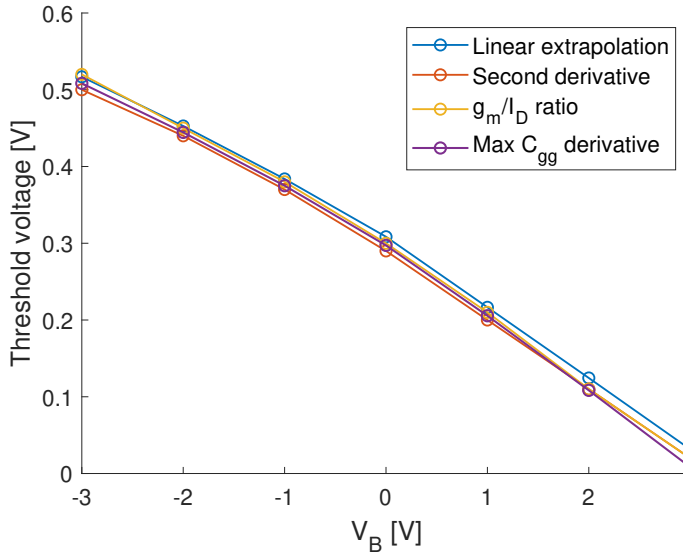


Figure 3.19: Comparison of the coupling characteristics of UTBB FDSOI nMOSFETs with N-type (LVT) ground plane obtained from different threshold voltage extraction methods ($L_g = 30\,\text{nm}$).

Method	Slope (in mV/V) for $V_B < 0\,\mathrm{V}$	Slope (in mV/V) for $V_B > 0\,\mathrm{V}$
Linear extrapolation	-69	-92
Second derivative	-70	-90
g_m/I_D ratio	-73	-94
Max of C_{gg} derivative	-70	-96

Table 3.4: List of slopes of the coupling characteristics for each method ($L_g = 30\,\mathrm{nm}$).

3.4.2 Measurements

In the previous section, several threshold voltage extraction methods were compared using 2D TCAD simulations. In this section, the same methods will be applied to experimental data. The measurements were performed on a four-port SLVT nFET with $L_g = 20\,\mathrm{nm}$ and 64 fingers with $W_{finger} = 1\,\mu\mathrm{m}$. Their are implemented using the 22FDX technology from *GlobalFoundries*. The Si film, the BOX and the substrate thicknesses are 6 nm, 20 nm and 150 µm, respectively.

The I-V curves were measured in the linear regime at $V_{DS} = 50\,\mathrm{mV}$ and the front-gate voltage was swept from $V_G = -0.2\,\mathrm{V}$ to $V_G = 0.92\,\mathrm{V}$ by steps of 10 mV. In order to compute the coupling characteristics, the back-gate voltage was also swept from $V_B = 0\,\mathrm{V}$ to $V_B = 3\,\mathrm{V}$.

The C_{gg} measurements were obtained by averaging the imaginary part of $Y_{GG}/2\pi f$ over the frequency range $f = [1; 5\,\mathrm{GHz}]$ as shown in Figure 3.20. Thus, the S-parameters measured in cold FET regime ($V_{DS} = 0\,\mathrm{V}$) with $V_G = [-0.2; 0.5\,\mathrm{V}]$ by steps of 10 mV were converted into Y-parameters. The same back-gate bias range used for the I-V curves was employed for S-parameters measurements. Y_{GG} is defined as $Y_{GG} = i_g/v_g\big|_{v_k=0\,\mathrm{V}}$ where v_k is the small-signal voltage at port $k \neq g$. "g" refers to the gate, "d" to the drain, "s" to the source and "b" to back-gate.

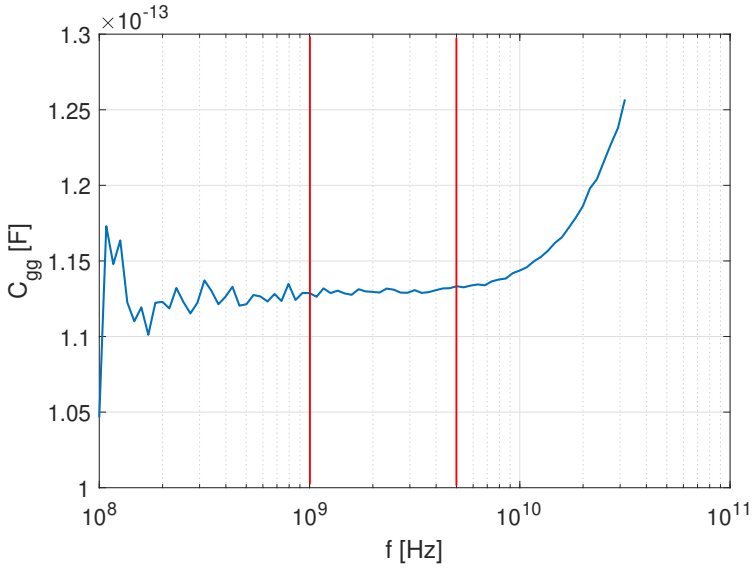
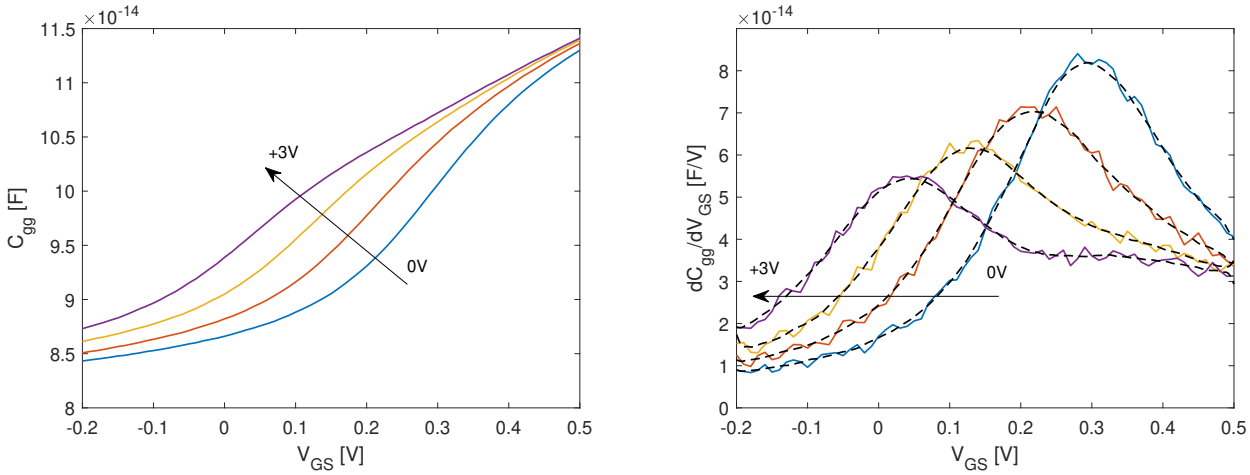


Figure 3.20: Extraction of C_{gg} by averaging $Y_{GG}/2\pi f$ between 1 GHz and 5 GHz. The bias conditions here are $V_G = 0\,\mathrm{V}$, $V_{DS} = 0\,\mathrm{V}$ (cold FET) and $V_B = 0\,\mathrm{V}$.

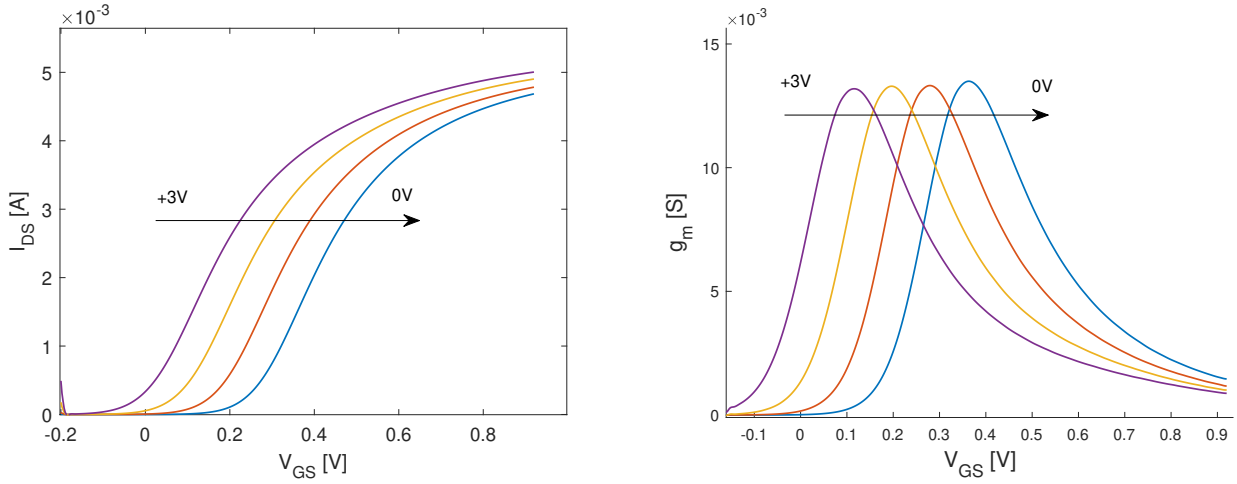
The $C_{gg}(V_{GS})$ curves as well as their derivatives for positive back-gate bias are shown in Figures 3.21a and 3.21b, respectively. Before extracting V_{TH}, the C_{gg} derivative curves were first interpolated and then smoothed by a moving average filter in order to attenuate the "noise" and have a well-defined peak. The dashed lines correspond to the interpolated and smoothed version of C_{gg} derivative curves. One can also note the formation of a second peak corresponding to $V_{THf}^{back,Inv}$ at $V_B = 3\,\mathrm{V}$ around $V_G \approx 0.4\,\mathrm{V}$.



(a) (b)

Figure 3.21: (a) C_{gg} as a function of the front-gate voltage V_{GS} for V_B ranging from 0 V to 3 V by steps of 1 V. (b) C_{gg} derivative versus V_{GS} for V_B ranging from 0 V to 3 V by steps of 1 V.

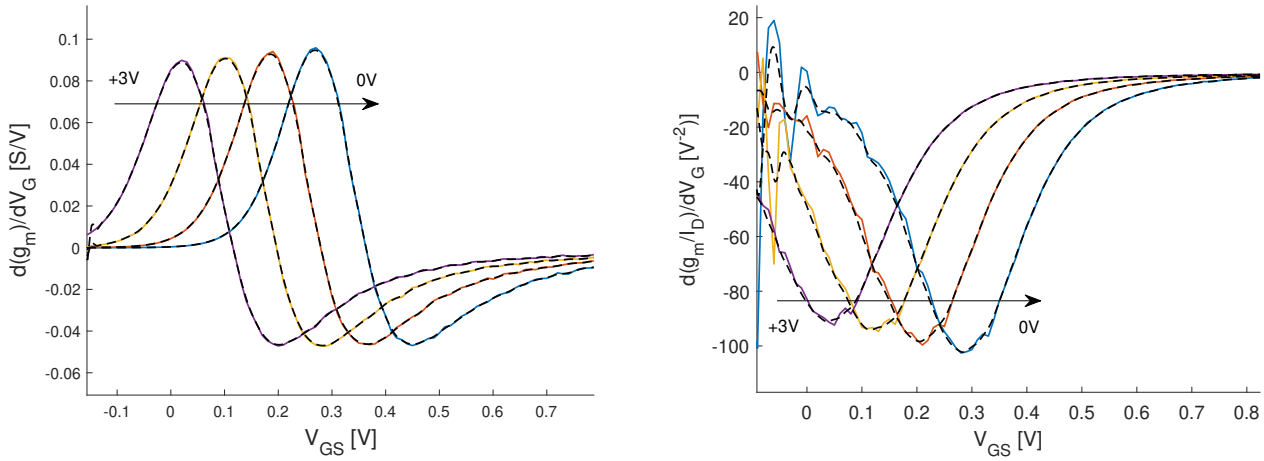
In linear regime, the drain current and the transconductance as a function of V_{GS} are shown in Figures 3.22a and 3.22b. The 0.5 V (i.e. 0.5 V,1.5 V,2.5 V) steps are omitted for clarity. The drain current clearly displays non-linear behaviour with respect to V_{GS} which is deemed to be the S/D resistance effect. Only a single peak can be observed in the transconductance which agrees with TCAD simulations for short-channel transistors (see Figure 3.18 and the findings in [23].



(a) (b)

Figure 3.22: (a) Drain current and (b) transconductance as a function of V_{GS} for V_B ranging from 0 V to 3 V by steps of 1 V. $V_{DS} = 50\,\text{mV}$.

In order to extract V_{TH} using drain-based methods, the same interpolation and smoothing steps are applied to $\mathrm{d}g_m/\mathrm{d}V_G$ and $\mathrm{d}(g_m/I_D)/\mathrm{d}V_G$. The fitted results are shown in Figures 3.23a and 3.23b. The implementation of these two methods are highly sensitive to measurement error and noise and thus required good experimental setup [33]. Aside from numerical smoothing techniques, fitting a semi-empiric model is also a common technique used to reduce measurement noise. In our case, one can see that $\mathrm{d}(g_m/I_D)/\mathrm{d}V_G$ is more impacted by measurement noise than $\mathrm{d}g_m/\mathrm{d}V_G$.



(a) (b)

Figure 3.23: (a) Derivative of (a) the transconductance and (b) the g_m/I_D ratio with respect to V_{GS} for V_B ranging from 0 V to 3 V by steps of 1 V.

All the threshold voltage extraction methods presented above are applied to the same transistor coming from three different dies. By comparing multiple die measurements, one can assess the global trend of each method and their variability. Since all the coupling curves of the three dies

have similar trends (see Figures A.2,A.3, A.4 and A.5) and that the errors between them are within the range of $\Delta V_{GS} = 10\,\text{mV}$ step[1], it was decided to only show the coupling characteristics of Die 1. Figure 3.24 shows the coupling characteristics of Die 1 obtained from different threshold voltage extraction techniques.

First, it can be seen that the maximum of C_{gg} derivative method mostly gives higher V_{TH} values than other current-based methods. This result was quite unexpected because in general, C_{gg} derivative method is taken as a reference for the comparison between the second derivative and g_m/I_D ratio methods which are both affected by gate-voltage dependent mobility and series resistance (g_m/I_D ratio method being less sensitive to these effects [31]). One hypothesis is that this method is strongly dependent on the mean channel position (centroid position) as well as the coupling between the front and back gates while others methods only see the "global picture" from drain current data (difficulty to distinguish the front channel from the back channel). The larger values at $V_B = 0\,\text{V}$ and $V_B = 1\,\text{V}$ could be due to the formation of a depletion region just beneath the BOX. Another hypothesis is the implementation of the method itself. Indeed, the extraction of V_{TH} was directly performed on C_{gg} derivative instead of C_{gc} derivative. Therefore, strong parasitic elements, especially for short transistors, should be expected to impact the capacitance measurements and could greatly jeopardize the results of the method. However, varying the frequency range used to extract C_{gg} versus V_{GS} curves (in a "reasonable" manner where $\text{Im}\{Y_G G/(2\pi f)\}$ looks flat) does not significantly impact the threshold voltage extraction.

The second important point is that the g_m/I_D ratio method is shifted by 10 mV at $V_B = 0\,\text{V}$ compared to SD method. This discrepancy increases up to 16 mV at $V_B = 3\,\text{V}$. In [31; 34], Rudenko et al. demonstrated that $\text{d}g_m/\text{d}V_G$ method yields higher V_{TH} values than $\text{d}g_m/I_D/\text{d}V_G$ and $\text{d}C_{gc}/\text{d}V_G$ methods which was attributed to the mobility rise with V_G near threshold. However, instead of a positive shift ($\text{d}g_m/\text{d}V_G$ values higher than $\text{d}g_m/I_D/\text{d}V_G$), a negative shift was observed in the coupling characteristics of Figure 3.24. The reason for that is still unclear but one can mention that all methods require a heavily smoothing step before extracting V_{TH} and thus, it could influence its value depending on the implementation of such filter.

[1] At $V_B = 0\,\text{V}$, Die 3 has the largest difference due to the irregularities in the drain current characteristics as illustrated in Figure A.6.

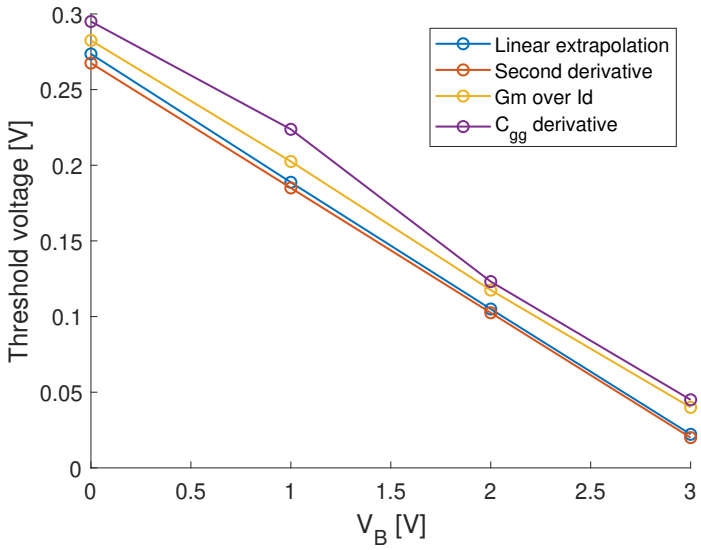


Figure 3.24: Comparison of the coupling characteristics of a SLVT transistor ($L_g = 20\,\text{nm}$) obtained from different threshold voltage extraction methods.

Finally, the slopes for each method are given in Table 3.5. Similar values in the range of 80 mV/V can be found in the literature [30] for the modulation of the threshold voltage by the back-gate bias. However, by comparing these values with the ones previously extracted from TCAD simulations (see Table 3.4), one can observe an approximate difference of $-10\,\text{mV/V}$. First, one should remember that the 28FDSOI technology features different Si film, BOX and effective oxide thicknesses than the 22FDX technology, so it is not suprising to have some differences. 22FDX transistors have a 20 nm-thick BOX against 25 nm for 28FDSOI transistors. A thinner BOX enhances the control of the back-gate on the channel, thereby it does not explain the overall lower slopes of the 22FDX technology. The effective oxide thickness of the 22FDX technology is 1.25 nm whereas it is 1.3 nm for the 28FDSOI technology. A smaller effective oxide thickness means a better control of the channel by the front-gate, therefore it could be a reason for the lower slopes observed in the 22FDX technology. Finally, the smaller Si film thickness of the 22FDX technology (6 nm vs 6.7 nm in 28FDSOI) could also explain these results due to a stronger coupling between the front and back interfaces.

Method	Slope (in mV/V) for $V_B > 0\,\text{V}$
Linear extrapolation	-84
Second derivative	-82
g_m/I_D ratio	-81
Max of C_{gg} derivative	-85

Table 3.5: List of the slopes of the coupling characteristics for each method (Die 1).

3.5 Dependency of other parameters on the back-gate bias

This small section aims to describe the extraction of different parameters and study their dependence on the back-gate bias.

3.5.1 Series resistances

In long-channel transistors, the parasitic series resistances R_S and R_D are usually considered constant and negligible in comparison to the channel resistance R_{ch}. However, as the transistors dimensions decrease, they become comparable to the channel resistance and drastically reduce the transistor performance. Therefore, several extraction methods have been developed. One of them is the total resistance method which can be written as [35]:

$$R_{tot} = R_{ch} + R_{SD} = \frac{L_{eff}}{\mu_{eff} W_{eff} C_{ox} (V_{GS} - V_{TH})} + R_{SD} \tag{3.25}$$

Where L_{eff}, W_{eff} and μ_{eff} are the effective length, width and mobility respectively. By plotting R_{tot} as a function of L_{eff} and doing a linear extrapolation, R_{SD} can be extracted from the intercept with the y-axis at $L_{eff} = 0\,\text{nm}$. This method is often used to extract R_{SD} at a single V_{GS} assuming that R_{SD} is bias-independent. However, by repeating this method for multiple V_{GS}, Henry et al. [36] extracted a bias-dependent resistance $R_{SD}(V_{GS})$. The goal of this section is thus to study if R_{SD} is also dependent on the back-gate bias V_B.

The extraction of $R_{SD}(V_{GS}, V_B)$ will be performed by repeating the same procedure as for $R_{SD}(V_{GS})$ (linear extrapolation with L_{eff}) for each V_B. It will rely on the following assumptions/parameters:

- To compute L_{eff}, Morelle et al. extracted $\Delta L = 1.8\,\text{nm}$ from the linear extrapolation of $C_{gg,norm}$ versus L. This value is also used here since exactly the same transistor deck (Sentaurus simulations) is employed.
- Only two transistors of total length $L_g = 30\,\text{nm}$ and $L_g = 120\,\text{nm}$ are used.
- The threshold voltage variation with the length is neglected but V_{TH} is a function of V_B. To confirm this hypothesis, the threshold voltage of each transistor is computed using the C_{gg} derivative method. The maximum threshold voltage difference between the two transistors is 40 mV at $V_B = 3\,\text{V}$.
- The effective mobility is supposed to be independent of L_{eff}.

Figure 3.25 shows the extracted $R_{SD}(V_{GS}, V_B)$ values obtained from $R_{tot} - L_{eff}$ plots. It can be seen that the variation of V_{TH} due to the back-gate shifts the curves towards lower V_{GS}. In order to have a fair comparison, each curves can be plotted as a function of $V_{ov} = V_{GS} - V_{TH}(V_B)$. This result is depicted in Figure 3.26 where V_{ov} is restricted to $[0.25; 0.66\,\text{V}]$. From this figure, one can conclude that the series resistance R_{SD} is also affected by the back-gate bias. A drop of $48\,\Omega$ (from $304\,\Omega$ to $256\,\Omega$) is measured at $V_{ov} = 0.66\,\text{V}$ by increasing V_B from $-3\,\text{V}$ to $3\,\text{V}$. This could be due to the shift of the mean channel position toward the Si film/BOX interface.

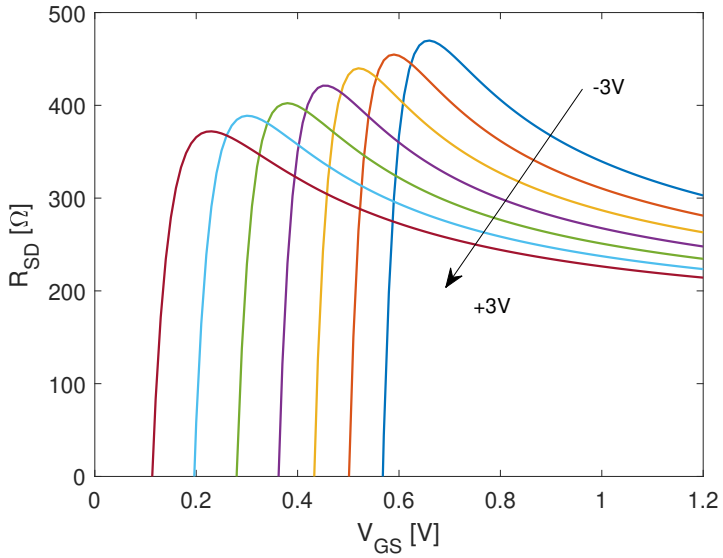


Figure 3.25: R_{SD} versus V_{GS} curves extracted from TCAD simulations with $V_B = [-3; 3\,\mathrm{V}]$.

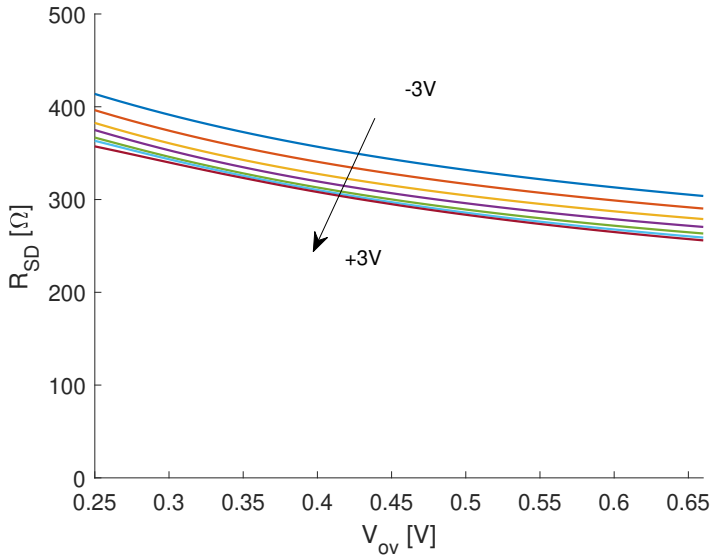


Figure 3.26: R_{SD} versus V_{ov} extracted from TCAD simulations by shifting the curves of Figure 3.25 by the threshold voltage: $V_{ov} = V_{GS} - V_{TH}(V_B)$.

3.5.2 N-well-P-Substrate capacitance

As it will be shown in Section 4.4.2, the reduction of the N-well/P-Substrate capacitance $C_{well-sub}$ with the back-gate bias V_B is one of the main causes of the improvement of the back-gate cut-off frequency f_{Tbg} with V_B. This junction capacitance corresponds to the reversely biased diode between the N-well and P-substrate as illustrated in Figure 3.27. In this simplified schematic, all intrinsic and parasitic elements have been removed except those related to the back-gate (only capacitances).

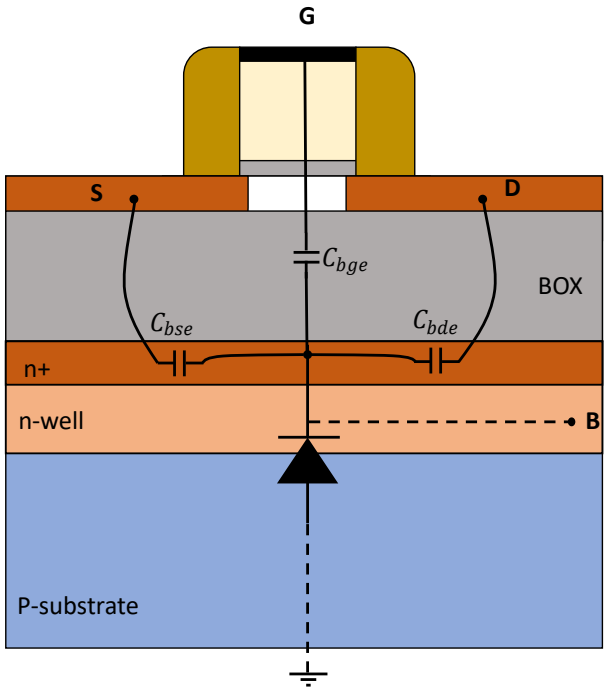


Figure 3.27: Cross-section of the UTBB FDSOI nMOSFET. The access to the n-well from the back-gate contact has been simplified. Only the back-gate related capacitances are represented.

The transistor is here considered to be biased in cold regime ($V_{DS} = 0\,\mathrm{V}$) with $V_{GS} = 0\,\mathrm{V}$. In these conditions, the front and back transconductances g_m and g_{mb} are negligible. By doing a small-signal AC analysis, one can obtain the Y-parameters which describe how the current at terminal i would react if a voltage at terminal j is applied. i and j can be the same and correspond in this case to one of the four terminals of the UTBB FDSOI transistor (i.e. gate, drain, source and back-gate). Supposing that the impact of the series resistances on the *capacitance* matrix ($\mathrm{Im}\{Y\}$) is negligible at low frequencies, one can write

$$\mathrm{Im}\{Y_{41}\} \approx -j\omega C_{bge} \tag{3.26}$$
$$\mathrm{Im}\{Y_{42}\} \approx -j\omega C_{bde} \tag{3.27}$$
$$\mathrm{Im}\{Y_{43}\} \approx -j\omega C_{bse} \tag{3.28}$$
$$\mathrm{Im}\{Y_{44}\} \approx j\omega(C_{bge} + C_{bde} + C_{bse} + C_{well-sub}) \tag{3.29}$$

Where the notation "e" is for extrinsic elements (see Section 4.2.2). $C_{well-sub}$ can thus computed by rearranging the preceding equations

$$C_{well-sub} = \mathrm{Im}\{Y_{44} + Y_{43} + Y_{42} + Y_{41}\}/\omega \tag{3.30}$$

The graphs associated with this step are shown in Figure 3.28 for various back-gate biases. The reduction of $C_{well-sub}$ due to positive V_B is also visible. By doing a cutline of Figure 3.28b at $f = 1\,\mathrm{MHz}$ (as long as it remains below 100 MHz, the chosen frequency has no importance here), one obtains the $C_{well-sub}$ versus V_B curve presented in Figure 3.29. According to this figure, $C_{well-sub}$ seems to be inversely proportional to V_B. Finally, by trying to fit the model of an

abrupt PN junction with $C_{well-sub}$, one can observe a very similar behaviour which confirms the decreasing trend with V_B. The transition capacitance can be obtained from

$$C_T = \frac{AK_a}{\sqrt{\phi_0 + V_b}} \tag{3.31}$$

Where K_a is defined as $\sqrt{\frac{q\epsilon}{2}\frac{N_A N_D}{(N_A+N_D)}}$, ϕ_0 is the junction potential, A is the surface area and $N_{D/A}$ are the doping concentrations.

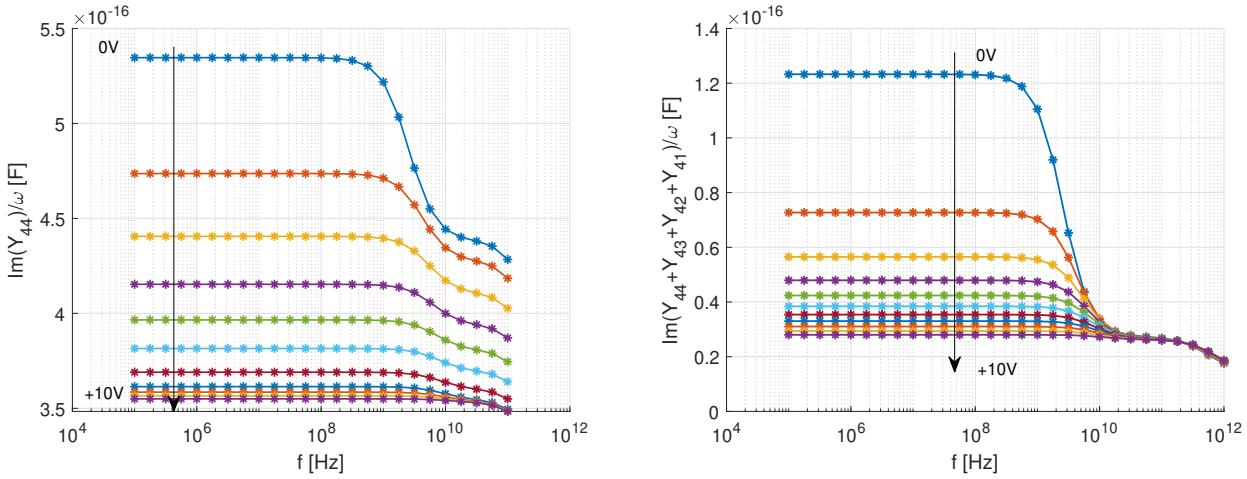


Figure 3.28: (a) $\mathrm{Im}\{Y_{44}\}/\omega$ and (b) $\mathrm{Im}\{Y_{44} + Y_{43} + Y_{42} + Y_{41}\}/\omega$ versus frequency for various back-gate biases: $V_B = [0; 10\,\mathrm{V}]$ by steps of $1\,\mathrm{V}$. $V_{DS} = 0\,\mathrm{V}$ and $V_{GS} = 0\,\mathrm{V}$.

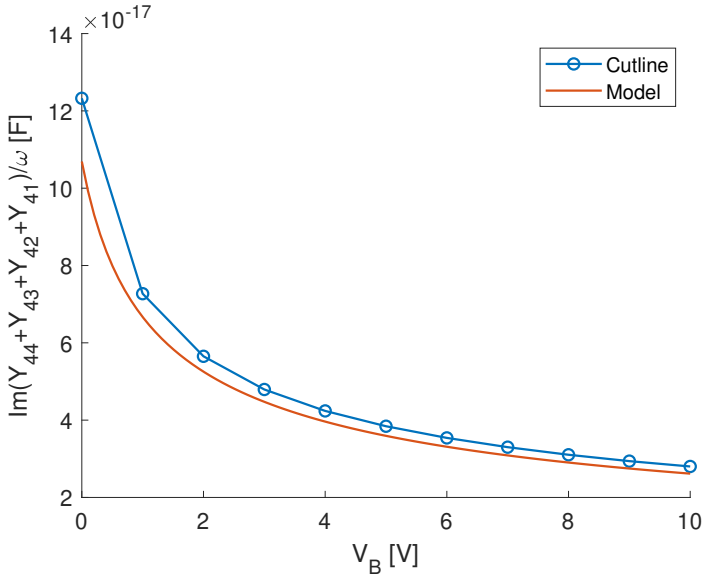


Figure 3.29: Dependence of $C_{well-sub}$ on the back-gate bias. The model of the diode transition capacitance (abrupt doping profiles) is plotted in orange. $V_{DS} = 0\,\mathrm{V}$ and $V_{GS} = 0\,\mathrm{V}$.

3.6 Conclusion

In this chapter, the impact of the back-gate bias on the $I_D - V_{GS}$ characteristics and on the threshold voltage was studied. It was shown that applying a back-gate bias shifts the $I_D - V_{GS}$ characteristics to the left for FBB and to the right for RBB. This effect was analyzed from an analytical point of view by comparing the coupling characteristics obtained with TCAD simulations to the model developed by Rudenko et al. [7]. The formation of a second inversion layer at the BOX/substrate interface was observed to significantly enhance the drivability of the transistor. Then, different V_{TH} extraction techniques were compared and applied to both simulation and experimental data. Although different coupling slopes were observed due to the structural difference between the 28FDSOI and 22FDX technologies, the overall trends are similar. Finally, two parameters, namely the source-to-drain resistance R_{SD} and the N-well/P-substrate capacitance $C_{sub-well}$, demonstrated variations with the back-gate bias.

To summarize, it can be said that Forward Back-Biasing is dedicated to performance enhancement for applications requiring high I_D (and g_m) whereas Reverse Back-Biasing is more appropriate to low-power applications by reducing the leakage current.

Chapter 4

A wideband characterization of UTBB FD-SOI with back-gate access

4.1 Introduction

As described in the previous chapter, one of the most unique features of the UTBB FDSOI technology is the possibility to tune the threshold voltage by applying a back-gate bias. Thanks to ultra-thin buried oxide and GP implementation, dual-gate architectures and back-gate control schemes are achievable [6]. This technology also demonstrates excellent analog and RF performances as reported in [3; 37; 4].

The aim of the present chapter is thus to assess the RF performance of the UTBB FDSOI technology and the impact of the back-gate bias on the main RF Figures of Merit f_T and f_{max}.

This chapter is organized as follows: In Section 4.2, the general theory of small-signal equivalent circuits is presented. The distinction between "intrinsic", "extrinsic" and "access" elements is made. Section 4.3 focuses on the description and extraction of two small-signal equivalent circuits, one being a 3-Port device in a common-source configuration and the other one being a 4-Port device. Finally, the 3-port small-signal equivalent circuit is applied to experimental measurements on 22FDX SLVT transistors in Section 4.4. The impact of the back-gate on both front and back-gate RF FoMs is also analyzed.

4.2 Small signal circuit description

Before describing the extraction procedure developed for 3-port and 4-port UTBB FDSOI MOSFETs, the general theory of small-signal equivalent circuits is presented. The choice of the equivalent circuit topology is important because it can significantly simplify the characterization and modeling tasks [9]. Therefore, the small-signal equivalent circuit described in the next sections is constructed based on the geometry and the underlying physics of the device. Starting from the useful effect of the MOSFETs, all the parasitic elements will be introduced. The complete quasi-static small-signal model derived by Tsividis [38] serves as a basis of this work but it will be further augmented to take into account the extrinsic parasitic elements and the substrate node.

4.2.1 Intrinsic elements

The basic working principle of a transistor consists of the modulation of the current I_{DS} flowing between the source and drain electrodes by a voltage applied to the gate V_{GS}. This is called the useful effect of the transistor. This effect can be modelled by a voltage controlled current source placed between the source and drain as shown in Figure 4.1. The intrinsic transconductance g_{mi} is defined as follows

$$g_{mi} = \frac{\partial I_d}{\partial V_{gs}}\Big|_o = \frac{i_d}{v_{gs}}\Big|_o \tag{4.1}$$

Where "o" means that all other voltages than the one at the denominator are assumed to be constant and equal to their values at the DC bias point. From a small-signal point of view, this means that the small-signal voltages are equal to zero.

Throughout the rest of this work, the following convention is adopted:

- Any voltage or current beginning with a capital letter refers to a DC value.
- Any voltage or current beginning with a lowercase letter refers to a small-signal variation.

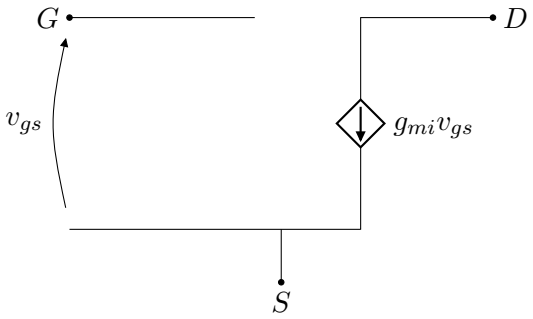


Figure 4.1: Useful effect of the transistor.

However, the equivalent circuit presented in Figure 4.1 is not sufficient to describe the behaviour of the transistor as a large number of parasitic elements also need to be taken into account. Firstly, an intrinsic output conductance is introduced in order to model the MOSFET being an imperfect current source. The output conductance g_{dsi} is defined as

$$g_{dsi} = \frac{\partial I_d}{\partial V_{ds}}\Big|_o = \frac{i_d}{v_{ds}}\Big|_o \tag{4.2}$$

Secondly, the variation of charges at one terminal induced by a small-signal voltage applied to another terminal of the intrinsic transistor is modelled by intrinsic capacitances. Under the quasi-static operation assumption [38], the intrinsic capacitances are defined by the following expressions

$$C_{kki} = -\frac{\partial Q_k}{\partial V_k}\Big|_o \qquad C_{kli} = \frac{\partial Q_k}{\partial V_l}\Big|_o \quad \text{with } k \neq l \tag{4.3}$$

Where k and l are any of the four intrinsic terminals: G (gate), S (source), D (drain) and B (back-gate in our case). In general, C_{kli} is different from C_{lki}. The most straightforward example of this non-reciprocity property is the ideal transistor in saturation. Indeed, varying the drain

voltage will not introduce any variation of the gate charges because of pinch-off and thus, the drain-to-gate capacitance will be zero. However, in the opposite case, a variation of the gate voltage will induce a variation of the drain charges (due to the change in the inversion layer charges) resulting in a non-zero gate-to-drain capacitance.

One of the ways to introduce the non-reciprocal effect in the small-signal model is by adding a term to the transconductance. This modified transconductance $y_m i$, known as transadmittance, is defined by

$$y_{mi} = g_{mi} - j\omega C_{mi} \tag{4.4}$$

Where the transcapacitance is

$$C_{mi} = C_{dgi} - C_{gdi} \tag{4.5}$$

The back-gate terminal has been so far neglected but by using similar definitions as above, the transconductance and transcapacitances related to the back-gate can be introduced

$$y_{mbi} = g_{mbi} - j\omega C_{mbi} \tag{4.6}$$
$$C_{mbi} = C_{dbi} - C_{bdi} \tag{4.7}$$
$$C_{mxi} = C_{bgi} - C_{gbi} \tag{4.8}$$
$$\tag{4.9}$$

The final intrinsic equivalent circuit is shown in Figure 4.2. Because the intrinsic elements are dependent on both the dimensions of the transistor and the bias conditions, the extraction methods often rely on these dependencies in order to simplify the equivalent circuit and identify each element.

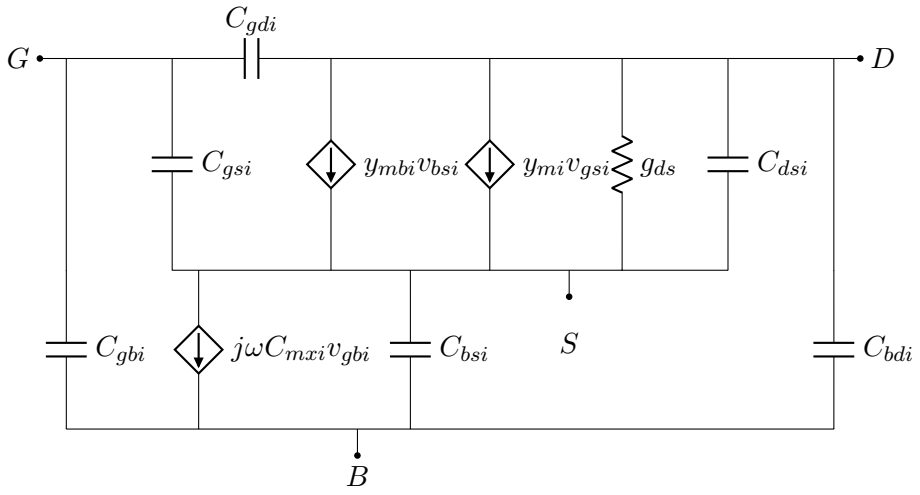


Figure 4.2: Small-signal model of the intrinsic part of the transistor.

4.2.2 Extrinsic elements

In the previous section, the small-signal model is only composed of intrinsic elements which are geometry and bias dependent. However, due to the physical structure of the transistor, its active part is surrounded by other parasitic elements which are mainly bias independent. These elements are called "extrinsic" and can be classified as follows

- Extrinsic parasitic capacitances are associated with fringing fields and overlaps located around the channel as shown in Figure 4.3. For example, the extrinsic gate-to-source (C_{gse}) and gate-to-drain (C_{gde}) capacitances are the combination of the two effects. During the fabrication process, the diffusion of the doping atoms from the source and drain to the channel creates overlaps with the gate oxide. The effective channel length L_{eff} which corresponds to the part of the channel contributing to the intrinsic characteristics of the transistor is thus smaller than the mask channel length L. It can be written as $L_{eff} = L - \Delta L$.
- Extrinsic series resistances represent the resistive losses from the accesses to the intrinsic part. The extrinsic source R_{se} and drain R_{de} resistances include the metallic losses, the contact resistance (between the metal and the semiconductor) and the losses in the source and drain implant regions. The extrinsic gate resistance R_{ge} includes the losses in some metallic lines and the resistance of the gate fingers. As it can be seen in Figure 4.3, the back-gate access is made through a n-well resting on the p-substrate. A heavily doped n-type ground plane is also implemented just below the BOX. This is the so-called flip-well architecture [30]. It was thus decided to divide the series resistance associated to the back-gate into two parts. The first resistance R_{b1e} has a similar meaning than the other series resistances, representing the resistive losses from the back-gate access to the n-well while the second resistance R_{b2e} corresponds to the ground plane resistance. In this model, the distributed nature of resistances is neglected and equivalent lumped resistances are used instead.
- Extrinsic series inductances can also be introduced to increase the validity of the small-signal equivalent circuit at higher frequency but in this case, they are neglected because for sub-micron MOSFETs, their effect is negligible in the studied frequency band [10].

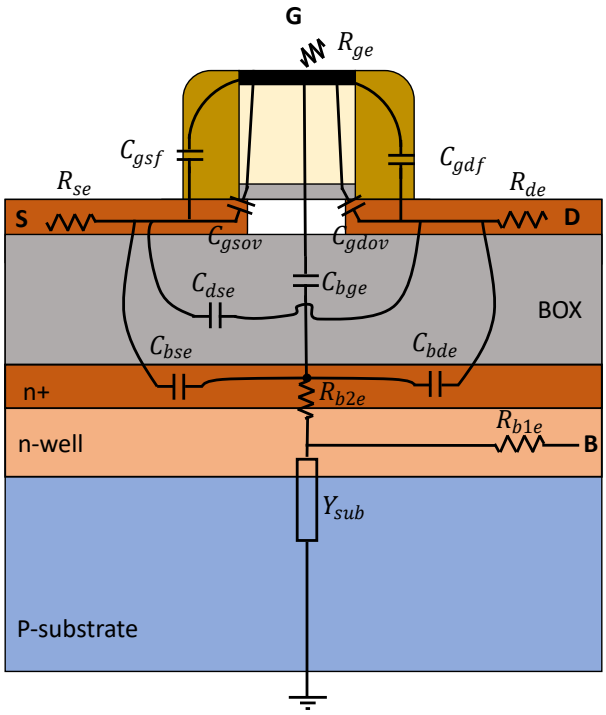


Figure 4.3: Parasitic extrinsic capacitances and resistances in UTBB FD-SOI transistor with back-gate access.

The final small-signal equivalent circuit is shown in Figure 4.4. A generic substrate element is added along the back-gate connection path (between R_{b1} and R_{b2}). More details about Y_{sub} will be given in the next sections. The index "e" used for extrinsic elements will be dropped for the series resistances. The extrinsic capacitances are in parallel with the intrinsic ones, therefore the sum of the two is noted C_{kltot} (for "total" capacitance) with k and l being any of the four terminals.

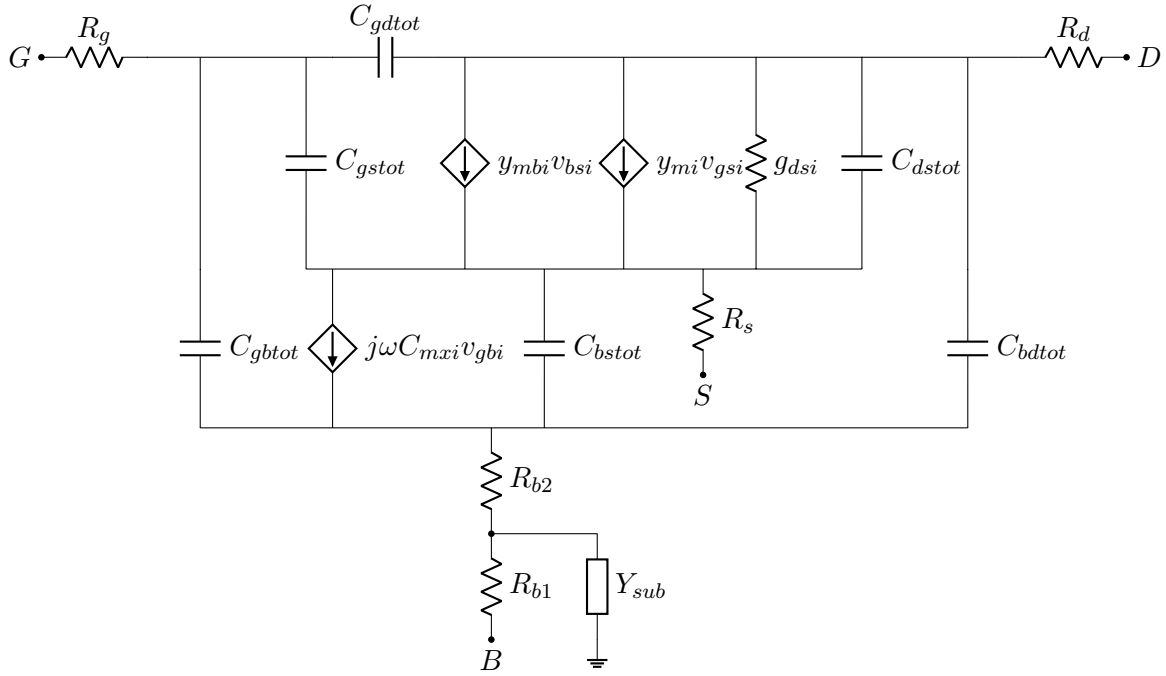


Figure 4.4: Complete small-signal equivalent circuit of the UTBB FD-SOI MOSFET.

4.2.3 Parasitic access elements

The parasitic access elements are caused by the metal connections that remain at the input and output of the transistor after the calibration procedure. Indeed, small-signal measurements require RF pads for placing the tips of the probes. The RF pads and the necessary interconnections thus introduce unwanted parasitics in the measurements because the reference plane is not located at the intrinsic device terminals but at the end of the probes tips. Therefore, several de-embedding procedures exist to move the reference plane as close as possible to the intrinsic device. For this purpose, dedicated de-embedding structures, also called de-embedding dummies, have been developed to remove the parasitic impedance and admittance of the RF pads and interconnections. For example, "Open" and "Short" de-embedding structures are illustrated in Figure 4.5.

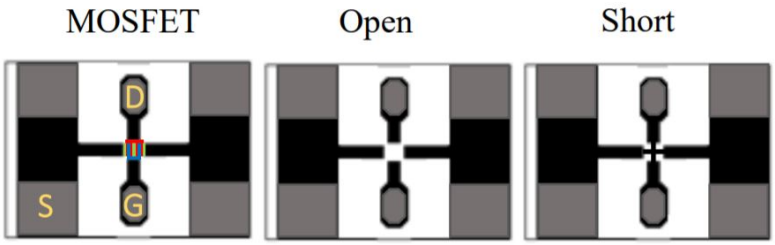


Figure 4.5: MOSFET and its associated "Open" and "Short" de-embedding structures [39].

The parasitic access elements are independent of the transistor dimensions and are considered constant under normal bias conditions.

4.3 Extraction method based on *ELDO* simulations.

In this section, the small-signal model of the UTBB FD-SOI MOSFET proposed in Figure 4.4 is studied both as a 3-port and 4-port device. All the parasitic elements are extracted from *ELDO* simulations. Since the 22FDX technology from *GlobalFoundries* is used in the experimental devices (see Section 3.4.2), the associated compact model is employed for the following developments. The structural parameters are coded to be the same as the ones of the experimental 20n-SLVT transistor having 64 fingers of 1 µm width each. The main RF Figures of Merit (FoM), namely f_t and f_{max}, are also evaluated.

This section will essentially present the extraction procedure of each elements. Therefore, the back-gate voltage will initially be set to $V_B = 0\,\mathrm{V}$. The dependency on the back-gate bias will be studied at length in Section 4.4 on experimental measurements. Self-heating effect is also not considered here.

4.3.1 3-Port small-signal model

The 3-port small-signal equivalent circuit is shown in Figure 4.6. The device is connected in a common-source configuration and the front-gate (G), the drain (D) and the back-gate (B) terminals are respectively connected to RF Port 1, Port 2 and Port 3. Therefore, the following notation will be used interchangeably:

$$Y_{3-Port} = \begin{bmatrix} Y_{gg} & Y_{gd} & Y_{gb} \\ Y_{dg} & Y_{dd} & Y_{db} \\ Y_{bg} & Y_{bd} & Y_{bb} \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \tag{4.10}$$

The generic substrate admittance Y_{sub} was replaced by a single capacitance $C_{well-sub}$ representing the n-well/p-substrate junction capacitance. Finally, the resistance R_{b2} was removed because it was shown using Keysight ADS software that its impact on the **3-Port** Y and Z-matrices was negligible.

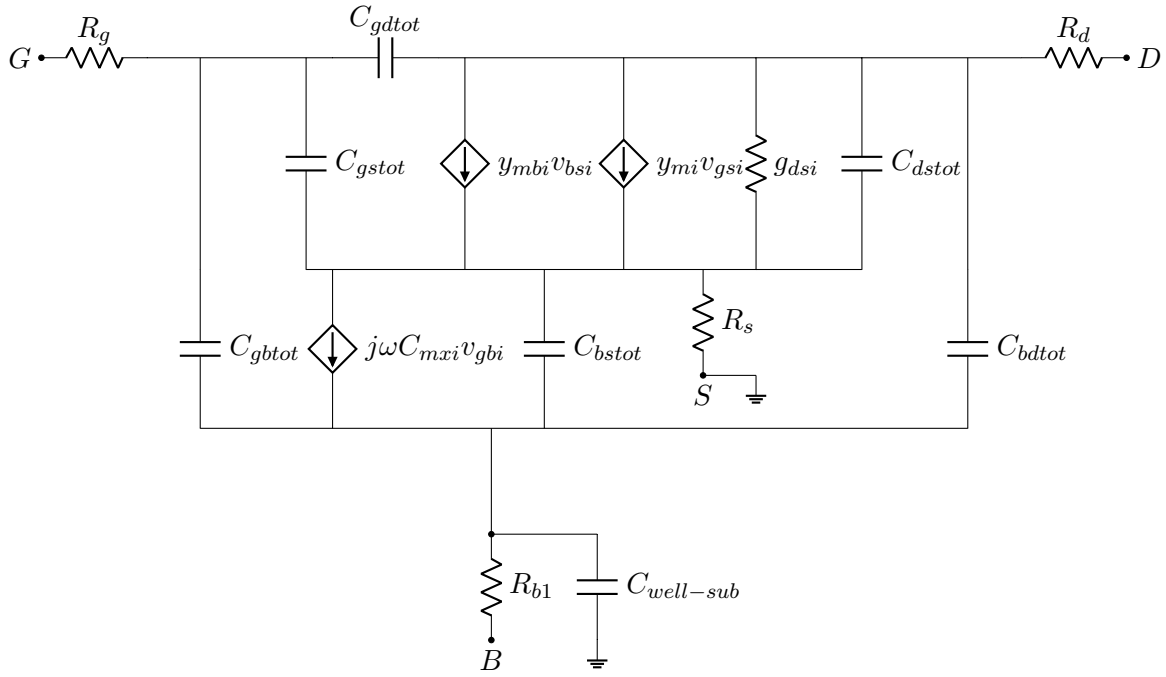


Figure 4.6: Small-signal equivalent circuit of the 3-port UTBB FD-SOI MOSFET. The notation "*tot*" refers to the sum of intrinsic and extrinsic elements as previously.

Extraction of parasitic series resistances

Since the extrinsic series resistances strongly degrade the RF performances of MOSFETs, many different extraction methods of the series resistances have been proposed in the literature [35; 40; 41]. Among them, the Bacale's method [41] was selected for this work since Tinoco et al. [42] showed that it was able to provide more accurate results compared to other methods. This extraction method consists of biasing the transistor in strong inversion ($V_{GS} >> V_{TH}$) and cold FET ($V_{DS} = 0\,\mathrm{V}$) and thus only one transistor of a given length is required. Under these conditions, the output conductance g_{ds} is assumed to be proportional to the inverse of the gate voltage overdrive ($GVO = V_{GS} - V_{TH}$) and the intrinsic transconductance g_{mi} is assumed to be zero. It also relies on the assumptions that $C = C_{gs} = C_{gd}$ (symmetrical channel) and that the effective mobility is constant. The series resistances can finally be extracted by doing a simple linear regression of the real part of Z-parameters as a function of $1/GVO$:

$$\mathrm{Re}\{Z_{11} - Z_{12}\} = R_g - \frac{1}{4g_{ds}} \tag{4.11}$$

$$\mathrm{Re}\{Z_{12}\} = R_s + \frac{1}{2g_{ds}} \tag{4.12}$$

$$\mathrm{Re}\{Z_{22} - Z_{12}\} = R_d + \frac{1}{2g_{ds}} \tag{4.13}$$

Where $g_{ds} \propto V_{GS} - V_{TH}$. However, the latter results are only valid for a 2-port device in common-source configuration, therefore, a similar approach will be developed for the studied 3-port device.

The 3-port small-signal equivalent circuit biased in "cold regime" and strong inversion is illustrated in Figure 4.7. The back-gate voltage V_B is set to $0\,\mathrm{V}$. As for the Bracale's method, both

transconductances g_{mi} and g_{mbi} are approximately equal to zero.

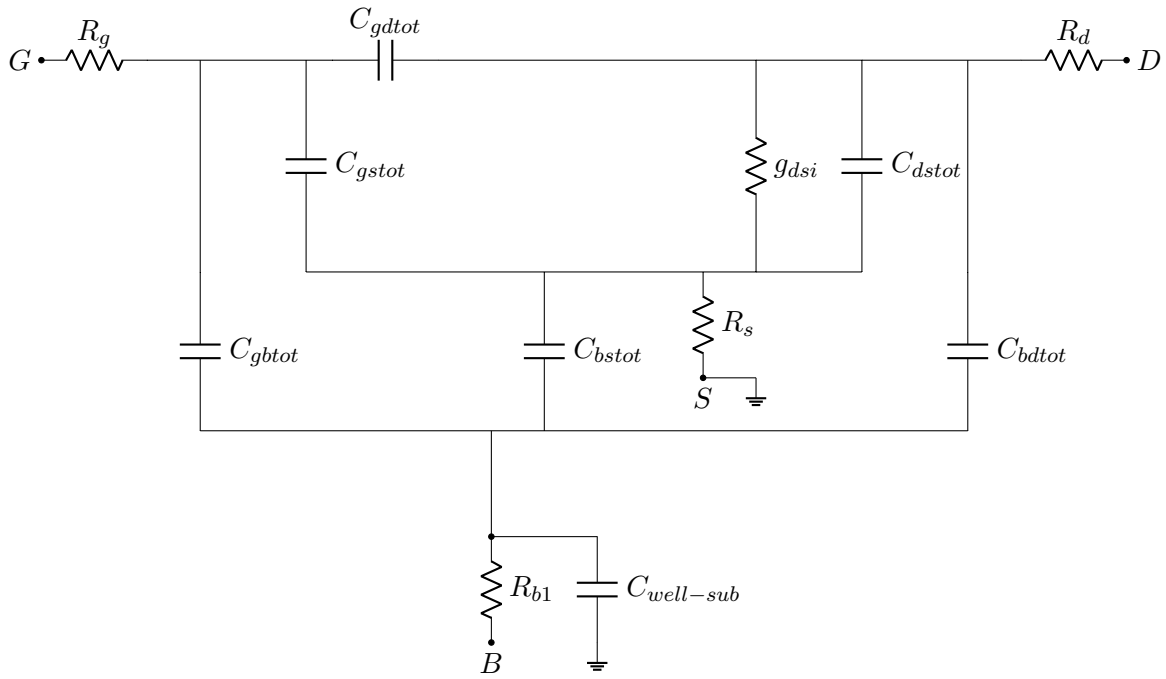


Figure 4.7: Small-signal equivalent circuit of the 3-port UTBB FD-SOI MOSFET in cold FET (cold: $V_{DS} = 0\,\mathrm{V}$, strong inversion: $V_{GS} >> V_{TH}$).

Under cold conditions, the source capacitance C_{gstot} should theoretically be almost equal to the drain capacitance C_{gdtot} due to the symmetrical operation of the transistor. The same goes for C_{bstot} and C_{bdtot}. One then has

$$C_1 = C_{gstot} = C_{gdtot} \qquad C_2 = C_{bstot} = C_{bdtot} \tag{4.14}$$

Moreover, supposing that the substrate path is negligible compared to the well path, one obtains the following expressions

$$\mathrm{Re}\{Z_{11}\} = R_g + R_s + \frac{g_{ds}}{G^2\omega^2 + 4g_{ds}^2} \tag{4.15}$$

$$\mathrm{Re}\{Z_{12}\} = \mathrm{Re}\{Z_{21}\} = \mathrm{Re}\{Z_{23}\} = \mathrm{Re}\{Z_{32}\} = R_s + \frac{2g_{ds}}{G^2\omega^2 + 4g_{ds}^2} \tag{4.16}$$

$$\mathrm{Re}\{Z_{13}\} = \mathrm{Re}\{Z_{31}\} = R_s + \frac{g_{ds}}{G^2\omega^2 + 4g_{ds}^2} \tag{4.17}$$

$$\mathrm{Re}\{Z_{22}\} = R_d + R_s + \frac{4g_{ds}}{G^2\omega^2 + 4g_{ds}^2} \tag{4.18}$$

$$\mathrm{Re}\{Z_{33}\} = R_{b1} + R_s + \frac{g_{ds}}{G^2\omega^2 + 4g_{ds}^2} \tag{4.19}$$

Where $G = C_1 + C_2 + 2C_{ds}$. Because the term $G^2\omega^2$ is supposed to be negligible on all the frequency band, one obtains the same relationships as with the Bracale's method for the terms

$\mathrm{Re}\{Z_{11}\}$, $\mathrm{Re}\{Z_{12}\}$, $\mathrm{Re}\{Z_{21}\}$ and $\mathrm{Re}\{Z_{22}\}$. The linear regression as a function of the gate voltage overdrive with $GVO_{min} = 0.4\,\mathrm{V}$ is shown in Figure 4.8.

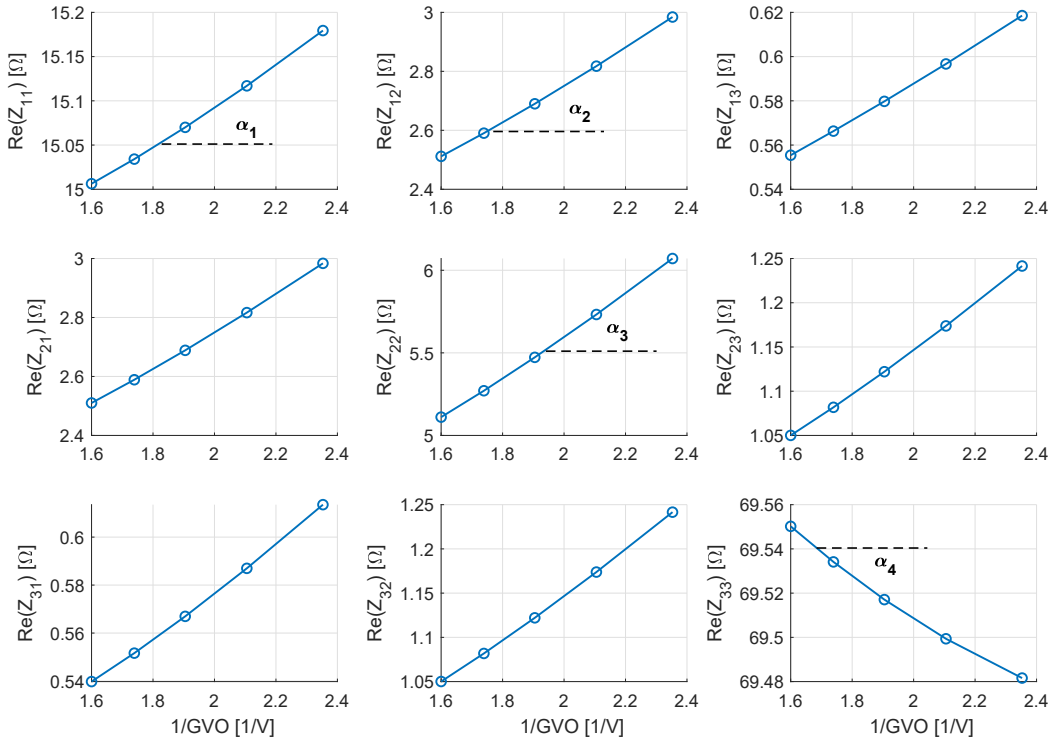


Figure 4.8: Extraction of series resistances based on a $1/GVO$ linear regression in cold FET ($V_{DS} = 0\,\mathrm{V}$, $GVO_{min} = 0.4\,\mathrm{V}$, $f = 10\,\mathrm{GHz}$).

The threshold voltage was calculated using the maximum of C_{gg} derivative since this method is not impacted by the effects of access resistances and the gate-voltage dependent mobility as other current-based methods (see Section 3.4). It yields $V_{TH} = 0.26\,\mathrm{V}$ for $V_B = 0\,\mathrm{V}$. One can notice in Figure 4.8 that all $\mathrm{Re}\{Z_{ij}\}$ follow a linear trend. The negative slope of $\mathrm{Re}\{Z_{33}\}$ is very small ($\alpha_4 = -0.09$) and is disregarded. Hence, R_{b1} can directly be extracted from the real part of Z_{33} in cold FET and strong inversion. However, based on Equation 4.16, $\mathrm{Re}\{Z_{12}\} = \mathrm{Re}\{Z_{21}\}$ should theoretically be equal to $\mathrm{Re}\{Z_{23}\} = \mathrm{Re}\{Z_{32}\}$ under these bias conditions (and the corresponding assumptions), which is not the case. This discrepancy can be attributed to the substrate network which was so far neglected for the series resistances extraction. The n-well/p-substrate capacitance can thus be introduced in the calculations of Z-parameters giving the following expressions:

$$\mathrm{Re}\{Z_{11}\} \approx R_g + 4\alpha_1\beta R_s + \frac{\alpha_1}{(V_{GS} - V_{TH})} \tag{4.20}$$

$$\mathrm{Re}\{Z_{12}\} \approx 2\alpha_2\beta R_s + \frac{\alpha_2}{(V_{GS} - V_{TH})} \tag{4.21}$$

$$\mathrm{Re}\{Z_{22}\} \approx R_d + R_s + \frac{\alpha_3}{(V_{GS} - V_{TH})} = R_d + R_s + \frac{1}{\beta(V_{GS} - V_{TH})} \tag{4.22}$$

$$\mathrm{Re}\{Z_{33}\} \approx R_{b1} + 4\alpha_4\beta R_s + \frac{\alpha_4}{(V_{GS} - V_{TH})} \tag{4.23}$$

The expanded version of these equations can be found in Appendix B. The factor β is defined such that $g_{dsi} = \beta(V_{GS} - V_{TH})$. From this result, one finds the series resistances

$$R_s = \frac{\mathrm{Re}\{Z_{12}\}|_{1/GVO=0}}{2\alpha_2}\alpha_3 \tag{4.24}$$

$$R_g = \mathrm{Re}\{Z_{11}\}|_{1/GVO=0} - \frac{\alpha_1}{\alpha_3}R_s \tag{4.25}$$

$$R_d = \mathrm{Re}\{Z_{22}\}|_{1/GVO=0} - R_s \tag{4.26}$$

$$R_{b1} = \mathrm{Re}\{Z_{33}\}|_{1/GVO=0} - \frac{\alpha_4}{\alpha_3}R_s \tag{4.27}$$

The values of the series resistances extracted from the intercept of the linear regression with the y-axis and using the correction introduced by Equations 4.24-4.27 are available in Table 4.1. One can note that the two methods give very similar values with a back-gate resistance R_{b1} almost five times the front-gate resistance. Moreover, by introducing the n-well/p-substrate capacitance, the parameters $\mathrm{Re}\{Z_{12}\} = \mathrm{Re}\{Z_{21}\}$ are not equal to $\mathrm{Re}\{Z_{23}\} = \mathrm{Re}\{Z_{32}\}$ anymore. However, since $\mathrm{Re}\{Z_{23}\}$ and $\mathrm{Re}\{Z_{32}\}$ are not required for the extraction of the series resistances, their analytical expressions are not shown here but are available in Appendix B.

Method	R_g [Ω]	R_d [Ω]	R_s [Ω]	R_{b1} [Ω]
Direct linear regression	13.17	1.494	1.441	68.26
Corrected linear regression	13.56	1.471	1.465	70.12

Table 4.1: Extracted series resistances from *ELDO* simulations using direct and "corrected" linear regressions as a function of $1/GVO$ (in strong inversion).

The removal of the series resistances from the device impedance matrix $Z_{DUT-tot}$ is done in two steps. First, R_g, R_d and R_{b1} are de-embedded using

$$Z_{DUT1} = Z_{DUT-total} - R_{series1} \tag{4.28}$$

Where $R_{series1}$ is expressed by

$$R_{series1} = \begin{bmatrix} R_g & 0 & 0 \\ 0 & R_d & 0 \\ 0 & 0 & R_{b1} \end{bmatrix} \tag{4.29}$$

Then, the effects of the n-well/p-substrate capacitance $C_{well-sub}$ can be removed by subtracting the following matrix from $Y_{DUT1} = Z_{DUT1}^{-1}$

$$Y_{DUT2} = Y_{DUT1} - Y_{sub} = Y_{DUT1} - \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & j\omega C_{well-sub} \end{bmatrix} \tag{4.30}$$

Finally, the source resistance R_s is also removed by means of an impedance matrix Z_{R_s}:

$$Z_{DUT} = Z_{DUT2} - Z_{R_s} = Z_{DUT2} - \begin{bmatrix} R_s & R_s & R_s \\ R_s & R_s & R_s \\ R_s & R_s & R_s \end{bmatrix} \tag{4.31}$$

Where the related admittance matrix $Y_{DUT} = Z_{DUT}^{-1}$ encompasses the intrinsic ("i") and extrinsic ("e") elements:

$$Y_{DUT} = Y_i + Y_e \tag{4.32}$$

In order to follow these steps, one still needs to compute $C_{well-sub}$ which is the subject of the next section.

Extraction of extrinsic and n-well/p-substrate capacitances

After removing the series impedance matrix $R_{series1}$ from $Z_{DUT-total}$, the next step is to removed the contribution of $C_{well-sub}$ capacitance. The extraction of $C_{well-sub}$ capacitance is performed in cold FET ($V_{DS} = 0\,\mathrm{V}$) and deep depletion ($V_{GS} < 0\,\mathrm{V}$) just as the extraction of the extrinsic capacitances. The small-signal equivalent circuit under these conditions is shown in Figure 4.9.

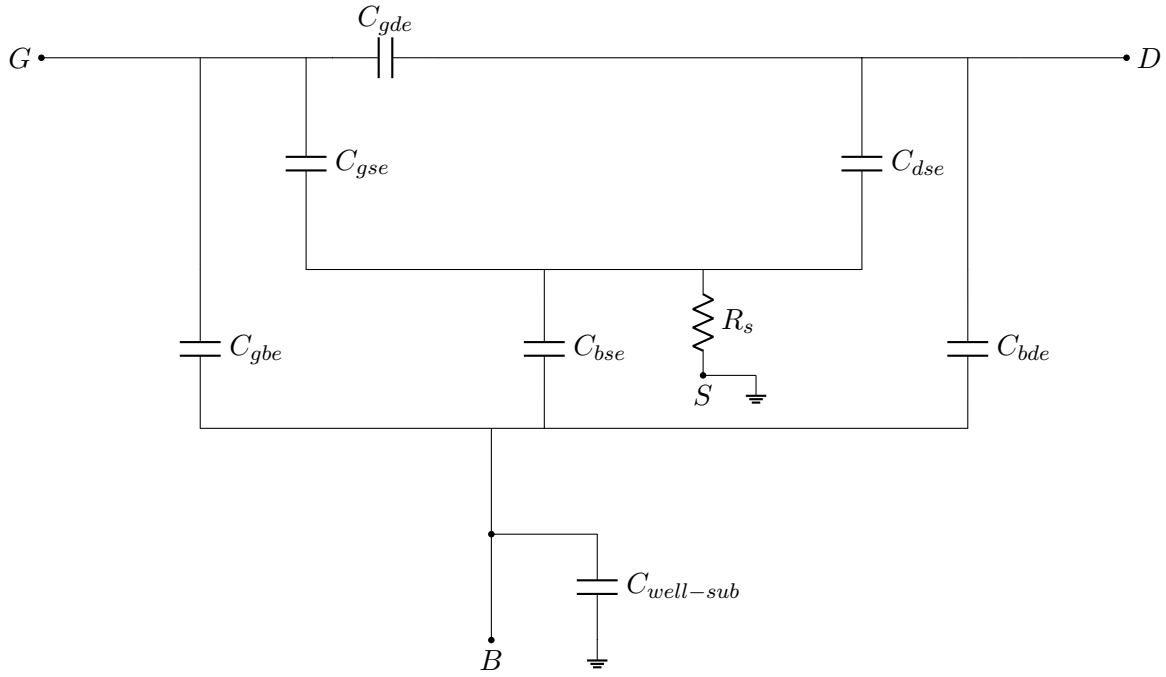


Figure 4.9: Small-signal equivalent circuit of the 3-port UTBB FD-SOI MOSFET in cold FET ($V_{DS} = 0\,\mathrm{V}$) and deep depletion ($V_{GS} < 0\,\mathrm{V}$).

Supposing that C_{bse} is identical to C_{bde} (which is confirmed by TCAD simulations for a perfectly symmetrical transistor), one can expressed $C_{well-sub}$ as

$$j\omega C_{well-sub} = Y_{33}^{deep-dep.} + 2Y_{32}^{deep-dep.} + Y_{31}^{deep-dep.} \tag{4.33}$$

In order to get this expression, it was also assumed that R_s did not impact significantly the capacitances extraction in deep depletion. This hypothesis was verified "a posteriori". Once $C_{well-sub}$ is found, its corresponding admittance matrix Y_{sub} (Equation 4.30) as well as the impedance matrix Z_{R_s} (Equation 4.31) can be removed from $Y^{deep-dep.}$ using the following equation:

$$Y^{deep-dep.\prime} = ((Y^{deep-dep.} - Y_{sub})^{-1} - Z_{R_s})^{-1} \tag{4.34}$$

This matrix can be expressed in terms of extrinsic capacitances as

$$Y^{deep-dep.\prime} = \begin{bmatrix} j\omega(C_{gse} + C_{gde} + C_{gbe}) & -j\omega C_{gde} & -j\omega C_{gbe} \\ -j\omega C_{gde} & j\omega(C_{dse} + C_{bde} + C_{gde}) & -j\omega C_{bde} \\ -j\omega C_{bge} & -j\omega C_{bde} & j\omega(C_{bse} + C_{bde} + C_{gbe}) \end{bmatrix} \tag{4.35}$$

Finally, the extrinsic capacitances can be extracted from

$$C_{gse} = \mathrm{Im}\Big\{Y_{11}^{deep-dep.\prime} + Y_{12}^{deep-dep.\prime} + Y_{13}^{deep-dep.\prime}\Big\}/\omega \tag{4.36}$$

$$C_{gde} = -\,\mathrm{Im}\Big\{Y_{12}^{deep-dep.\prime}\Big\}/\omega \tag{4.37}$$

$$C_{gbe} = -\,\mathrm{Im}\Big\{Y_{13}^{deep-dep.\prime}\Big\}/\omega \tag{4.38}$$

$$C_{dse} = \mathrm{Im}\Big\{Y_{21}^{deep-dep.\prime} + Y_{22}^{deep-dep.\prime} + Y_{23}^{deep-dep.\prime}\Big\}/\omega \tag{4.39}$$

$$C_{bde} = -\,\mathrm{Im}\Big\{Y_{32}^{deep-dep.\prime}\Big\}/\omega \tag{4.40}$$

$$C_{bse} = \mathrm{Im}\Big\{Y_{31}^{deep-dep.\prime} + Y_{32}^{deep-dep.\prime} + Y_{33}^{deep-dep.\prime}\Big\}/\omega \tag{4.41}$$

A summary of their values is given in Table 4.2 where C_{gge} and C_{bbe} correspond to the front and back-gate extrinsic capacitances, respectively. From this table, it can be see that $C_{well-sub}$ is approximately equal to four times C_{dbe} and C_{bse}, which makes it the main contribution to the parameter $\mathrm{Im}\Big\{Y_{33}^{deep-dep.\prime}\Big\}/\omega$. One should also expect a dependence of $C_{well-sub}$ on the back-gate voltage V_B. Indeed, $C_{well-sub}$ corresponds to the junction capacitance between the n-well and the p-substrate. By applying a positive back-gate bias, the n-well which is connected to the back-gate becomes more positive and as a result the diode becomes reversely biased. Therefore, the transition capacitance decreases due the wider depletion region. This effect is discussed in Section 4.4.2.

Parameter	C_{gge}	C_{dse}	C_{bbe}	C_{dbe}	C_{bse}	$C_{well-sub}$
Value	35.8 fF	26 fF	12.5 fF	4.6 fF	4.6 fF	18.4 fF

Table 4.2: Extracted extrinsic and n-well/p-substrate capacitances in cold regime ($V_{DS} = 0\,\mathrm{V}$) and deep depletion ($V_{GS} = -0.2\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$) at $f = 1\,\mathrm{GHz}$.

Extraction intrinsic parameters and total capacitances

In this section, the intrinsic parameters as well as the total capacitances are extracted in saturation and strong inversion. Since the nominal value recommended by *GlobalFoundries* for the drain voltage is $V_{DS} = 0.8\,\mathrm{V}$, this value will be used for the next developments. The front-gate voltage is set to $V_{GS} = 0.8\,\mathrm{V}$. One important remark is that under these conditions, the total capacitances (i.e. C_{gstot} and C_{gdtot}) are no longer the same due to the presence of pinch-off at the drain side (non-symmetrical inversion layer). The small-signal circuit after removal of the series resistances and n-well/p-substrate capacitance is shown in Figure 4.10. This circuit is only valid for extracting the intrinsic/total parameters from the **Y-matrix** (Z-matrix should not be used due to the removal of the substrate network).

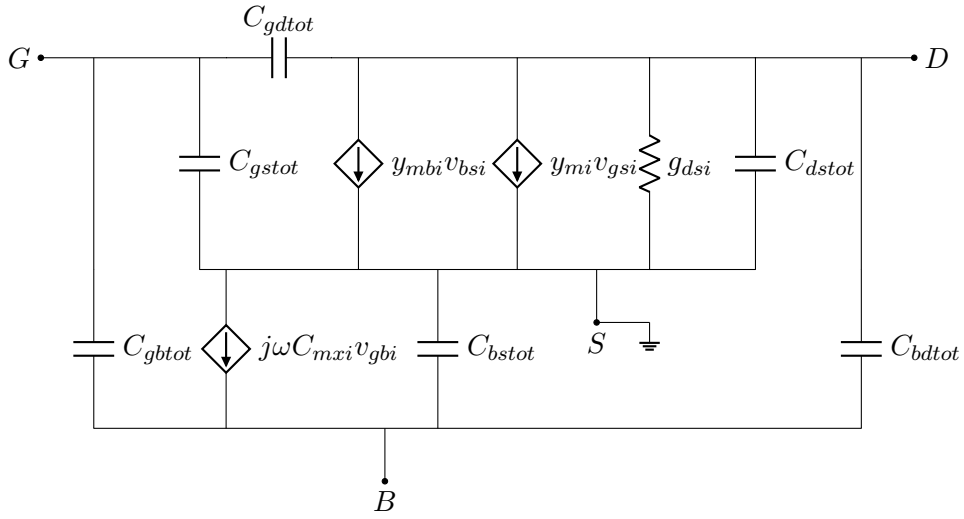


Figure 4.10: Small-signal equivalent circuit of the 3-port UTBB FD-SOI MOSFET in saturation and strong inversion after removal of series resistances and $C_{well-sub}$.

From the small-signal model of Figure 4.10 and by replacing y_{mi}, y_{mbi} and C_{mxi} by their expressions, one obtains

$$Y_{DUT} = \begin{bmatrix} j\omega(C_{gstot} + C_{gdtot} + C_{gbtot}) & -j\omega C_{gdtot} & -j\omega C_{gbtot} \\ g_{mi} - j\omega C_{dgtot} & g_{dsi} + j\omega(C_{dstot} + C_{gdtot} + C_{bdtot}) & g_{mbi} - j\omega C_{dbtot} \\ -j\omega C_{bgtot} & -j\omega C_{bdtot} & j\omega(C_{bstot} + C_{bdtot} + C_{bgtot}) \end{bmatrix} \tag{4.42}$$

Therefore, each element can be extracted from

$$g_{mi} = \mathrm{Re}\{Y_{DUT21}\} \tag{4.43}$$
$$g_{mbi} = \mathrm{Re}\{Y_{DUT23}\} \tag{4.44}$$
$$g_{dsi} = \mathrm{Re}\{Y_{DUT22}\} \tag{4.45}$$
$$C_{gstot} = \mathrm{Im}\{Y_{DUT11} + Y_{DUT12} + Y_{DUT13}\}/\omega \tag{4.46}$$
$$C_{gdtot} = -\mathrm{Im}\{Y_{DUT12}\}/\omega \tag{4.47}$$
$$C_{gbtot} = -\mathrm{Im}\{Y_{DUT13}\}/\omega \tag{4.48}$$
$$C_{dgtot} = -\mathrm{Im}\{Y_{DUT21}\}/\omega \tag{4.49}$$
$$C_{dstot} = \mathrm{Im}\{Y_{DUT22} + Y_{DUT12} + Y_{DUT13}\}/\omega \tag{4.50}$$
$$C_{dbtot} = -\mathrm{Im}\{Y_{DUT23}\}/\omega \tag{4.51}$$
$$C_{bgtot} = -\mathrm{Im}\{Y_{DUT31}\}/\omega \tag{4.52}$$
$$C_{bdtot} = -\mathrm{Im}\{Y_{DUT32}\}/\omega \tag{4.53}$$
$$C_{bstot} = \mathrm{Im}\{Y_{DUT33} + Y_{DUT31} + Y_{DUT32}\}/\omega \tag{4.54}$$

The corresponding intrinsic capacitances C_{kli} can easily be computed by subtracting the extrinsic

contribution from the total capacitances.

$$C_{kli} = C_{kltot} - C_{kle} \tag{4.55}$$

Where k, l being a terminal (g, d or b).

A summary of the new extracted parameters can be found in Tables 4.3 and 4.4. These results are compared with the values obtained from the 4-Port small-signal model in Section 4.3.2.

Parameter	g_{mi}	g_{mbi}	g_{dsi}
Value	120.9 mS	10.1 mS	9.9 mS

Table 4.3: Extracted intrinsic tranconductances and output conductance in saturation ($V_{DS} = 0.8\,\mathrm{V}$) and strong inversion ($V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$) at $f = 1\,\mathrm{GHz}$.

Parameter	C_{gstot}	C_{gdtot}	C_{gbtot}	C_{dgtot}	C_{dstot}	C_{dbtot}	C_{bgtot}	C_{bdtot}	C_{bstot}
Value	46.98 fF	16.3 fF	2.27 fF	15.92 fF	34.89 fF	7.75 fF	2.09 fF	4.44 fF	6.29 fF

Table 4.4: Extracted total capacitances in saturation ($V_{DS} = 0.8\,\mathrm{V}$) and strong inversion ($V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$) at $f = 1\,\mathrm{GHz}$.

Validation of the model

In order to validate the small-signal equivalent circuit, the Y-matrix of the device is reconstructed step by step from the extracted intrinsic elements to the series resistances and compared to the initial Y-matrix obtained in saturation and strong inversion. It can be seen that all reconstructed Y-parameters (red dashed lines) are in good agreement with the initial ones (full blue lines) at low frequency. However, the small-signal model starts to diverge from the *ELDO* simulations at higher frequency showing the limitations of the model.

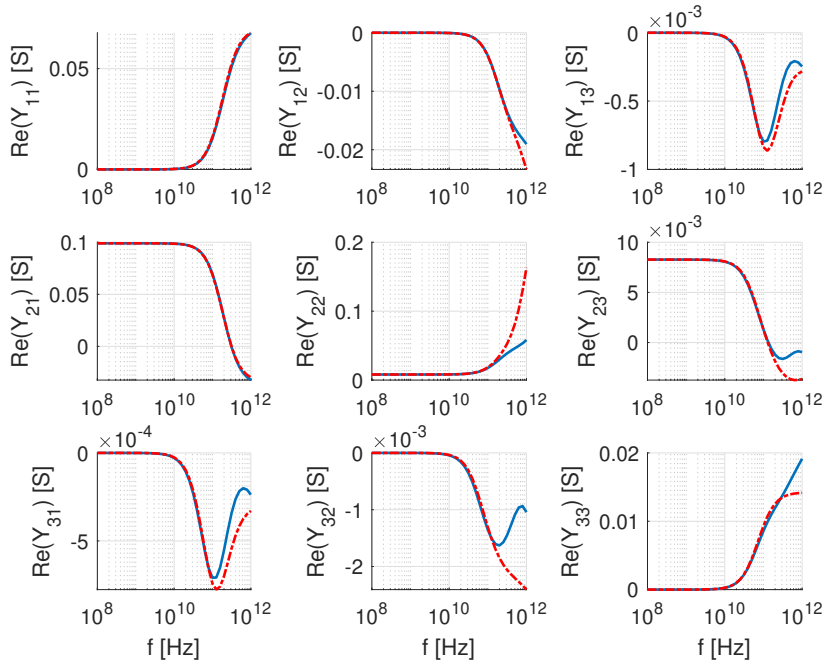


Figure 4.11: Reconstructed (dashed) vs initial (full) $\mathrm{Re}\{Y_{ij}\}$ in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$ for a 3-port device.

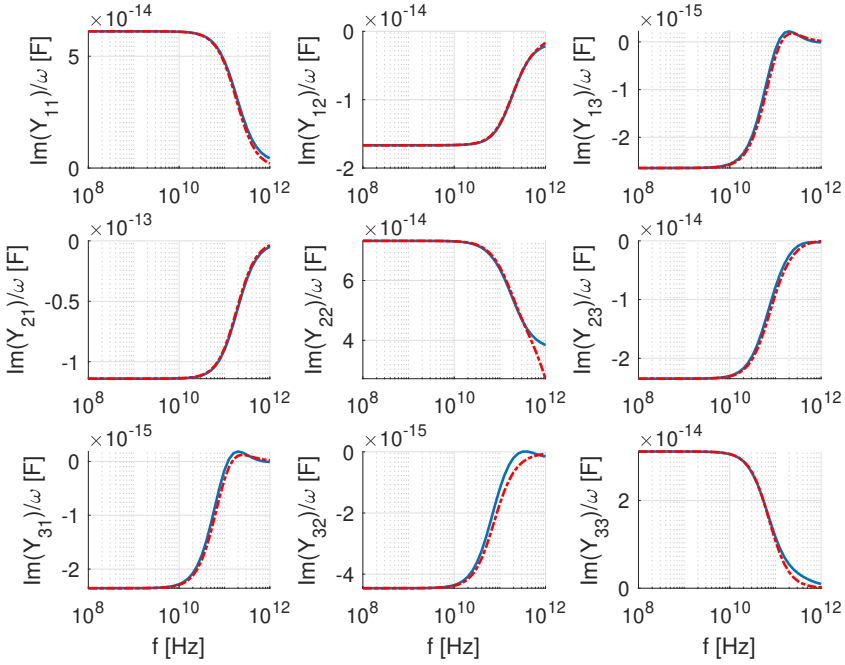


Figure 4.12: Reconstructed (dashed) vs initial (full) $\mathrm{Im}\{Y_{ij}\}/\omega$ in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$ for a 3-port device.

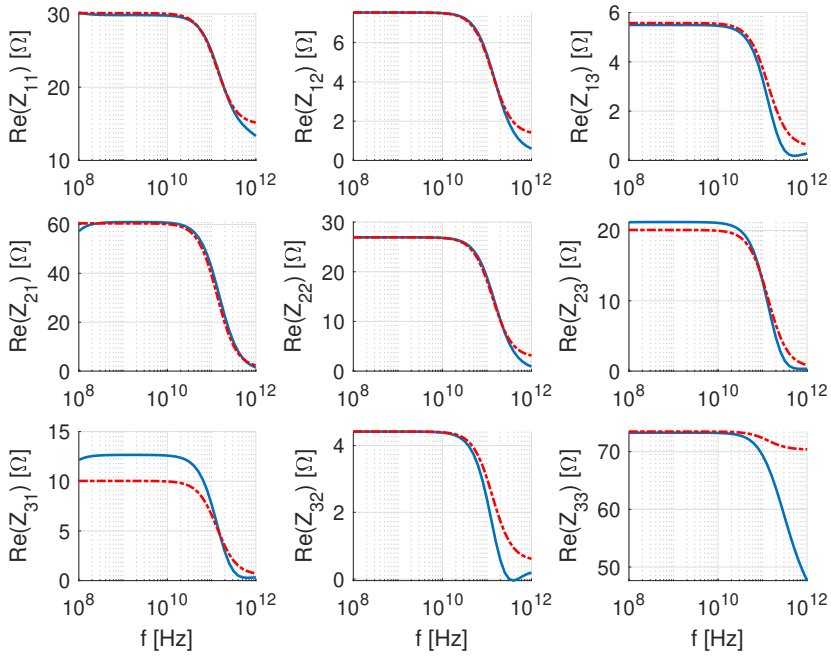


Figure 4.13: Reconstructed (dashed) vs initial (full) $\mathrm{Re}\{Z_{ij}\}$ in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$ for a 3-port device.

RF Figures of Merit Extraction

RF MOSFET performance is mainly assessed by two Figures of Merit, namely f_T and f_{max}. The cut-off frequency f_T is the frequency at which the current gain H_{21} is equal to unity (0 dB) while the maximum oscillation frequency f_{max} is the frequency at which the Mason's gain U is equal to unity (0 dB). Both values can be extracted by doing a linear extrapolation of their respective gains to 0 dB (intercept with frequency-axis). In order to evaluate the back-gate related Figures of Merit, one still needs to find suitable definitions for 3-port devices. By adapting the 4-port methodology proposed by Barbé et al. [43] to 3-port devices, one can found the following set of expressions for the front and back-gate current gains [6]:

$$H_{21} = \frac{Y_{21}Y_{33} - Y_{23}Y_{31}}{Y_{11}Y_{33} - Y_{13}Y_{31}} \tag{4.56}$$

$$H_{23} = \frac{Y_{23}Y_{11} - Y_{21}Y_{13}}{Y_{11}Y_{33} - Y_{13}Y_{31}} \tag{4.57}$$

Where Port 1, 2 and 3 are connected to the front gate, drain and back-gate respectively. More detail about how the above equations are obtained from hybrid parameters H can be found in Appendix C. Keeping coherence with 2-port definitions, one can also define the front and back-gate unilateral gains:

$$U = \frac{1}{4}\frac{|Y_{21} - Y_{12}|^2}{\mathrm{Re}\{Y_{11}\}\,\mathrm{Re}\{Y_{22}\} - \mathrm{Re}\{Y_{21}\}\,\mathrm{Re}\{Y_{12}\}} \tag{4.58}$$

$$U_{bg} = \frac{1}{4}\frac{|Y_{23} - Y_{32}|^2}{\mathrm{Re}\{Y_{33}\}\,\mathrm{Re}\{Y_{22}\} - \mathrm{Re}\{Y_{23}\}\,\mathrm{Re}\{Y_{32}\}} \tag{4.59}$$

Using the extracted parameters of the small-signal model, the front-gate FoMs [39] can be approximated as

$$f_T \approx \frac{g_{me}}{2\pi(C_{gstot} + C_{gdtot} + C_{gbtot})} = \frac{g_{me}}{2\pi C_{ggtot}} \tag{4.60}$$

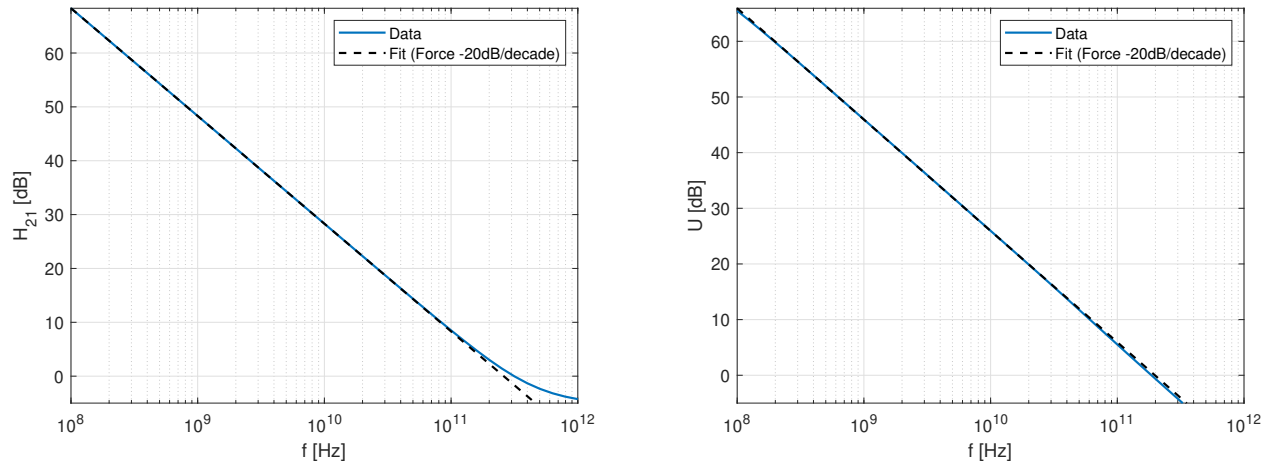
$$f_{max} \approx \frac{f_T}{2\sqrt{(R_s + R_g)g_{ds} + 2\pi f_T R_g C_{gdtot}}} \tag{4.61}$$

Where g_{me} is defined as $\mathrm{Re}\{Y_{21} - Y_{12}\}$. By analogy, similar expressions can be found for the back-gate FoMs

$$f_{Tbg} \approx \frac{g_{mbe}}{2\pi(C_{bstot} + C_{bdtot} + C_{bgtot} + C_{well-sub})} = \frac{g_{mbe}}{2\pi(C_{bbtot} + C_{well-sub})} \tag{4.62}$$

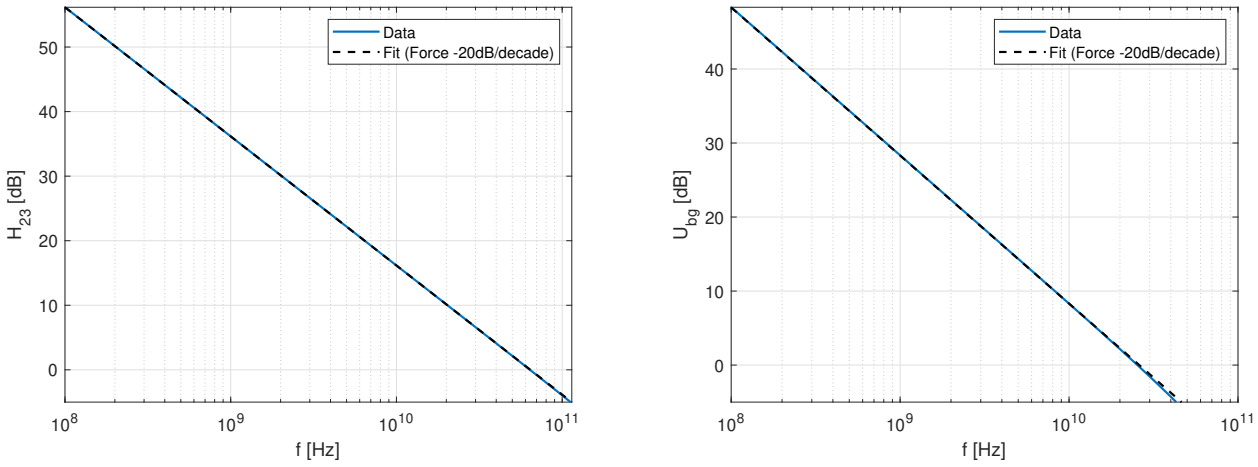
$$f_{maxbg} \approx \frac{f_{Tbg}}{2\sqrt{(R_s + R_{bg})g_{ds} + 2\pi f_{Tbg} R_b C_{bdtot}}} \tag{4.63}$$

In Figures 4.14 and 4.15, the different front and back-gate gains calculated with Equations 4.56-4.59) as a function of frequency are illustrated. The bias conditions are $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$. It can be see that both current gains and unilateral gains exhibit a $-20\,\mathrm{dB/dec}$ slope. Therefore, all FoMs are extracted from the intercept of a linear extrapolation with the frequency-axis by forcing a $-20\,\mathrm{dB/dec}$ slope. The extracted front and back-gate FoMs are given in Table 4.5. On one hand, by comparing these results with the ones obtained by doing a linear extrapolation of the *reconstructed* Y-matrix (based on the elements of the small-signal model), one can see that all FoMs are either equal or very close. This can be explained by the good agreement between the reconstructed Y-parameters and the initial Y-matrix seen in Section 4.3.1. On the other hand, all FoMs obtained by using the analytical expressions 4.60-4.63 are lower than the corresponding linear extrapolated FoMs. It is believed to be due to the approximations made to derive these expressions. For example, the non-reciprocal capacitances are not taken into account in these formulas.



(a) (b)

Figure 4.14: (a) H_{21} and (b) U versus frequency in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$. The dashed lines indicate the linear extrapolation realized by forcing a $-20\,\mathrm{dB/dec}$ slope.



(a) (b)

Figure 4.15: (a) H_{23} and (b) U_{bg} versus frequency in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$. The dashed lines indicate the linear extrapolation realized by forcing a $-20\,\mathrm{dB/dec}$ slope.

Method	f_T[GHz]	f_{max}[GHz]	f_{Tbg}[GHz]	f_{maxbg}[GHz]
Extrapolation	260	198	64	26
"Reconstructed" extrapolation	260	193	64	26
Formulas	240	173	42	24

Table 4.5: Comparison of different extraction methods of the front and back-gate FoMs at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$.

Finally, at $g_m = g_{m,max}$ which corresponds to $V_{GS} = 0.6\,\mathrm{V}$, one can achieve f_T value above 300 GHz as shown in Table 4.6.

Method	f_T[GHz]	f_{max}[GHz]	f_{Tbg}[GHz]	f_{maxbg}[GHz]
Extrapolation	325	251	78	31

Table 4.6: Front and back-gate FoMs at $g_m = g_{m,max}$ with $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.6\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$.

4.3.2 4-Port small-signal model

In the 3-port small signal equivalent circuit, the second back-gate resistance R_{b2} associated with the GP was not considered. Moreover, the substrate network was simply modelled by a capacitance between the n-well and p-substrate. The purpose of this section is thus to propose a more complete model by taking advantage of the additional information provided by 4-Port measurements. Figure 4.16 shows the new 4-Port small-signal equivalent circuit. The resistance R_{b2} is reintroduced and a substrate resistance R_{sub} below $C_{well-sub}$ is also added. The latter

element has been so far completely omitted. In order to keep the size of this section relatively short, only the differences with the 3-Port small-signal equivalent circuit are presented.

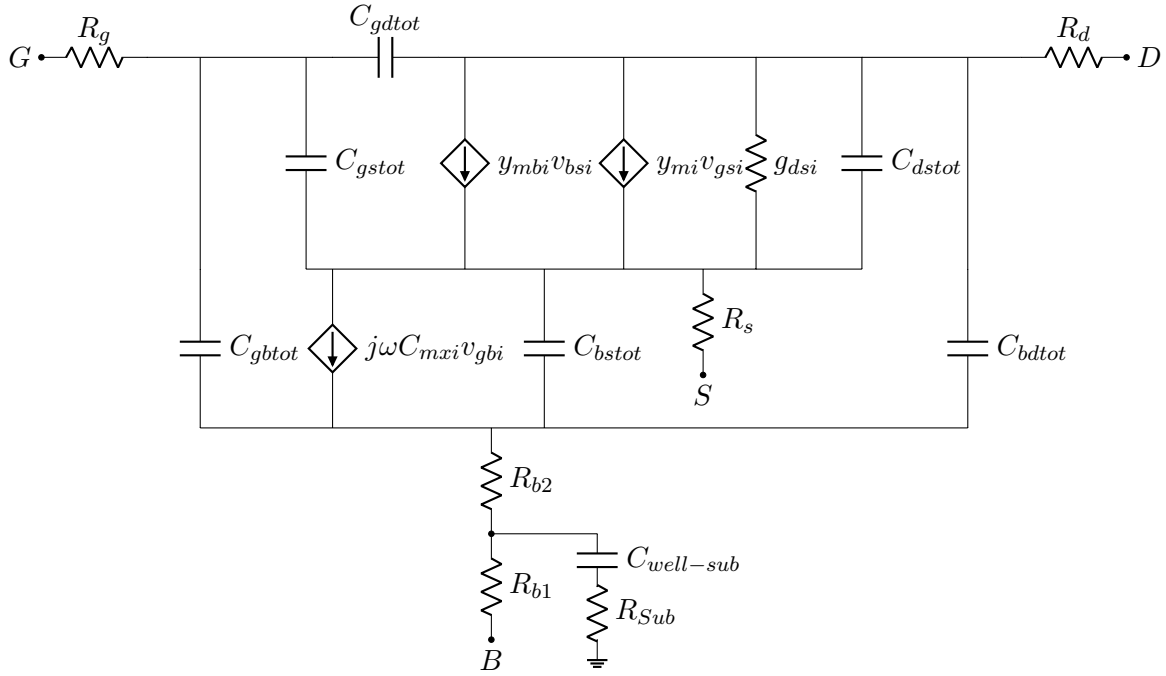


Figure 4.16: Complete 4-Port small-signal equivalent circuit of the UTBB FD-SOI MOSFET.

As before, a notation based on port number rather than terminal letter is used:

$$Y_{4-Port} = \begin{bmatrix} Y_{gg} & Y_{gd} & Y_{gs} & Y_{gb} \\ Y_{dg} & Y_{dd} & Y_{ds} & Y_{db} \\ Y_{sg} & Y_{sd} & Y_{ss} & Y_{sb} \\ Y_{bg} & Y_{bd} & Y_{bs} & Y_{bb} \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \tag{4.64}$$

Where Port 1, 2, 3 and 4 can be identified as the gate, drain, source and back-gate, respectively.

The series resistances are extracted in cold regime at $V_{DS} = 0\,\mathrm{V}$. Under these conditions, g_{mi} and g_{mbi} are almost equal to zero. The following extraction also assumes symmetrical capacitances

$$C_1 = C_{gstot} = C_{gdtot} \qquad C_2 = C_{bstot} = C_{bdtot} \tag{4.65}$$

Additionally, the contribution of C_{ds} is neglected. Figure 4.17 shows the simplified small-signal equivalent circuit in cold regime.

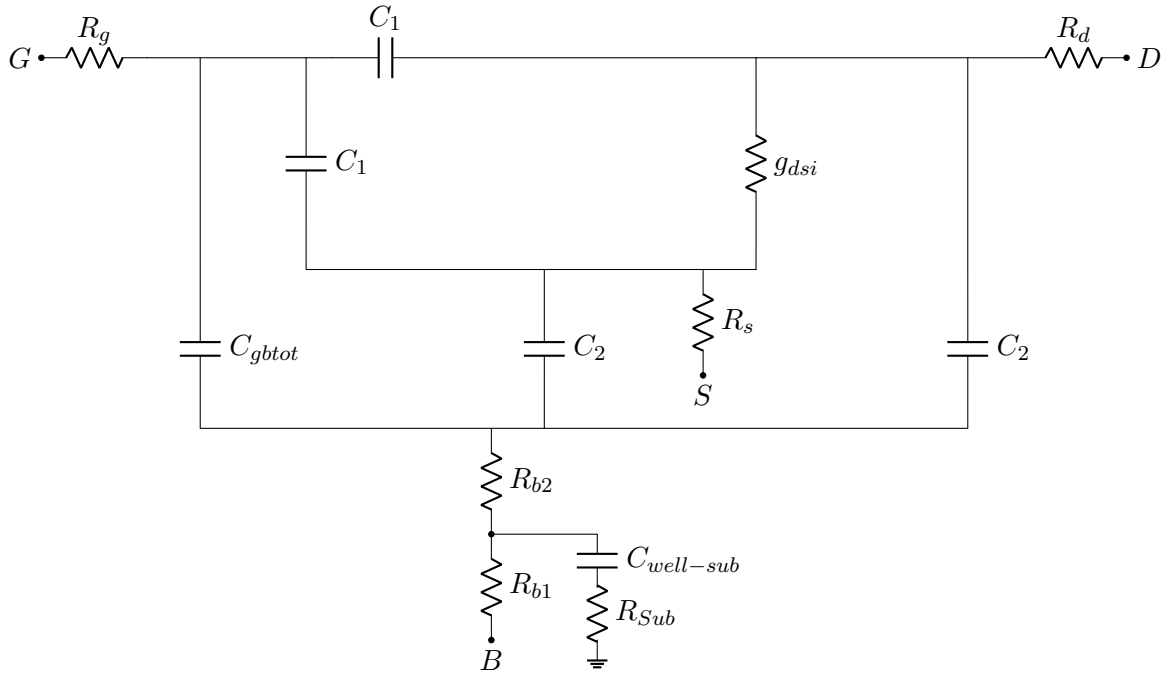


Figure 4.17: 4-Port small-signal equivalent circuit of the UTBB FD-SOI MOSFET at $V_{DS} = 0\,\mathrm{V}$ and assuming symmetrical capacitances.

According to this schematic, the substrate is connected to the ground through the resistance R_{sub}. One can also notice that the series terminal resistances (i.e. R_g,R_d,R_s and R_{b1}) can easily be removed by an impedance matrix with all resistances along the diagonal of the matrix. Furthermore, because the only "grounded" terminal is the substrate, Z-parameters will be referenced to the substrate terminal. As a result, all Z-parameters should "see" the substrate network. By using appropriate delta-star transformations, one obtains the real part of the Z-matrix defined as

$$\mathrm{Re}\{Z_{11}\} = R_g + R_{b2} + R_{sub} \tag{4.66}$$

$$\mathrm{Re}\{Z_{12}\} = \mathrm{Re}\{Z_{21}\} = R_{b2} + R_{sub} \tag{4.67}$$

$$\mathrm{Re}\{Z_{22}\} = R_d + \frac{g_{ds}}{4g_{ds}^2 + \omega^2(C_1 + C_2)^2} + R_{b2} + R_{sub} \tag{4.68}$$

$$\mathrm{Re}\{Z_{32}\} = \mathrm{Re}\{Z_{23}\} = -\frac{g_{ds}}{4g_{ds}^2 + \omega^2(C_1 + C_2)^2} + R_{b2} + R_{sub} \tag{4.69}$$

$$\mathrm{Re}\{Z_{33}\} = R_s + \frac{g_{ds}}{4g_{ds}^2 + \omega^2(C_1 + C_2)^2} + R_{b2} + R_{sub} \tag{4.70}$$

$$\mathrm{Re}\{Z_{42}\} = \mathrm{Re}\{Z_{24}\} = \mathrm{Re}\{Z_{41}\} = \mathrm{Re}\{Z_{14}\} = R_{sub} \tag{4.71}$$

$$\mathrm{Re}\{Z_{44}\} = R_{b1} + R_{sub} \tag{4.72}$$

To extract all resistances, g_{ds} is supposed to be proportional to $V_{GS} - V_{TH}$ (as in the Bracale's method with all the underlying assumptions) and the term $\omega^2(C_1 + C_2)^2$ is considered negligible in comparison to $4g_{ds}^2$. Figure 4.18 shows the extraction procedure of the resistances by plotting $\mathrm{Re}\{Z_{ij}\}$ versus the inverse of the gate voltage overdrive GVO (strong inversion regime is assumed). First, it can be seen that $\mathrm{Re}\{Z_{11}\}$ is linearly dependent on $1/GVO$ whereas Equation 4.66 is not. This decreasing trend is however very small with a slope of $-0.077\,\Omega\,\mathrm{V}$. In fact, by computing the imaginary part of Y_{12}/ω and Y_{13}/ω (not shown) representing respectively C_{gdtot} and C_{gstot}, a difference of 0.8% was found meaning that the hypothesis of symmetrical capacitances is not totally verified. One can also notice that all Z-parameters except those related to the back-gate are around $45\,\Omega$ or above. This will be linked to the resistance R_{b2}.

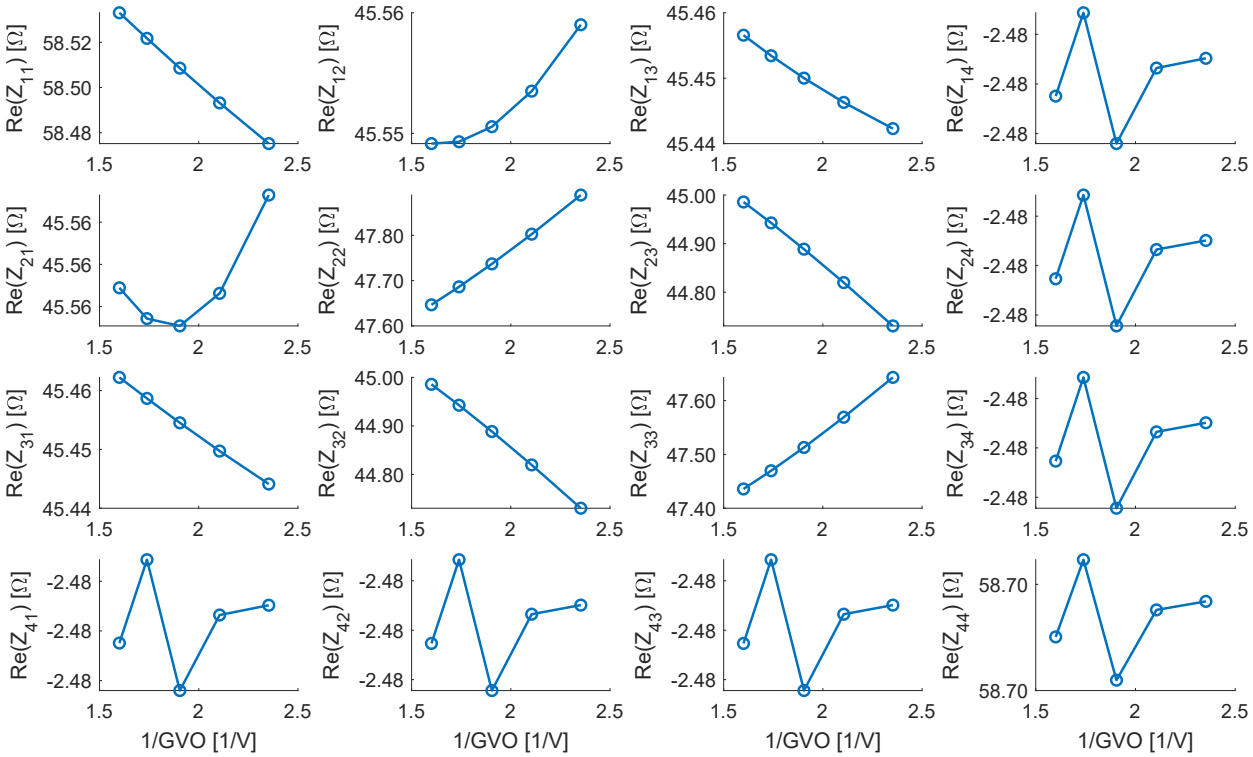


Figure 4.18: Extraction of series resistances based on a $1/GVO$ linear regression in cold FET ($V_{DS} = 0\,\mathrm{V}$) with $GVO_{min} = 0.4\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$. The device considered here is a 4-Port UTBB FDSOI MOSFET whose small-signal equivalent circuit is shown in Figure 4.16.

Finally, all resistances can be found from

$$R_{sub} = \mathrm{Re}\{Z_{42}\} \tag{4.73}$$
$$R_{b2} = \mathrm{Re}\{Z_{12}\} - R_{sub} \tag{4.74}$$
$$R_g = \mathrm{Re}\{Z_{11}\} - R_{sub} - R_{b2} \tag{4.75}$$
$$R_d = \mathrm{Re}\{Z_{22}\}|_{1/GVO=0} - R_{sub} - R_{b2} \tag{4.76}$$
$$R_s = \mathrm{Re}\{Z_{33}\}|_{1/GVO=0} - R_{sub} - R_{b2} \tag{4.77}$$
$$R_{b1} = \mathrm{Re}\{Z_{44}\} - R_{sub} \tag{4.78}$$

Since $\mathrm{Re}\{Z_{42}\}$ is negative and approximately equal to $-2.482\,\Omega$, it was decided to set R_{sub} to $0\,\Omega$. From that, all resistances are computed based on Equations 4.73-4.78. The extracted resistances values are given in Table 4.7.

R_g	R_d	R_s	R_{b1}	R_{b2}	R_{sub}
$13.11\,\Omega$	$1.59\,\Omega$	$1.45\,\Omega$	$58.7\,\Omega$	$45.54\,\Omega$	$0\,\Omega$

Table 4.7: Extracted series resistances from *ELDO* simulations using a 4-P small-signal model.

By comparing these values with the ones obtained from the 3-Port small-signal model (see Table 4.1), one can observe that the extracted values of R_g and R_s are close. However, R_d is 8% higher in the 4-Port case. Moreover, R_{b1-3P} is approximately $20\,\Omega$ higher than R_{b1-4P}. This is most probably due to the fact that R_{b1-3P} takes somehow the contribution of both R_{b1-4P} and R_{b2-4P} into account.

The series resistances can be removed from the total device impedance matrix as follows

$$Z_{DUT} = Z_{DUT-total} - R_{series} \tag{4.79}$$

Where R_{series} is defined as

$$R_{series} = \begin{bmatrix} R_g + R_{b2} & R_{b2} & R_{b2} & 0 \\ R_{b2} & R_d + R_{b2} & R_{b2} & 0 \\ R_{b2} & R_{b2} & R_{se} + R_{b2} & 0 \\ 0 & 0 & 0 & R_{b1} \end{bmatrix} + R_{sub}\mathbf{1} \tag{4.80}$$

With **1** a matrix only composed of 1.

After the removal of the access resistances (and R_{sub} which is equal to 0 here) and $C_{well-sub}$ (obtained in cold regime and deep depletion as for the 3-Port model), the total capacitances as well as the transconductances and output conductance are extracted in saturation and strong inversion regime. The admittance matrix $Y_{DUT} = Z_{DUT}^{-1} = (Z_{DUT-total} - R_{series})^{-1}$ is given by

$$\mathbf{Y_{DUT}} = \begin{bmatrix} \mathbf{Y_A} & \mathbf{Y_B} \\ \mathbf{Y_C} & \mathbf{Y_D} \end{bmatrix} \tag{4.81}$$

Where $\mathbf{Y_A}$, $\mathbf{Y_B}$, $\mathbf{Y_C}$ and $\mathbf{Y_D}$ are defined as

$$\mathbf{Y_A} = \begin{bmatrix} j\omega(C_{gstot} + C_{gdtot} + C_{gbtot}) & -j\omega C_{gdtot} \\ y_{mi} - j\omega C_{gdtot} & g_{dsi} + j\omega(C_{dstot} + C_{gdtot} + C_{bdtot}) \end{bmatrix} \tag{4.82}$$

$$\mathbf{Y_B} = \begin{bmatrix} -j\omega C_{gstot} & -j\omega C_{gbtot} \\ -y_{mi} - y_{mbi} - g_{dsi} - j\omega C_{dstot} & y_{mbi} - j\omega C_{bdtot} \end{bmatrix} \tag{4.83}$$

$$\mathbf{Y_C} = \begin{bmatrix} -y_{mi} - j\omega C_{gstot} & -g_{dsi} - j\omega C_{dstot} \\ -j\omega C_{bgtot} & -j\omega C_{bdtot} \end{bmatrix} \tag{4.84}$$

$$\mathbf{Y_D} = \begin{bmatrix} y_{mi} + y_{mbi} + g_{dsi} - j\omega(C_{dstot} + C_{gstot} + C_{bstot}) & -y_{mbi} - j\omega C_{bstot} \\ -j\omega C_{bstot} & j\omega(C_{bstot} + C_{bdtot} + C_{bgtot}) \end{bmatrix} \tag{4.85}$$

Therefore, most of the elements can be extracted from either the real or imaginary part of Y_{DUTij}. For example, one has

$$g_{mi} = \mathrm{Re}\{Y_{A21}\} \tag{4.86}$$
$$g_{mbi} = \mathrm{Re}\{Y_{B22}\} \tag{4.87}$$
$$g_{dsi} = \mathrm{Re}\{Y_{A22}\} \tag{4.88}$$
$$C_{ggtot} = \mathrm{Im}\{Y_{A11}\}/\omega \tag{4.89}$$
$$C_{bbtot} = \mathrm{Im}\{Y_{D22}\}/\omega \tag{4.90}$$

By comparing the extracted values of the 4-Port model presented in Table 4.8 with the ones of the 3-Port model (see Table 4.3), one can see that the percentage of error on g_{mi} is under 1% between the two models. In addition, g_{mbi} and g_{dsi} are even equal. The same can be said for the total front and back-gate capacitances where an absolute deviation of 0.28 fF and 0.48 fF is measured respectively.

Parameter	g_{mi}	g_{mbi}	g_{dsi}	C_{ggtot}	C_{bbtot}	$C_{well-sub}$
Value	120.8 mS	10.1 mS	9.9 mS	65.27 fF	13.3 fF	17.9 fF

Table 4.8: Extracted intrinsic/total elements in saturation ($V_{DS} = 0.8\,\mathrm{V}$ and $V_{GS} = 0.8\,\mathrm{V}$) using the 4-Port small-signal model. $C_{well-sub}$ is extracted in deep depletion and cold FET ($V_{DS} = 0\,\mathrm{V}$).

Finally, in order to assess the quality of the model, the reconstructed Y-parameters are compared to the initial Y-matrix in saturation. As it can be seen in Figures 4.19 and 4.20, the small-signal model is in good agreement with the results of *Eldo* simulations up to 10 GHz. The real part of the Z-parameters is plotted in Figure 4.21. Because R_{sub} was set to $0\,\Omega$, the back-gate related parameters except $\mathrm{Re}\{Z_{44}\}$ are flat and almost equal to $0\,\Omega$.

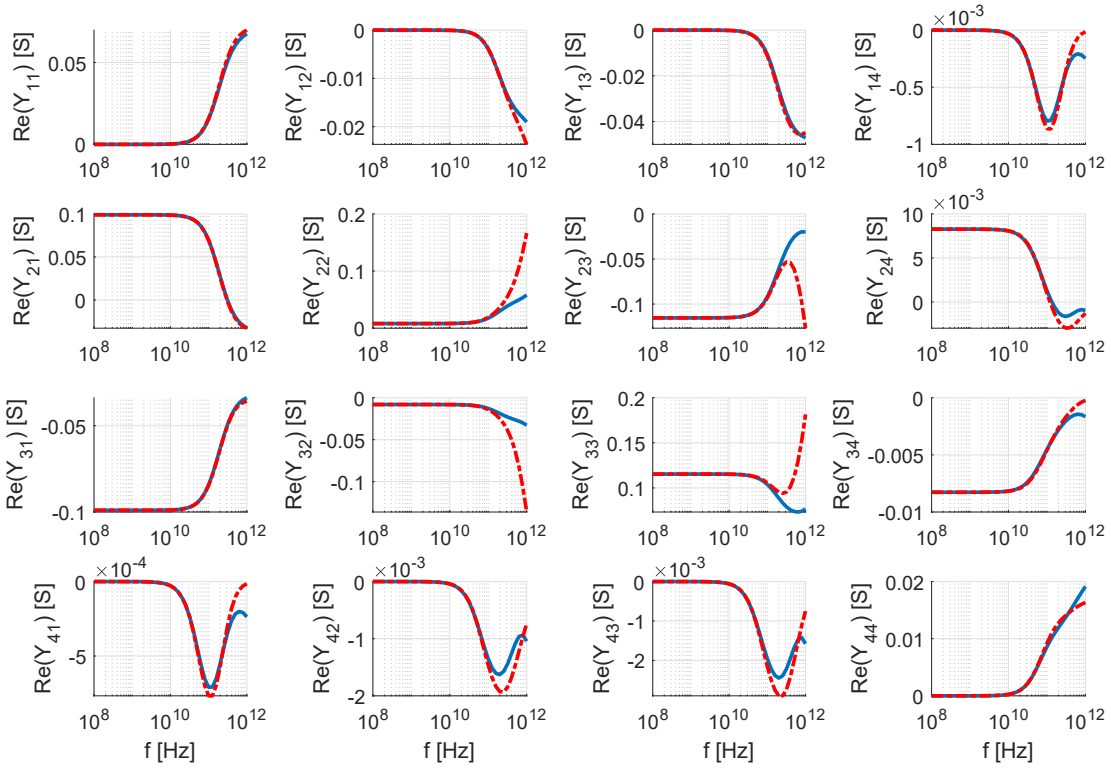


Figure 4.19: Reconstructed (dashed) vs initial (full) $\mathrm{Re}\{Y_{ij}\}$ in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$ for a 4-port device.

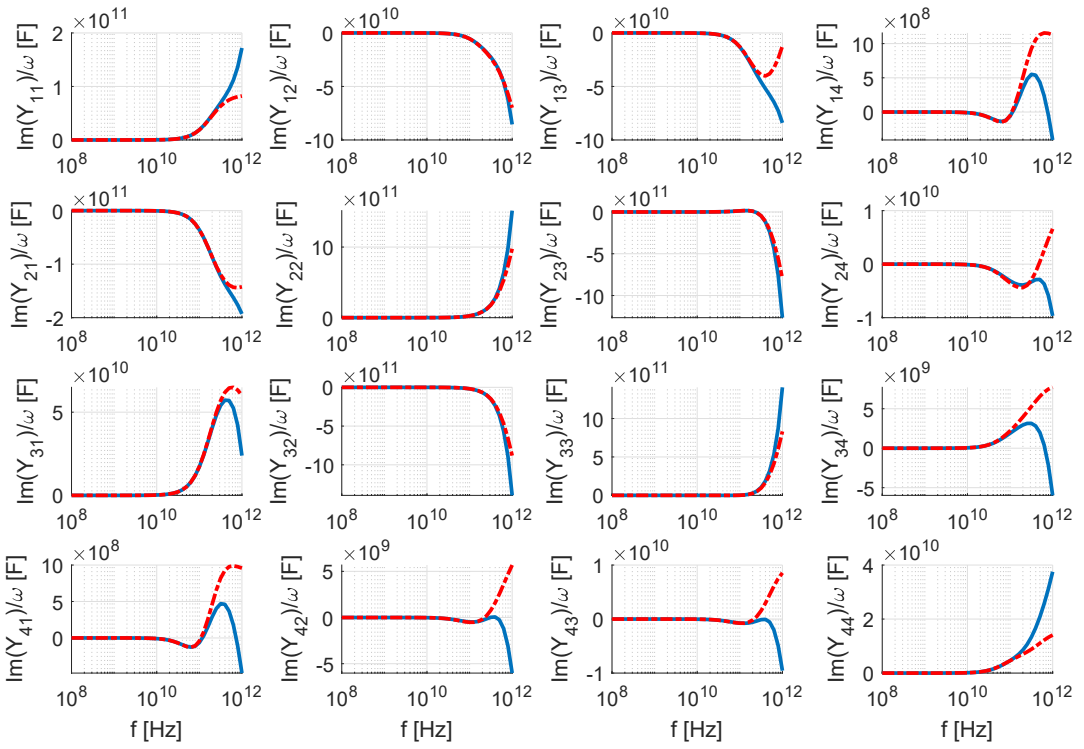


Figure 4.20: Reconstructed (dashed) vs initial (full) $\mathrm{Im}\{Y_{ij}\}/\omega$ in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$ for a 4-port device.

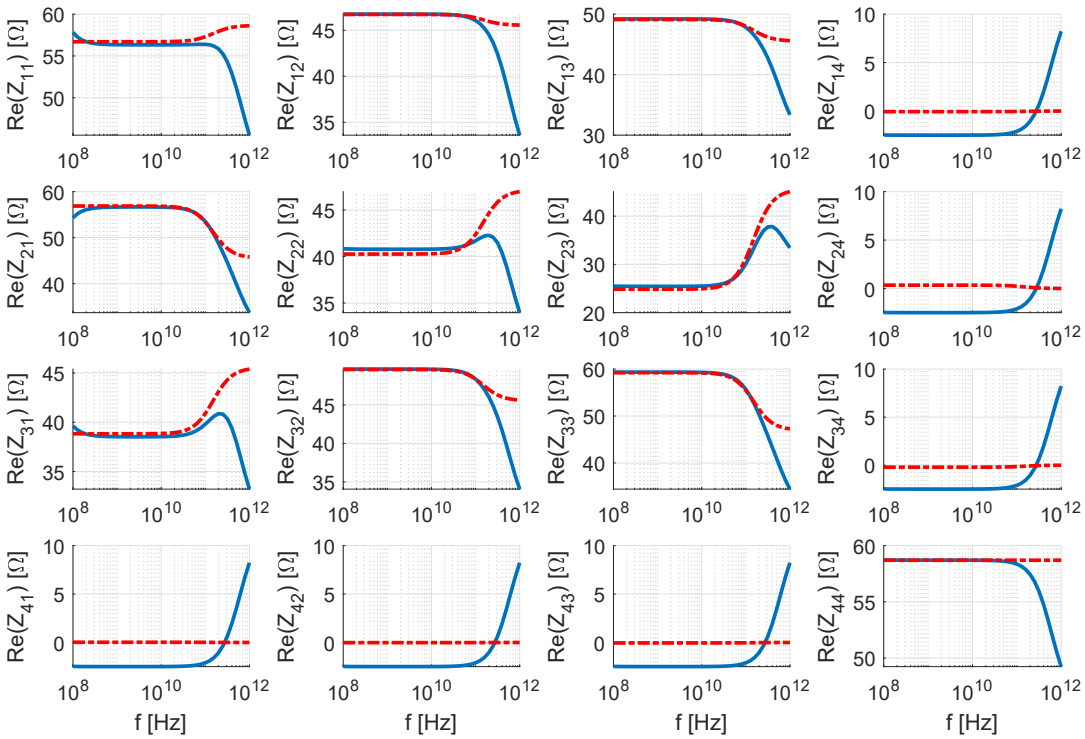


Figure 4.21: Reconstructed (dashed) vs initial (full) $\mathrm{Re}\{Z_{ij}\}$ in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$ for a 4-port device.

Although the 4-port small-signal equivalent circuit gives more information and can be used to extract R_{b2} and R_{sub}, it was found that its application on the 4-Port measurements was difficult, especially for the first step being the extraction of series resistances. Indeed, as it can be seen in Figure 4.22, the real part of the Z-parameters in cold regime and after de-embedding is highly dependent on the frequency. Moreover, the "open" de-dembedding results in a strong increase of the Z-parameters. For example, at $f = 10\,\mathrm{GHz}$, $\mathrm{Re}\{Z_{22}\} \approx 5\,\Omega$ without de-embedding while $\mathrm{Re}\{Z_{22}\} \approx 104\,\Omega$ with de-embedding. Therefore, in the next section, only the 3-Port small-signal model will be used to analyze the experimental measurements.

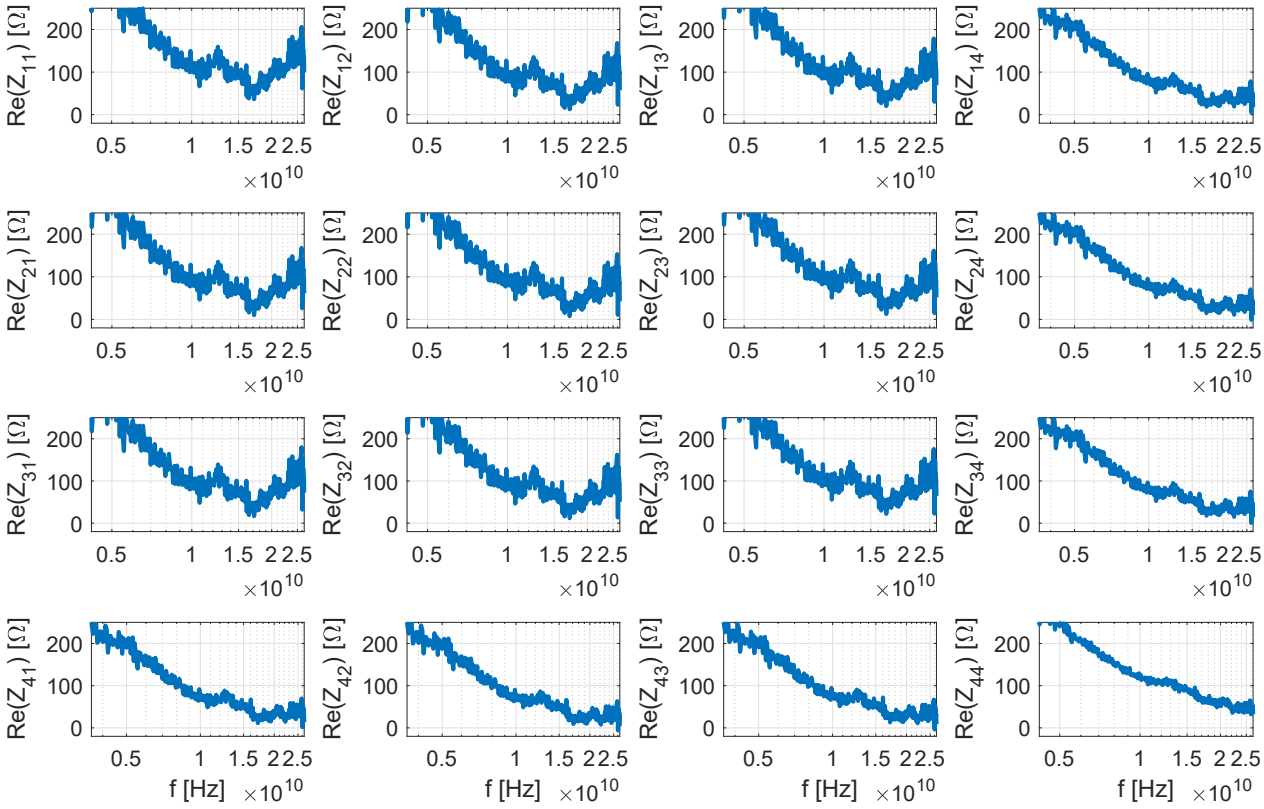


Figure 4.22: Z-parameters of a 20 nm-SLVT transistors in cold regime at $V_{GS} = 0.9\,\mathrm{V}$.

4.4 Measurements and discussion

In this section, the methodology developed for 3-port FDSOI MOSFETs (see Section 4.3.1) will be applied to measurements performed on 22FDX SLVT transistors from *GlobalFoundries*. The measured devices feature a 20 nm-gate length (L_g) and 64 fingers of 1 µm width. The Si film, the buried oxide (BOX) and the substrate thicknesses are 6 nm, 20 nm and 150 µm, respectively. A back-gate RF contact is also available enabling 4-port measurements up to 26.5 GHz (VNA frequency limit) for different bias conditions (cold, saturation). The 4x4 scattering matrix is de-embedded by a dedicated open structure and then converted into Y-parameters. Finally, the 4x4 admittance matrix is reduced to a 3x3 matrix in order to apply the 3-port small-signal model:

$$Y_{4-Port} = \begin{bmatrix} Y_{gg} & Y_{gd} & Y_{gs} & Y_{gb} \\ Y_{dg} & Y_{dd} & Y_{ds} & Y_{db} \\ Y_{sg} & Y_{sd} & Y_{ss} & Y_{sb} \\ Y_{bg} & Y_{bd} & Y_{bs} & Y_{bb} \end{bmatrix} \quad \Longrightarrow \quad Y_{3-Port} = \begin{bmatrix} Y_{gg} & Y_{gd} & Y_{gb} \\ Y_{dg} & Y_{dd} & Y_{db} \\ Y_{bg} & Y_{bd} & Y_{bb} \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \tag{4.91}$$

As before, Port 1 refers to the gate, Port 2 to the drain and Port 3 to the back-gate.

4.4.1 Extraction of small-signal equivalent circuit

As explained in Section 4.3.1, the extrinsic series resistances are extracted from "cold" FET measurements ($V_{DS} = 0\,\mathrm{V}$) by employing a method similar to the Bracale's method [41]. The threshold voltage is extracted from the maximum of C_{gg} derivative after smoothing and filtering $C_{gg} - V_{GS}$ curve (see Section 3.4.2). This method gives $V_{TH} = 0.295\,\mathrm{V}$ while other current-based methods give slightly lower V_{TH}. At $V_B = 0\,\mathrm{V}$, a maximum difference of $\Delta V_{TH} = 0.025\,\mathrm{V}$ is observed between $\mathrm{d}C_{gg}/\mathrm{d}V_{GS}$ method and other current-based methods. In our case, this represents a variation in the order of 3% of R_s and R_d.

Figure 4.23 shows the measured $\mathrm{Re}\{Z_{ij}\}$ in cold FET for different front-gate bias. From these graphs, one can compute each element as an average over a specific frequency range. In this case, the frequency range chosen for each element is represented by two vertical dashed lines.

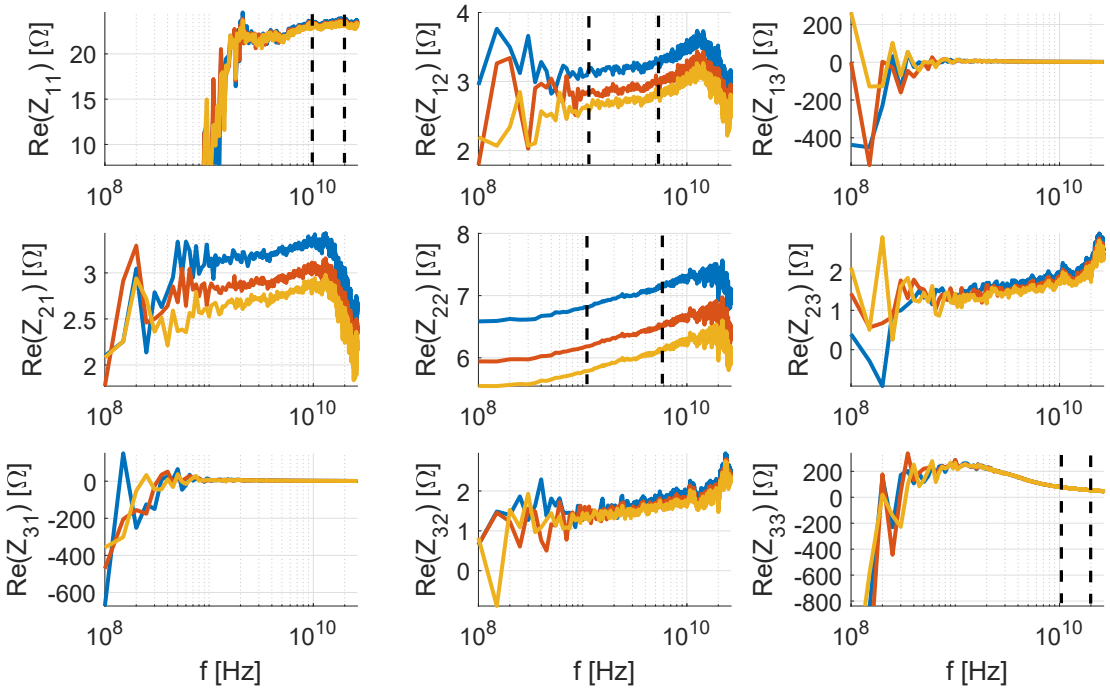


Figure 4.23: $\mathrm{Re}\{Z_{ij}\}$ in cold regime ($V_{DS} = 0\,\mathrm{V}$) for V_{GS} ranging from 0.7 V to 0.9 V and $V_B = 0\,\mathrm{V}$. The dashed lines represent the frequency range to compute the average elements.

The extraction procedure of series resistances from a linear extrapolation is illustrated in Figure 4.24. To ensure that the transistor operates in strong inversion, the gate voltage overdrive is set to $GVO_{min} = 0.4\,\mathrm{V}$. However, at this GVO_{min}, only three points remain making the linearity assumption difficult to verify (mobility variation with V_{GS} and asymmetric drain and source capacitances are still neglected here). The extracted series resistances are given in Table 4.9.

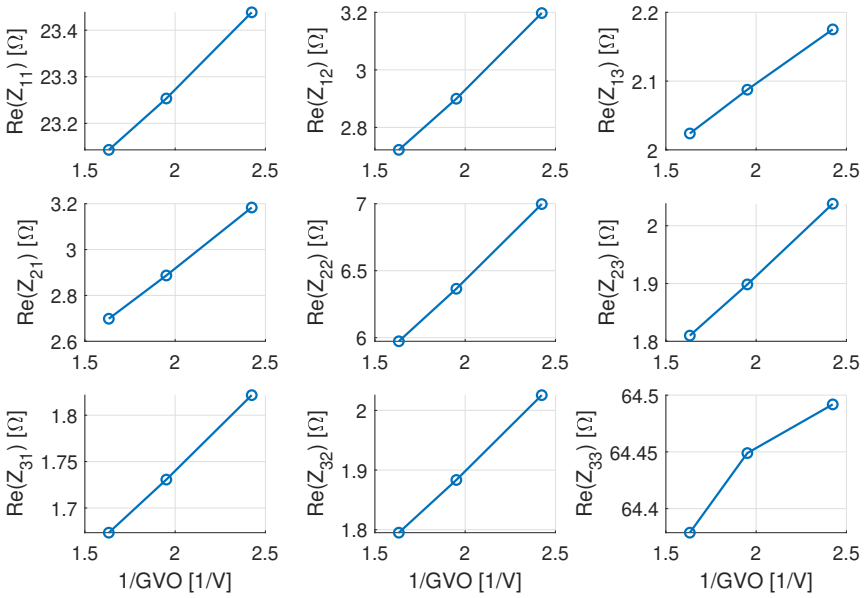


Figure 4.24: Extraction of series resistances based on a $1/GVO$ linear regression in cold FET ($V_{DS} = 0\,\mathrm{V}$) with $GVO_{min} = 0.4\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$.

R_g	R_d	R_s	R_{b1}
$20.37\,\Omega$	$1.98\,\Omega$	$1.88\,\Omega$	$63.36\,\Omega$

Table 4.9: Extracted series resistances using "corrected" linear regressions as a function of $1/GVO$ (in strong inversion).

Following the steps described in Section 4.3.1, the extrinsic capacitances can be extracted in cold FET and deep depletion ($V_{GS} = -0.2\,\mathrm{V}$) while the intrinsic transconductances, output conductance and total capacitances can be extracted in saturation ($V_{DS} = 0.8\,\mathrm{V}$). An average over the $1 - 2$GHz frequency range is used to evaluate each parameter. Table 4.10 summarizes the main extrinsic "e", intrinsic "i" and total "tot" (sum of intrinsic and extrinsic) parameters. As it can be noticed, the parasitic elements (C_{gge} and C_{bbe}) can become an important fraction of the total elements in nano-scaled devices. Thus, their impact is no longer small (compared to the intrinsic elements) and can even dominate device performance [3].

Parameter	g_{mi}	g_{mbi}	g_{dsi}	C_{ggtot}	C_{bbtot}	C_{gge}	C_{bbe}	$C_{well-sub}$
Value	122.9 mS	9.7 mS	13.8 mS	65.7 fF	14.3 fF	38.7 fF	13.8 fF	22.4 fF

Table 4.10: Extracted intrinsic/total and extrinsic parameters in saturation ($V_{DS} = 0.8\,\mathrm{V}$ and $V_{GS} = 0.8\,\mathrm{V}$) and cold FET ($V_{DS} = 0\,\mathrm{V}$), respectively ($V_B = 0\,\mathrm{V}$).

The results of reconstructed small-signal equivalent circuit are compared to measurements in Figures 4.25-4.27. Several important points can be drawn from these results. First, it can be seen that the extrinsic output conductance $g_{dse} = \mathrm{Re}\{Y_{22}\}$ showcases a small hump. It can be attributed to dynamic self-heating and substrate effects [44]. The concavity of this hump

changes at around $V_{GS} = 0.62\,\mathrm{V}$ (and below) demonstrating the presence of the ZTC point. By sweeping temperature in *Eldo* simulations, one finds a current invariable with temperature at $V_{GS} = 0.57\,\mathrm{V}$ which is close the previous value. Secondly, all parameters start to diverge from the measurements at higher frequency. This behaviour was expected since this simple model does not take into account series inductances, non-quasi static effects and distributed elements. The de-embedding procedure can also strongly affect the final S-parameters. Finally, $\mathrm{Im}\{Y_{33}\}/\omega$ and $\mathrm{Re}\{Z_{33}\}$ clearly exhibit a non-linear behaviour which is completely ignored by the model. It could be due to important substrate effects which were not properly modelled (simple junction capacitance). A more complex substrate network could probably improve the fitting between the model and the measurements.

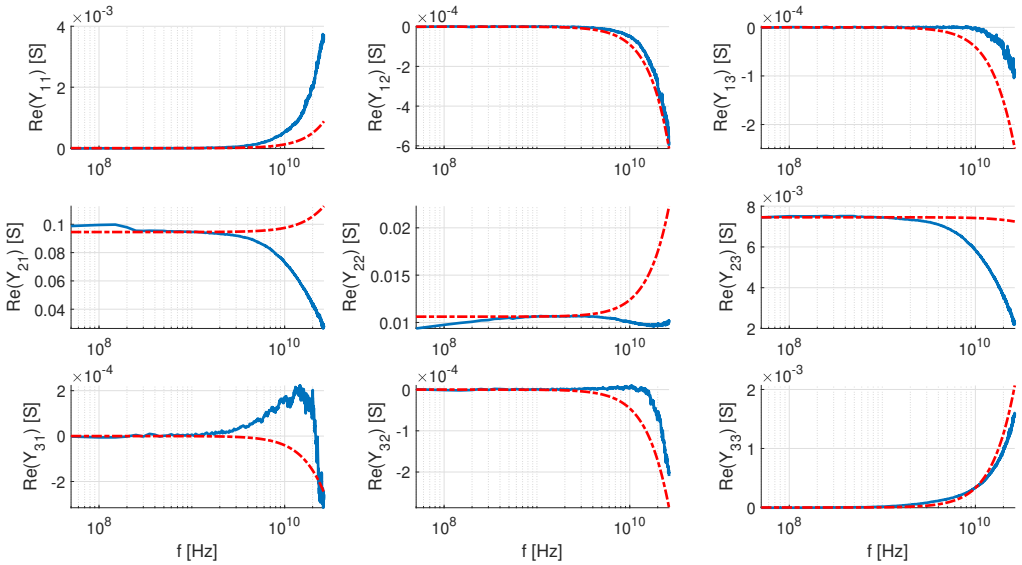


Figure 4.25: Model (dashed) vs measurements (full) of $\mathrm{Re}\{Y_{ij}\}$ in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$ for a 3-port device.

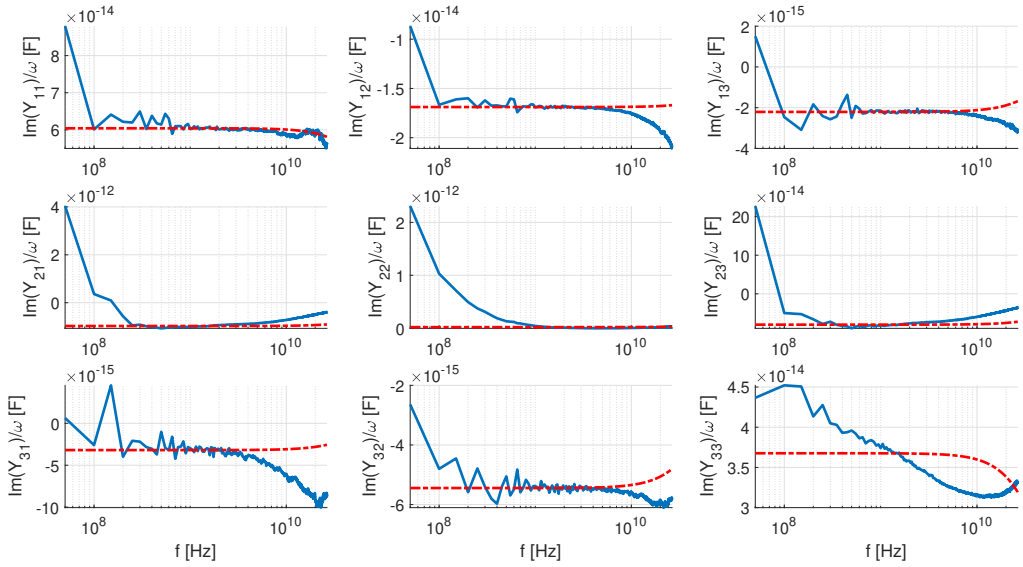


Figure 4.26: Model (dashed) vs measurements (full) of $\mathrm{Im}\{Y_{ij}\}$ in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$ for a 3-port device.

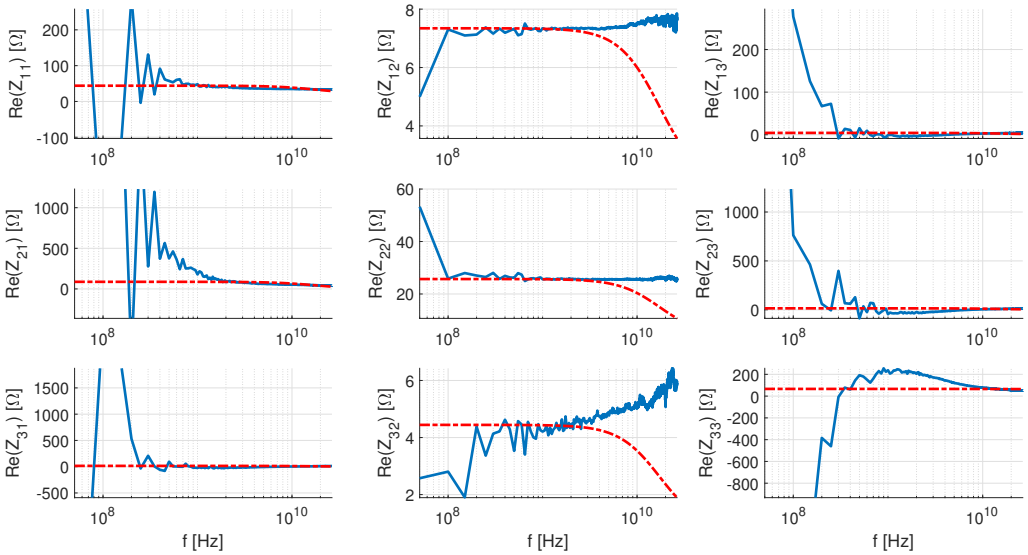
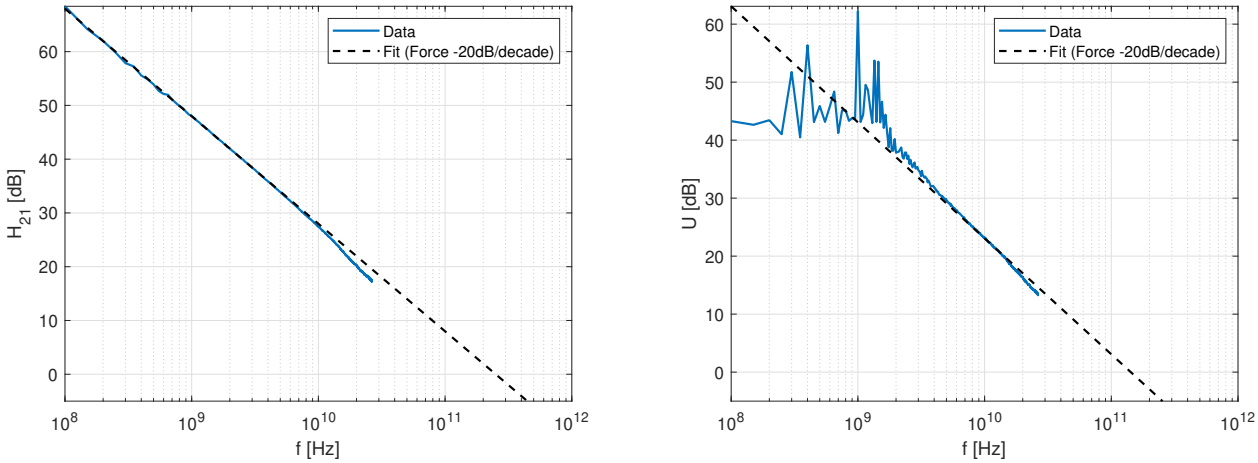


Figure 4.27: Model (dashed) vs measurements (full) of $\mathrm{Re}\{Z_{ij}\}$ in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$ for a 3-port device.

4.4.2 RF Figures of Merit and discussion

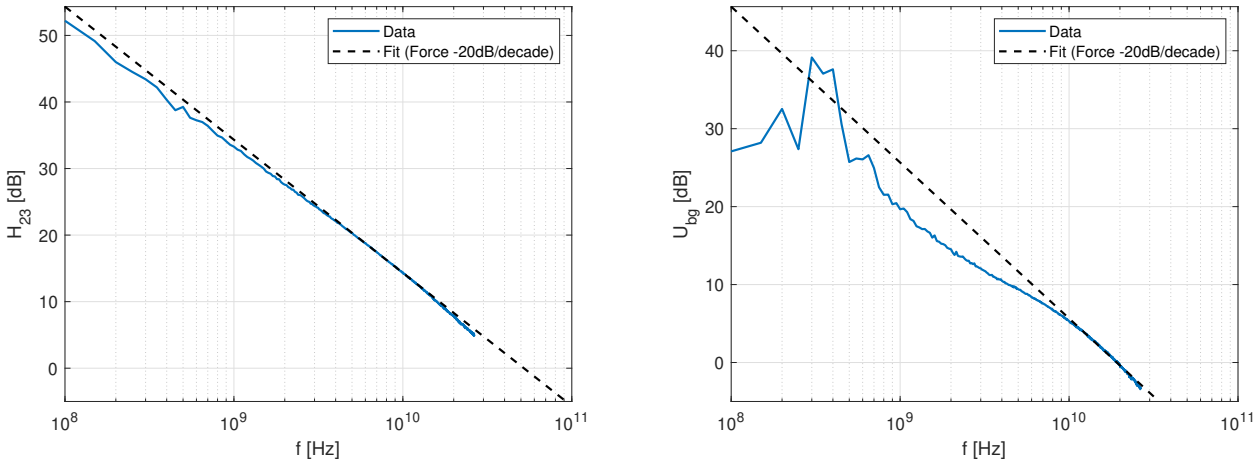
In this section, the two main front and back-gate RF Figures of Merit, namely the cut-off frequency and the maximum oscillation frequency, are studied. Their dependence on the back-gate bias V_B is also analyzed. Once again, f_T and f_{max} are calculated by doing a linear extrapolation of H_{21} and U (H_{23} and U_{bg} for the back-gate) to unity (0 dB). However, as represented in Figures 4.28b and 4.29b, U and U_{bg} deviate from the $-20\,\mathrm{dB/dec}$ theoretical slope predicted by the small-signal equivalent circuit at lower frequencies. In fact, both expressions of U and

U_{bg} (Equations 4.61 and 4.63) are dependent on the output conductance which is affected by dynamic self-heating and substrate effects [44]. Therefore, based on another common way to extract f_T and f_{max} (see Appendix D), an appropriate frequency range is chosen for each linear extrapolation. "Appropriate" means here that the corresponding slope is close to $-20\,\mathrm{dB/dec}$. The chosen frequency ranges are specified in Table 4.11.



(a) (b)

Figure 4.28: (a) H_{21} and (b) U versus frequency in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$. The dashed lines indicate the linear extrapolation realized by forcing a $-20\,\mathrm{dB/dec}$ slope.



(a) (b)

Figure 4.29: (a) H_{23} and (b) U_{bg} versus frequency in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$. The dashed lines indicate the linear extrapolation realized by forcing a $-20\,\mathrm{dB/dec}$ slope.

Parameter	Frequency range [GHz]
f_T	1-3
f_{max}	10-13
f_{Tbg}	7-12
f_{maxbg}	11-15

Table 4.11: Frequency range chosen for the linear extrapolation of each parameter.

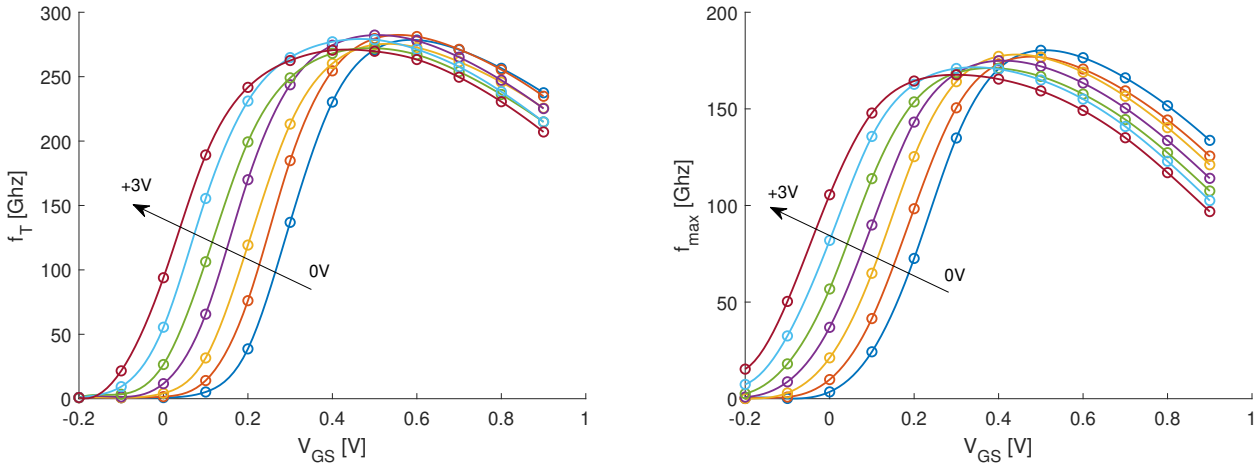
Front-gate RF FoMs

Figure 4.30 shows the front-gate cut-off frequency f_T and maximum oscillation frequency f_{max} versus the front-gate voltage V_{GS} for different back-gate biases. Their values are extracted in saturation ($V_{DS} = 0.8\,\mathrm{V}$) for each bias point by doing a linear extrapolation as explained in the preceding section. The back-gate voltage is swept from 0 V to 3 V by steps of 0.5 V. First, it can be seen that the maximum achievable f_T is 282 GHz at $V_{GS} = 0.56\,\mathrm{V}$ and $V_B = 0.5\,\mathrm{V}$. This value is unexpectedly low compared to the 347 GHz reported in [45] for this technology. It is most probably due to presence of strong parasitic elements which were not properly cancelled by de-embedding. In fact, an improvement of 84% (153 GHz to 282 GHz) was already observed by de-embedding S-parameters with an "Open" structure.

Then, following Equation 4.60 one should expect the transconductance g_m and the cut-off frequency f_T to exhibit similar behaviour since one parameter (f_T) depends on another. As it can be seen in Figure 4.31a, the extrinsic transconductance (without removal of series resistances) can be correlated to f_T curves. Indeed, the maximum cut-off frequency $f_{T,max}$ tends to decrease for positive back-gate biases exactly as the maximum extrinsic transconductance $g_{me,max}$ due to the shift of the mean channel position towards the Si film/BOX interface. However, f_T is not maximum at the same front-gate voltage V_{GS} than $g_{me,max}$. This can be explained by the slight dependence of the total front-gate capacitance on the back-gate voltage as illustrated in Figure 4.31b. A 3% difference is observed between the lowest and highest values at $V_{GS} = 0.6\,\mathrm{V}$. It is also the reason why $f_{T,max}$ does not occur at $V_B = 0\,\mathrm{V}$ but at $V_B = 0.5\,\mathrm{V}$.

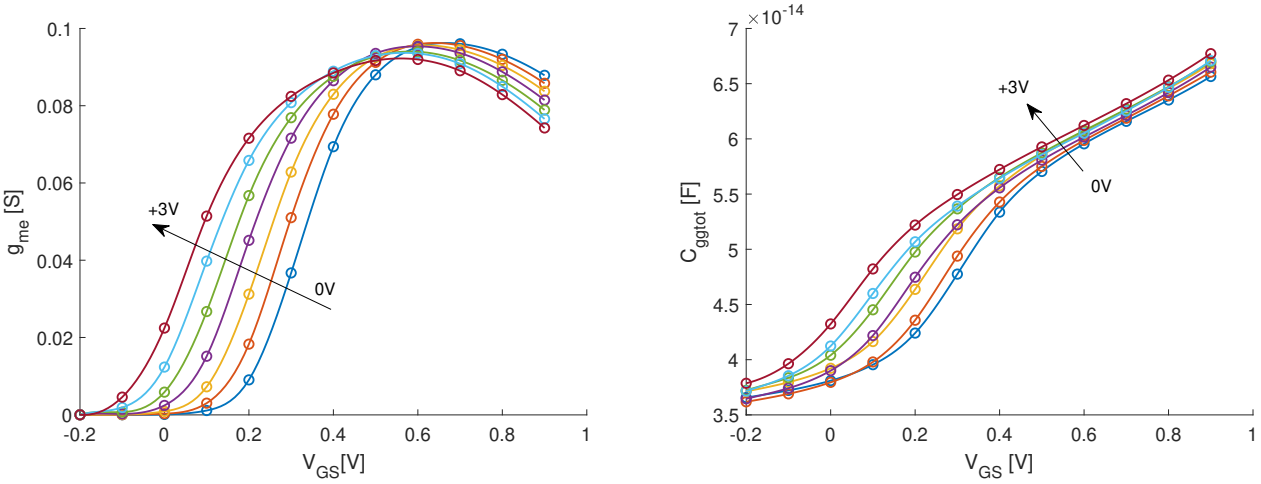
The series resistance R_g also impacts the RF performance of the transistor as shown by the additional reduction of f_{max} compared to f_T. A maximum f_{max} of 180 GHz is reported. Furthermore, by increasing the back-gate bias, the threshold voltage is shifted to lower V_{GS} and as a result the output conductance measured at one V_{GS} increases with V_B. This trend is depicted in Figure 4.32. At $V_{GS} = 0.6\,\mathrm{V}$, the output conductance even doubles (5.5 mS to 11 mS) by increasing V_B from 0 V to 3 V. Thus, this effect will further reduce f_{max}.

Finally, one can notice that positive back-gate biasing flattens the $f_T(V_{GS})$ and $f_{max}(V_{GS})$ curves. Consequently, high f_T and f_{max} values can be achieved over wider range of front-gate voltage.



(a) (b)

Figure 4.30: Extracted (a) f_T and (b) f_{max} versus V_{GS} in saturation ($V_{DS} = 0.8\,\mathrm{V}$) for different back-gate bias ranging from 0 V to 3 V by steps of 0.5 V.



(a) (b)

Figure 4.31: Extracted (a) g_{me} and (b) C_{ggtot} versus V_{GS} in saturation ($V_{DS} = 0.8\,\mathrm{V}$) for different back-gate bias ranging from 0 V to 3 V by steps of 0.5 V.

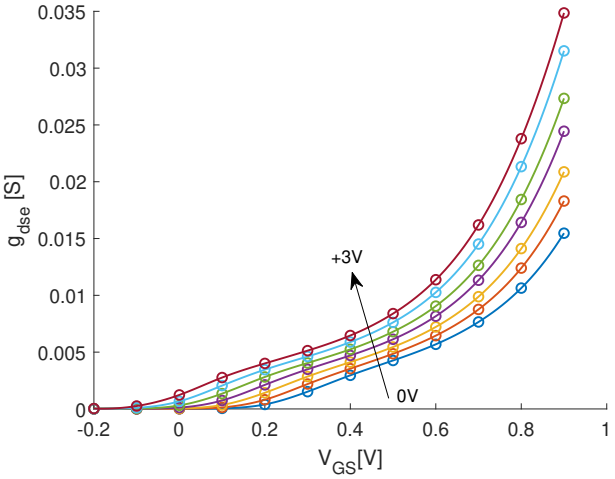
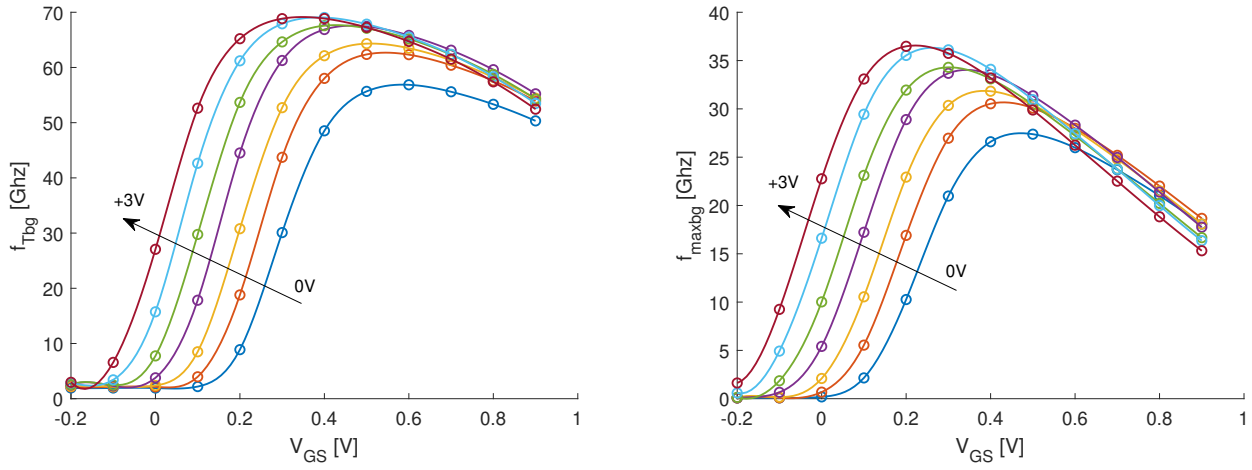


Figure 4.32: Extracted g_{dse} versus V_{GS} in saturation ($V_{DS} = 0.8\,\mathrm{V}$) for different back-gate bias ranging from 0 V to 3 V by steps of 0.5 V.

Back-gate RF FoMs

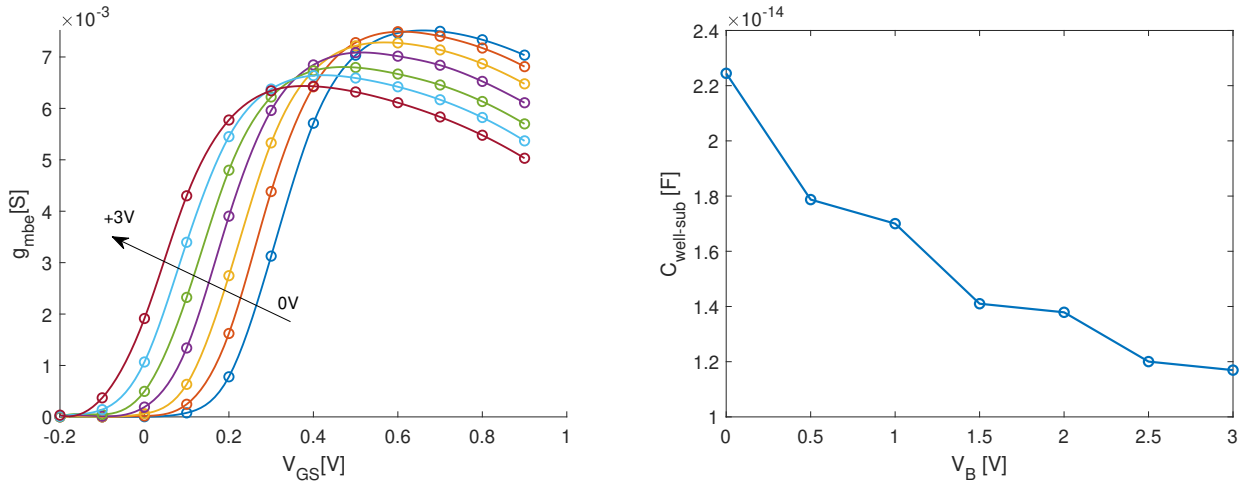
The back-gate RF FoMs f_{Tbg} and f_{maxbg} versus the front-gate voltage are plotted for various back-gate biases in Figure 4.33. It can seen that the maximum achievable f_{Tbg} and f_{maxbg} are respectively 69 GHz and 36 GHz both at $V_B = 3\,\mathrm{V}$. Similarly to the front-gate case, the onsets of f_{Tbg} curves can be correlated to the extrinsic back-gate transconductance g_{mbe} shown in Figure 4.34. However, unlike f_T curves which flatten with a shift of $f_{T,max}$ to lower V_{GS} for positive back-gate bias, f_{Tbg} curves display a more pronounced peak $f_{Tbg,max}$ (still at lower V_{GS}) when V_B is increased. Since the maximum extrinsic back-gate transconductance $g_{mbe,max}$ drops with V_B, this cannot explain the improvement of $f_{Tbg,max}$. Thus, it was attributed to the reduction of $C_{well-sub}$ with V_B. Indeed, one can notice in Figure 4.34b a significant impact of the back-gate bias on the extracted values of $C_{well-sub}$ with a drop of 10.8 fF (almost halved) between $V_B = 0\,\mathrm{V}$ and $V_B = 3\,\mathrm{V}$. In fact, this junction capacitance between the n-well and p-substrate $C_{well-sub}$ (reverse-bias diode) is inversely proportional to V_B. Moreover, one can also observe a similarity between this result and the curve found in Section 3.5.2 from TCAD simulations. In [6], K. Esfeh et al. reached the same conclusion with the only difference being that the contribution of $C_{well-sub}$ was merged to the extrinsic back-gate/source capacitance C_{bse}.

Regarding f_{maxbg}, lower maximum values are achieved compared to f_{Tbg} due to the high back-gate resistance R_b and the output conductance g_{dse}. However, the maximum back-gate oscillation frequency $f_{maxbg,max}$ is still obtained for $V_B = 3\,\mathrm{V}$ like $f_{Tbg,max}$ due to the improvement of $C_{well-sub}$. For $V_{GS} > 0.6\,\mathrm{V}$, higher V_B results in decreasing f_{maxbg} which could be due to the increasingly contribution of g_{dse} in these conditions (see Figure 4.32), thereby dominating over the improvement of $C_{well-sub}$.



(a) (b)

Figure 4.33: Extracted (a) f_{Tbg} and (b) f_{maxbg} versus V_{GS} in saturation ($V_{DS} = 0.8\,\mathrm{V}$) for different back-gate bias ranging from 0 V to 3 V by steps of 0.5 V.



(a) (b)

Figure 4.34: (a) Extracted g_{mbe} versus V_{GS} in saturation ($V_{DS} = 0.8\,\mathrm{V}$) for different back-gate bias ranging from 0 V to 3 V by steps of 0.5 V. (b) $C_{well-sub}$ vs V_B extracted in cold regime ($V_{DS} = 0\,\mathrm{V}$) and deep depletion $-0.2\,\mathrm{V}$.

4.5 Conclusion

In this chapter, the impact of the back-gate bias on the main RF FoMs (f_T and f_{max}) was studied. First, the small-signal circuit theory was described, introducing the concepts of intrinsic, extrinsic and access elements. Then, the extraction of a 3-Port and 4-Port small-signal model was performed on *ELDO* simulations. In the 3-Port model case, the extrinsic resistances were obtained by a modified version of the Bracale's method. The series resistances were not simply taken as the intercept of the $\mathrm{Re}\{Z_{ij}\}$ versus $1/GVO$ curves with the y-axis but by applying an additional correction factor based on the slopes of these characteristics. In the 4-port model case, the resistance R_{sub} was added to the substrate network but it turned out that its contribution

to the Z-parameters was negligible in *ELDO* simulations (it is not the case for experimental measurements). However, the extraction of R_{b2}, which was associated to the GP resistance, was still possible. Finally, it was observed that both models were in good agreement expect for the back-gate resistances. This was latter attributed to the fact that the unique back-gate resistance of the 3-port model took into account the contribution of the two back-gate resistances of the 4-port model.

In a second phase, the extraction procedure of the 3-port small-signal equivalent circuit was applied to measurements on 22FDX SLVT transistors. Thanks to the dedicated back-gate RF pad, both front and back-gate RF FoMs were then extracted. It was shown that applying a back-gate bias had a major impact on RF FoMs. Shifting and flattening the f_T versus V_{GS} and f_{max} versus V_{GS} characteristics were the main consequences of back-gate biasing.

Finally, the following maximum front and back-gate cut-off and maximum oscillation frequencies were obtained:

$$\begin{aligned} f_T &= 282\,\text{GHz} \\ f_{max} &= 180\,\text{GHz} \\ f_{Tbg} &= 69\,\text{GHz} \\ f_{maxbg} &= 36\,\text{GHz} \end{aligned}$$

Chapter 5

Conclusion

In today's world, very high speed communication and real-time data collection are expected to become increasingly used with the advent of 5G. All kind of "connected" products from IoT to health care are also going to appear on the market. However, transistors meeting the high requirements of 5G specifications are still necessary. One of the promising technology is the UTBB FDSOI with highly doped region under the BOX.

In this work, this technology was assessed both in DC and RF operation. The **impact of the back-gate bias** on the threshold voltage and RF FoMs was studied.

In Chapter 3, it was shown that applying a back-gate bias shifts the $I_D - V_{GS}$ characteristics to the left for FBB and to the right for RBB. This effect can then be used to optimize performance or reduce power consumption (increasing the threshold voltage reduces the leakage current). A modulation of V_{TH} as high as -85mV/V was found for the 22FDX SLVT transistors in accordance with the values found in the literature.

In Chapter 4, the impact of the back-gate bias on the main RF FoMs (f_T and f_{max}) was studied. First, a modified version of the Bracale's method was developed in order to extract the series resistances of the 3-Port model. Only a small difference was observed by directly extracting the resistance from the intercept. The removal of C_{sub} before R_s thus had little importance. In 4-port, the resistances R_{sub} and R_{b2} were added but R_{sub} was negligible in *ELDO* simulations. However, the extraction of R_{b2}, which was associated to the GP resistance, was still possible. Finally, it was observed that both models were in good agreement expect for the back-gate resistances. This was latter attributed to the fact that the unique back-gate resistance of the 3-port model took into account the contribution of the two back-gate resistances of the 4-port model.

After that, the RF FoMs of 22FDX SLVT transistors were extracted for both front and back-gate. It was shown that applying a back-gate bias had a major impact on RF FoMs. Shifting and flattening the f_T versus V_{GS} and f_{max} versus V_{GS} characteristics were the main consequences of back-gate biasing. The following maximum front and back-gate cut-off and maximum oscillation frequencies were obtained:

$$f_T = 282\,\text{GHz}$$
$$f_{max} = 180\,\text{GHz}$$
$$f_{Tbg} = 69\,\text{GHz}$$
$$f_{maxbg} = 36\,\text{GHz}$$

Finally, one can cite two main future research objectives which correspond to the limitations of the present work.

- In this work, the **substrate network** was simply modelled by a $C_{well-sub}$ capacitance to ease the extraction of the other parameters. However, in all rigor, one should construct a group of RC parallel network in order to take into account minority and majority carriers in the substrate.
- **Self-heating** effect was neglected in the extraction of small-signal equivalent circuits. However, Makovejev et al. [44] demonstrated a degradation of the output conductance with self-heating. This degradation was also observed in the experimental measurements in Figure 4.25. Therefore, a first step would be to simulate this effect by means of TCAD simulations as shown in Figure 5.1. Changing the default Sentaurus model by the hydrodynamic model is necessary to compute temperature profiles. "Well-defined" boundary conditions are still subject to investigate. Biasing the transistor at ZTC point would also be interesting to decorrelate substrate effects from self-heating effects.

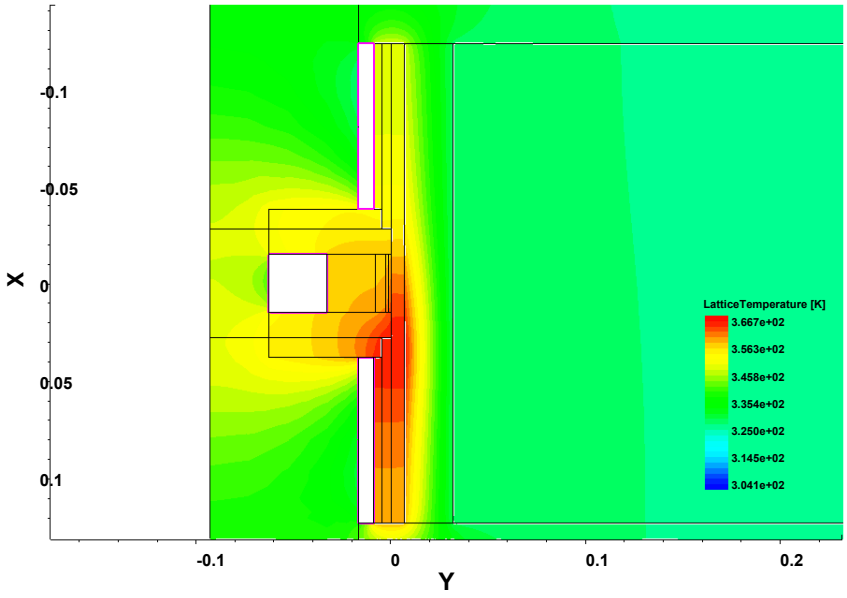


Figure 5.1: Temperature distribution in saturation $V_{DS} = 1\,\text{V}$ and strong inversion $V_{GS} = 1\,\text{V}$ ($V_B = 0\,\text{V}$). The drain is the "bottom" terminal where temperature is maximum.

Bibliography

[1] T. Tanaka, Tatsuya Usuki, Toshiro Futatsugi, Y. Momiyama, and Toshihiro Sugii. Vth fluctuation induced by statistical variation of pocket dopant profile. pages 271 – 274, 02 2000.

[2] Jerry G. Fossum and Vishal P. Trivedi. *Fundamentals of Ultra-Thin-Body MOSFETs and FinFETs*. Cambridge University Press, 2013.

[3] Valeriya Kilchytska, Sergej Makovejev, Mohd Khairuddin Md Arshad, Jean-Pierre Raskin, and Denis Flandre. *Perspectives of UTBB FD SOI MOSFETs for Analog and RF Applications*, pages 27–46. Springer International Publishing, Cham, 2014.

[4] Jean-Pierre Raskin. FinFET and UTBB for RF SOI communication systems. *Solid-State Electronics*, 125, 07 2016.

[5] B. Kazemi Esfeh, V. Kilchytska, B. Parvais, N. Planes, M. Haond, D. Flandre, and J. . Raskin. Back-gate bias effect on fdsoi mosfet rf figures of merits and parasitic elements. In *2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, pages 228–230, 2017.

[6] B. Kazemi Esfeh, V. Kilchytska, B. Parvais, N. Planes, M. Haond, D. Flandre, and J. . Raskin. Back-gate bias effect on FDSOI MOSFET RF Figures of Merits and parasitic elements. In *2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, pages 228–230, 2017.

[7] T. Rudenko, Alexei Nazarov, Valeria Kilchytska, and Denis Flandre. A review of special gate coupling effects in long-channel SOI MOSFETs with lightly doped ultra-thin bodies and their compact analytical modeling. *Solid-State Electronics*, 117, 11 2015.

[8] Synopsys. Sentaurus Device User Guide. `http://www.sentaurus.dsod.pl/manuals/data/sdevice_ug.pdf`, note = Accessed: 2020-01-14.

[9] J-P. Raskin. *Modeling, Characterization and Optimization of MOSFET's and Passive Elements for the Synthesis of SOI MMIC's*. PhD thesis, Université catholique de Louvain, December 1997.

[10] M. Dehan. *Characterization and modeling of SOI RF integrated components*. PhD thesis, Université catholique de Louvain, November 2003.

[11] J. . Colinge. Subthreshold slope of thin-film SOI MOSFET's. *IEEE Electron Device Letters*, 7(4):244–246, 1986.

[12] M.K. Md Arshad, S. Makovejev, S. Olsen, F. Andrieu, J.-P. Raskin, D. Flandre, and V. Kilchytska. UTBB SOI MOSFETs analog figures of merit: Effects of ground plane

and asymmetric double-gate regime. *Solid-State Electronics*, 90:56 – 64, 2013. Selected papers from EUROSOI 2012.

[13] A. Morelle. Assessment of the split CV mobility extraction method in 28nm FDSOI transistors. Master's thesis, Ecole Polytechnique de Louvain, 2020.

[14] K. Henson, H. Bu, M. H. Na, Y. Liang, U. Kwon, et al. Gate length scaling and high drive currents enabled for high performance SOI technology using high-/metal gate. In *2008 IEEE International Electron Devices Meeting*, pages 1–4, 2008.

[15] G. Masetti, M. Severi, and S. Solmi. Modeling of carrier mobility against carrier concentration in arsenic-, phosphorus-, and boron-doped silicon. *IEEE Transactions on Electron Devices*, 30(7):764–769, 1983.

[16] S. Reggiani, E. Gnani, A. Gnudi, M. Rudan, and G. Baccarani. Low-Field Electron Mobility Model for Ultrathin-Body SOI and Double-Gate MOSFETs With Extremely Small Silicon Thicknesses. *IEEE Transactions on Electron Devices*, 54(9):2204–2212, 2007.

[17] Nobuyuki Sugii, Ryuta Tsuchiya, Takashi Ishigaki, Yusuke Morita, Hiroyuki Yoshimoto, Kazuyoshi Torii, and Shin'ichiro Kimura. Comprehensive study on vth variability in silicon on Thin BOX (SOTB) CMOS with small random-dopant fluctuation: Finding a way to further reduce variation. In *2008 IEEE International Electron Devices Meeting*, pages 1–4, 2008.

[18] Babak Kazemi, Valeria Kilchytska, V. Barral, N. Planes, M. Haond, Denis Flandre, and Jean-Pierre Raskin. Assessment of 28nm utbb fd-soi technology platform for rf applications: Figures of merit and effect of parasitic elements. *Solid-State Electronics*, 117, 12 2015.

[19] J-P. Colinge. *Silicon-on-Insulator Technology: Materials to VLSI 3rd.* Springer Science & Business Media, 2004.

[20] Hyung-Kyu Lim and J. G. Fossum. Threshold voltage of thin-film Silicon-on-insulator (SOI) MOSFET's. *IEEE Transactions on Electron Devices*, 30(10):1244–1251, 1983.

[21] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa. Double-gate silicon-on-insulator transistor with volume inversion: A new device with greatly enhanced performance. *IEEE Electron Device Letters*, 8(9):410–412, 1987.

[22] Sheng S. Li (auth.) Sorin Cristoloveanu. *Electrical Characterization of Silicon-on-Insulator Materials and Devices.* The Springer International Series in Engineering and Computer Science 305. Springer US, 1 edition, 1995.

[23] A. Ohata, Sorin Cristoloveanu, Anne Vandooren, Mikaël Cassé, and F. Daugé. Coupling effect between the front and back interfaces in thin SOI MOSFETs. *Microelectronic Engineering - MICROELECTRON ENG*, 80:245–248, 06 2005.

[24] Vishal Trivedi, Jerry Fossum, and Weimin Zhang. Threshold voltage and bulk inversion effects in nonclassical CMOS devices with undoped ultra-thin bodies. *Solid-State Electronics*, 51:170–178, 01 2007.

[25] T. Rudenko, Valeria Kilchytska, Jean-Pierre Raskin, Alexei Nazarov, and Denis Flandre. *Special features of the back-gate effects in ultra-thin body SOI MOSFETs*, pages 323–339. 02 2011.

[26] Chan-Kwang Park, Chang-Yeol Lee, Kwyro Lee, Byung-Jong Moon, Young Hee Byun, and M. Shur. A unified current-voltage model for long-channel nMOSFETs. *IEEE Transactions on Electron Devices*, 38(2):399–406, 1991.

[27] Stéphane Burignat, Denis Flandre, Mohd Khairuddin Md A, Valeria Kilchytska, F. Andrieu, O. Faynot, and Jean-Pierre Raskin. Substrate impact on threshold voltage and subthreshold slope of sub-32nm ultra thin SOI MOSFETs with thin buried oxide and undoped channel. *Solid-State Electronics*, 54:213–219, 02 2010.

[28] Pragya Kushwaha, Navid Paydavosi, Sourabh Khandelwal, Chandan Yadav, Harshit Agarwal, et al. Modeling the impact of substrate depletion in FDSOI MOSFETs. *Solid-State Electronics*, 104, 11 2014.

[29] J. . Noel, O. Thomas, C. Fenouillet-Beranger, M. . Jaud, P. Scheiblin, and A. Amara. A simple and efficient concept for setting up multi-vt devices in thin box fully-depleted soi technology. In *2009 Proceedings of the European Solid State Device Research Conference*, pages 137–140, 2009.

[30] Sylvain Clerc, Thierry Gilio, and A. Cathelin. *The Fourth Terminal Benefits of Body-Biasing Techniques for FDSOI Circuits and Systems: Benefits of Body-Biasing Techniques for FDSOI Circuits and Systems*. 01 2020.

[31] T. Rudenko, V. Kilchytska, M. K. M. Arshad, J. Raskin, A. Nazarov, and D. Flandre. On the MOSFET Threshold Voltage Extraction by Transconductance and Transconductance-to-Current Ratio Change Methods: Part I—Effect of Gate-Voltage-Dependent Mobility. *IEEE Transactions on Electron Devices*, 58(12):4172–4179, 2011.

[32] D. Flandre, V. Kilchytska, and T. Rudenko. g_m/i_d method for threshold voltage extraction applicable in advanced mosfets with nonlinear behavior above threshold. *IEEE Electron Device Letters*, 31(9):930–932, 2010.

[33] Adelmo Ortiz-Conde, Francisco García-Sánchez, Juan Muci, Alberto Barrios, J.J. Liou, and Ching-Sung Ho. Revisiting MOSFET threshold voltage extraction methods. *Microelectronics and Reliability*, 53:90–104, 09 2013.

[34] T. Rudenko, V. Kilchytska, M. K. Md Arshad, J. Raskin, A. Nazarov, and D. Flandre. On the MOSFET Threshold Voltage Extraction by Transconductance and Transconductance-to-Current Ratio Change Methods: Part II—Effect of Drain Voltage. *IEEE Transactions on Electron Devices*, 58(12):4180–4188, 2011.

[35] D. K. Schroder. *Series Resistance, Channel Length and Width, and Threshold Voltage*, pages 185–250. 2006.

[36] Jean-Baptiste Henry. *Contribution à l'étude expérimentale des résistances d'accès dans les transistors de dimensions deca-nanométrique des technologies CMOS FD-SOI*. PhD thesis, 06 2018.

[37] B. K. Esfeh, V. Kilchytska, N. Planes, M. Haond, D. Flandre, and J. . Raskin. Comparative study of parasitic elements on RF FoM in 28 nm FD SOI and bulk technologies. In *2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, pages 1–3, 2015.

[38] Yannis Tsividis. *Operation and Modeling of the Mos Transistor*. Oxford University Press, Inc., USA, 2004.

[39] B. Kazemi Esfeh. *RF characterization of state-of-the-art SOI technologies*. PhD thesis, Université catholique de Louvain, June 2019.

[40] R. Torres-Torres, R. S. Murphy-Arteaga, and S. Decoutere. Mosfet bias dependent series resistance extraction from rf measurements. *Electronics Letters*, 39(20):1476–1478, 2003.

[41] A. Bracale, V. Ferlet-Cavrois, N. Fel, D. Pasquet, Julia Gautier, J. Pelloie, and J. Poncharra. A New Approach for SOI Devices Small-Signal Parameters Extraction. *Analog Integrated Circuits and Signal Processing*, 25:157–169, 11 2000.

[42] Julio Tinoco and Jean-Pierre Raskin. New rf extrinsic resistances extraction procedure for deep-submicron mos transistors. *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, 23:107 – 126, 01 2009.

[43] J. Barbé, L. Lucci, A. Siligaris, P. Vincent, and O. Faynot. 4-port rf performance assessment and compact modeling of utbb-fdsoi transistors. In *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 355–358, May 2015.

[44] S. Makovejev, Valeria Kilchytska, Mohd Khairuddin Md A, Denis Flandre, F. Andrieu, O. Faynot, S. Olsen, and Jean-Pierre Raskin. Self-heating and substrate effects in ultra-thin body ultra-thin box devices. pages 1 – 4, 04 2011.

[45] S. N. Ong, S. Lehmann, W. H. Chow, C. Zhang, C. Schippel, et al. A 22nm FDSOI Technology Optimized for RF/mmWave Applications. In *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pages 72–75, 2018.

Appendix A

Additional figures of Chapter 3

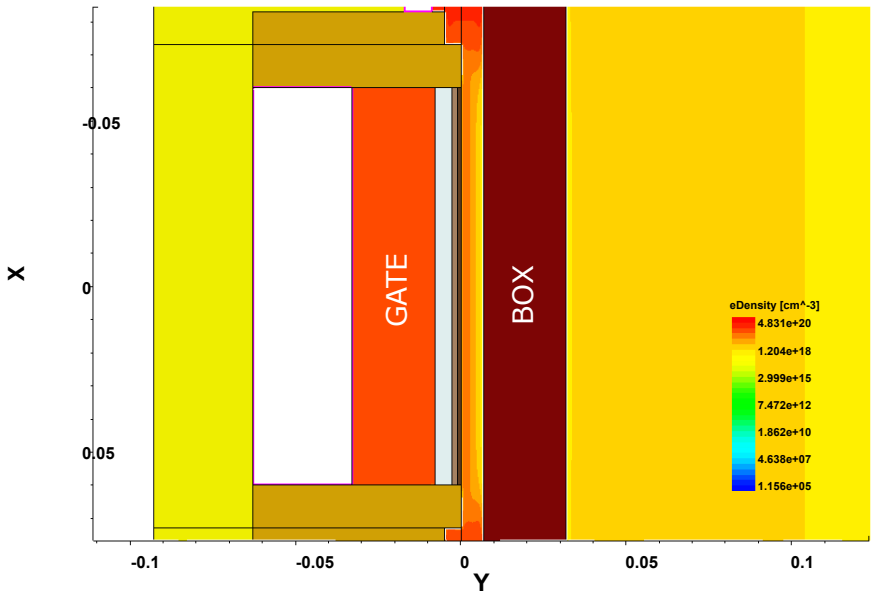


Figure A.1: Electron density distribution at $V_{DS} = 0\,\mathrm{V}$, $V_{GS} = 1\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$.

The following figures compare the results obtained from three different dies for each V_{TH} extraction methods. One can notice that the extracted V_{TH} of Die 3 at $V_B = 0\,\mathrm{V}$ is significantly different from the values obtained from the two other dies. It can be explained by the irregularities found in the drain current characteristics at $V_B = 0\,\mathrm{V}$ as illustrated in Figure A.6.

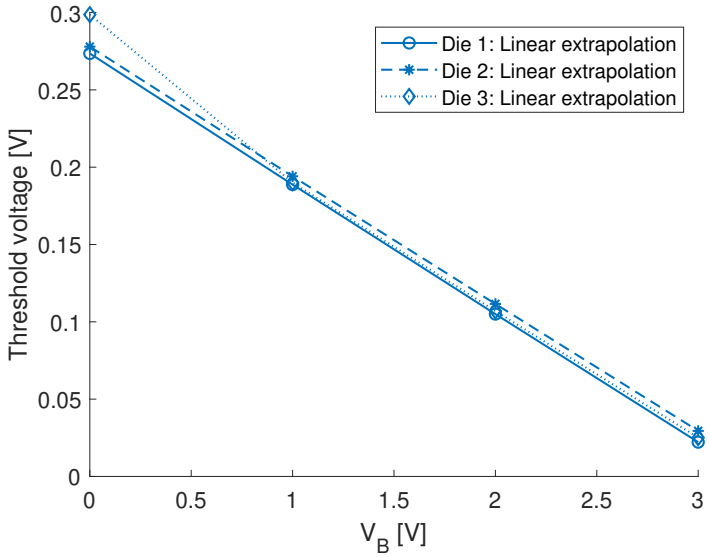


Figure A.2: Comparison of the results of the linear extrapolation method for three different dies.

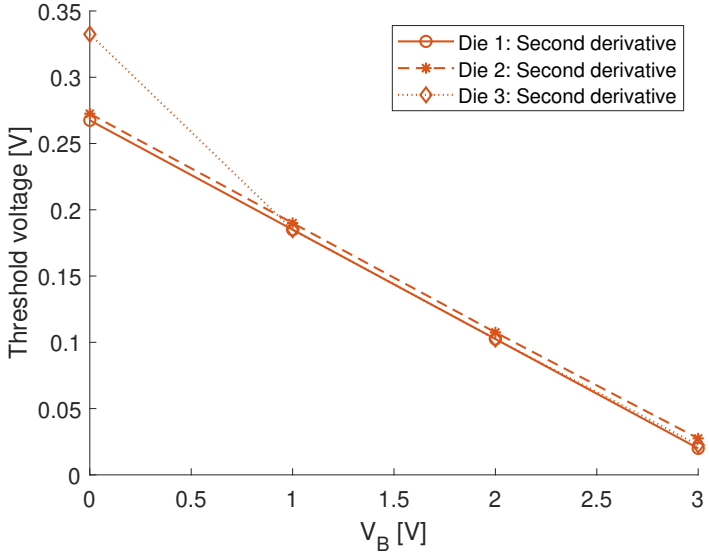


Figure A.3: Comparison of the results of the second derivative method for three different dies.

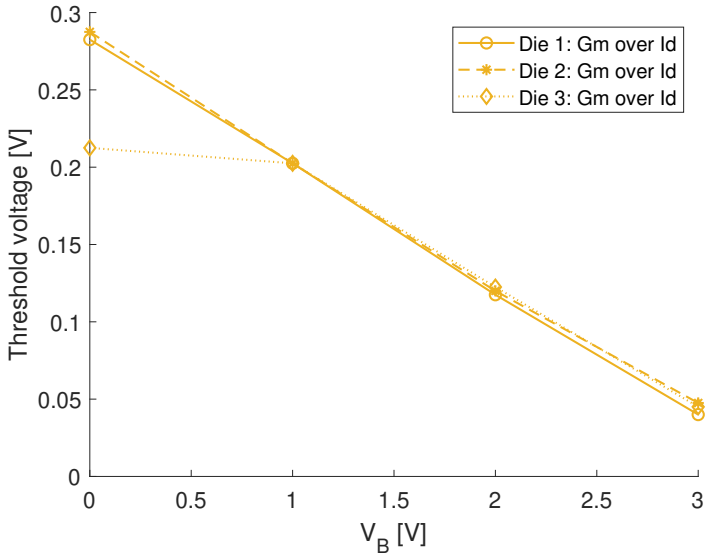


Figure A.4: Comparison of the results of the g_m/I_D ratio method for three different dies.

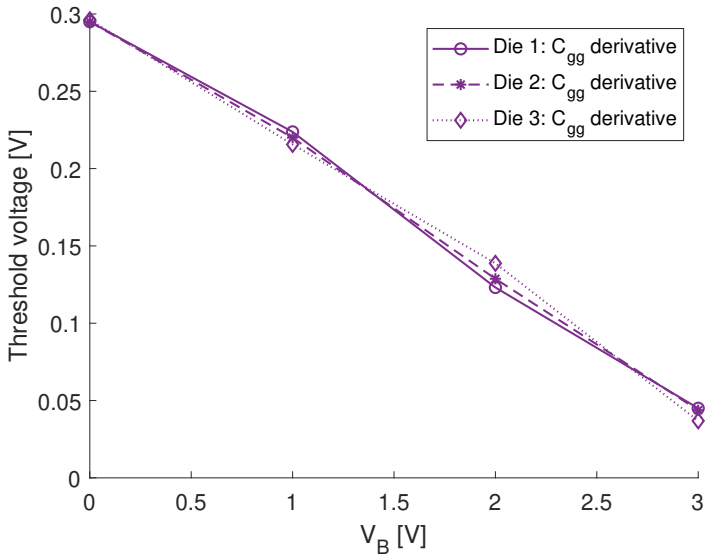


Figure A.5: Comparison of the results of the C_{gg} derivative method for three different dies.

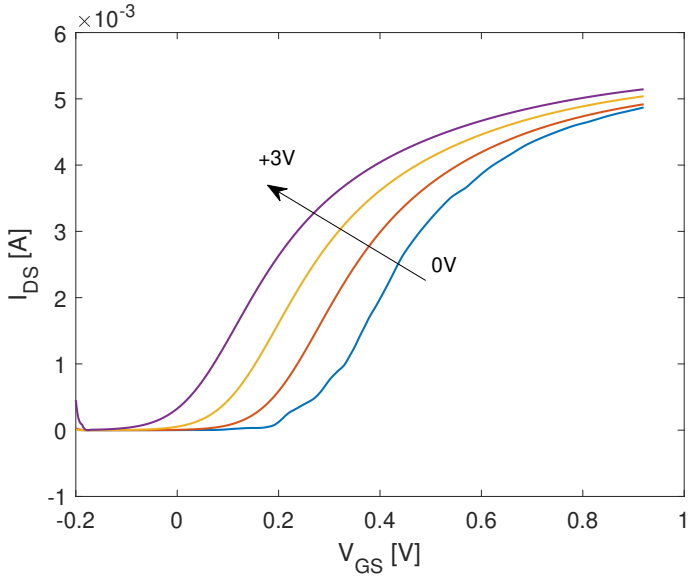


Figure A.6: $I_D - V_{GS}$ characteristics of Die 3 at $V_{DS} = 50\,\mathrm{mV}$ for various back-gate biases.

Appendix B

Analytical expressions of $\mathrm{Re}\{Z_{ij}\}$ for series resistances extraction

Based on the small-signal equivalent circuit of Figure 4.7, one can derive the Z-parameters (real part) of the device. First, in order to simplify the notation, some redundant terms are grouped together under global variables as follows:

$$G = (C_1 + C_2 + 2C_{ds}) \tag{B.1}$$

$$H = (2C_1C_2 + C_1C_{bg} + C_2C_{bg}) \tag{B.2}$$

$$\begin{aligned} E &= 2C_1C_2^2 + 2C_1^2C_2 + C_1^2C_{bg} + C_2^2C_{bg} + 2C_1C_2C_{bg} + 4C_1C_2C_{ds} + 2C_1C_{bg}C_{ds} + 2C_2C_{bg}C_{ds} \\ &= (C_1 + C_2 + 2C_{ds})(2C_1C_2 + C_1C_{bg} + C_2C_{bg}) \\ &= GH \end{aligned} \tag{B.3}$$

$$F = C_1^2 + 2C_1C_2 + C_1C_{bg} + C_2C_{bg} + 2C_1C_{ds} + C_{bg}C_{ds} \tag{B.4}$$

$$A = (E + FC_{sub} + 2HC_{sub}R_sg_{ds}) \tag{B.5}$$

$$\begin{aligned} B &= -(2H + 2C_1C_{sub} + C_{bg}C_{sub})g_{ds} + EC_{sub}R_s\omega^2 \\ &\approx -(2H + 2C_1C_{sub} + C_{bg}C_{sub})g_{ds} \end{aligned} \tag{B.6}$$

Where $C_{well-sub}$ has been replaced by C_{sub} for simplicity. Then, the real part of the Z-parameters can be written as

$$
\begin{aligned}
\mathrm{Re}\{Z_{11}\} &= R_g + \frac{(ER_s\omega^2 - (C_{bg}+C_{sub}+2C_2)g_{ds} + (C_1^2+C_2^2+2C_1C_2+2C_1C_{ds}+2C_2C_{ds})C_{sub}R_s\omega^2)A}{\omega^2A^2+B^2} \\
&- \frac{B(C_2^2+H+2C_2C_{ds}+C_1C_{sub}+C_2C_{sub}+C_{bg}C_{ds}+C_{ds}C_{sub}+(2H+2C_1C_{sub}+2C_2C_{sub})R_sg_{ds})}{\omega^2A^2+B^2} \\
&\approx R_g + \frac{4(C_1^2C_{sub}^2+2HC_1C_{sub}+H^2)R_sg_{ds}^2}{\omega^2A^2+B^2} + \frac{(C_1^2C_{sub}^2+2HC_1C_{sub}+H^2)}{\omega^2A^2+B^2}g_{ds} \\
&- \frac{(2C_1+C_{bg})C_{bg}C_{ds}C_{sub}+2HC_{bg}C_{ds}}{\omega^2A^2+B^2}g_{ds} \\
&\approx R_g + \frac{4(C_1^2C_{sub}^2+2HC_1C_{sub}+H^2)R_sg_{ds}^2}{B^2} + \frac{(C_1^2C_{sub}^2+2HC_1C_{sub}+H^2)}{B^2}g_{ds} \\
&\approx R_g + 4\alpha_1\beta R_s + \frac{\alpha_1}{(V_{GS}-V_{TH})}
\end{aligned} \tag{B.7}
$$

$$
\begin{aligned}
\mathrm{Re}\{Z_{12}\} &= \frac{R_s\omega^2G(H+C_1C_{sub})A}{\omega^2A^2+B^2} - \frac{(2R_sg_{ds}+1)(H+C_1C_{sub})B}{\omega^2A^2+B^2} \\
&\approx -\frac{(2R_sg_{ds}+1)(H+C_1C_{sub})B}{\omega^2A^2+B^2} \\
&\approx -\frac{(2R_sg_{ds}+1)(H+C_1C_{sub})}{B} \\
&\approx 2\alpha_2\beta R_s + \frac{\alpha_2}{(V_{GS}-V_{TH})}
\end{aligned} \tag{B.8}
$$

$$
\begin{aligned}
\mathrm{Re}\{Z_{22}\} &= R_d + \frac{R_s\omega^2(E+FC_{sub})A}{B^2+\omega^2A^2} - \frac{(R_sg_{ds}+1)(2H+2C_1C_{sub}+C_{bg}C_{sub})B}{B^2+\omega^2A^2} \\
&\approx R_d + R_s + \frac{1}{g_{ds}} \\
&\approx R_d + R_s + \frac{\alpha_3}{(V_{GS}-V_{TH})} = R_d + R_s + \frac{1}{\beta(V_{GS}-V_{TH})}
\end{aligned} \tag{B.9}
$$

$$
\begin{aligned}
\mathrm{Re}\{Z_{33}\} &= R_b + \frac{(ER_s\omega^2 - (C_{bg}+2C_1)g_{ds})A}{\omega^2A^2+B^2} - \frac{(C_1^2+H+2C_1C_{ds}+C_{bg}C_{ds}+2HR_sg_{ds})B}{\omega^2A^2+B^2} \\
&\approx R_b - \frac{(F+2HR_sg_{ds})B}{\omega^2A^2+B^2} - \frac{g_{ds}(2C_1+C_{bg})A}{\omega^2A^2+B^2} \\
&\approx R_b + \frac{4H^2R_sg_{ds}^2}{\omega^2A^2+B^2} + \frac{H^2g_{ds}}{\omega^2A^2+B^2} \\
&\approx R_b + \frac{4H^2R_sg_{ds}^2}{B^2} + \frac{H^2g_{ds}}{B^2} \\
&\approx R_b + 4\alpha_4\beta R_s + \frac{\alpha_4}{(V_{GS}-V_{TH})}
\end{aligned} \tag{B.10}
$$

$$\begin{aligned}\mathrm{Re}\{Z_{13}\} &= \frac{(ER_s\omega^2 - C_{bg}g_{ds})A}{\omega^2A^2 + B^2} - \frac{(C_1C_2 + C_1C_{bg} + C_2C_{bg} + C_{bg}C_{ds} + 2HR_sg_{ds})B}{\omega^2A^2 + B^2} \\ &\approx \frac{g_{ds}^2(2H + 2C_1C_{sub})2HR_s}{\omega^2A^2 + B^2} \\ &+ \frac{(C_1C_2 + C_1C_{bg} + C_2C_{bg} + C_{bg}C_{ds})(2H + 2C_1C_{sub} + C_{bg}C_{sub}) - C_{bg}(E + FC_{sub})}{\omega^2A^2 + B^2}g_{ds}\end{aligned} \tag{B.11}$$

$$\begin{aligned}\mathrm{Re}\{Z_{23}\} = \mathrm{Re}\{Z_{32}\} &= \frac{R_sw^2HGA}{\omega^2A^2 + B^2} - \frac{(2R_sg_{ds} + 1)HB}{\omega^2A^2 + B^2} \\ &\approx -\frac{(2R_sg_{ds} + 1)HB}{\omega^2A^2 + B^2}\end{aligned} \tag{B.12}$$

All the above equations have been obtained by neglecting the frequency-dependent terms. Finally, α_1, α_2, α_3 and α_4 are given by

$$\alpha_1 = \frac{(C_1^2C_{sub}^2 + 2HC_1C_{sub} + H^2)}{(2H + 2C_1C_{sub} + C_{bg}C_{sub})^2\beta} \tag{B.13}$$

$$\alpha_2 = \frac{(H + C_1C_{sub})}{(2H + 2C_1C_{sub} + C_{bg}C_{sub})\beta} \tag{B.14}$$

$$\alpha_3 = \frac{1}{\beta} \tag{B.15}$$

$$\alpha_4 = \frac{H^2}{(2H + 2C_1C_{sub} + C_{bg}C_{sub})^2\beta} \tag{B.16}$$

Where β is defined such that $g_{dsi} = \beta(V_{GS} - V_{TH})$.

As verification, one can set $C_{sub} = 0\,\mathrm{fF}$ and finds back the equations of the Bracale's method (see Section 4.3.1).

Appendix C

Current gain and Mason's unilateral gain for a 4-port device

In order to evaluate the back-gate related figures of merit, Barbé et al. [43] proposed to use the following set of hybrid parameters:

$$v_1 = H_{11}i_1 + H_{12}v_2 + H_{13}v_3 + H_{14}i_4 \tag{C.1}$$
$$i_2 = H_{21}i_1 + H_{22}v_2 + H_{23}v_3 + H_{24}i_4 \tag{C.2}$$
$$i_3 = H_{31}i_1 + H_{32}v_2 + H_{33}v_3 + H_{34}i_4 \tag{C.3}$$
$$v_4 = H_{41}i_1 + H_{42}v_2 + H_{43}v_3 + H_{44}i_4 \tag{C.4}$$

Where Port 1, 2, 3 and 4 are connected to the gate, drain, source and the back-gate, respectively. The currents and voltages can also be expressed in terms of Y-parameters as follows

$$i_1 = Y_{11}v_1 + Y_{12}v_2 + Y_{13}v_3 + Y_{14}v_4 \tag{C.5}$$
$$i_2 = Y_{21}v_1 + Y_{22}v_2 + Y_{23}v_3 + Y_{24}v_4 \tag{C.6}$$
$$i_3 = Y_{31}v_1 + Y_{32}v_2 + Y_{33}v_3 + Y_{34}v_4 \tag{C.7}$$
$$i_4 = Y_{41}v_1 + Y_{42}v_2 + Y_{43}v_3 + Y_{44}v_4 \tag{C.8}$$

To keep coherence with the 2-port definitions, the front-gate figures of merit f_T and f_{max} can still be determined using H_{21} and U. By applying an appropriate matrix transformation, one can find H_{21} in terms of Y-parameters.

$$\begin{aligned} H_{21} &= \frac{i_2}{i_1}|_{v_2=v_3=0,i_4=0} \\ &= \frac{Y_{21}v_1 + Y_{24}v_4}{Y_{11}v_1 + Y_{14}v_4} \\ &= \frac{Y_{21}Y_{44} - Y_{24}Y_{41}}{Y_{11}Y_{44} - Y_{14}Y_{41}} \end{aligned} \tag{C.9}$$

Where the Y-parameters under $v_2 = v_3 = 0, i_4 = 0$ are given by

$$i_1 = Y_{11}v_1 + Y_{14}v_4 \tag{C.10}$$
$$i_2 = Y_{21}v_1 + Y_{24}v_4 \tag{C.11}$$
$$i_3 = Y_{31}v_1 + Y_{34}v_4 \tag{C.12}$$
$$0 = Y_{41}v_1 + Y_{44}v_4 \tag{C.13}$$

The unilateral power gain U is defined in the same way as for the 2-port device:

$$U = \frac{1}{4}\frac{|Y_{21} - Y_{12}|^2}{\mathrm{Re}\{Y_{11}\}\,\mathrm{Re}\{Y_{22}\} - \mathrm{Re}\{Y_{21}\}\,\mathrm{Re}\{Y_{12}\}} \tag{C.14}$$

Using similar expressions, the back-gate related figures of merit f_{Tbg} and f_{maxbg} can respectively be extracted from H_{24} and U_{bg} defined as

$$H_{24} = \frac{Y_{24}Y_{11} - Y_{21}Y_{14}}{Y_{11}Y_{44} - Y_{14}Y_{41}} \tag{C.15}$$

$$U_{bg} = \frac{1}{4}\frac{|Y_{24} - Y_{42}|^2}{\mathrm{Re}\{Y_{44}\}\,\mathrm{Re}\{Y_{22}\} - \mathrm{Re}\{Y_{24}\}\,\mathrm{Re}\{Y_{42}\}} \tag{C.16}$$

Appendix D

Extraction of RF FoMs

The following figures present another common way to extract f_T and f_{max} when the curve becomes flat, which corresponds to a $-20\,\mathrm{dB/dec}$ slope.

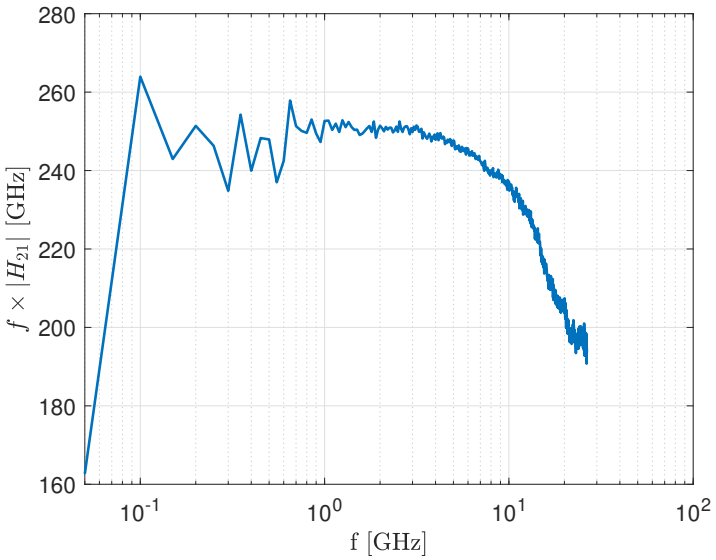


Figure D.1: $f \times |H_{21}|$ versus frequency in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$. Flat curve corresponds to a $-20\,\mathrm{dB/dec}$ slope.

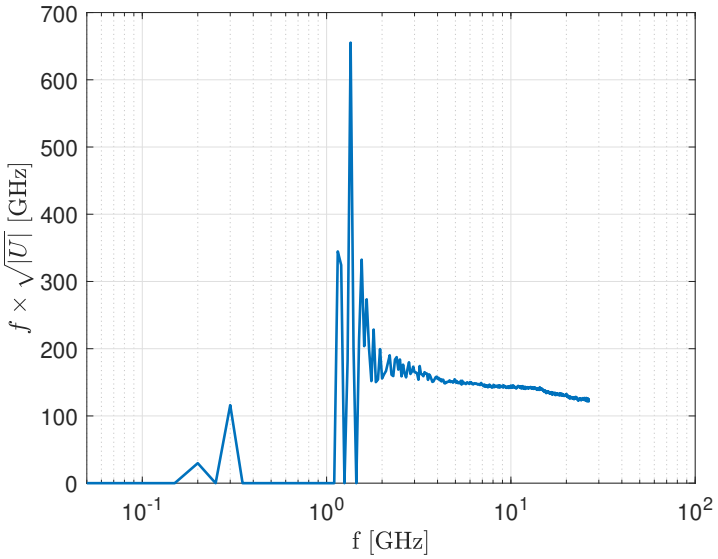


Figure D.2: $f \times \sqrt{|U|}$ versus frequency in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$. Flat curve corresponds to a $-20\,\mathrm{dB/dec}$ slope.

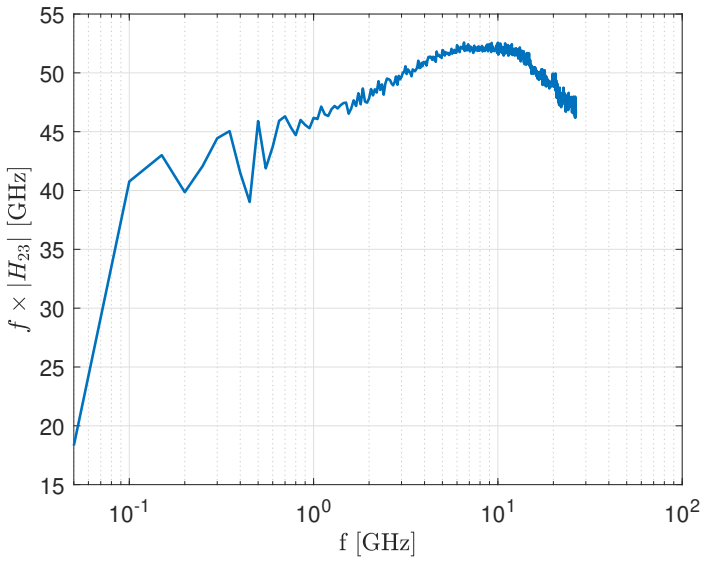


Figure D.3: $f \times |H_{23}|$ versus frequency in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$. Flat curve corresponds to a $-20\,\mathrm{dB/dec}$ slope.

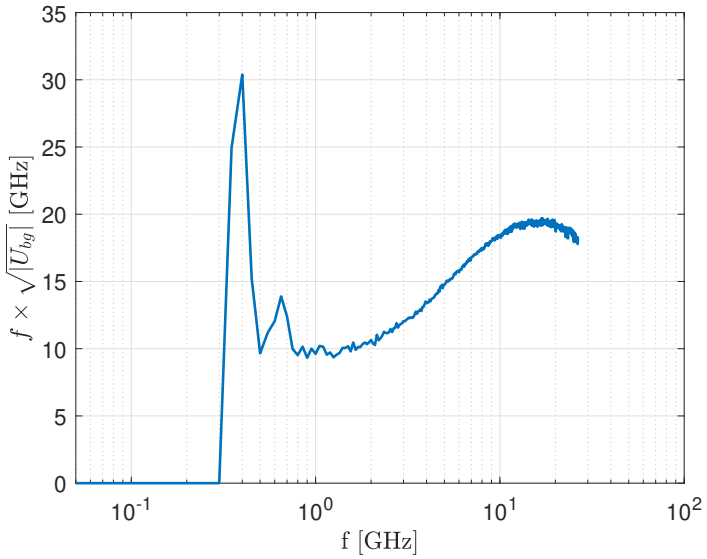


Figure D.4: $f \times \sqrt{|U_{bg}|}$ versus frequency in saturation at $V_{DS} = 0.8\,\mathrm{V}$, $V_{GS} = 0.8\,\mathrm{V}$ and $V_B = 0\,\mathrm{V}$. Flat curve corresponds to a $-20\,\mathrm{dB/dec}$ slope.

UNIVERSITÉ CATHOLIQUE DE LOUVAIN
École polytechnique de Louvain
Rue Archimède, 1 bte L6.11.01, 1348 Louvain-la-Neuve, Belgique | **www.uclouvain.be/epl**