

École polytechnique de Louvain

Impact of HVDC interconnectors on the transient stability performance of power systems

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Academic year 2021–2022

Master [120] in Electrical Engineering

Master [120] in Electro-mechanical Engineering

Abstract

In 2019, the first High-Voltage Direct Current (HVDC) link in Belgium was inaugurated : *Nemolink*. It connects the United Kingdom with the Belgian grid and can transport up to 1000MW of power. A year later, a second HVDC connection named *ALEGrO* was created with Germany, allowing to exchange up to 1000MW as well. Nowadays, a third HVDC connection is being studied to interlink Belgium and Denmark [1, 2, 3]. Belgium is not an exception : multiple interconnections in HVDC are being developed all over the world. These direct current connections meet the growing need to interconnect the networks of different countries. Indeed, an interconnected network contributes to the sustainability and security of supply. In addition, the growing share of renewable energies contributes to the volatility of the electrical production, and interconnections between electrical networks allow to gain flexibility. During high peak of production, if the consumption is not sufficient to balance the network, the excess of electricity can be sent elsewhere. The same applies when electricity production is not sufficient to support the consumption. This flexibility in the transmission is therefore an important aspect of the production of renewable energies. These HVDC interconnections can play an important role in the future and their presence is growing. This work aims to study their impact on the transient stability of the power system. In conclusion, it has been established that reactive power support is feasible with the MMC and plays an important role during the three-phase fault to support the synchronous generator and to improve its transient stability.

Remerciements

Nous souhaitons par ces quelques lignes, et en français, remercier le Professeur DE JAEGER de nous avoir donné la possibilité de travailler sur ce sujet. Nous sommes reconnaissants de ses précieux conseils durant cette année ainsi que du temps qu'il nous a consacré. Sa porte a toujours été ouverte pour toutes questions.

Nous tenions aussi à remercier Quentin DELHAYE de nous avoir soutenus, et parfois réconfortés, tout au long de cette année. Ses conseils ainsi que ses remarques lors de la relecture de notre travail nous ont été d'une grande aide pour sa finalisation. Nous voulions aussi le remercier pour tout le temps qu'il nous a consacré afin de dénicher nos erreurs dans *Simulink*.

Nous remercions aussi Professeur BEKEMANS d'avoir accepté de relire notre travail ainsi que de se joindre à Professeur DE JAEGER et Quentin DELHAYE afin de constituer notre jury final.

Duc Huy

Par ces quelques lignes, je tenais aussi à remercier tous les membres de mon entourage pour leur soutien constant durant ces derniers mois ainsi que leur encouragements tout au long de mes études. Tout cela n'aurait pas été possible sans leur présence...

Gil

À Roxane, pour nos voyages clandestins
À Martine, pour notre escapade volcanique
À mon frère, pour ses tendres conseils
À mes parents
et aux étoiles

Introduction

The objective of this work was to analyse the transient stability and the interaction between the electrical power system and the HVDC interconnectors. This work was divided into two distinct parts. The first part addresses the state of the art of HVDC interconnectors based on the Modular Multilevel Converter (MMC) technology. The focus has been principally made on the structure, the modelling and the control of this kind of converters. Afterwards, the second part consists of the implementation of an HVDC link based on an averaged model. A validation section has been firstly elaborated followed by simulations of different transient situations.

The structure of this work is the following :

Chapter 1 presents the advantages and disadvantages of the DC transmission systems with respect to AC transmission systems. The different existing technologies are briefly discussed and compared.

Chapter 2 develops and explains the working principle of Modular Multilevel Converters with a special attention to how the different type of sub-modules used to compose the converter are working.

Chapter 3 discusses the different developed models in order to represent and simulate the behaviour of the MMC. Four different models have been developed in this chapter.

Chapter 4 addresses the different levels of control of the converter. Particular attention is paid to the higher level controls with the inner and outer controllers.

Chapter 5 justifies the value of the elements used in the developed model. The chapter also demonstrates the correctness of the model throughout theoretical calculations around an equilibrium point followed by a discussion.

Chapter 6 gathers the results of the simulation of different transient situations such as power reversal, three-phase fault with or without synchronous generator.

Finally, chapter 7 concludes the work by suggesting some improvements to the model and other possible simulations that could be performed.

List of Figures

1.1	Comparison of the losses of HVAC and HVDC in function of the distance [12]	3
1.2	Comparison of the cost of HVAC and HVDC in function of the distance [12]	4
1.3	Line commutated converters (LCC) : Rectifier [12]	5
1.4	Voltage Source Converters (VSC) : Inverter [12]	6
1.5	Classification of voltage source converter [7]	7
1.6	Three-level neutral-point clamped converter [7]	8
1.7	Active neutral-point clamped converter [7]	9
1.8	Four-level flying capacitor converter [7]	10
1.9	Four-level nested neutral-point clamped converter [7]	11
1.10	Cascaded H-Bridge converter [7]	12
1.11	Cascaded neutral-point clamped converter [7]	13
2.1	Half-Bridge [7]	17
2.2	Full-Bridge [7]	18
2.3	Flying Capacitor [7]	19
2.4	Cascaded Half-Bridge [7]	20
2.5	Double Clamp [7]	21
2.6	Modular Multilevel Converter - Single phase [26]	23
2.7	AC output voltage of a MMC of 10 levels [26]	23
2.8	Modular Multilevel Converter - Topology [7]	24
3.1	Different modellings and their decreasing complexity [28]	28
3.2	a) Modelling of an IGBT switch b) Non-linear resistance V-I characteristic [27]	29
3.3	Half-Bridge equivalent model with a Type II simplification [27] . . .	30
3.4	Thevenin equivalent circuit for a sub-module [29]	30
3.5	Model III equivalent circuit of an arm. a) ON/OFF states b) Blocked state [28]	32
3.6	A detailed MMC representation [31]	33

3.7	AVM : AC-side [31]	35
3.8	AVM : DC-side [33]	37
4.1	Control hierarchy of a MMC station [27]	38
4.2	(a) Stationary $\alpha\beta$ reference frame [33]	40
4.3	(b) Rotating $dq0$ reference frame [33]	40
4.4	Block diagram of the Phase-locked loop [33]	41
4.5	Upper-level control overview including the Outer and the Inner controls [12]	42
4.6	Upper-level : PI controller of active power P and reactive power Q [33]	43
4.7	Upper-level : PI controller of DC voltage [33]	44
4.8	Upper-level : PI controllers of AC voltage [33]	45
4.9	Equivalent circuit of the converter [29]	45
4.10	Inner Controller [29]	47
4.11	Lower-level : CCSC [29]	48
4.12	Phase-Disposition Modulation representation [29]	49
4.13	Phase-Shift Modulation representation [29]	50
4.14	Continuous reference, discrete reference using the NLC approach, and the voltage output [42]	51
4.15	NLC modulation representation [33]	51
4.16	NLC performance normalised by $V_{arm}/2$ [7]	52
4.17	a) : Insertion of a cell ; b) bypassing of a cell [29]	53
4.18	Global view of the algorithm of BCA [33]	54
5.1	MMC-HVDC transmission system with the control associated to each MMC station	57
5.2	MMC-HVDC transmission system [27]	57
5.3	THD of U_{abc} at the PCC	60
5.4	MMC-HVDC transmission system in MATLAB & SIMULINK/SIMSCAPE	60
5.5	MMC : AVM of the Rectifier (Station 1)	61
5.6	Active power in the DC link	64
5.7	Reactive power at station 1	64
6.1	Schematic of the weakening of the network 1	66
6.2	Short-Circuit Power	67
6.3	Transmitted Power	67
6.4	Frequency Variation	67
6.5	Voltage Variation	67
6.6	Root Locus with $K_{p,PLL}$ varying from 0 to 200 with two different SCR [51]	68

6.7	Minimal S_{CC} needed in function of the HVDC active power transmitted [54]	69
6.8	Schematic of system simulated	70
6.9	Active power in the DC link	70
6.10	DC Current in the DC link	70
6.11	DC Voltage in the DC link	71
6.12	AC voltage at PCC of station 1 during power reversal (RMS)	71
6.13	AC voltage at PCC of station 2 during power reversal (RMS)	71
6.14	AC current at PCC of station 1 during power reversal	72
6.15	AC current at PCC of station 1 during power reversal (RMS)	72
6.16	AC current at PCC of station 2 during power reversal	72
6.17	AC current at PCC of station 2 during power reversal (RMS)	72
6.18	DC Voltage in the DC link for a 2 [s] power reversal	73
6.19	Configuration of the three-phase fault	74
6.20	Fault-ride-through profile of an HVDC converter station [56]	75
6.21	Active power reference signal, reduced during the fault	76
6.22	Reactive power reference signal, increased during the fault	76
6.23	AC voltage at PCC during the three-phase fault when $P = 0.75$ [pu] and $Q = 0.33$ [pu]	77
6.24	AC voltage at PCC during the three-phase fault when $P = 0.75$ [pu] and $Q = 0.14$ [pu]	77
6.25	AC current at rectifier PCC during the three-phase fault with $P = 0.19$ [pu]	77
6.26	Reactive power at station 1 with the reference value	78
6.27	Reactive power at station 1 - Zoom on the fault time	78
6.28	DC power transmitted from station 1 to the station 2 with $P = 0.19$ [pu]	78
6.29	DC current at DC link during the three-phase fault with $P = 0.19$ [pu]	78
6.30	Arm current in phase A, with $P=0.18$ [pu]	79
6.31	Arm current in phase A, with $P=0.75$ [pu]	79
6.32	Three-phase voltage at the PCC of station 1	80
6.33	Q component of the voltage at the PCC of station 1	80
6.34	AC voltage at station 1 PCC during the severe three-phase fault . .	81
6.35	AC current at station 1 PCC during the severe three-phase fault . .	81
6.36	Active power at station 2	82
6.37	AC arm current in phase A during the severe three-phase fault . . .	82
6.38	Schematic with the synchronous machine	83
6.39	Reference set points of the simulation	84
6.40	Active Power at the MMC 1	84
6.41	Active power from the synchronous machine and the grid AC sources .	85

6.42	Reactive power from the synchronous machine and the grid AC sources	85
6.43	Mechanical Power and Active Power set point	86
6.44	Reactive Power set point	86
6.45	Active power output of the machine with different reactive powers from the MMC	87
6.46	RMS AC voltage at the PCC of station 1	87
6.47	Reactive power consumed by the machine	87
6.48	RMS AC current of the machine with different reactive powers from the MMC	87
6.49	Load angle of the machine with different reactive powers from the MMC	88
6.50	Rotor Speed of the machine with different reactive powers from the MMC	88
6.51	Electromagnetic Torque of the machine with different reactive powers from the MMC	88
6.52	Reference set points for Q, P and P_{mech}	89
6.53	Active power output of the machine with varying distance and constant Q from the MMC	90
6.54	DC active power transmitted in the DC link	90
6.55	RMS AC currents of the machine with varying distance and constant Q from the MMC	90
6.56	RMS AC voltage at the PCC of station 1	90
6.57	Load angle of the machine with varying distance and constant Q from the MMC	91
6.58	Rotor Speed of the machine with varying distance and constant Q from the MMC	91
6.59	Electromagnetic Torque of the machine with varying distance and constant Q from the MMC	91
6.60	Schematic with the synchronous machine and the three-phase fault	92
6.61	AC voltage at station 1 PCC during the fault	93
6.62	Active power output of the synchronous machine	94
6.63	Reactive power output of the synchronous machine	94
6.64	Load angle with 2 different reactive powers from MMC	94
6.65	Rotor speed with 2 different reactive powers from MMC	94
6.66	DC power transmitted from station 1 to the station 2	95
6.67	DC current at DC link during the three-phase fault	95
6.68	Arm current in phase A, with $P=0.94[\text{pu}]$ and $Q=0.33[\text{pu}]$	95
6.69	Active power measured at station 2	98
6.70	Reactive power measured at the PCC	98
6.71	Active power of the synchronous generator	98

6.72	Currents of the synchronous machine during the fault	98
6.73	RMS Voltage at the PCC of station 1	99
6.74	Arm current with P control to 0.18[pu] during fault	99
6.75	Load angle during the fault $U_{ret} = 0.2$ [pu]	99
6.76	Rotor speed during the fault $U_{ret} = 0.2$ [pu]	100
6.77	Electromagnetic Torque during the fault $U_{ret} = 0.2$ [pu]	100
A.1	Control blocks of Station 1	104
A.2	Active power control block diagram	105
A.3	Reactive power control block diagram	105
A.4	DC voltage control block diagram	105
A.5	Inner control block diagram	106
A.6	Gate signal generation for controlled voltage sources	106
A.7	Signal generation for controlled current sources	107
A.8	Synchronous machine block diagram	107

List of Abbreviations

AVM Average Modelling Model. [27](#)

CCSC Circulating Current Suppression Controller. [xiii](#), [47](#)

CSC Current Source Converter. [4](#)

FET Field-Effect Transistor. [5](#)

HVAC High Voltage Alternating Current. [xii](#), [1–3](#)

HVDC High-Voltage Direct Current. [i](#)

IGBT Insulated Gate Bipolar Transistor. [5](#)

IGCT Integrated Gate-Commutated Thyristor. [5](#)

LCC Line-Commutated Converter. [4](#)

MMC Modular Multilevel Converter. [4](#)

MTDC Multi-Terminal Direct Current. [102](#)

NLC Nearest-Level Control. [50](#)

NPC Neutral-Point Clamped. [7](#)

PCC Point of Common Coupling. [40](#)

PI Proportional-Integral. [43](#)

PLL Phase Locked Loop. [39](#)

PWM Pulse-Width Modulation. [49](#)

SCC Short Circuit Capacity. [65](#)

SCR Short Circuit Ratio. [67](#)

SM Sub-Module. [xiii](#), [58](#)

SVC Static Var Compensator. [96](#)

THD Total Harmonics Distorsion. [vi](#), [59](#), [60](#)

VCO Voltage Controlled Oscillator. [40](#)

VSC Voltage Source Converter. [4](#), [5](#)

Contents

Abstract	i
Acknowledgements	i
Introduction	ii
List of figures	iv
List of abbreviations	x
 I State of the art	 xv
1 Introduction	1
1.1 Context	1
1.2 Advantages of the HVDC transmission compared to HVAC	1
1.3 Current technologies of HVDC lines	4
1.3.1 Line-Commutated Converters - LCC	4
1.3.2 Voltage Source Converter - VSC	5
 2 Modular Multilevel Converter	 15
2.1 General overview	15
2.2 Operational principle of the sub-module	16
2.2.1 Half-Bridge	16
2.2.2 Full-Bridge	17
2.2.3 Flying Capacitor :	19
2.2.4 Cascaded Half-bridge	20
2.2.5 Double Clamp	20
2.3 Operational principle of the MMC	22
2.3.1 Single-Phase MMC :	22
2.3.2 Three-phase MMC :	24
2.4 Technical constrains :	25

3	Modelling of the Modular Multilevel Converter	27
3.1	Modelling of Modular Multilevel Converters	27
3.1.1	Full Physics Based Models	28
3.1.2	Model I : Full Detailed-Models	29
3.1.3	Model II : Equivalent Circuit-Based Model	29
3.1.4	Model III : MMC Arm Switching Function	31
3.1.5	Model IV : Average Modelling Model	32
4	Control of the Modular Multilevel Converter	38
4.1	Park transformation and Phase Locked Loop	39
4.1.1	Synchronous Park reference frame	39
4.1.2	PLL-Phase Locked Loop	40
4.2	Upper-level Controls - VSC Controls	41
4.2.1	General overview of the Upper-level Control	41
4.2.2	Outer Controllers	42
4.2.3	Inner Controllers	45
4.3	Lower-level Controls - MMC Controls	47
4.3.1	CCSC - Circulating Current Suppression Controller	47
4.3.2	Modulation	48
4.3.3	BCA - Balancing Control Algorithm	52
II	Implementation of the model	55
5	HVDC transmission system: modelling and validation	56
5.1	Choice of the model type and control of the MMC	56
5.2	Choice of the parameters of the model	57
5.2.1	Arm Inductance	58
5.2.2	SM capacitor	58
5.2.3	DC link	59
5.2.4	AC Filters	59
5.3	Implementation	60
5.4	Validation	61
5.4.1	Equations in steady state	61
5.4.2	Comparison	62
5.4.3	Graphical Validation	64
5.4.4	Discussion	64
6	Simulations	65
6.1	Stability of HVDC system for a weak grid	65
6.1.1	Results	66

6.1.2	Discussion	67
6.2	Transient stability : Power Reversal	69
6.2.1	Results	70
6.2.2	Discussion	72
6.3	Transient stability : Three-phase fault	73
6.3.1	Requirements : fault-ride-through capability of an HVDC station	74
6.3.2	Control strategy during the three-phase fault	75
6.3.3	Results for $U_{ret} \geq 0.2$ [pu]	76
6.3.4	Discussion for $U_{ret} \geq 0.2$ [pu]	79
6.3.5	Results for more severe fault ($U_{ret} < 0.2$ [pu])	81
6.3.6	Discussion when $U_{ret} \approx 0$	82
6.4	Connection of a synchronous generator : Interaction with the electrical grid	82
6.4.1	Synchronous generator parameters	83
6.4.2	Results	84
6.4.3	Discussion	85
6.5	Variation of the injected reactive power from the MMC	86
6.5.1	Results	86
6.5.2	Discussion	88
6.6	Synchronous generator distance variation from the MMC	89
6.6.1	Results	89
6.6.2	Discussion	91
6.7	Three-Phase Fault with a synchronous generator	92
6.7.1	Three-phase fault with a synchronous generator and $U_{ret} \approx 0.5$	92
6.7.2	Three-phase fault with a synchronous generator and $U_{ret} \approx 0.2$	97
7	Conclusion	101
7.1	Future perspectives	101
III	Appendix	103
A	Simulink Bloc Diagram	104

Part I

State of the art

Chapter 1

Introduction

1.1 Context

The direct and alternating currents clashed at the end of the 19th century, in what is known as the *War of the currents*. Thomas Edison's company pushed for direct current transmission while George Westinghouse's company promoted alternating current. In the end, alternating current distribution was chosen for the American grid. However, in the middle of the 20th century, a new use of direct current was implemented to connect an isolated island with the mainland in Sweden at very high voltage. In 1954, the first commercially used High-Voltage Direct Current link was created [4], connecting Gotland to Stockholm. The successful implementation was followed by numerous projects using the high voltage DC transmission. The following sections will explain the advantages the HVDC transmissions has over the HVAC ones and the different technologies used to convert alternating and direct currents.

1.2 Advantages of the HVDC transmission compared to HVAC

Using HVDC over HVAC transmissions brings several advantages. These advantages are explained in this section.

- **Connection between asynchronous power systems**

HVDC lines must be used to connect two asynchronous systems together [5]. As an example, the Japanese grid is separated in 2 regions : one operating at 50[Hz] while the other is operating at 60[Hz]. In order to strengthen the connection between these two asynchronous networks, Japan is planning to

use HVDC line. The Higashi-Shimizu link is scheduled to be usable in 2028 and will exchange 600[MW] between two asynchronous networks [6].

- **Integration of renewable energy sources**

The current grid infrastructure is based on large power plants that are placed near cities or industrial centres. These power plants generate the electricity demanded by the customer [7]. Nowadays, a rise in the production of electricity with renewable energy sources can be seen. Production with sources such as wind or solar energies are constantly increasing in the last years [8]. However, the renewable power plants can be placed remotely of these cities, or even offshore in the case of wind farm. A big challenge is the transportation of such an energy produced by the remote renewable energy sources. The HVDC connections could be a precious help in this matter, in particular with offshore energy. Indeed, DC transmission presents the advantage of lower losses and reduced cost in long transmission, especially in underground or undersea cables, compared to AC transmission.

- **Losses over distance**

Another advantage of the HVDC over the HVAC transport is the reduced losses after a certain line length, called the break-even distance. The main contribution in losses for HVAC are due to the cable in the line, while for the HVDC it is mainly due to the converter losses [9]. For the same power transported, the losses in the line of the HVDC are indeed lower than for a HVAC line [10]. AC transmission suffers of **skin effect**. This effect is due to opposing Eddy currents that is induced by the changing magnetic field of the alternating current [11]. The current will thus mainly flow near the outer surface of the conductor. This will lead to a reduction in the density of the current, and an increase in the resistance of the conductor and the losses. A representation of the losses of HVAC and HVDC can be seen in FIGURE 1.1.

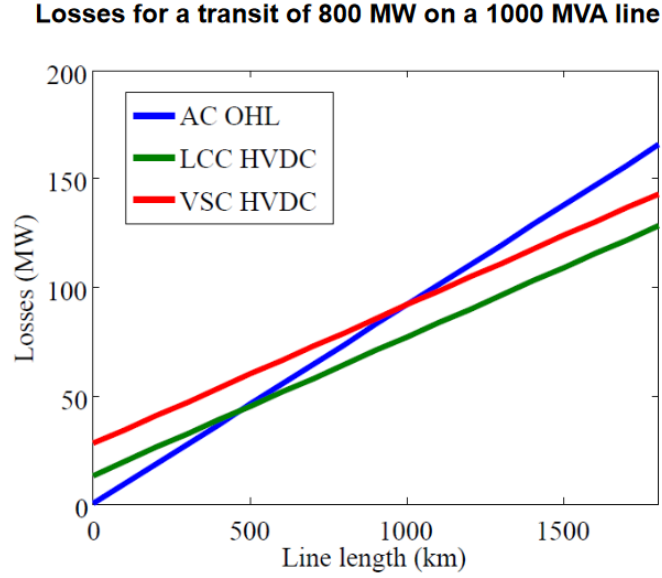


FIGURE 1.1: Comparison of the losses of HVAC and HVDC in function of the distance [12]

- **Submarine or underground power transmission**

AC underground cables suffer of capacitive effects with the ground or the sea, known as **Corona effect**, which leads to large losses in the electricity transport. The active power transmitted can be entirely converted in reactive power after a certain distance. To compensate these capacitive effects, shunt compensations must be connected regularly in the underground line, which will increase the cost of the line [13].

A great advantage of HVDC is therefore the possibility to perform underground or submarine transport of power. Because of the continuous current, there is no interaction with the parasitic capacitance, which increases the maximal distance of transport, especially for submarines lines. When power systems are separated by more than 40[km] in deep water, it is necessary to use HVDC [14]. For that reason, long submarine or undersea transmissions are done in DC to connect remote islands, offshore wind parks or neighbouring countries.

- **Cost over distance**

In the economical point of view, the HVDC transmissions cost less than HVAC transmissions after a break-even distance. The initial cost in HVDC is caused by the terminal stations on both side of the line, where the converters execute the AC/DC or DC/AC conversion [10]. The system using two lines for the DC instead of the three lines of the AC contributes to a diminution

of the cost in the towers. Another factor of the lower cost is the reduced cost in maintenance for the HVDC systems [5]. A representation of the cost over the line length can be seen in FIGURE 1.2.

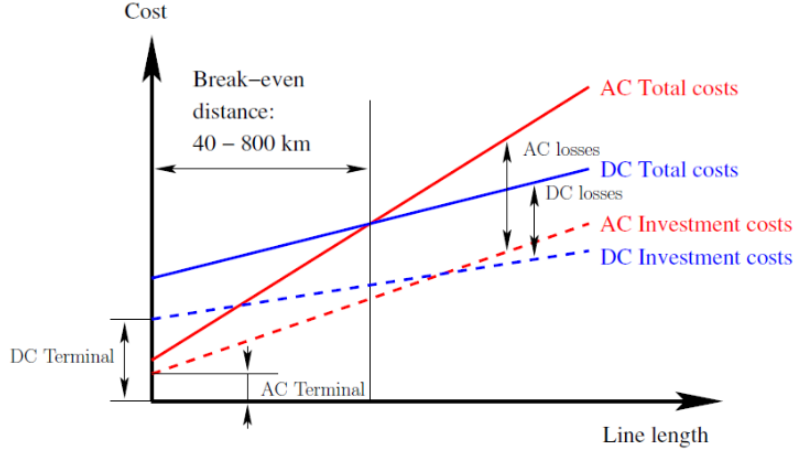


FIGURE 1.2: Comparison of the cost of HVAC and HVDC in function of the distance [12]

1.3 Current technologies of HVDC lines

The use of HVDC implies a conversion from alternating currents to direct currents and conversely using power electronics devices. Rectifiers are used to convert from AC to DC at the transmitting end, while inverters are used to convert the current back to AC at the receiving end of the line [15]. Two types of converters are used to perform these conversions : the Line-Commutated Converter (LCC) and the Voltage Source Converter (VSC). Later, a new type of VSC emerged, known as Modular Multilevel Converter (MMC). The MMC is particularly adapted to very high voltage conversion and will be thoroughly studied in this work [16].

1.3.1 Line-Commutated Converters - LCC

Line-Commutated Converters, also called Current Source Converter (CSC), work like current sources. These converters produce a constant DC current that will always flows in the same direction. To change the power flow, one needs to reverse the DC voltage polarity [17]. This kind of converters are made with thyristors [18], but were first made with thyratrons or mercury valves [7]. These thyristors are used to build two 6-pulse bridges. They are commutating naturally and must therefore be connected to a grid with a high short circuit power in order to avoid

commutation faults [19].

Historically, the LCCs were the first converters used to build HVDC connection. Nowadays, this technology is still used because of its cheapness and low losses (0.7% per converter, compared to 1.7% per converter for the VSC [20]). A major drawback is the needed connection to a strong grid to be able to reverse the voltage and avoid any commutation faults. The absorption of reactive power from the grid that can not be controlled is an another downside [20]. It can not be controlled because the control is done with the firing angle at the gate signal of the rectifier and the inverter. This parameter is linked to the magnitude of the direct current and the power factor. Therefore, one station will handle the control of the direct current while the other will handle the control of the angles. This reactive power can only be consumed because a minimum value of the firing angle is needed to make the converter works, and this leads to a non-unity power factor and a constant reactive power consumption [12, 15].

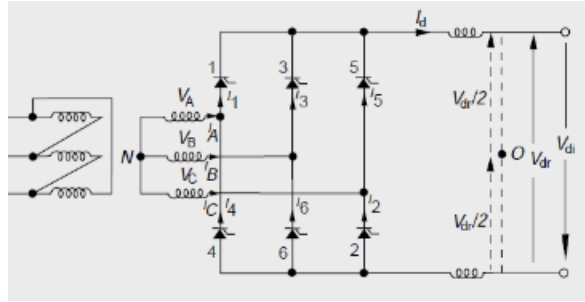


FIGURE 1.3: Line commutated converters (LCC) : Rectifier [12]

1.3.2 Voltage Source Converter - VSC

The apparition and spread use of semi-conductors that can be turned off with gate signals, such as IGCT, IGBT or FET, have made possible the forced current commutations, in contrast with the natural commutations of the LCC [18]. The Voltage Source Converters act like a voltage source and produce a constant DC voltage in the DC line. Therefore, the power reversal is done by changing the DC current direction [20].

VSC and LCC have similar topologies. The thyristors in the 6-pulse bridges of the LCC are replaced by transistors such as IGBT [15]. The reverse voltage blocking diode can be replaced by a thyristor as well. Its purpose is to protect the DC voltage to reverse its polarity. One VSC is depicted in FIGURE 1.4 where an inverter station is represented.

The main characteristics of VSC can be listed :

- The control of reactive power and active power can be done independently

from each other [20, 7]. Both the rectifier and the inverter will control their reactive power exchanged with the grid, while one station will be in charge of the control of the active power and the other will manage the DC voltage.

- A connection to a weaker grid is allowed because of the control of reactive power exchanged with the system [21]. But
- The VSC can perform even during a black-start because of its capability to turn on or off the current, regardless of the AC voltage [15]. The VSC can provide the required power to restart a thermal power station using the power transported by the HVDC link [22].
- The fast switching PWM reduces the harmonic rejection compared to LCC technology [12].

In comparison to the LCC, VSC has nevertheless some limitations :

- The fault currents cannot be cleared in the station. Thus, AC breakers must be added to the VSC to be able to suppress the fault currents.
- The losses are equal to 1.7% per converter, which is higher than the LCC [20].
- When higher voltage are needed for HVDC transmission, difficulties appear with the VSC because of the blocking voltage capability of the semi-conductors. A connection in series of these semi-conductors is possible, but becomes quickly very complex to handle due to the needed synchronisation of the transistors [7].

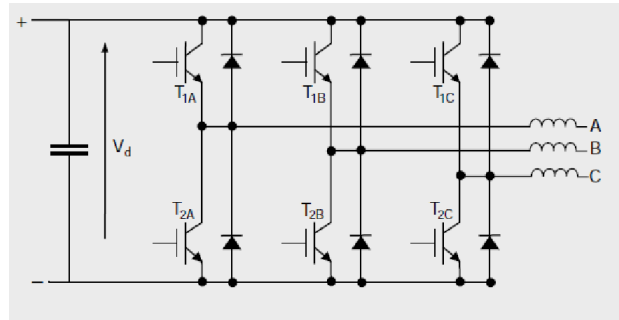


FIGURE 1.4: Voltage Source Converters (VSC) : Inverter [12]

Different classifications for VSC

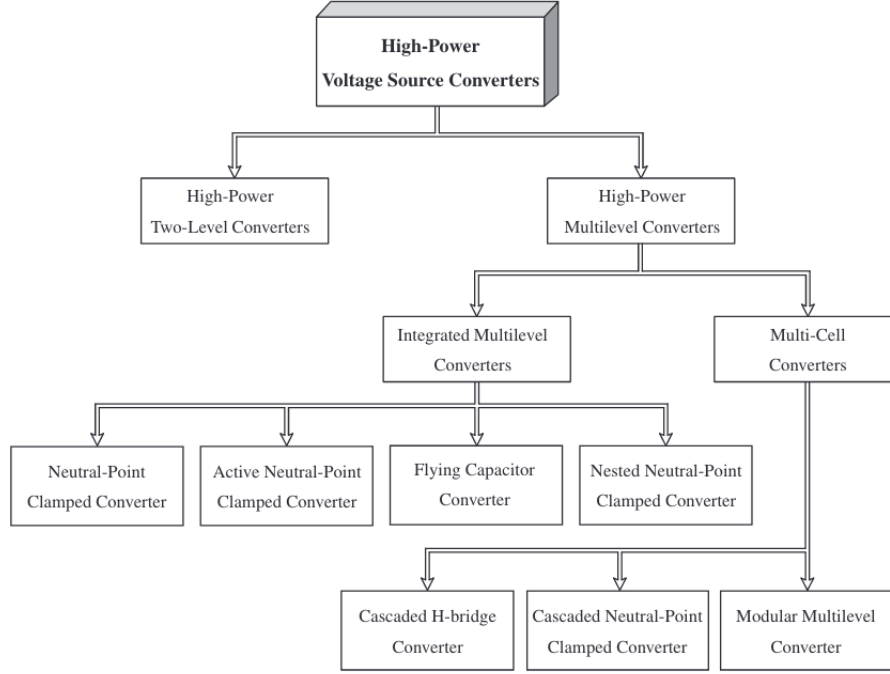


FIGURE 1.5: Classification of voltage source converter [7]

The VSC can be split into two power classification, the low and the high power. FIGURE 1.5 depicts the classification of high power VSC. Throughout this work, the high power part will be more detailed since the MMC is considered as high power converter. Inside the classification, it exists two families of converters. The first one is the high power two-level converter which can be assimilated in series to carry medium-voltage with low capacitor current and in parallel to carry high-current at low-voltage. Nevertheless, series and parallel connections do not bring extra features to the converter (harmonics suppression, voltage rate reduction) which make two-level converter not the best for high power applications.

On the other hand, the multilevel converter is declined into integrated and multi-cell converters. The integrated family includes 4 types of converters which are briefly detailed here-after:

1. **Neutral-Point Clamped Converter :** The three-level neutral-point clamped (3L-NPC) converters are basically composed of two traditional two-level VSCs stacked one over the other with several modifications in the connections. As shown in FIGURE 1.6, the negative bar of the upper converter

is connected with the positive bar of the lower converter forming an output phase. This 3L-NPC converter has its operating voltage and power rating two times greater than the two-level converter. The neutral point of the 3L-NPC converters allows to generate zero voltage level along with $-\frac{V_{DC}}{2}$ and $\frac{V_{DC}}{2}$ which result in low $\frac{dv}{dt}$ and harmonic content in the output voltage and current waveform. The major issues in the 3L-NPC is the neutral-point balancing and low-frequency ripple at higher modulation indices. To counter these issues, the increase of capacitance is traditionally used to minimise the voltage oscillations. Several modulation schemes have been presented to address these issues : Pulse-Width-Modulation technique, the nearest three vectors and virtual vector based space vector modulation (SVM). Furthermore, the 3L-NPC converter has unequal loss distribution between the inner and outer semiconductor devices in each leg. The semiconductor devices are then cooled with separate heat sinks and cooling systems [7].

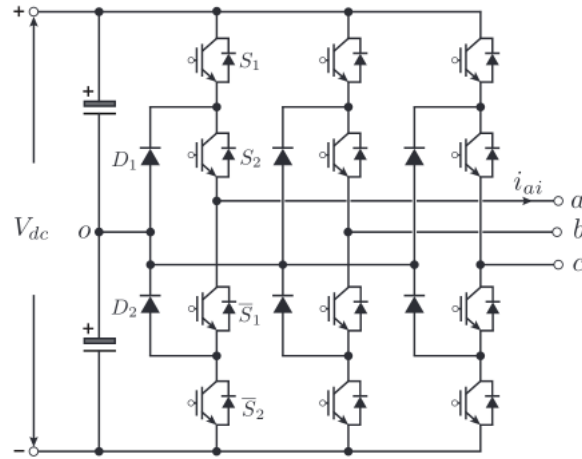


FIGURE 1.6: Three-level neutral-point clamped converter [7]

2. **Active Neutral-Point Clamped Converter :** As discussed above, one of the major issue of the 3L-NPC is the unequal loss distribution between the inner and outer semiconductor devices. This issue is set with heat sinks and cooling systems but those elements result in the asymmetrical distribution of junction temperatures between the semiconductor devices influencing the cooling systems design and the output power limits and the switching frequency of the converters. To overcome these drawbacks, clamping diodes are replaced by active switches as shown in FIGURE 1.7. The active switches provide a controllable path for the neutral-point current allowing the symmetrical

loss distribution among the devices and helping to balance the neutral-point voltage [7].

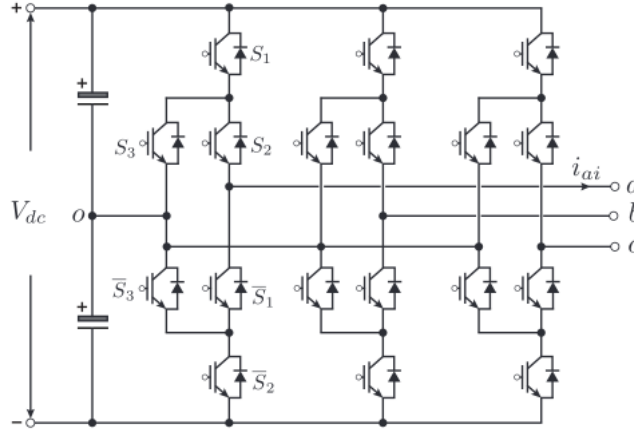


FIGURE 1.7: Active neutral-point clamped converter [7]

3. **Flying Capacitor Converter :** The flying capacitor (FC) converter is quite similar to the NPC converter except that the clamping diodes in the NPC are replaced with flying capacitors. As shown in FIGURE 1.8, each pair of semiconductor devices with flying capacitor forms a power cell. The output voltage level is determined with the number of added power cells which make the FC converter modular. In the FIGURE 1.8, a four-level FC (4L-FC) converter is depicted. The 4L-FC topology has two flying capacitors C_{c1} and C_{c2} at their rated voltage of $\frac{V_{DC}}{3}$ and $\frac{2V_{DC}}{3}$ respectively, and six semiconductor devices with a voltage rating of $\frac{V_{DC}}{3}$. To generate four-level voltage waveform at the output, the flying capacitors have zero initial voltage and must be regulated at their rated value. Therefore, the FC converter needs a pre-charging circuit during the start-up procedure and a balancing control during the steady-state phase.

One of the drawbacks of 4L-FC converters is the capacitor voltage ripple. Its magnitude increases proportionally with the magnitude of the load current and inversely to the switching frequency. To limit this capacitor voltage ripple, the use of larger flying capacitor can be done leading to higher cost and converter size. It is also possible to increase the switching frequency which leads to higher switching losses depreciating the converter efficiency. For these reasons, the applications of flying capacitor are limited to medium

switching frequency [7].

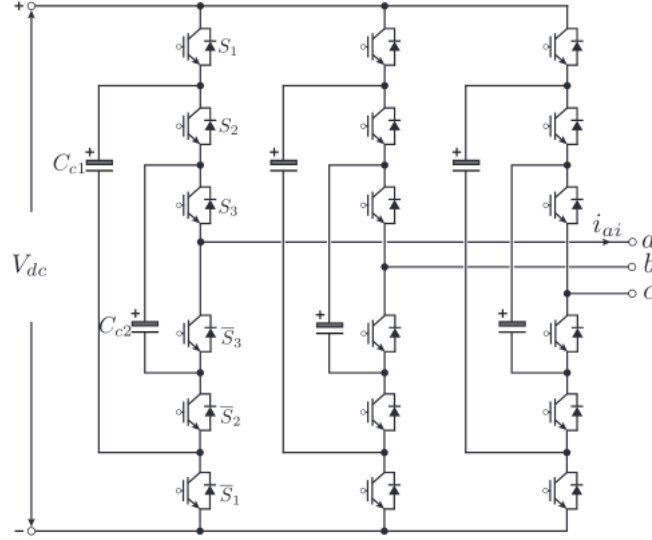


FIGURE 1.8: Four-level flying capacitor converter [7]

4. **Nested Neutral-Point Clamped Converter :** The Nested neutral-point clamped (NNPC) converter combines the structure of an NPC converter and FC converter such as in FIGURE 1.9. The flying capacitor is divided into two equal one and the mid-point is clamped with a diode. In order for the NNPC to generate a four-level voltage waveform at the output, the flying capacitor has to be maintained at $\frac{V_{DC}}{3}$. This type of converters needs less semiconductor devices and passive components compare to the four-level multilevel converters [7].

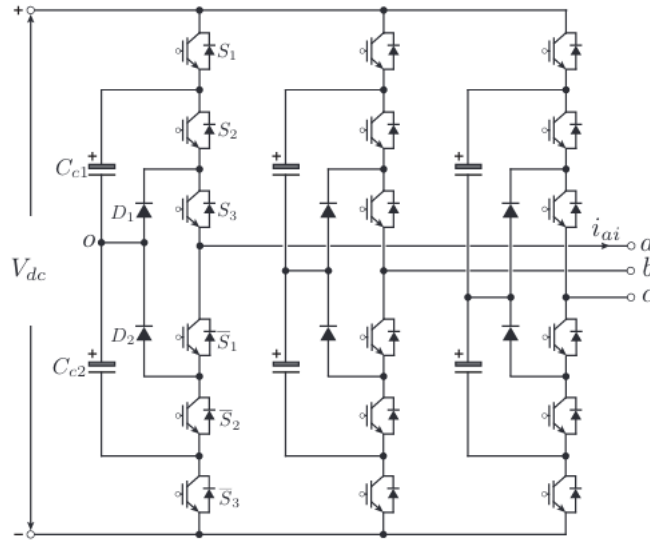


FIGURE 1.9: Four-level nested neutral-point clamped converter [7]

Finally, the multi-cell family is composed by 3 types of converters.

1. **Cascaded H-Bridge Converter** : As already said before, the previous technologies are not cost-effective for high power applications above 6.6 [kV]. Therefore, people decided to invent cascaded converter such as Cascaded H-Bridge (CHB) converter to operate above 6.6 [kV] at a lower cost and with low-voltage IGBT technology. This CHB converter consists in several three-level H-bridge power modules in cascaded as depicted in FIGURE 1.10. An isolated DC-source is required in each power module which is created by a phase-shifting transformer with multiple secondary winding and diode bridge rectifier. By connecting in series H-bridge power modules, the converter voltage increases and consequently the power rating too. The output voltage waveform is then with a higher number of voltage levels and the lowest harmonic distortion is obtained. The numbers of voltage levels achievable is $2N + 1$, where N represents the number of H-bridge power module per phase. However, the CHB requires an large amount of isolated DC-source to power each H-bridge which limits the numbers of H-bridge power modules in each phase. Phase-shifting transformer is also required which increase the the volume, the size and the overall cost of the converter. This topology has a modular advantage which allows fault-tolerant operation with redundant power modules. It also exists two different type of CHB converter, the symmetrical and the asymmetrical but they will not be further describe here in this work [7].

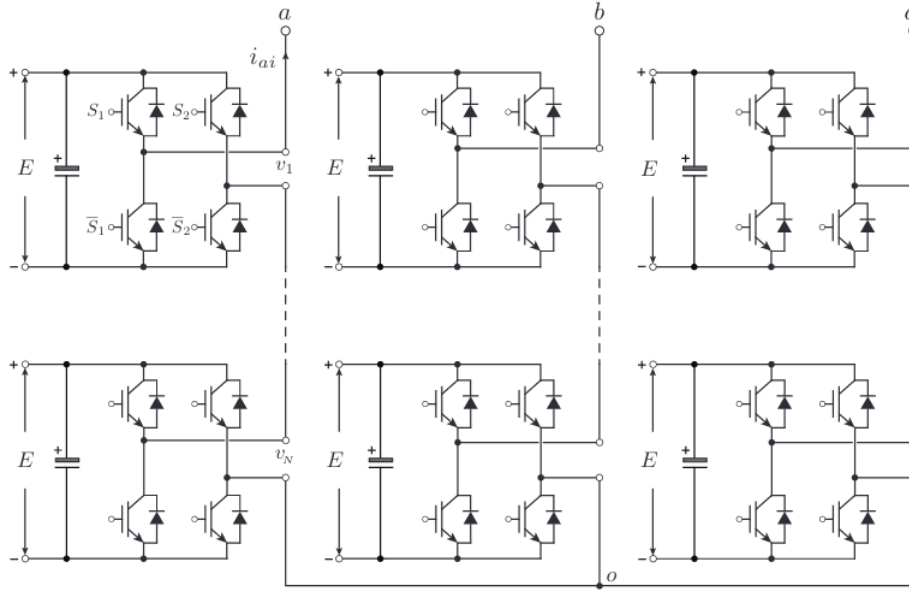


FIGURE 1.10: Cascaded H-Bridge converter [7]

2. **Cascaded Neutral-Point Clamped Converter :** One of the drawbacks of the asymmetrical CHB converters is the loss of the modularity feature and requires that the devices is used with different voltage ratings and thermal designs. This is overcome by replacing the three-level H-bridge power modules with other type of multilevel converters. The most popular topology is the neutral-point clamped converter (CNPC) depicted in FIGURE 1.11. This topology consists in the two three-level neutral-point clamped converter legs in order to form an H-bridge in each phase. A five levels waveform is generated at the output of each HNPC power module. However, the control complexity makes that the number of HNPC modules in CNPC converter is limited to one [7].

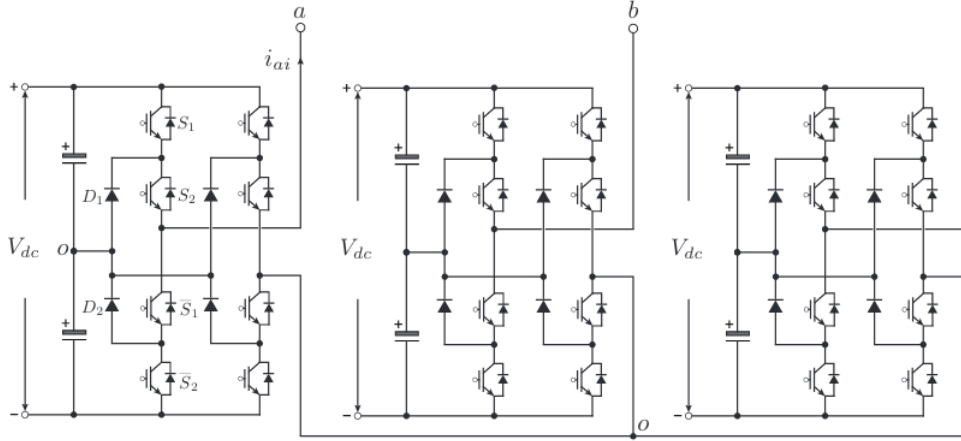


FIGURE 1.11: Cascaded neutral-point clamped converter [7]

Finally, to summarise this introduction chapter, TABLE 1.1 contains the key elements to compare the line-commutated converter with the voltage source converter. The green boxes represent an advantage over the other converter.

	LCC	VSC
Technology	Thyristors Natural commutation	IGBT Forced commutation
Losses	0.7% per converter station	up to 1.7% per converter station
Harmonics	High harmonic content : Important filter banks needed	Low harmonic content : Small filters on AC side still necessary
Active power	Power reversal done by inverting the voltage polarity	Power reversal done by inverting the current flow
Reactive power	Always a consumption	Generate or absorb reactive power
DC fault	Thyristor can control the DC current of the fault	DC breakers needed
AC fault	Can create commutation failures	Can ride through an AC fault
Black start	Not possible because of the need of a very synchronous voltage source	Possible
Grid strength	Need a high short circuit ratio to commute	Grid can be weak but strong enough to synchronise the PLL
Power rating	Up to 7000MW per bipole	Up to 1000MW per symmetric monopole

TABLE 1.1: Comparison between LCC and VSC

Chapter 2

Modular Multilevel Converter

In this chapter, the Modular Multilevel Converter will be detailed from the description of its basic structure to the purpose of each element present inside the converter passing through the different sub-module configurations. One of the main advantage of such converter is its ability to operate at high power with low-voltage insulated gate bipolar transistor. This technology is nowadays increasingly used in HVDC interconnector, the first time it was used was in 2010 as part of the Trans Bay Cable project in the United States of America. This project transfers 400[MW] of electrical power from Pittsburg to the city of San Francisco using an 88[km] undersea cable [23].

2.1 General overview

Nowadays, Modular Multilevel Converter is becoming the most common technology used for High Voltage Direct Current (HVDC) transmission purpose. Indeed, this technology presents several advantages compared to the existing LCC and the two or three-level VSC technologies. Among the major advantages of MMC for HVDC interconnections, one can find an efficiency comparable to thyristor-based HVDC plant which is better than traditional VSC technology. For two-level converter, the use of filters is needed in order to mitigate the pulse frequency. These filters need space. Currently, the compromise to lower the space occupation of these filters is to increase the switching frequency as high as possible, leading also to losses. With MMC, the filters are not needed anymore so that the switching frequency could be reduced hence also the losses. Furthermore, the low harmonics content of this converter is an other big advantage of the MMC [23].

2.2 Operational principle of the sub-module

Before explaining the working principle of the MMC, it is important to have a deeper look in the sub-module which constitute the arm and leg of the converter. Many type of sub-modules are developed for MMC. They all have advantages and disadvantages such as the cost or the ability to suppress DC fault current. Among all the sub-modules configurations, only a few of them as the half-bridge and the full-bridge have emerged in the industry. Indeed, half-bridge has the advantage to be simplest sub-module structure which used the least semi-conductor among the existing sub-modules topologies, hence reducing the losses throughout the converter. Furthermore, the full-bridge converter have the ability to manage DC fault current by reversing the DC-voltage with the lowest losses possible which is the major advantage of this sub-module [24, 25]. Therefore, only the half-bridge and the full-bridge sub-modules will be deeply developed whereas the other will only be mentioned.

2.2.1 Half-Bridge

The half-bridge is among the sub-module configurations the most popular one due to its simplicity and its low cost. The majority of the HVDC link are using this configuration, however this sub-module does not have the capability to manage DC faults currents. As depicted in the FIGURE 2.1a, the half-bridge sub-module is composed by two IGBTs (S_1 & $\bar{S}_1$) with anti-parallel diodes and one capacitor C .

The IGBTs are working in complementary meaning that the sub-module can be in two different states :

1. **The upper IGBT is inserted¹ & lower IGBT blocked²** : The current i_c is equal to the AC current i_{xy} . The capacitor is charging if the current i_{xy} is positive and discharging if the AC current is negative. The output voltage of the sub-module is $v_h = v_c$.
2. **The upper IGBT is blocked & lower is inserted** : The current i_c is zero and the capacitor C is by-passed. The output voltage of the sub-module is then equal to zero too $v_h = 0$.

¹inserted : the IGBT is ON

²blocked : the IGBT is OFF

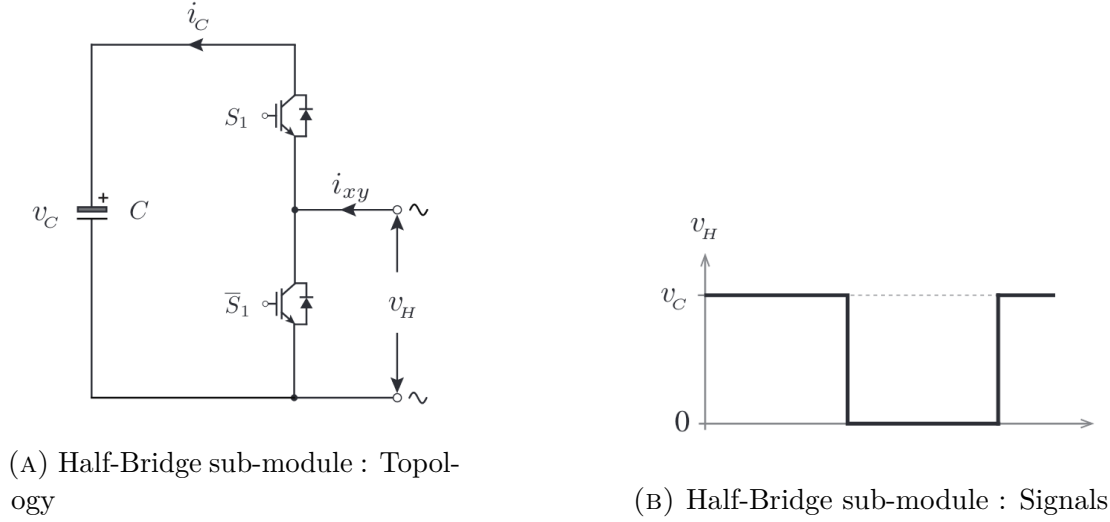


FIGURE 2.1: Half-Bridge [7]

Considering that S_1 is the switching state of the sub-module, the half-bridge converter can be expressed throughout this following EQUATION 2.1.

$$i_c = S_1 i_{xy} \qquad v_h = S_1 v_c \qquad (2.1)$$

The switching state of the sub-module can be summarised in the TABLE 2.1.

State	S_1	v_H	$i_{xy} > 0$	$i_{xy} \leq 0$
1	1	v_c	Increasing v_c	Decreasing v_c
2	0	0	$v_c \approx$	$v_c \approx$

TABLE 2.1: Switching states of the half-bridge

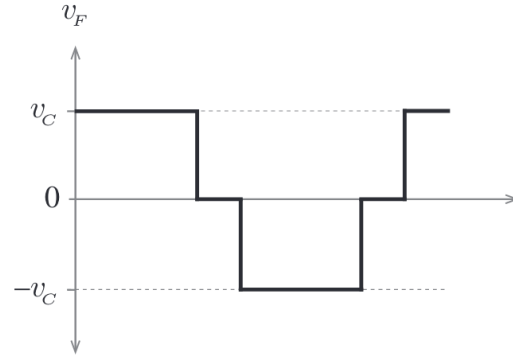
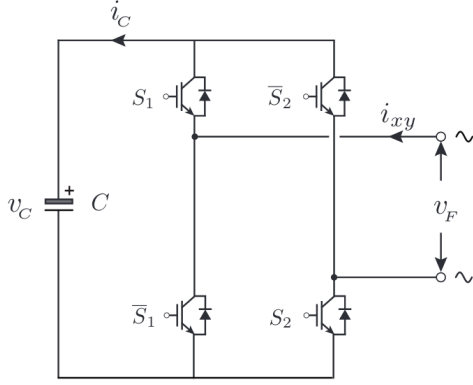
2.2.2 Full-Bridge

The full-bridge is also one of the most popular sub-module. Contrary to the half-bridge, this sub-module is more expensive due to its larger number of components. This sub-module consists in two half-bridge legs in parallel and a capacitor (see in FIGURE 2.2a). Both IGBTs S_1 and S_2 are used to regulate the DC capacitor voltage and have their complementary IGBTs on the lower branch of the sub-module. This configuration allows the sub-module to deliver 3 voltages levels with 4 different states (see in FIGURE 2.2b) :

1. **Both IGBTs are inserted** ($S_1 = S_2 = 1$): In this switching state, the AC current i_{xy} is equal to the capacitor current i_c . Therefore, the positive voltage

of the AC side is connected to the positive DC voltage and the negative AC side voltage to the negative DC voltage. The output voltage v_F is then equal to the capacitor voltage v_c .

2. **IGBT S_1 is inserted ($S_1 = 1$) and S_2 ($S_2 = 0$) is blocked or the Boolean :** In this configuration, the output voltage is equal to zero. No matter the current inside the capacitor i_c , the AC output voltage is equal to zero because the electrical terminals are both short-circuited.
3. **Both IGBTs are blocked :** The output voltage under this configuration is equal to $-v_c$. This switching state is used to limit the current during DC-side faults.



(A) Full-Bridge sub-module : Topology

(B) Full-Bridge sub-module : Signals

FIGURE 2.2: Full-Bridge [7]

As for the half-bridge sub-module, it is possible to translate the different states of the sub-module throughout EQUATION 2.2.

$$i_c = (S_1 S_2 - \bar{S}_1 \bar{S}_2) i_{xy} \quad v_F = (S_1 S_2 - \bar{S}_1 \bar{S}_2) v_c \quad (2.2)$$

The different switching states are summarised in the TABLE 2.2.

State	S_1	S_2	v_F	$i_{xy} > 0$	$i_{xy} \leq 0$
1	1	1	v_c	Increasing v_c	Decreasing v_c
2	1	0	0	$v_c \approx$	$v_c \approx$
3	0	1	0	$v_c \approx$	$v_c \approx$
4	0	0	$-v_c$	Decreasing v_c	Increasing v_c

TABLE 2.2: Switching states of the full-bridge

Beside the half-bridge and the full-bridge configurations, it exists several other types of sub-modules such as :

2.2.3 Flying Capacitor :

The topology of this sub-module is depicted in the FIGURE 2.3a & 2.3b. Flying capacitor sub-module is composed of four IGBTs and two capacitors. There is also four switching states summarised in TABLE 2.3.

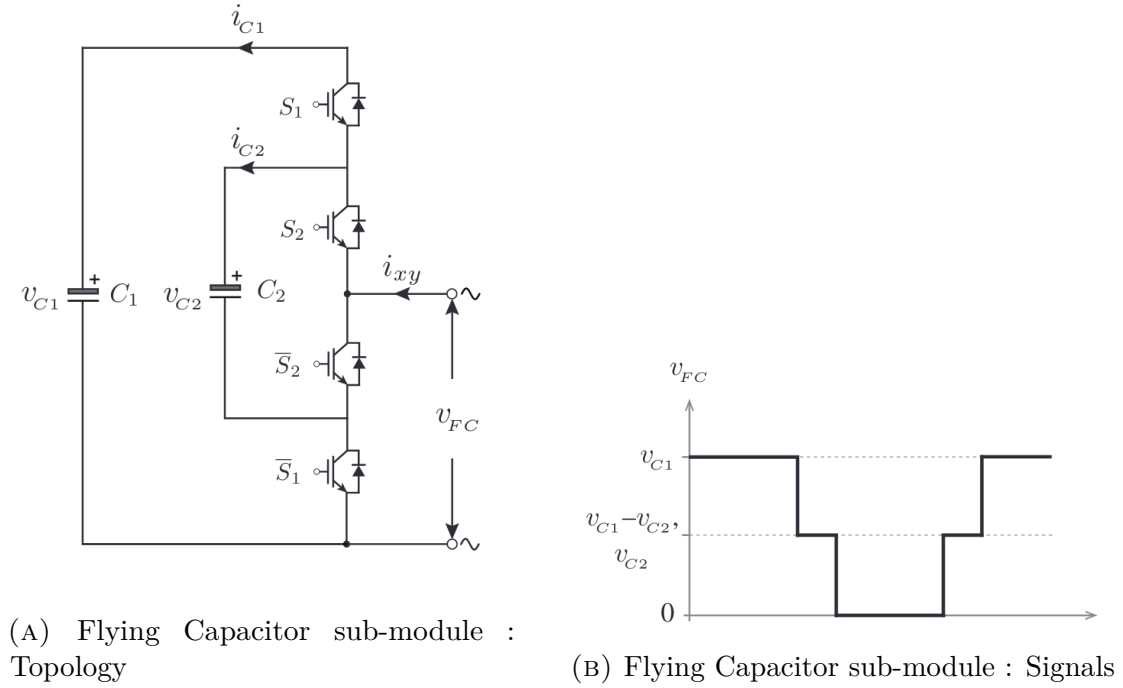


FIGURE 2.3: Flying Capacitor [7]

State	S_1	S_2	v_{FC}
1	1	1	v_{c1}
2	1	0	v_{c2}
3	0	1	$v_{c1} - v_{c2}$
4	0	0	0

TABLE 2.3: Switching states of the flying-capacitor sub-module

2.2.4 Cascaded Half-bridge

This sub-module is composed of two identical half-bridge sub-modules connected in series. The topology is depicted in the FIGURE 2.4a & 2.4b. The switching states are also summarised in TABLE 2.4.

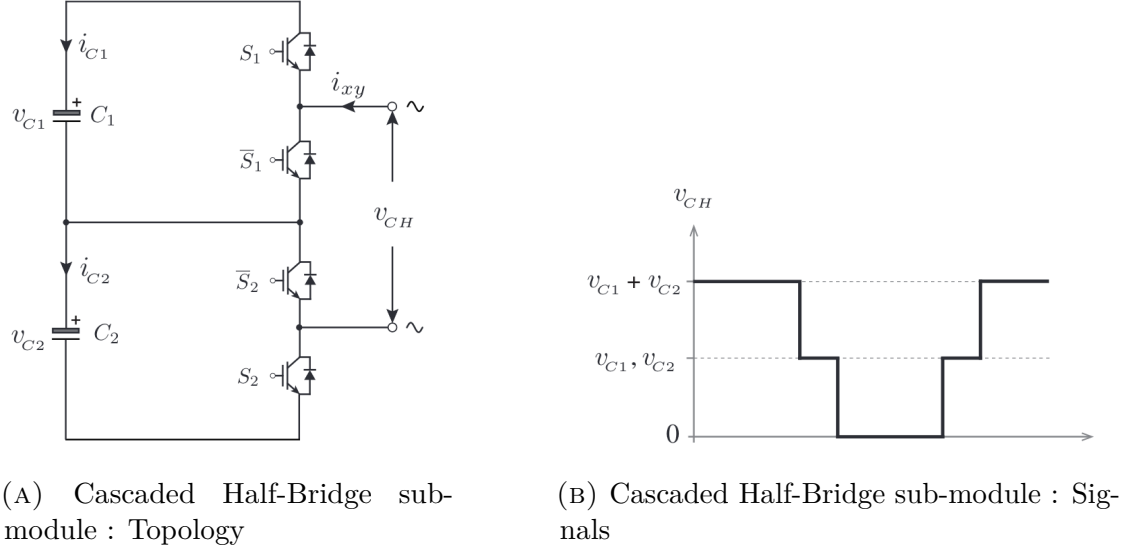


FIGURE 2.4: Cascaded Half-Bridge [7]

State	S_1	S_2	v_{CH}
1	1	1	$v_{c1} + v_{c2}$
2	1	0	v_{c1}
3	0	1	v_{c2}
4	0	0	0

TABLE 2.4: Switching states of the Cascaded Half-Bridge sub-module sub-module

2.2.5 Double Clamp

This configuration is showed in the FIGURE 2.5a and include five IGBTs and two blocking diodes. This configuration allows to have six different switching states summarised in TABLE 2.5 and depicted in the FIGURE 2.5b

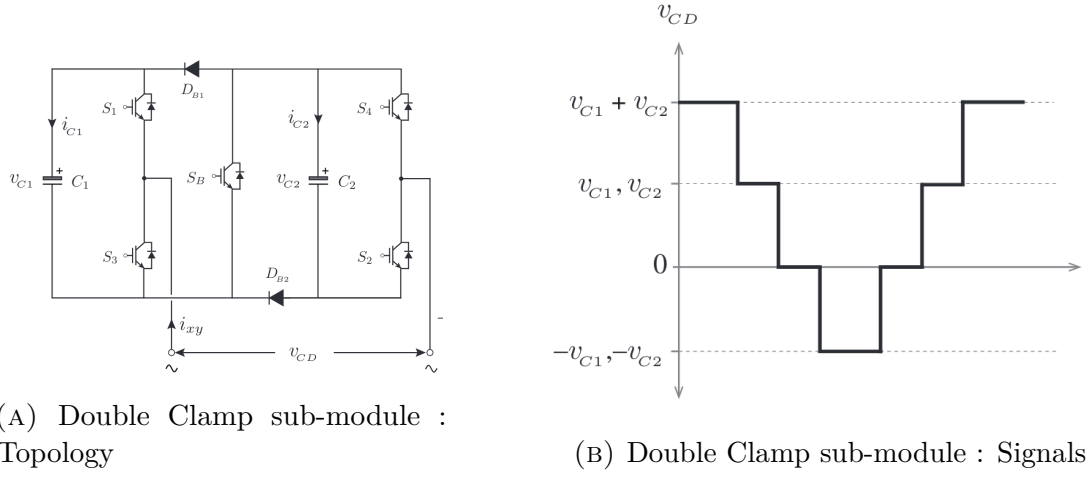


FIGURE 2.5: Double Clamp [7]

State	S_1	S_2	S_3	S_4	S_B	v_{CD}
1	1	1	0	0	1	$v_{c1} + v_{c2}$
2	1	0	0	1	1	v_{c1}
3	0	1	1	0	1	v_{c2}
4	0	0	1	1	1	0
5	0	0	0	0	0	$v_{c1} + v_{c2}$
6	0	0	0	0	0	$-v_{c1}, -v_{c2}$

TABLE 2.5: Switching states of the Double Clamp sub-module sub-module

2.3 Operational principle of the MMC

2.3.1 Single-Phase MMC :

To have a clear understanding of the working principles of a three-phase modular multilevel converter, it is important to understand the single phase MMC. As depicted in FIGURE 2.6, the AC voltage source v_s is connected to the middle point between the two arm of the leg through one resistance R and an inductance L . Each arms are also composed by one inductance L_s and resistance R_s with naturally a number of sub-modules connected in series depending on the numbers of levels N intended. For instance, if four sub-modules are used in one arm, the converter will be able to deliver $N + 1$ voltage levels, so 5 levels. The special case for which the number of sub-module N per arm is equal to one leads to the traditional two-level VSC ($N + 1 = 2$) .

In order to operate the MMC, the number of sub-modules connected in the leg have to remain constant meaning that if, for instance, one sub-module in the *upper arm* is connected, one sub-module in the *lower arm* has to be bypassed. If this is not the case, the number of inserted sub-modules would be $N + 1$ leading to the change of the average voltage of each module to $V_{mod} = \frac{V_{DC}}{N+1}$. To avoid this, if the number of inserted sub-modules in the *upper arm* is n , the number of inserted sub-modules in the *lower arm* will be $N - n$. Finally, because of that only half of the sub-module are used for any instance, the total voltage across all the capacitance is $2V_{DC}$ [26].

An example can be illustrated here-below to explain clearly the operating principle of the MMC. As depicted in the FIGURE 2.7, the output voltage of the single MMC is represented. Different regions are highlighted in order to describe in four states the working principles of the MMC. The regions are :

1. **Maximum voltage (region A) :** In this configuration, all the sub-modules in the *upper arm* are blocked so that the AC voltage point is directly connected to the positive DC voltage $\frac{V_{DC}}{2}$. The *lower arm* sub-modules are all inserted in series and account a total voltage across the arm of V_{DC} .
2. **Decreasing voltage (region B) :** To decrease the voltage at the output of the MMC, one has to increasingly insert sub-module in the *upper arm* and by-pass the sub-module in the *lower arm* at the same time to keep the number of sub-modules inserted constant.
3. **Minimum voltage (region C) :** The minimum voltage is obtained when the *upper arm* sub-modules are all inserted and the *lower* sub-modules are

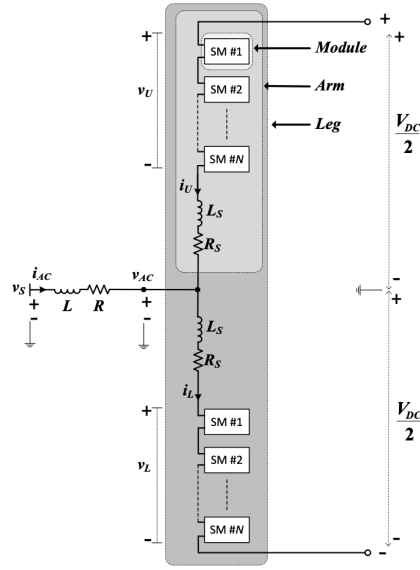


FIGURE 2.6: Modular Multilevel Converter - Single phase [26]

by-passed.

4. **Increasing voltage (region D) :** The same principle as for the **region B** is applicable. To increase the output voltage, one has to block *upper* sub-modules while inserting lower one at the same time.

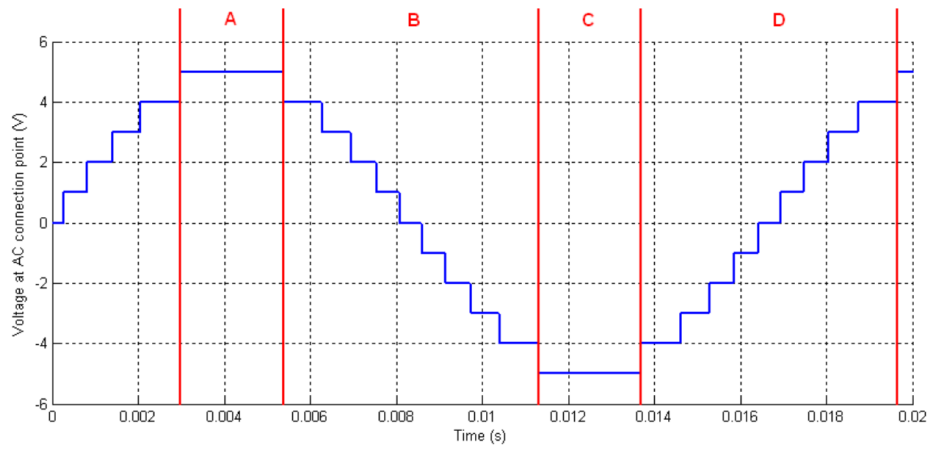


FIGURE 2.7: AC output voltage of a MMC of 10 levels [26]

The power flow in the converter is then regulated thanks to the number of sub-modules inserted in the arms/legs adjusting the middle-point voltage.

Furthermore, in this converter, the energy is not stored in one big capacitance as in the VSC. The capacitance is divided into several smaller capacitance present in each sub-module meaning that each capacitance is equal to $C_{eq,i} = \frac{C_{eq}}{N}$.

2.3.2 Three-phase MMC :

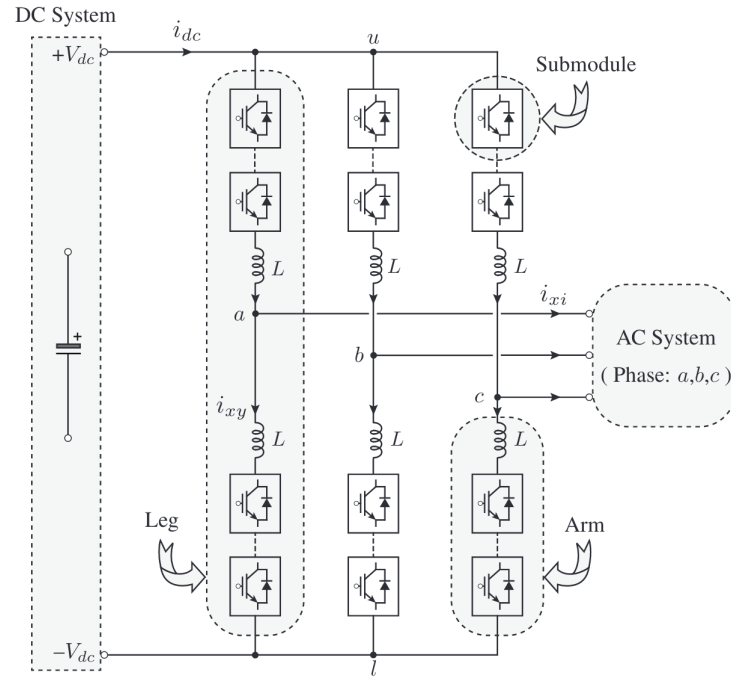


FIGURE 2.8: Modular Multilevel Converter - Topology [7]

As depicted in the FIGURE 2.8, the three-phase MMC topology is three times the single phase MMC placed in parallel. Each phase is then connected to one middle point of each leg to form the three-phase output voltage. Of course, a phase-shift has to be introduced between the phases.

One major difference with the single-phase MMC is the possibility that current circulates between the phases. These currents are called the circulating currents. They are created when there is a voltage imbalance between two legs. They do not have any influence on the DC or AC side of the converter but contribute to major losses through the converter. Therefore, these currents are important to be managed and suppressed with special control methods (see SECTION 4.3). Also, one solution to limit these circulating currents is the arm inductance L . Higher

the inductance are, lower are the circulating currents. However, higher value will lead to lower the reaction time of the system which will not allow rapid current change [26].

2.4 Technical constrains :

There are technical challenges associated with the operation and the control of such a converter. Among these challenges, one can mention :

1. **Design Constraints :** In this converter, there are two passives components, the capacitor and the arm inductance. The sizing of the inductance depends on the arm current ripple and the short-circuit current. Also the suppression of undesirable low-frequency currents needs to be considered during the design of the inductance. For the voltage capacitor sub-module, the size is decided on the trade-off between the size/cost and the capacitor voltage ripple.
2. **Pre-charging process of the sub-module capacitor :** Each sub-module inside the arm have a floating capacitor with a zero initial voltage. This capacitor has to be charged at nominal voltage before starting the normal operation. However this charging process leads to an inrush current due to the small equivalent impedance of the converter during start-up or after a fault.
3. **Voltage control of the sub-module capacitor :** The regulation of the each capacitor voltage in the sub-module represents also an other challenge. Indeed, in MMC, there often is several sub-modules per arm which make the number of capacitor voltage to regulate rapidly consequent. The regulation of the voltage is often separated into three different stages :
 - **Leg voltage control :** In this control, the regulation of the energy inside the leg is controlled thanks to the DC-link current
 - **Arm voltage control :** As the voltage unbalanced between the arms leads to circulating current, the circulating control current is used to control the arm voltage.
 - **Sub-module voltage control :** This control depends on the arm current direction and capacitor voltage error. It also required a large amount of sensors to measure the capacitor voltages and arm currents.
4. **Voltage Ripple of the sub-module capacitor :** The voltage ripple is coming from the interaction between the arm current and voltage. The ripple is dominated by the fundamental and second-order harmonic component. This

phenomena is deeper present in motor drive applications. The suppression of the voltage ripple is a trade-off between performance/efficiency/reliability and the cost/size of the converter

5. **Circulating current** : The circulating current is present due to voltage unbalanced between the arm of the converter. This leads to the presence of negative sequence. The circulating current does not have any impact of the AC output side however it increases the peak and RMS value of the arm current, leading to higher power losses. These currents must be suppressed in order to improve the reliability and efficiency of the MMC
6. **Fault Tolerance** : During fault tolerances, the MMC is designed such that the fault impact is minimised by inserting redundant sub-modules when the faulty sub-module are by-passed by a switch. The challenge is to keep the inrush current in a acceptable range during the process. Also the DC-link short-circuit fault is another challenge. The use of circuit breaker help to mitigate the fault or the use of sub-modules with the capability to suppress these currents can also be an other alternative [7].

Chapter 3

Modelling of the Modular Multilevel Converter

3.1 Modelling of Modular Multilevel Converters

Although the large number of sub-modules in the MMC has improved the voltage scalability for HVDC links, it has also brought a great challenge for the modelling. Indeed, to simulate the behaviour of such converters in a detailed model, thousands of semiconductor switches must be represented with a very small numerical integration time-steps in order to represent an accurate dynamic response. This is a tedious task for the computers and, therefore, many simplified models have been developed to reduce the simulation burden. These simplified models can be divided into different types, and classified from the most complex to the simplest [27] :

- **Full Physics Based Models**
The closest model to reality. It uses differential equations and simulates every switching events in the nanoseconds reference frame
- **Model I : Full Detailed-Models**
It is a very complete model, where each sub-modules are simulated independently.
- **Model II : Equivalent Circuit-Based Model**
This model computes a Thevenin equivalent circuit for each sub-module.
- **Model III : MMC Arm Switching Function**
It uses a simplified circuit that models the arm of the converter.
- **Model IV : Average Modelling Model - AVM**
AVM uses two equivalent circuits for the whole MMC : an AC-side and a DC-side. The behaviour is simulated using voltage and current sources.

The different modellings and simplifications are represented in FIGURE 3.1.

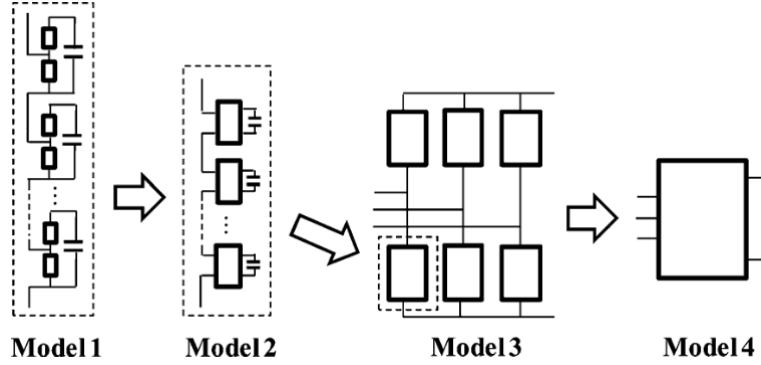


FIGURE 3.1: Different modellings and their decreasing complexity [28]

The different computation times are represented in the TABLE 3.1. It was simulated using the same MMC-HVDC system and calculated with the same computer [29].

Model used	Time-step (μs)	Computing times (s)	Type of studies
Model I	20	1000	Validation of simpler models
Model II	20	900	AC and DC faults
Model III	20	30	Large transients on AC or DC side
Model IV	20	2	Large disturbances on AC side

TABLE 3.1: Computing times for the same MMC-HVDC system

3.1.1 Full Physics Based Models

In a Full Physics Based Models, semiconductors, diodes and switches are simulated using differential equations. An equivalent circuit is then made to simulate a sub-module behaviour, which are then connected in series one by one in order to create an arm. The accuracy of these models is excellent. The simulation uses a time-step of a few nanoseconds and represents all the small switching events in the model.

Full Physics Based Model is a good choice when an accurate simulation of a sub-module behaviour is needed, typically for one sub-module converter. However, this type of modelling is not used to simulate power systems because of the tremendous computation time required [27].

3.1.2 Model I : Full Detailed-Models

In a Type I model, the IGBT switches are modelled with a controlled ideal switch and two non-ideal switches consisting of series and anti-parallel diodes, and a snubber circuit. The snubber circuit is there to copy the reverse recovery condition [28]. The non-ideal diodes are represented as non-linear resistors using the diode V-I curve, with the characteristics taken from the manufacturer. A representation can be seen in FIGURE 3.2.

This model is very accurate for the representation of IGBTs, reproducing precisely the switching events. Moreover, it represents the distribution of the currents but does not represent the switching losses. Although accurate, the simulation of multilevel converters is still very time consuming. The Detailed-Models are typically used to validate simpler models [29].

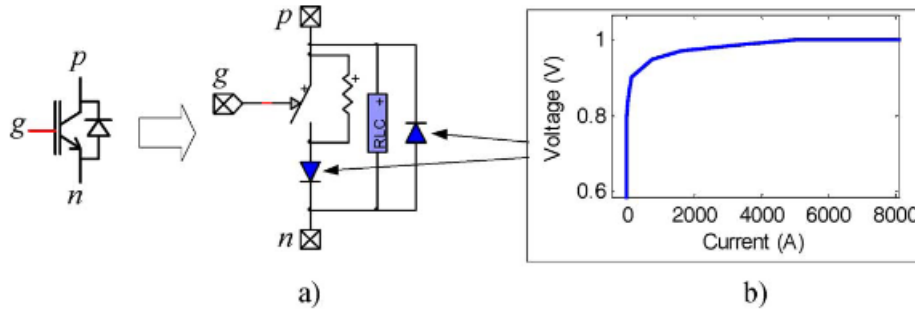


FIGURE 3.2: a) Modelling of an IGBT switch b) Non-linear resistance V-I characteristic [27]

3.1.3 Model II : Equivalent Circuit-Based Model

In a Type II model, the switches are represented as two resistors : R_{ON} , with a value small value and R_{OFF} with huge value [28]. Depending on the gate signals and the current direction, the R_{ON} and R_{OFF} values will be attributed to either R_1 or R_2 , the two resistors of the equivalent circuit of the sub-module. This allows to decrease the complexity and the computational times, by reducing the number of operations. The capacitor of the sub-module is represented as a voltage history source $v_{C,i}^h(t - \Delta t)$ with a resistor $R_C = \frac{\Delta t}{2C}$ in series, where Δt is the time-step [27].

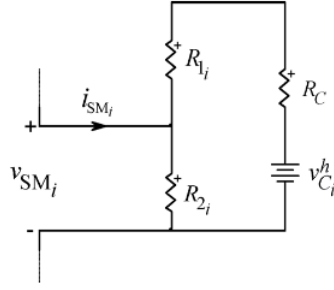


FIGURE 3.3: Half-Bridge equivalent model with a Type II simplification [27]

If i is the index of the sub-module, one can deduce from FIGURE 3.3 a Thevenin equivalent for the i^{th} sub-module :

$$R_{SM,i}(t) = \frac{R_{2,i}(R_{1,i} + R_C)}{R_{1,i} + R_{2,i} + R_C} \quad (3.1)$$

$$v_{SM,i}^h(t - \Delta t) = v_{C,i}^h(t - \Delta t) \cdot \left(\frac{R_{2,i}}{R_{2,i} + R_{1,i} + R_C} \right) \quad (3.2)$$

And therefore the voltage of the i^{th} sub-module can be expressed as :

$$v_{SM,i} = R_{SM,i}(t)i_{SM,i}(t) + v_{SM,i}^h(t - \Delta t) \quad (3.3)$$

Where the Thevenin resistance is depending on the time because the values R_1 and R_2 are changing over time, depending on the gate signals and current direction as stated before. The Thevenin equivalent for the circuit is represented in FIGURE 3.4.

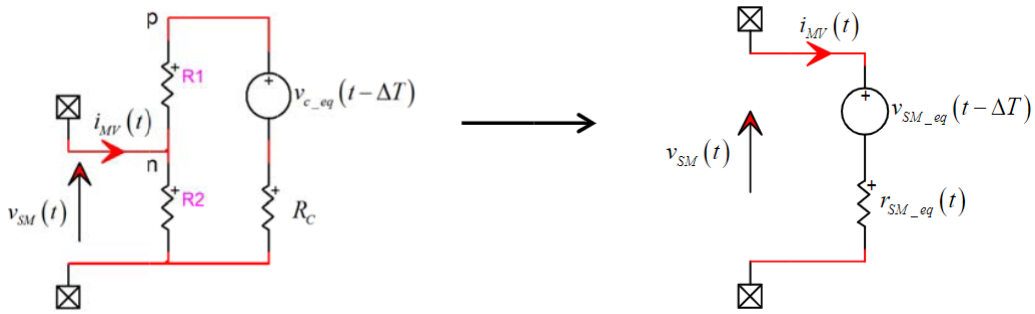


FIGURE 3.4: Thevenin equivalent circuit for a sub-module [29]

With this Thevenin equivalent circuit of the sub-module, and considering that the current in the Thevenin equivalent $i_{SM,i}$ is the same in the whole arm, the

whole arm consists of Thevenin equivalent circuit in series, which can be expressed as one Thevenin equivalent for the entire arm [29] :

$$v_{SM}(t) = \left(\sum_{i=1}^N R_{SM,i}(t) \right) i_{SM}(t) + \sum_i^N v_{SM,i}(t - \Delta t) \quad (3.4)$$

$$= R_{eq} i_{SM}(t) + v_{eq}(t - \Delta t) \quad (3.5)$$

All these simplifications slightly improve the performance of the simulations. However, the system must still consider each sub-modules individually to compute the equivalent Thevenin circuits, and must keep in memory the individual capacitor voltage.

The Model II is typically used to perform analysis on DC or AC side, but also to tune the parameters of the Lower-Level Controls [29].

3.1.4 Model III : MMC Arm Switching Function

In the simplification of the physical model, the Model III is the first step in the averaging concept. The arms of the MMC converter will be averaged with the help of a switching function using the same behaviour as the Half-Bridge, presented in SECTION 2.2.1.

Let S_i be the switching function of the sub-module i :

$$S_i = \begin{cases} 0 & \text{if the state of the SM is OFF} \\ 1 & \text{if the state of the SM is ON} \end{cases} \quad (3.6)$$

For each sub-module, the EQUATION 2.1 remain valid. If the capacitor voltage of each sub-module is supposed to be balanced, and neglecting the voltage difference between the capacitors, the voltage capacitors are equal and can be summed to $v_{c,tot}$, the sum of all capacitor voltages of an arm. An equivalent arm capacitor can be deduced : $C_{arm} = \frac{C}{N}$. The EQUATION 2.1 can be expressed as [30] :

$$v_{c,i} = v_{c,1} = v_{c,2} = \frac{v_{c,tot}}{N} \quad (3.7)$$

The precision of this assumption rises when the number of sub-module increases. It becomes very accurate from $N = 101$ [28]. If the switching function is extended to the whole arm, it gives :

$$s_n = \frac{1}{N} \sum_{i=1}^N S_i \quad (3.8)$$

And the EQUATION 2.1 of the ON/OFF states of a Half-Bridge become :

$$v_{arm} = s_n \cdot v_{c,tot} + i_{arm}(N \cdot R_{ON}) \quad (3.9)$$

$$i_{c,tot} = s_n \cdot i_{arm} \quad (3.10)$$

Where R_{ON} , representing the linear conductivity losses for each sub-module, is added to the equation. A representation of the Model III circuit using the EQUATION 3.9 can be seen in FIGURE 3.5. In the ON/OFF state model, one can note the diode D is in parallel with the arm capacitor to avoid any negative voltage. In the Blocked State model, the MMC arms are represented by an equivalent Half-Bridge diode, in parallel with the equivalent arm capacitor [28].

In Model III, the individual behaviour of each sub-module is no more represented, as the perfectly balanced capacitor voltage is assumed. However, the linear conduction losses and the energy transfer from DC-side or AC-side to the arms are still represented and taken into account. The simplifications greatly decrease the computing times, as it runs 30 times faster than Model II.

Model III is typically used to simulate transient with large disturbances in the AC-side and can be used to tune parameters of the upper-level control [29].

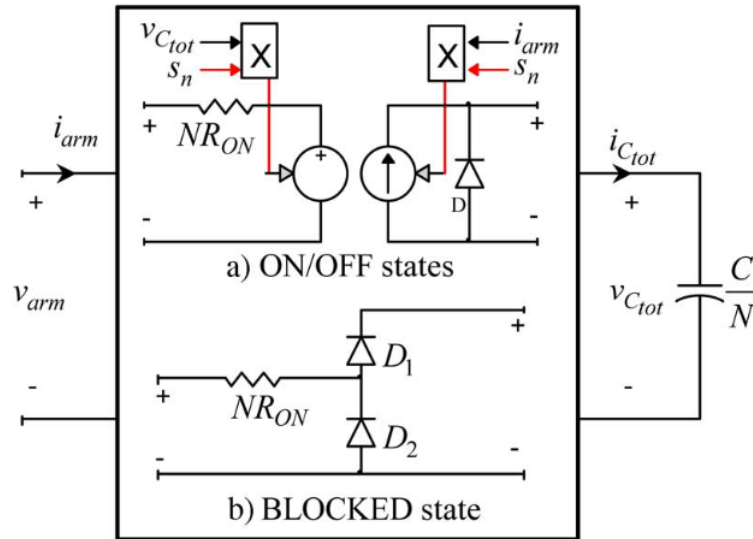


FIGURE 3.5: Model III equivalent circuit of an arm. a) ON/OFF states b) Blocked state [28]

3.1.5 Model IV : Average Modelling Model

In the Model IV, the IGBTs will no longer be represented directly. The behaviour of the MMC will be modelled by controlled voltage and current sources. The source reference voltages are the outputs of the upper-level controllers, detailed in SECTION 4.2.

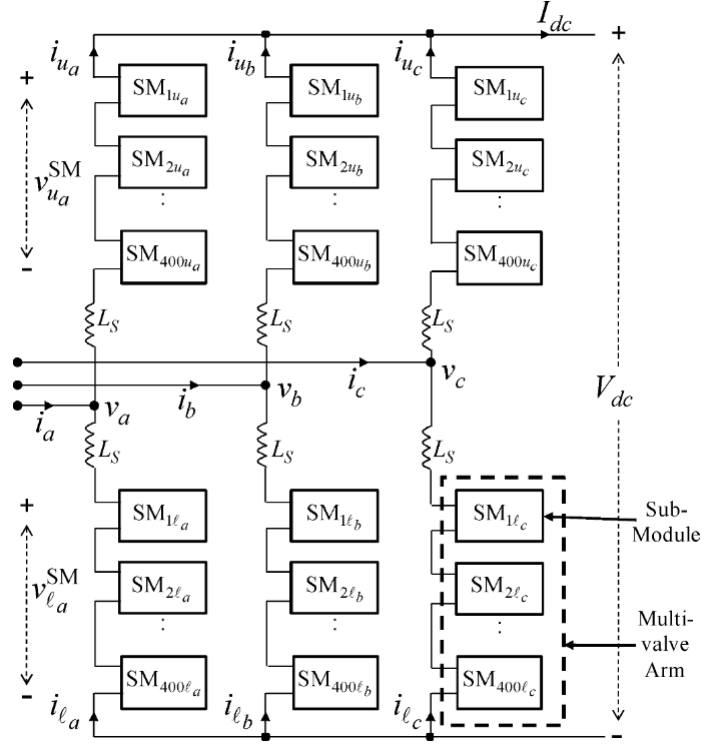


FIGURE 3.6: A detailed MMC representation [31]

Modelling of the AC-side

The AC-side of the MMC will be represented using controlled voltage sources, with the reference voltage coming from the upper-level control.

From FIGURE 3.6, for the phase $j=(a,b,c)$, one can express the total upper and lower arm voltage v_{uj} and v_{lj} , including the voltage of the reactor L_s [29, 31]:

$$v_{uj} = v_{uj}^{SM} - L_s \frac{di_{uj}}{dt} \quad (3.11)$$

$$v_{lj} = v_{lj}^{SM} - L_s \frac{di_{lj}}{dt} \quad (3.12)$$

Where v_{uj}^{SM} and v_{lj}^{SM} are the upper and lower voltage of all the sub-modules. They are dependent on the number of capacitor voltages ($v_{c,uji}$ or $v_{c,lji}$) that are inserted ($S_{u,ji}$ or $S_{l,ji} = 1$ when ON) :

$$v_{uj}^{SM} = \sum_{i=1}^N (S_{u,ji} \cdot v_{c,uji}) \quad (3.13)$$

$$v_{lj}^{SM} = \sum_{i=1}^N (S_{l,ji} \cdot v_{c,lji}) \quad (3.14)$$

The phase voltages are given by :

$$v_j = -v_{uj} + \frac{V_{DC}}{2} = v_{lj} - \frac{V_{DC}}{2} \quad (3.15)$$

Using the EQUATIONS 3.11 and 3.15, the upper and lower arm voltages of all the sub-modules can be express as :

$$v_{uj}^{SM} = -v_j + L_S \frac{di_{uj}}{dt} + \frac{V_{DC}}{2} \quad (3.16)$$

$$v_{lj}^{SM} = v_j + L_S \frac{di_{lj}}{dt} + \frac{V_{DC}}{2} \quad (3.17)$$

The arm currents inside the converters at each phase j can be expressed as [32] :

$$i_{uj} = \frac{i_j}{2} + i_{zj} \quad (3.18)$$

$$i_{lj} = -\frac{i_j}{2} + i_{zj} \quad (3.19)$$

$$i_a + i_b + i_c = 0 \quad (3.20)$$

$$i_{z,a} + i_{z,b} + i_{z,c} = 0 \quad (3.21)$$

Therefore :

$$i_{zj} = \frac{i_{uj} + i_{lj}}{2} \quad (3.22)$$

Where $j = a, b, c$ is the 3 different phases, i_{uj}, i_{lj} are the upper and lower phase currents in the converters and i_{zj} represent the circulating currents in each phase j. AVM modelling assume that the voltage of all the capacitors are perfectly balanced, at any time. It means that the circulating currents $i_{zj} = 0$. With this assumption, EQUATION 3.18 becomes :

$$i_{uj} = \frac{i_j}{2} \quad (3.23)$$

$$i_{lj} = -\frac{i_j}{2} \quad (3.24)$$

And EQUATION 3.16 representing the upper and lower arm voltage become :

$$v_{uj}^{SM} = -v_j + L_S \frac{di_j}{dt} + \frac{V_{DC}}{2} \quad (3.25)$$

$$v_{lj}^{SM} = v_j - L_S \frac{di_j}{dt} + \frac{V_{DC}}{2} \quad (3.26)$$

By introducing a new voltage $e_j = \frac{v_{lj}^{SM} - v_{uj}^{SM}}{2}$, the phase voltage can finally be expressed as :

$$v_j = \frac{L_S}{2} \cdot \frac{di_j}{dt} + e_j \quad (3.27)$$

Finally, one can express the controlled voltage that corresponds to the upper and lower arm voltages of the MMC :

$$v_{uj}^{SM} = -e_j + \frac{V_{DC}}{2} \quad (3.28)$$

$$v_{lj}^{SM} = e_j + \frac{V_{DC}}{2} \quad (3.29)$$

Where the reference voltage e_j is generated by the inner controller developed in SECTION 4.2.3. The EQUATIONS 3.28 and 3.29 will be fed to the controlled voltage sources that will represent the AC-side of the MMC.

A representation of the AC-side of a MMC using an Average Modelling can be seen in FIGURE 3.7.

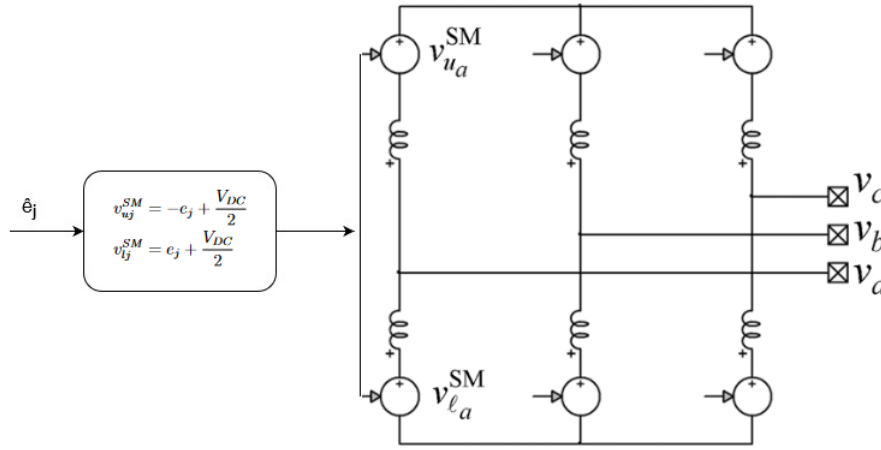


FIGURE 3.7: AVM : AC-side [31]

Modelling of the DC-side

The DC-side will be represented using controlled current sources.

Using the power-balance principle stating that the AC-side power is equal to the DC-side power, one can express :

$$P_{AC} = P_{DC,tot} = P_{DC} + P_{Loss} \quad (3.30)$$

$$\sum_{j=a,b,c} e_j \cdot i_j = V_{DC} \cdot I_{DC} + P_{Loss} \quad (3.31)$$

By introducing the *modulation index*: $m_j = 2 \cdot \frac{e_j}{V_{DC}}$, the power-balance becomes :

$$\frac{P_{ac}}{V_{DC}} = \frac{1}{2} \sum_{j=a,b,c} m_j \cdot i_j = I_{DC} + \frac{P_{Loss}}{V_{DC}} = I_c \quad (3.32)$$

On the DC side of the power balance, one can consider I_c the equivalent DC current that includes the converter losses and will be the current of the first current source in the DC-side.

If R is the equivalent resistance of the MMC representing both switching and resistive losses, one can express :

$$I_{Loss} = \frac{P_{Loss}}{V_{DC}} = R \cdot \frac{I_c^2}{V_{DC}} \quad (3.33)$$

The resistance value R is chosen depending on the full detailed model losses. For MMC, the power losses are in the magnitude of 1% per converter [20, 29]. A current source I_{Loss} can now be introduced in the DC-side AVM and will represent these 1% of losses. The representation of the DC-side of the MMC using an Average Modelling can be seen in FIGURE 3.8.

The capacitance C_e represents the equivalent capacitance of the whole detailed MMC. It can be computed using the principle of energy conservation :

$$E_{MMC} = 6 \sum_{i=1}^{N_{SM}} \frac{1}{2} C v_{c,i}^2 = \frac{1}{2} C_e V_{DC}^2 \quad (3.34)$$

Where N_{SM} is the number of sub-modules per arm, C is the capacitance of a sub-module, $v_{c,i}$ is the voltage per sub-module. If one takes the assumption that every sub-modules have the same voltage $v_{c,i} = v_c$, EQUATION 3.34 becomes :

$$E_{MMC} = 6N_{SM} \cdot \left(\frac{C \cdot v_c^2}{2} \right) = \frac{1}{2} C_e \cdot (v_c \cdot N_{SM})^2 \quad (3.35)$$

Considering the equivalent capacitor C_e :

$$C_e = \frac{6C}{N_{SM}} \quad (3.36)$$

The DC fault are represented by disconnecting the capacitor C_e to imitate the effect of diodes in the detailed model. In the mean time, in the AC-side, all the voltage sources will be bypassed to represent the bypassing of the sub-modules in the detailed model during a DC fault.

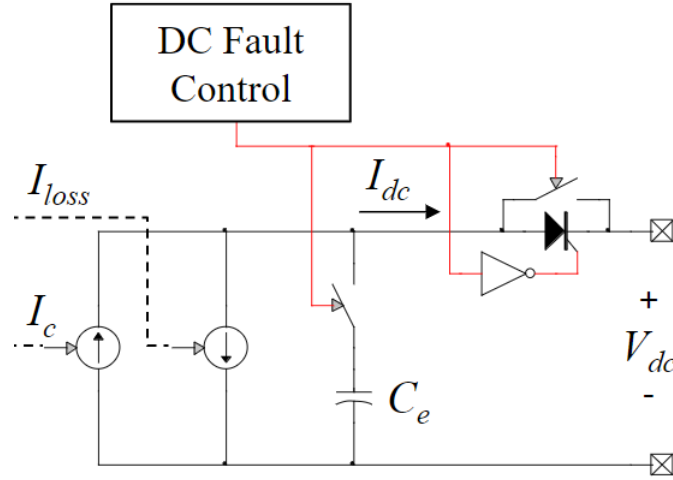


FIGURE 3.8: AVM : DC-side [33]

Model IV simulates accurately the dynamic performance of detailed model [27, 31]. It also accelerates the simulation because it does not represent the switching events and the lower-level control is not needed. It allows to use larger time-step to speed-up the simulation even more. However, it does not represent the DC-fault sufficiently well, thus more detailed models should be used if DC-faults need to be analysed [28].

Typically, Model IV is used to simulate large disturbance on AC grid, runs significantly faster than Model III (15 times faster than Model III for the same configuration) as it can be seen in TABLE 3.1 [29].

Chapter 4

Control of the Modular Multilevel Converter

The control of a MMC station can be separated into two distinct parts: the upper-level and the lower-level control. Each of these levels has multiple controls embedded and they will be detailed in this section. The upper-level consists in two blocks : The outer and inner controls. The first one controls the active power, the reactive power or the DC voltage by producing reference currents, while the inner control controls the reference voltage through the reference currents of the outer control. The upper-level controls the variables in a Park-reference frame. On the other hand, the lower-level control consists of three blocks that will be responsible of regulating the signals inside the MMC converter. A classical representation of the control of a MMC station can be seen in FIGURE 4.1.

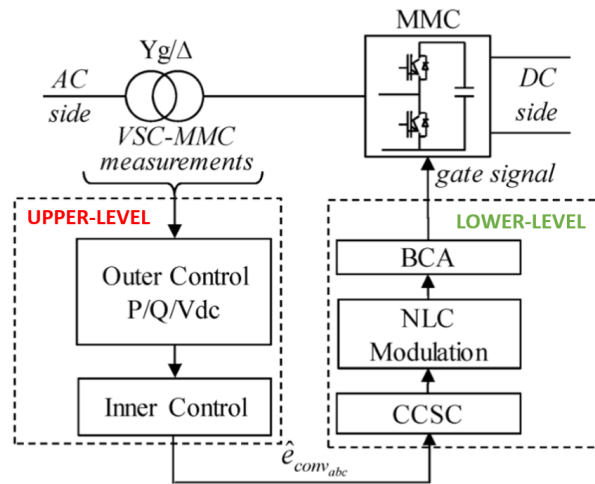


FIGURE 4.1: Control hierarchy of a MMC station [27]

4.1 Park transformation and Phase Locked Loop

To explain the control of the MMC stations, it is necessary to understand both the Park transformation and the Phase Locked Loop (PLL). The Park transformation is used in order to perform a vector control. The decoupling of the active and reactive power allows an independent control of each variable.

Afterwards, the PLL will be explained. It is used to ensure that the controllers are synchronised with the grid.

4.1.1 Synchronous Park reference frame

Using Clarke transformation (see EQUATION 4.1) where the amplitude of the vectors will be kept, the three-dimensions abc voltage can be transformed to a two-dimensions $\alpha\beta$ voltage.

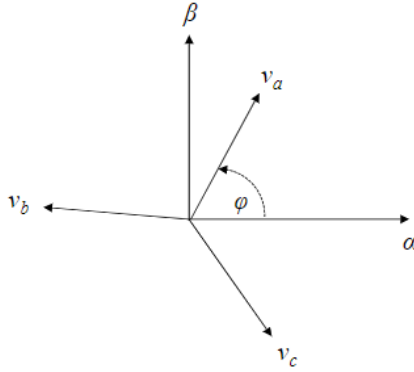
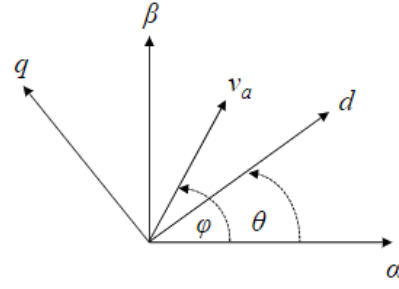
$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{3}{2} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (4.1)$$

Where v_a, v_b, v_c are the voltages in the abc reference frame and v_α, v_β are the associated voltages in the stationary frame represented in FIGURE 4.2.

A second operation is done, to convert the $\alpha\beta$ voltages in $dq0$ voltages, performing a Park transformation (see EQUATION 4.2). Assuming no zero-sequence component because of the transformer delta's connection [33] :

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \quad (4.2)$$

The Park transformation uses the rotating reference frame represented in FIGURE 4.3, which rotates the $\alpha\beta$ frame using the transformation angle $\theta = \omega t$, where ω is the angular frequency in $[rad/s]$ of the AC-grid.


 FIGURE 4.2: (a) Stationary $\alpha\beta$ reference frame [33]

 FIGURE 4.3: (b) Rotating $dq0$ reference frame [33]

From EQUATIONS 4.1 and 4.2, the $dq0$ system can be linked to the abc system and vice-versa using respectively the direct matrix $\mathbf{T}$ and the indirect matrix $\mathbf{T}^{-1}$. The link between both systems can be seen in EQUATION 4.3 and 4.4.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \mathbf{T} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \frac{3}{2} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (4.3)$$

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \mathbf{T}^{-1} \begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \cos(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \cos(\theta + \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad (4.4)$$

4.1.2 PLL-Phase Locked Loop

The frequency and the phase need to be detected for the control to be synchronised with the grid. This will be done by using a Phase-Locked Loop. The PLL circuit generates a reference frame angle θ based on the AC voltage at the point of common coupling (PCC) which will be used as a reference [21].

The PLL synchronises a local oscillator that takes the AC voltage at the PCC as its reference. It will ensure that the oscillator has the same frequency and phase as the AC reference voltage. The block diagram of the PLL can be seen in FIGURE 4.4, where V_q is the quadrature-axis voltage at the PCC and passes through a controller. w_o is the angular frequency of the system. The local oscillator is the voltage controlled oscillator (VCO) [33].

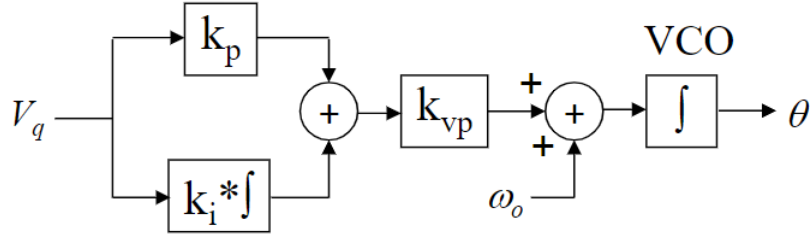


FIGURE 4.4: Block diagram of the Phase-locked loop [33]

4.2 Upper-level Controls - VSC Controls

The upper-level controls are based on a vector control approach. All the operations are performed in the Park reference frame because the active and reactive powers are decoupled using this transformation (see EQUATIONS 4.7 and 4.8). From the voltage measurements at the transformer of the AC grid, the outer control computes the currents required to operate at the reference powers. The active power will be controlled with the d-axis current I_d and the reactive power will be controlled with the q-axis current I_q . These currents will then be given to the inner control [31].

4.2.1 General overview of the Upper-level Control

Similar to HVDC using VSC, the MMC-rectifier and the MMC-inverter can be used to control two variables each. Generally, the first controlled variable is for both stations their respective reactive power or the AC voltage. The second controlled variable is either the DC voltage or the active power. However, when one station of the link controls the active power, the other must imperatively control the DC voltage, and vice-versa. Both stations cannot control the DC voltage and active power simultaneously [12, 34]. This leads to several control modes that can be achieved and they will be detailed further [33] :

- **Fixed active and reactive power control - P/Q**, where the control target is to maintain the powers P and Q controlling respectively I_d and I_q , the dq components of the currents in the rotating frame of FIGURE 4.3.
- **Fixed active power and AC voltage mode - P/V_{AC}**, where the control target is a constant active power, still achieved by regulating the d-axis current, and the ac voltage will be controlled by regulating the reactive power.
- **Fixed DC voltage and reactive power control - V_{DC}/Q**, where the control target is a constant DC voltage achieved by controlling the d-axis

current, while controlling the reactive power with the q-axis current.

- **Fixed voltage mode - V_{DC}/V_{AC}** , where the control target is to control the direct and alternating voltages by regulating the d-q components of the currents.

A representation of the upper-level control can be seen in FIGURE 4.5, where the switches represented after the black and red control boxes represent the different possible modes.

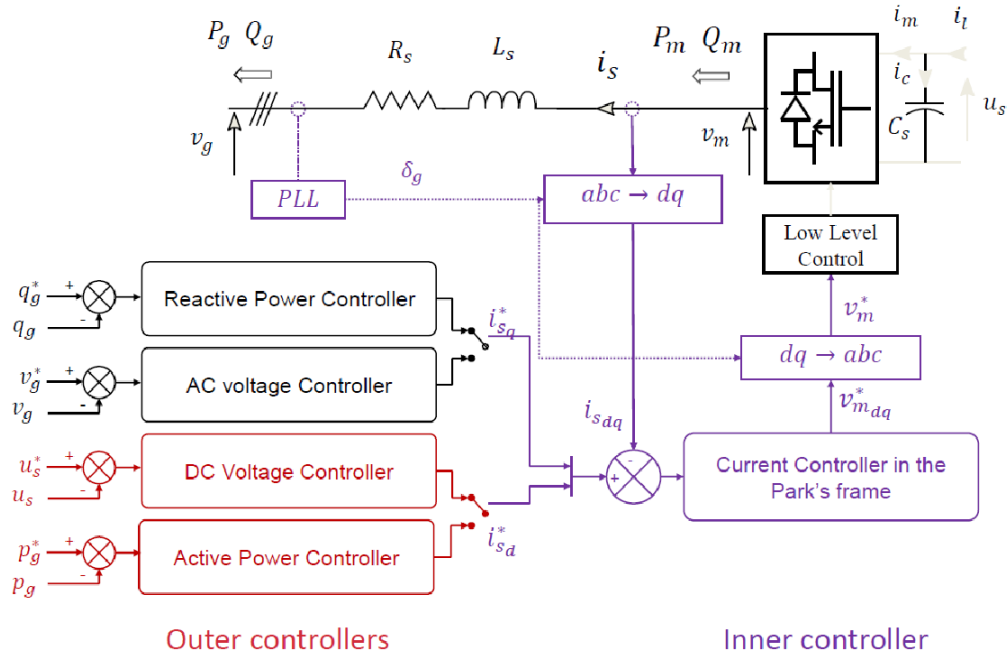


FIGURE 4.5: Upper-level control overview including the Outer and the Inner controls [12]

4.2.2 Outer Controllers

- **Active and Reactive Power Controllers**

From the dq0 axis EQUATIONS (4.4 and 4.3), the active and reactive powers can be expressed as [33]:

$$P_{ac} = \frac{3}{2}(V_d I_d + V_q I_q) \quad (4.5)$$

$$Q_{ac} = \frac{3}{2}(V_d I_q - V_q I_d) \quad (4.6)$$

If we consider the Park reference such as the d-axis voltage V_d is aligned with the ac voltage, the q-axis component of the voltage will be equal to $V_q = 0$. Both equations can be expressed as [33] :

$$P_{ac} = \frac{3}{2}(V_d I_d) \quad (4.7)$$

$$Q_{ac} = \frac{3}{2}(V_d I_q) \quad (4.8)$$

From (4.7) and (4.8), thanks to the Park reference frame, both active and reactive powers are decoupled and can be controlled independently with the d-axis and q-axis currents respectively. Using these equations, a Proportional-Integral PI controller can be designed :

$$I_{d,ref} = \frac{P_{ac,ref}}{V_d} + (k_p + \frac{k_i}{s})(P_{ac,ref} - P_{ac,meas}) \quad (4.9)$$

$$I_{q,ref} = \frac{Q_{ac,ref}}{V_d} + (k_p + \frac{k_i}{s})(Q_{ac,ref} - Q_{ac,meas}) \quad (4.10)$$

Where k_p and k_i are proportional and integral gains of the PI controller that can be seen in FIGURE 4.6, $P_{ac,ref}$ and $Q_{ac,ref}$ are the desired reference values, $P_{ac,meas}$ and $Q_{ac,meas}$ are the measured values of the system, and s is the Laplace variable.

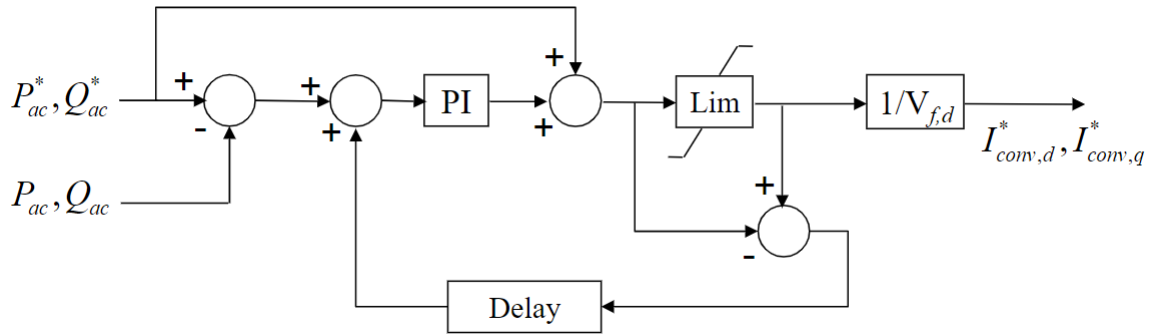


FIGURE 4.6: Upper-level : PI controller of active power P and reactive power Q [33]

In conclusion, the PI controllers are used to generate the reference of the currents in the dq0-frame to reach the desired values of powers. The limiter and the delay blocks depicted in FIGURE 4.6 represent together an anti-windup command. This command aims to enhance the response of the

controller by allowing saturation constraints and mitigate their effect on the closed loop dynamics [35].

- **DC voltage Controller**

Assuming the power balance between the AC-side and the DC-side (thus neglecting the 1% losses of the converter) and considering $V_q = 0$, the power balance can be expressed as :

$$P_{ac} = P_{dc} \quad (4.11)$$

$$\frac{3}{2}V_d I_d = V_{dc} I_{dc} \quad (4.12)$$

$$I_d = \frac{2V_{dc} I_{dc}}{3V_d} \quad (4.13)$$

And using a PI-controller, the dc voltage control can be expressed as :

$$I_{d,ref} = (k_p + \frac{k_i}{s})(V_{dc,ref} - V_{dc,meas}) \quad (4.14)$$

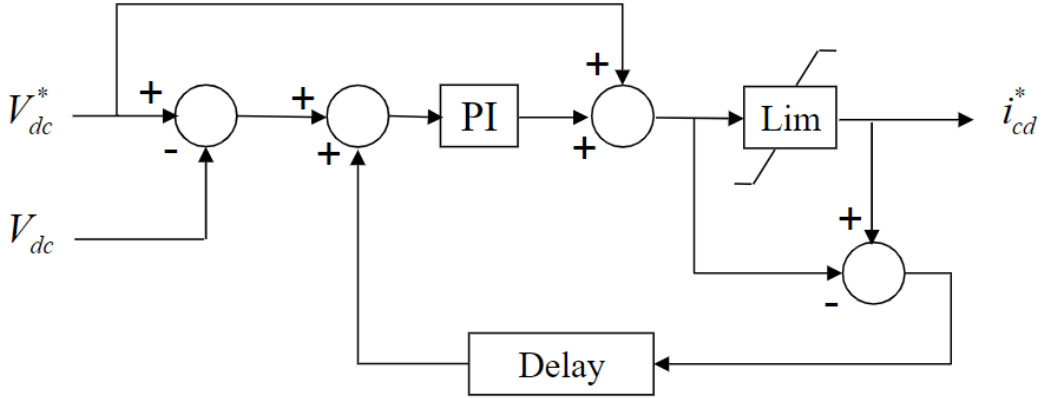


FIGURE 4.7: Upper-level : PI controller of DC voltage [33]

- **AC voltage Controller**

The AC voltage can be controlled using the reactive power. The error of AC voltage will be fed to a first PI-controller that computes and generates a reference reactive power. This reference reactive power will then be fed to a second controller, similar to the FIGURE 4.6.

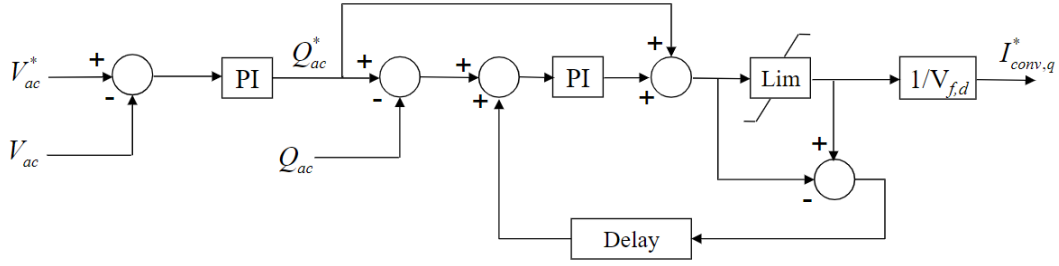


FIGURE 4.8: Upper-level : PI controllers of AC voltage [33]

4.2.3 Inner Controllers

The approach to design the inner controllers is to consider a switching model where an equivalent average circuit for the converter is used. The model becomes therefore time invariant, and is correct at a frequency well below the switching frequency [34]. The equivalent model considers the converters as three single-phase voltage sources with an inductance representing the arm inductance. The transformer is represented as an inductance, and the currents from three phases flow to the converter. The circuit is represented in FIGURE 4.9. The resistive losses of both the transformer and the converter are neglected because of the very high voltage ($L \gg R$).

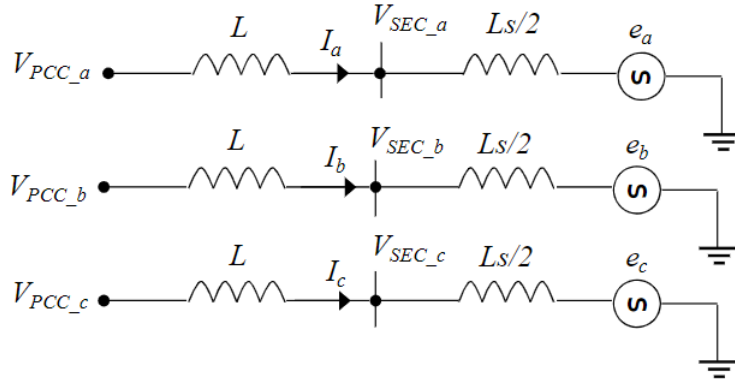


FIGURE 4.9: Equivalent circuit of the converter [29]

From FIGURE 4.9, one can write :

$$\left(L + \frac{L_s}{2}\right) \cdot \frac{di_a}{dt} = V_{PCC,a} - e_a \quad (4.15)$$

$$\left(L + \frac{L_s}{2}\right) \cdot \frac{di_b}{dt} = V_{PCC,b} - e_b \quad (4.16)$$

$$\left(L + \frac{L_s}{2}\right) \cdot \frac{di_c}{dt} = V_{PCC,c} - e_c \quad (4.17)$$

Where L is the transformer inductance, $\frac{L_s}{2}$ is the arm inductance; i_{abc} are the instantaneous line currents going through $\bar{L}$ and $V_{PCC,abc}$ are the voltages at the point of common coupling.

While performing a Park transformation, and assuming that the transformer is connected in delta, the zero-sequence can be considered at zero. Using EQUATION 4.3, one can write :

$$\left(L + \frac{L_s}{2}\right) \cdot \frac{di_d}{dt} = w_0 \left(L + \frac{L_s}{2}\right) \cdot i_q + V_{PCC,d} - e_d \quad (4.18)$$

$$\left(L + \frac{L_s}{2}\right) \cdot \frac{di_q}{dt} = -w_0 \left(L + \frac{L_s}{2}\right) \cdot i_d + V_{PCC,q} - e_q \quad (4.19)$$

Where w_0 is the frequency pulsation measured at PCC, the point of common coupling.

These equations show that the inner controller is a coupled control system [34]. To make the controller design easier, it exists the possibility to decouple both equations by implementing a feed-forward action. With this decoupling, any modification on the reference point $I_{d,ref}$ or $I_{q,ref}$ will not affect the current of the other axis, respectively i_q or i_d [29]. The complete inner current controller can be seen in FIGURE 4.10. The use of this decoupled inner control strategy is chosen to reduce the complexity of the control, while accelerating the system response [34].

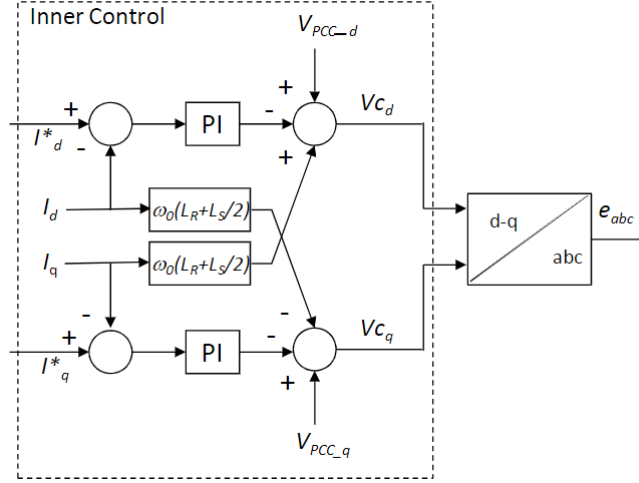


FIGURE 4.10: Inner Controller [29]

4.3 Lower-level Controls - MMC Controls

The purpose of the lower-level Control is to generate the AC waveforms requested by the the upper-level and to control the signals inside of the converter. While the upper-level is similar for the VSC and the MMC, the lower-level is only used for MMC converters and not the VSC. It depends in which topology the MMC is built. The following sections will discuss about the different blocks of the lower-level control, for a MMC using a Half-Bridge configuration for its sub-modules.

4.3.1 CCSC - Circulating Current Suppression Controller

The circulating current is due to the unequal current flow in each phase of the MMC. These circulating currents flow inside the converters and do not flow outside the converter and have no effect on the DC or AC side [36]. They can be suppressed by using an active control [37], or by using a resonant filter made up of parallel capacitors. This section will develop the active control.

The equations of the currents inside the converter are stated in SECTION 3.1.5.

These circulating currents have been investigated and it was showed that they consist of a negative sequence and their main frequency is the second harmonic [21, 33, 36].

These circulating currents can be developed as [38] :

$$i_{za} = I_{2f} \sin(2\omega_0 t + \phi_0) \quad (4.20)$$

$$i_{zb} = I_{2f} \sin(2\omega_0 t + \phi_0 - \frac{2\pi}{3}) \quad (4.21)$$

$$i_{zc} = I_{2f} \sin(2\omega_0 t + \phi_0 + \frac{2\pi}{3}) \quad (4.22)$$

The PI controller of the CCSC can be seen in FIGURE 4.11. It takes as input the upper and lower arm currents that are summed separately to obtain the circulating currents $i_{z,j}$. Then, the transformation of the double-frequency and negative sequence is applied to obtain the dq components of the circulating currents $i_{2f,dq}$. They are compared to the reference values of the second harmonic circulating currents that are set to zero, in order to eliminate these circulating currents. A feed-forward term is necessary. Indeed, the state equation can be expressed as [29] :

$$\begin{bmatrix} u_{zd} \\ z_{zq} \end{bmatrix} = L_s \cdot \frac{d}{dt} \begin{bmatrix} i_{2f,d} \\ i_{2f,q} \end{bmatrix} + \begin{bmatrix} 0 & -2\omega_0 L_s \\ 2\omega_0 L_s & 0 \end{bmatrix} \cdot \begin{bmatrix} i_{2f,d} \\ i_{2f,q} \end{bmatrix} \quad (4.23)$$

Where a coupling between the two dq-axis can be seen. Finally, after a reverse dq0-abc transformation, the resulting reference values are fed to the following block of the lower-level control [37].

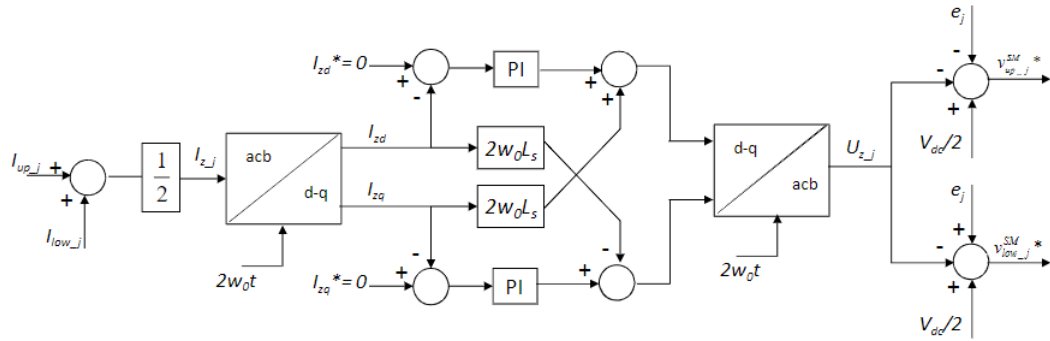


FIGURE 4.11: Lower-level : CCSC [29]

4.3.2 Modulation

The working principle of the modulation is to insert the right number of sub-modules to be able to generate the desired voltage at each time instance. The generation of the voltage will use the available voltage of the sub-modules of the converters, which are kept constant by capacitors.

There are many modulations techniques, and two main classes of modulation will be

presented. The first one is the Multi-Carrier-based modulation (i.e. : Pulse-Width Modulation) and the second one is a carrier-less modulation: Nearest-Level Control [7, 39, 40].

- Multi-Carrier Based Modulation (PWM)

Multi-carrier PWM will compare the modulating signal with a multi-carrier waveform, that usually is a triangular waveform. The classical modulations techniques using a Multi-carrier based modulation are the following [29] :

- Phase-Disposition Modulation (PD-PWM)

In the Phase-Disposition Modulation, triangular functions are compared with the reference voltage. The triangular functions are shifted in amplitude and their number is $N - 1$, where N is the number of levels of the converter.

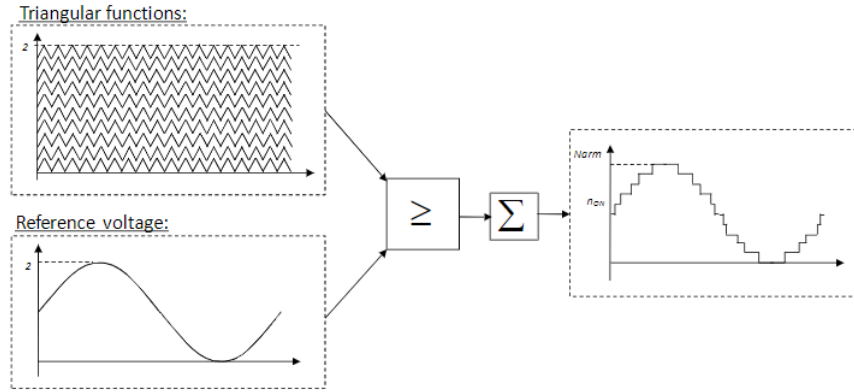


FIGURE 4.12: Phase-Disposition Modulation representation [29]

- Phase-Shift Modulation (PS-PWM) In the Phase-Disposition Modulation, triangular functions are compared with the reference voltage. The triangular functions are shifted in phase in this case. The shift of the carriers is equal to $\alpha = \frac{2\pi}{N}$ between each signal. Moreover, a phase shift θ between the lower and the upper arms exist if there is an even number of levels [41]:

$$\theta = \begin{cases} 0 & \text{if } N \text{ is odd} \\ \frac{\pi}{N} & \text{if } N \text{ is even} \end{cases}$$

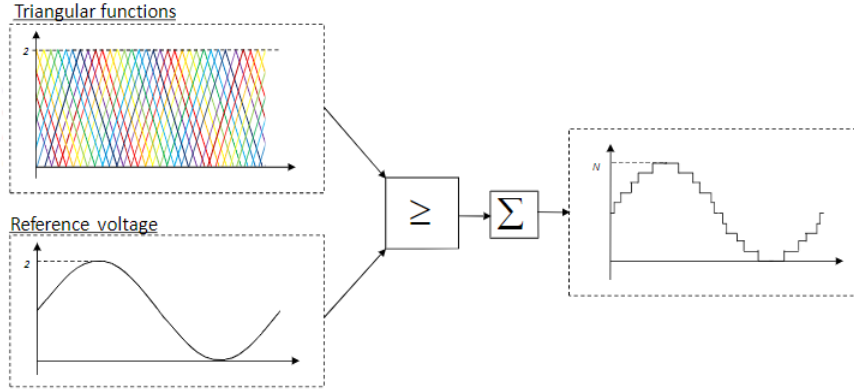


FIGURE 4.13: Phase-Shift Modulation representation [29]

- Carrier-Less Modulation

The Carrier-Based Modulation is often used with VSC transmissions, but as the number of levels increases with the MMC, the use of a carrier based modulation becomes impractical. Another family of modulation is thus preferable for MMC transmissions when the number of levels of the converters grows : the Nearest-Level Control [41, 29]. It is a great alternative because it is simple to implement, and its complexity does not grow when the number of levels of the converter grows.

- Nearest-Level Control - NLC

The principle is to sample the reference at a high frequency, and approximate this reference with its nearest available level. The upper and lower arm functions used as references represent the level of the upper and lower arm. This reference will be divided by the SM capacitor voltage ($v_{c,nom}$) and rounded up or down to its next higher or lower value [7] :

$$\text{round}(x) = \begin{cases} \text{floor}(x) & x < \text{floor}(x) + 0.5 \\ \text{ceil}(x) & x \geq +0.5 \end{cases}$$

Where $\text{floor}(x)$ is the largest integer that is smaller than x , and $\text{ceil}(x)$ is the lowest integer greater than x . In other words, the rounding is returning the closest integer of x . The reference waveform created will have the appearance of a staircase, as seen in FIGURE 4.14. After the rounding, the outputs are the time-varying modulated functions of the number of SM to switch on for the upper and lower arm : $N_{u,j}$ and $N_{l,j}$, where $j = a, b, c$ is the three-phase. The total number of sub-modules inserted $N_{u,j} + N_{l,j}$ is constant and is equal to the number of sub-modules the converter has.

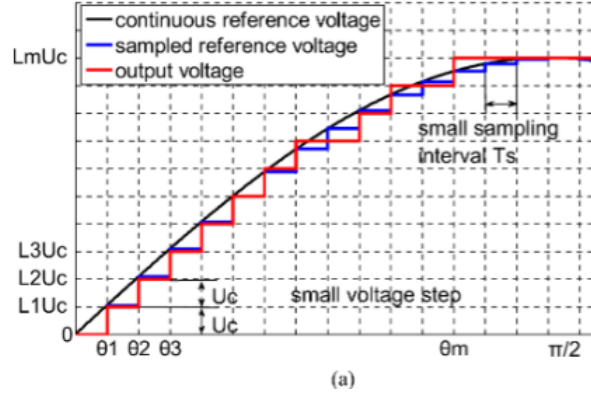
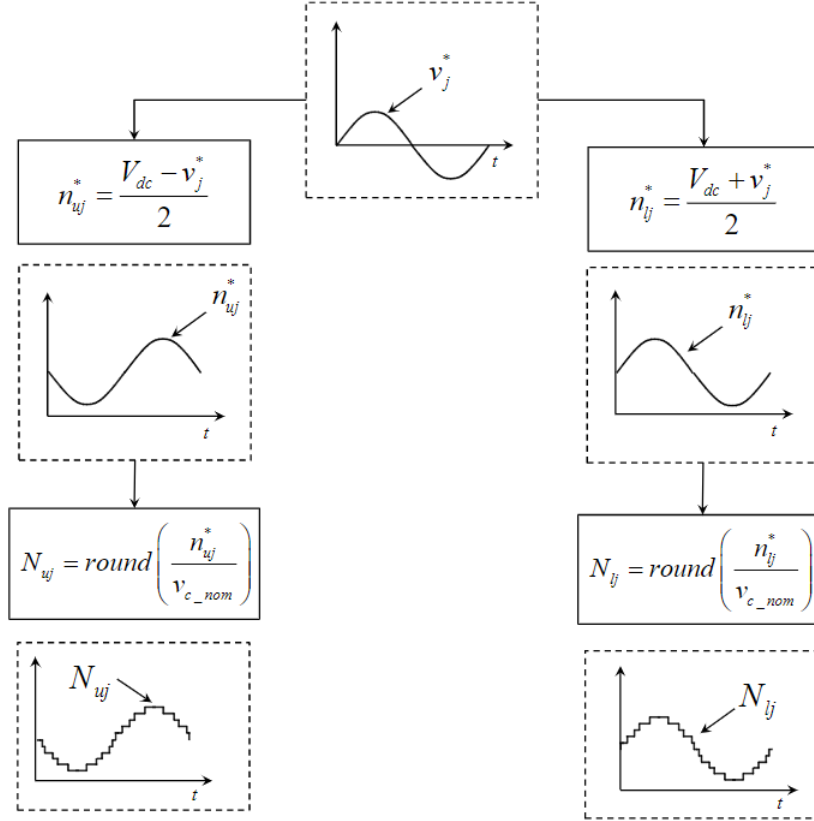


FIGURE 4.14: Continuous reference, discrete reference using the NLC approach, and the voltage output [42]



NLC performs better than multi-carrier modulations when the number of levels

N is high. However, if N is small, the harmonic distortion increases because there would be a small number of output voltage levels. The implementation of NLC is nevertheless simpler than PWM techniques [41].

The performance of a NLC can be observed in FIGURE 4.16. On the left, $N = 5$ and $f_s = 1kHz$ and on the right $N = 30$ and $f_s = 4kHz$. The two upper figures represent the continuous and discretised references, as well as a tracking error represented by dashed lines in the middle. It is clear that the error is smaller as the number of levels increases. The bottom two figures represent the amplitude spectrum computed with a Discrete Fourier Transform, where $THD = 13.8\%$ on the left, and $THD = 1.9\%$ on the right. The amplitude of the harmonics also decreases as the number of sub-modules increases [7].

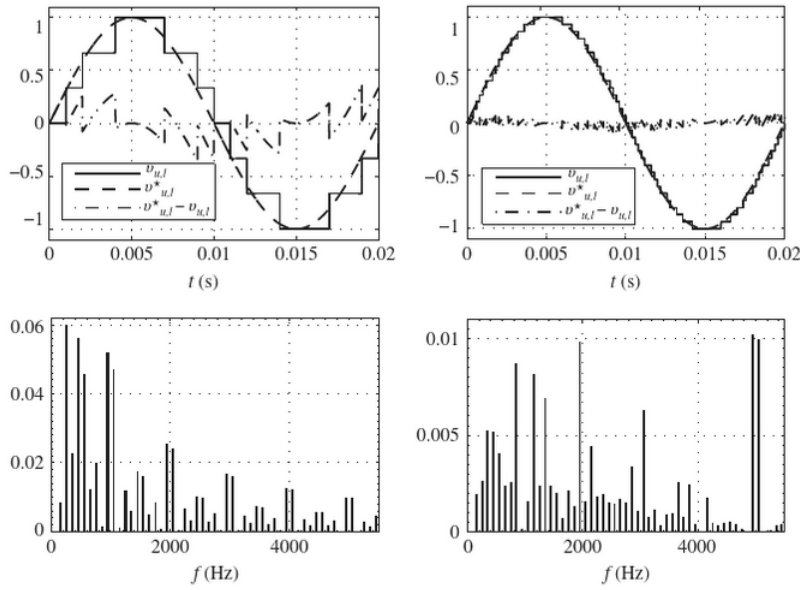


FIGURE 4.16: NLC performance normalised by $V_{arm}/2$ [7]

4.3.3 BCA - Balancing Control Algorithm

Another internal variable in the converter that needs to be controlled is the voltage of the capacitors in all the sub-modules. Without any control, these internal voltages can diverge rapidly and create an unnecessary imbalance. The following algorithm computes the necessary number of sub-modules to turn ON or OFF in the upper and lower arms for each phase. The algorithm creates four different states, based in the direction of the current and the cell state. These states can be seen in TABLE 4.1. In FIGURE 4.17 one can see a representation of the insertion and bypassing of a cell in a Half-Bridge configuration [29].

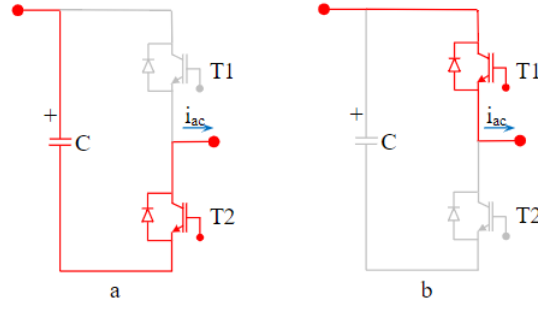


FIGURE 4.17: a) : Insertion of a cell ; b) bypassing of a cell [29]

Cell State	$i_{ac} < 0$	$i_{ac} > 0$
Insert cell	Insertion of the cell with the highest voltage	Insertion of the cell with the lowest voltage
Bypass cell	Bypass of the cell with the lowest voltage	Bypass of the cell with the highest voltage

TABLE 4.1: Four different states of the BCA - insertion or bypassing of a cell

To perform the BCA, a voltage measurement of the capacitors in each cell must be performed at a high frequency. The cells are then classified from the highest voltage to the lowest voltage. This measurement is done every time the number of SM N_{up} or N_{low} inserted changes in the normal operating modes of the MMC. To be able to balance the voltage, when a number of insertions are done in the upper arm, a bypassing of the same number must be done in the lower arm, and vice-versa. The sum of the inserted and bypassed cells must be equal. A global view of the algorithm can be seen in FIGURE 4.18.

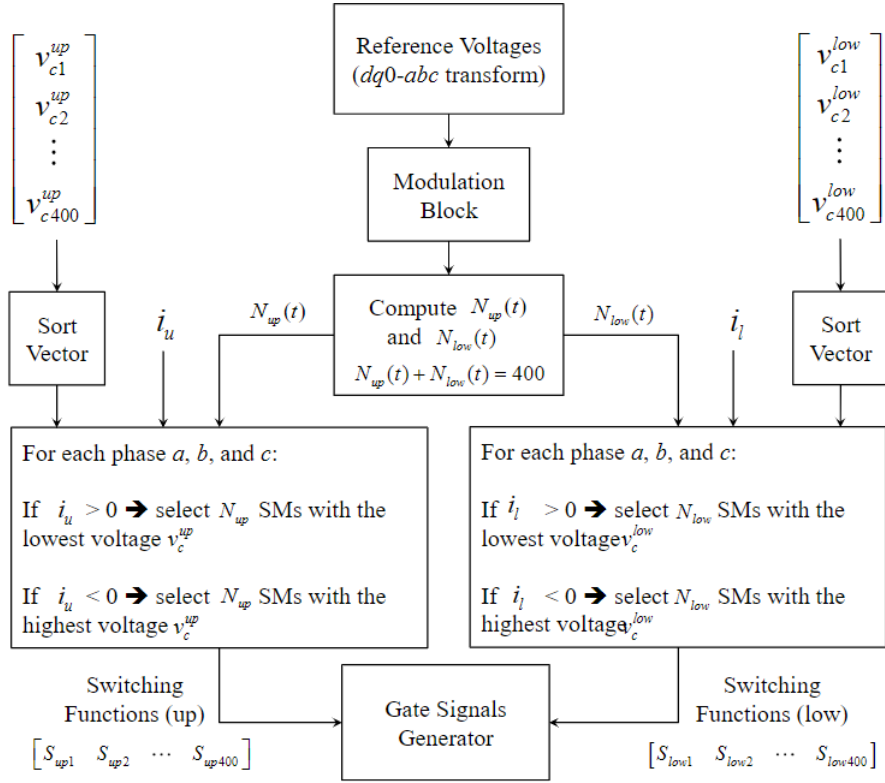


FIGURE 4.18: Global view of the algorithm of BCA [33]

Part II

Implementation of the model

Chapter 5

HVDC transmission system: modelling and validation

The choice of the model to simulate a MMC-HVDC link will be explained in this section. Afterwards, the parameters of the line and the converter will be computed and explained. The validation of the model used is going to be achieved comparing theoretical equations at the steady state of the system and the values obtained by the simulated model. Each simulation is performed using the MATLAB & SIMULINK/SIMSCAPE software.

5.1 Choice of the model type and control of the MMC

The MMC-HVDC link is simulated using the Model IV : Average Modelling Model (AVM), explained in the SECTION 3.1.5. This model has the ability to perform large transients on the AC side and has low computation times. In the same time, it simulates an accurate dynamic behaviour on the AC side of the converter, making it a good choice for the simulations planned for CHAPTER 6.

For the control of the MMC, the Upper-level control is chosen such that the station 1 of the HVDC link maintains the DC voltage constant while controlling the reactive power exchanged with the network (V_{DC}/Q control mode) while station 2 controls the active power exchanged in the DC link and the reactive power exchanged with the network (P/Q control mode). The structure of the controllers are explained in SECTION 4.2.2 and is depicted in FIGURE 5.1.

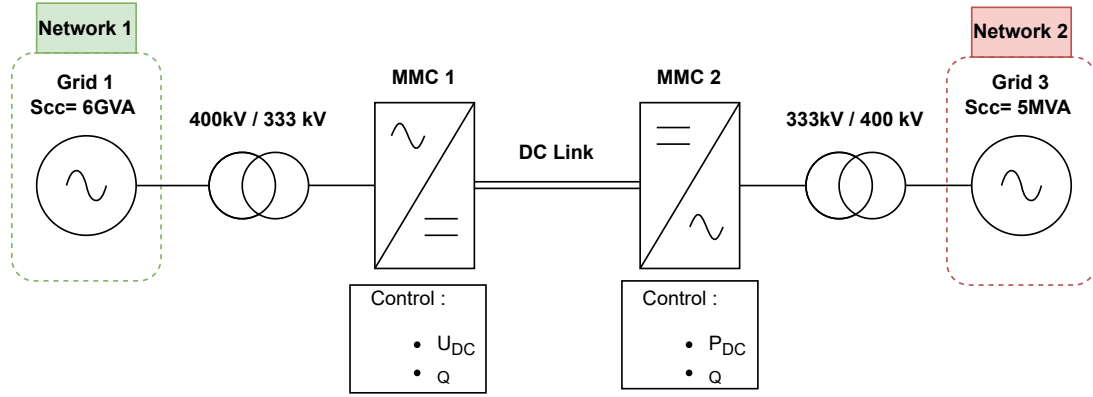


FIGURE 5.1: MMC-HVDC transmission system with the control associated to each MMC station

The AVM does not require a Lower-level control. Indeed, the assumptions of the perfectly balanced capacitor voltages and that circulating currents are suppressed replace the Lower-level control. Moreover, no modulation is needed because the reference voltages are directly generated by the voltage sources, contributing to the simplification of the simulation.

5.2 Choice of the parameters of the model

The modelled link is inspired from the existing HVDC link between France and Spain including MMC to perform the AC/DC conversions as represented in FIGURE 5.2. The nominal power of the link is $S = 1059[\text{MVA}]$ with $N = 401$ sub-modules per arm. The nominal active power transmittable is equal to $1000[\text{MW}]$. Both stations are connected to a three-phase 400 kV grid with the help of transformers, ensuring the transformation of voltage from 400 [kV] to 333 [kV] and reciprocally. Note that the transformers are in a Y/Δ connection which suppress the zero sequence of the Park transform [33]. An overview of the whole system parameters can be found in TABLE 5.1.

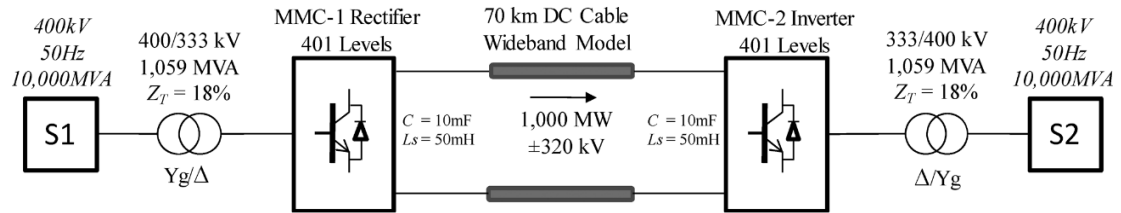


FIGURE 5.2: MMC-HVDC transmission system [27]

Parameters	Notation	Value	Unit
Nominal Apparent Power	S	1059	MVA
Nominal DC Power	P_{dc}	1000	MW
Nominal DC Voltage	V_{dc}	± 320 kV	kV
Nominal DC Current	I_{dc}	3125	A
DC Cable resistance	R_{dc}	0.011	Ω/km
DC Cable inductance	L_{dc}	2.615	mH/km
DC Cable capacitor	C_{dc}	0.1908	$\mu F/km$
DC Cable length	D	70	km
Primary Voltage	$V_{ac,1}$	400	kV
Secondary Voltage	$V_{ac,2}$	333	kV
Frequency of the grid	f	50	Hz
Transformer inductance	L	63.5	mH
Arm inductance	L_s	50	mH
Sub-module capacitor	C	10.4	mF
Sub-module voltage	v_c	1.596	kV
Number of level per arm	N_{arm}	401	/

TABLE 5.1: Overview of the parameters of the model simulated

5.2.1 Arm Inductance

The arm inductance value has been chose equal to $L = 50[mH]$ regarding the HVDC link between France and Spain. This value is, as previously explained in SECTION 2.3.2, determined on the trade-off between the limitation of the circulating current between the three-phases and the reaction time of the system.

5.2.2 SM capacitor

The sub-module capacitor is chosen such that the voltage ripple in the sub-module is in the range of 10%. It was computed that the energy stored in the sub-module should therefore be in the range of $E_{MMC} = [30 - 40]$ kJ/MVA to respect this voltage ripple [31]. Using EQUATIONS 3.35 and 3.36, the SM capacitor (C) can be computed as :

$$C = \frac{2 \cdot (E_{MMC} \cdot S_{MMC})}{6N_{arm} \cdot v_c^2} = 10.4[mF] \quad (5.1)$$

Where E_{MMC} is the sub-module energy per [MVA] and is fixed to 30[kJ/MVA], S_{MMC} is the nominal apparent power, N_{arm} is the number of sub-module per arm. The voltage per SM is computed with : $v_c = \frac{2V_{dc}}{N_{arm}} = 1.596[kV]$.

5.2.3 DC link

To represent a DC-Cable, PI-model or Bergeron model can be used to simulate accurately the propagation of the waves along the line, the reflexive effects etc. [43]. For the model simulated, a RLC circuit is chosen because the simulations of SECTION 6 are mainly focused on the AC-side. The aforementioned effects on the DC link will not be the main concern.

The parameters of the DC link were chosen according to realistic values. The DC cable modelled takes the values of the *HVDC XLPE (Cross-linked Polyethylene)*. It can transmit a power of $P = 1000[\text{MW}]$ with a voltage of $V_{dc} = \pm 320[\text{kV}]$ and support a rated current of $I_{dc} = 1900[\text{A}]$. It is used in practice for the HVDC link *Nemolink* between Belgium and Great Britain and for the link *IFA 2* between France and Great Britain [44, 45].

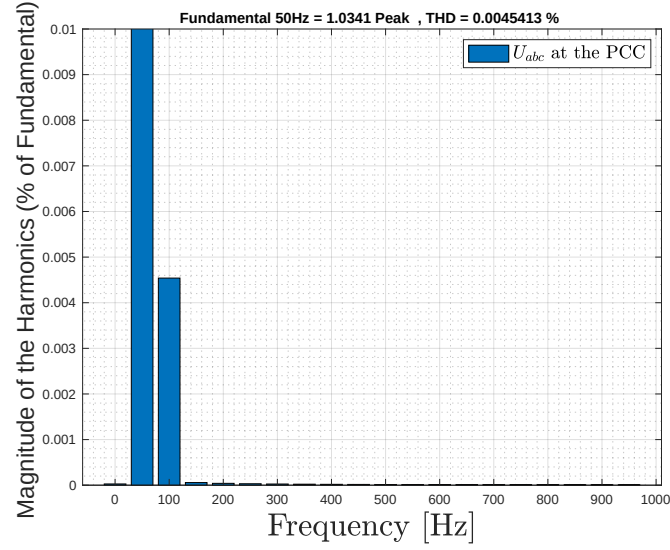
Typical values to represent a *HVDC XLPE* DC-cable can be found in TABLE 5.2.

R [Ω/km]	C [$\mu\text{F}/\text{km}$]	L [mH/km]
0.011	0.1908	2.615

TABLE 5.2: DC-cable parameter per length [29]

5.2.4 AC Filters

The presence of AC filters are not relevant for the model simulated. As the HVDC link with MMC technology produces a low level of harmonics, the AVM modelling implemented use perfect controlled voltage and current sources. Therefore, no modulation technique are needed to generate the signal gate such as PWM or NLC techniques since the voltage reference and current are directly implemented on the controlled voltage and current source. In order to show that, the harmonics content of the voltage at the PCC has been plotted in FIGURE 5.3. It shows that the magnitude of the second order harmonics is quite small $\pm 4 \times 10^{-3}$ while the other can be neglected. The Total Harmonic Distortion (THD) is an indicator of the quality of the signal. It is represented as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency [46]. The THD is expressed in percentage and has been computed to 4.5413×10^{-3} for our model. This value is pretty small confirming that AC filters are not needed.

FIGURE 5.3: THD of U_{abc} at the PCC

5.3 Implementation

The simulated link with the MATLAB & SIMULINK/SIMSCAPE software can be seen in FIGURE 5.4.

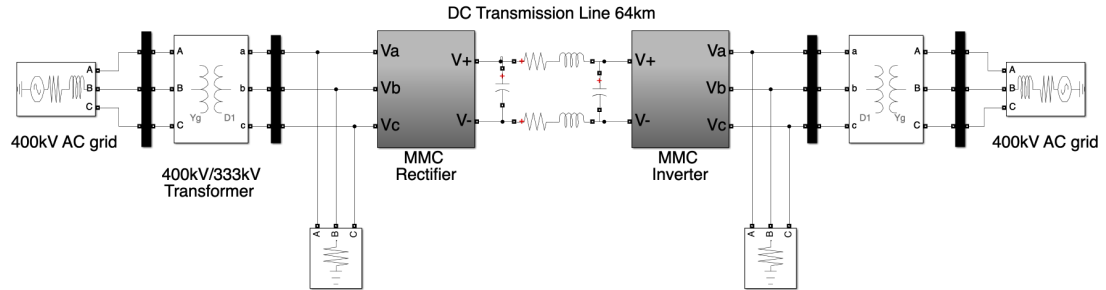


FIGURE 5.4: MMC-HVDC transmission system in MATLAB & SIMULINK/SIMSCAPE

The MMC Rectifier, implemented using an Average Modelling Model can be seen in FIGURE 5.5. It follows the implementation explained in SECTION 3.1.5

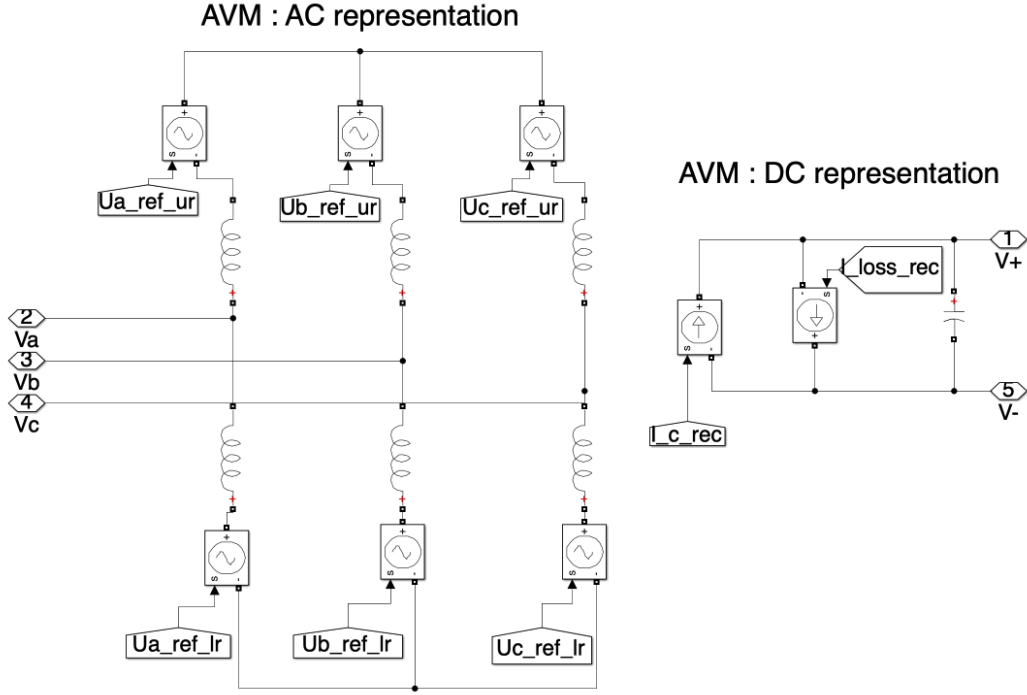


FIGURE 5.5: MMC : AVM of the Rectifier (Station 1)

5.4 Validation

5.4.1 Equations in steady state

To validate the system implemented in this chapter, theoretical equations of the system will be computed and compared to the values simulated [47]. One considers a Park transformation described in SECTION 4.1.1 and a PLL described in SECTION 4.1.2, with a reference frame angle θ for the PLL chosen such that $V_{1q} = 0[\text{pu}]$ and $V_{1d} = 1[\text{pu}]$ for the rectifier side, while $V_{2q} = 0[\text{pu}]$ and $V_{2d} = 1[\text{pu}]$ for the inverter side [47]. From EQUATION 4.5, one can determine the currents of the rectifier (station 1) in the dq-frame i_{rd} and i_{rq} :

$$i_{rd} = \frac{2P_r}{3V_{1d}} \quad (5.2)$$

$$i_{rq} = \frac{2Q_r}{3V_{1d}} \quad (5.3)$$

And the same for the inverter (station 2) currents in the dq-frame i_{id} and i_{iq} :

$$i_{id} = \frac{2P_i}{3V_{2d}} \quad (5.4)$$

$$i_{iq} = \frac{2Q_i}{3V_{2d}} \quad (5.5)$$

From the EQUATION 4.18 of the inner controllers, the corresponding values of the equations are $V_{PCC,d} = V_d$, $V_{PCC,q} = V_q$ and $e_d = v_{rd}$, $e_q = v_{rq}$ and $\omega_0 = 50 \times 2\pi$. In steady state, the derived currents are considered to be equal to zero [47]. For the rectifier, the equations then become :

$$0 = w_0 \left(L + \frac{L_s}{2} \right) \cdot i_{rq} + V_{1d} - v_{rd} \quad (5.6)$$

$$0 = -w_0 \left(L + \frac{L_s}{2} \right) \cdot i_{rd} + V_{1q} - v_{rq} \quad (5.7)$$

$$v_{rd} = w_0 \left(L + \frac{L_s}{2} \right) \cdot i_{rq} + V_{1d} \quad (5.8)$$

$$v_{rq} = -w_0 \left(L + \frac{L_s}{2} \right) \cdot i_{rd} + V_{1q} \quad (5.9)$$

Similarly for the inverter, the equations of the dq voltages can be expressed as :

$$v_{id} = -w_0 \left(L + \frac{L_s}{2} \right) \cdot i_{iq} + V_{2d} \quad (5.10)$$

$$v_{iq} = w_0 \left(L + \frac{L_s}{2} \right) \cdot i_{id} + V_{2q} \quad (5.11)$$

For the DC part, the losses are mainly due to Joule losses. Therefore, using the definition of Joule losses and the equation of the power balance :

$$P_{Joules} = RI_{dc}^2 = R \frac{P_r}{V_{dc,1}} \quad (5.12)$$

$$P_i = P_{dc} - P_{Joules} \quad (5.13)$$

$$V_{dc,2} = \frac{P_i}{I_{dc}} \quad (5.14)$$

5.4.2 Comparison

Considering the nominal operating point, and using the equations stated in SECTION 5.4.1, the theoretical values obtained and the measured values in the simulation will be compared.

The equilibrium point values can be found in TABLE 5.3. It was decided to transport

$P_{dc} = P_r = 1000[\text{MW}]$ of active power. To operate at nominal values, the reactive power was computed such that :

$$Q_r = \sqrt{S^2 - P_r^2} = 348[\text{MVar}] \quad (5.15)$$

The voltage in the Park frame was found using the transformation explained in SECTION 4.1.1 on the transformer voltage. It was assumed that the quadratic component of the voltage is equal to zero as stated before.

Parameters	Value	Unit
V_{1d}	326.6	kV
V_{1q}	0	kV
V_{2d}	326.6	kV
V_{2q}	0	kV
P_r	1000	MW
Q_r	348	MVar
Q_i	348	MVar

TABLE 5.3: Nominal operating point

The comparison of the theoretical values and the simulated values can be found in the TABLES 5.5, 5.6 and 5.7. The base values for the per unit computation can be seen in TABLE 5.4.

S_B	$V_{B,ac}$	$V_{B,dc}$
1059 MVA	333kV	640kV

TABLE 5.4: Per unit base values

Rectifier	V_{rd} (pu)	V_{rq} (pu)	I_{rd} (pu)	I_{rq} (pu)
Computed	0.9357	-0.1647	0.94	-0.3286
Simulated	0.904	-0.724	0.7454	-0.329

TABLE 5.5: Comparison between equations and measurement - Rectifier

Inverter	V_{id} (pu)	V_{iq} (pu)	I_{id} (pu)	I_{iq} (pu)
Computed	1.0643	0.1642	0.9414	-0.3286
Simulated	1.105	0.309	0.91	-0.3

TABLE 5.6: Comparison between equations and measurement - Inverter

DC link	$V_{dc,1}$ (pu)	$V_{dc,2}$ (pu)	P_r (pu)	P_i (pu)
Computed	1	0.9925	0.9443	0.941
Simulated	1	0.9931	0.943	0.9369

TABLE 5.7: Comparison of the DC link values

5.4.3 Graphical Validation

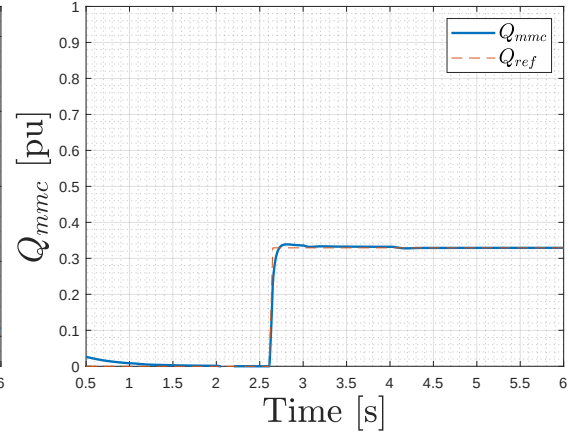
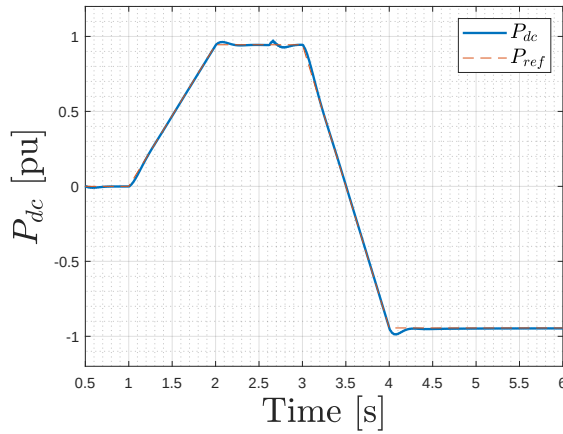


FIGURE 5.6: Active power in the DC link

FIGURE 5.7: Reactive power at station 1

5.4.4 Discussion

For some simulated and calculated values, a difference is observable. This is due to the fact that some elements are present in the simulated model but are not taken into account in the equations. Indeed, two loads are connected in parallel in the simulation and draw currents during the simulations. They have been placed to allow the MATLAB & SIMULINK/SIMSCAPE software to simulate correctly. A second approximation made in the theory is that V_{1q} and V_{2q} are equal to zero. In the simulations, these quadrature components, although close to zero, are not perfectly equal to zero. However, as confirmed in the FIGURE 5.6 and 5.7, the controllers accurately follow the desired references.

For the DC link values in the TABLE 5.7, the small differences between the active powers can be explained by the fact that the calculated values do not take into account the various capacitive and inductive losses of the DC cable, whereas the simulated model has these losses implemented.

Chapter 6

Simulations

In this chapter, simulations will be performed in order to investigate the impact of MMC on the transient stability of electrical power systems. In each section, the method of the simulation will be explained, the results will be displayed and a discussion about the aforementioned results will be made. Each simulation will be performed with using the HVDC link explained in SECTION 5.

For each simulation performed, the controllers of station 1 (rectifier) control the DC voltage of the HVDC line and the reactive power injected or absorbed into the network 1, while the controllers of station 2 (inverter) aim to control the active power transmitted through the HVDC line with the reactive power injected or absorbed into the network 2.

6.1 Stability of HVDC system for a weak grid

When the MMC is connected to an AC grid with a low Short Circuit Capacity (SCC), the simulated model is unstable. One of the main avenue to explore the instability is the way the PLL works when connected to a weaker grid. Indeed, the PLL is crucial for the control of the MMC. An error on its output would skew the control variables and would disrupt the system [48]. To investigate the consequences of a weakening of the grid, multiple AC sources has been connected in parallel in the system, simulating multiple generators. One by one, they will be disconnected by switches, simulating the losses of generators in the AC network. The system implemented can be seen in FIGURE 6.1. TABLE 6.1 gathers the simulation parameters used for this study case.

P_{dc}	Q_c	$S_{cc,max}$	$S_{cc,min}$
1000MW	0 MVar	6.7GVA	2.5GVA

TABLE 6.1: Simulation parameters for grid the weakening study case

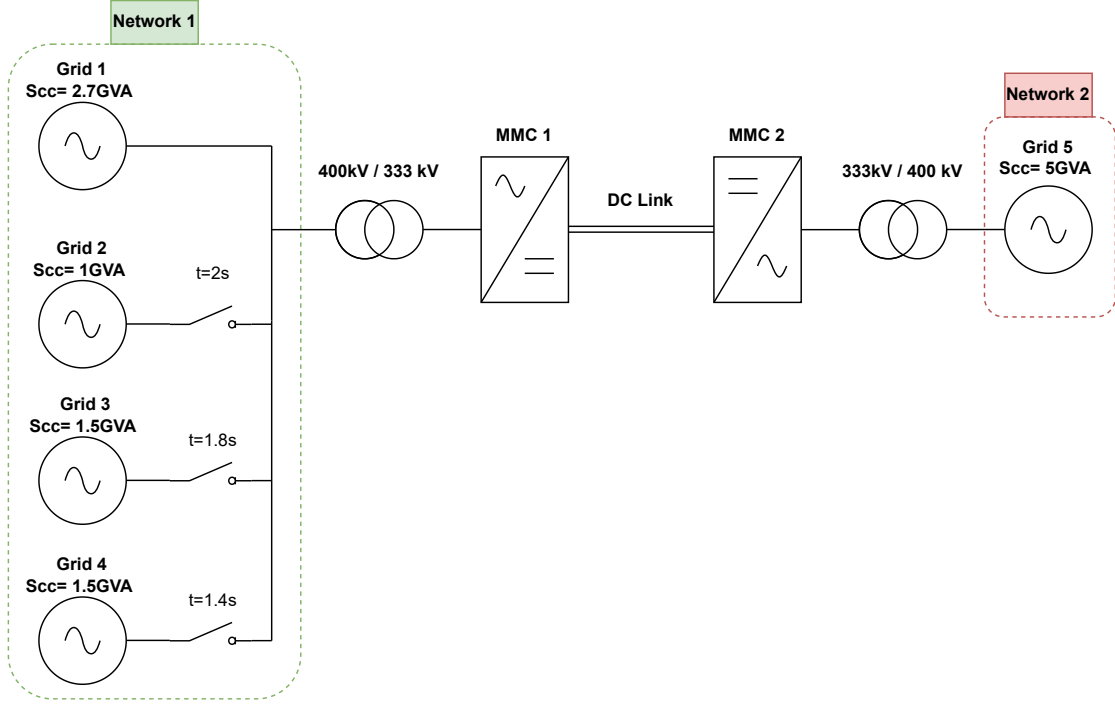


FIGURE 6.1: Schematic of the weakening of the network 1

6.1.1 Results

The limit of stability for the simulated model is $S_{cc} = 2.7[\text{GVA}]$. The short-circuit level is depicted in FIGURE 6.2. In FIGURE 6.5, the RMS AC voltage of the rectifier is slightly decreasing with the losses of generators. As the grid is becoming weaker and weaker, the system is at the limit of becoming unstable. For $S_{cc} = 2.5 [\text{GVA}]$, one can see that the system becomes unstable after the losses of the second to last generator. As depicted in FIGURE 6.4, the frequency tends to deviate from the 50[Hz] as well.

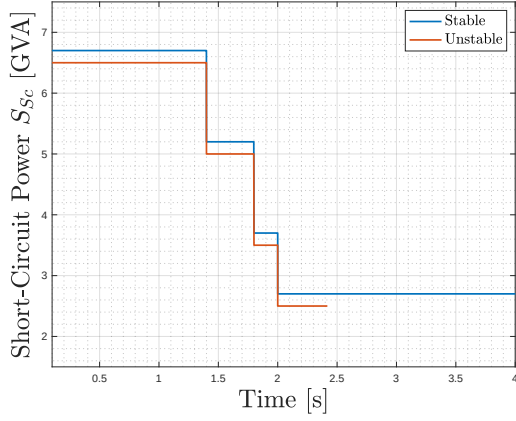


FIGURE 6.2: Short-Circuit Power

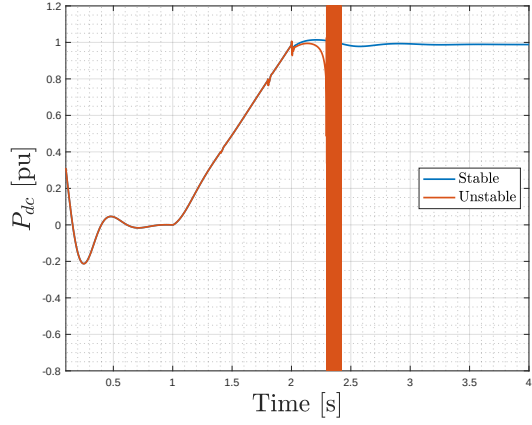


FIGURE 6.3: Transmitted Power

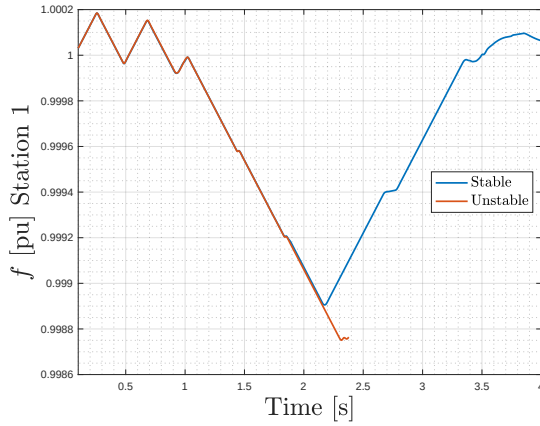


FIGURE 6.4: Frequency Variation

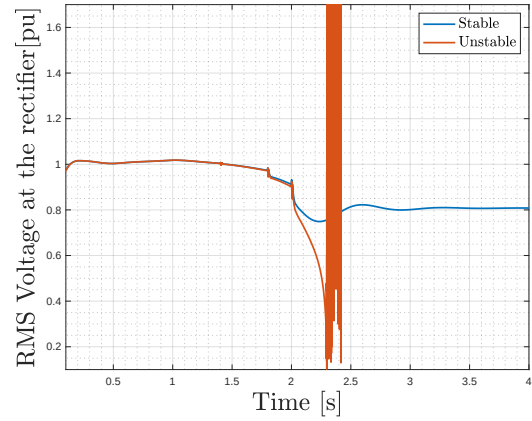


FIGURE 6.5: Voltage Variation

6.1.2 Discussion

The Short Circuit Ratio (SCR) is used to measure the robustness of the grid. It is expressed as [49, 50] :

$$SCR = \frac{S_{cc} - Q_c}{P_{dc}} \quad (6.1)$$

Where S_{cc} is the rated short circuit level of the AC grid, Q_c is the reactive power of the compensators and P_{dc} the rated active power of the MMC-HVDC. It was demonstrated by [51] that for a low SCR, the dominant eigen values of a VSC system would become unstable for a certain value of the PLL controller K_p , creating a *stability limit*. To model the system, they developed a small signal state-space

model using a state vector of 16 dimensions (10 variables for the controllers, and 6 variables for the AC network). In FIGURE 6.6a, the root locus when $SCR = 4$ shows that the dominant poles are stable because the larger goes K_p , the more negative the real part of dominant poles become. However, in FIGURE 6.6b when $SCR = 1.3$, it shows that for a $K_p = 60$, the real part of the complex dominant eigen values of the system becomes positive, and therefore unstable. A low short-circuit ratio limits thus the maximum value K_p of the PLL controller.

Other studies demonstrated that when the SCR decreases, the damping ratio of the secondary-order transfer function of the PLL will drop. During transient in an AC network with low SCR values, the damping ratio can become negative [52]. If the damping ratio drops below zero, the complex dominant eigen values of the system become positive, and the system is unstable as stated above. But even for damping ratio equal to a small positive value, the PLL can lose synchronisation [53]. The lower limit value of the damping ratio which preserves the stability of the PLL can be found between 0 and 0.2 [52, 54]. The limit brought by the damping ratio is called the *performance limit*. The performance limit requires a higher minimal SCR than the stability limit. As it was explained by [54], for a transmission of $P = 1000[\text{MW}]$ and $Q = 0[\text{MVar}]$, the stability limit of the system is $S_{cc} = 1.2[\text{GVA}]$ (thus $SCR = 1.2$), and the performance limit is $S_{cc} = 1.8[\text{GVA}]$ (thus $SCR = 1.8$).

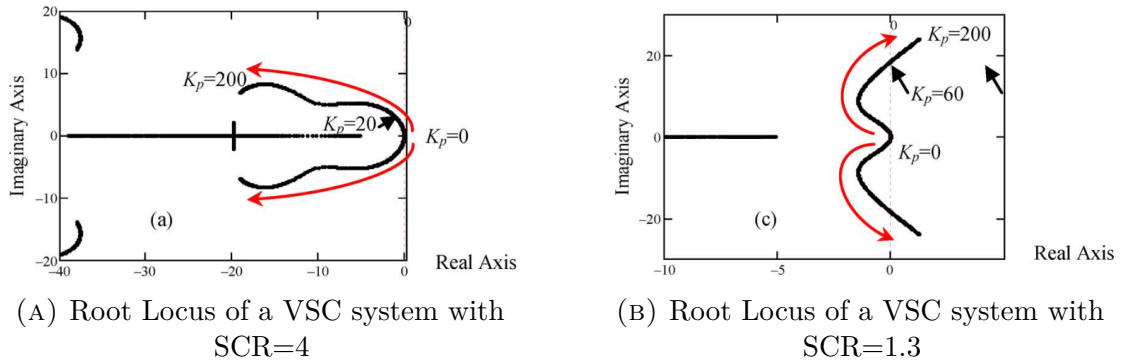


FIGURE 6.6: Root Locus with $K_{p,PLL}$ varying from 0 to 200 with two different SCR [51]

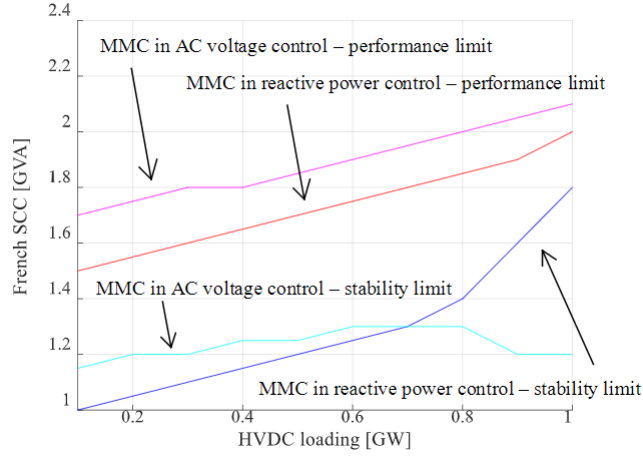


FIGURE 6.7: Minimal S_{CC} needed in function of the HVDC active power transmitted [54]

In conclusion, the limit of the simulated model in this work highlighted in Figures 6.3 and 6.5 might be due to the instability of the PLL for low SCR values. The higher value of the minimal SCR simulated ($SCR = 2.7[\text{GVA}]$) can be explained because the K_p value of the PLL controller of the model was set to be $K_p = 180$, which is a relatively high value when the PLL is connected to a weak grid.

6.2 Transient stability : Power Reversal

To simulate the impact that the active power flow has on the grid, a power reversal will be simulated by changing the active power reference. The system simulated is depicted in FIGURE 6.8. As stated in SECTION 5.1, station 2 controls the active power exchanged in the DC link. The initial point is set at $P = 1000[\text{MW}]$ transmitted from station 1 to station 2 (as depicted in FIGURE 6.9). At $t = 3[\text{s}]$, the power reversal is performed during $0.5[\text{s}]$. After the inversion, $P = 1000[\text{MW}]$ is transferred from station 2 to station 1. During the whole reversal process, the reactive power of each station is set to $Q = 0[\text{MVar}]$.

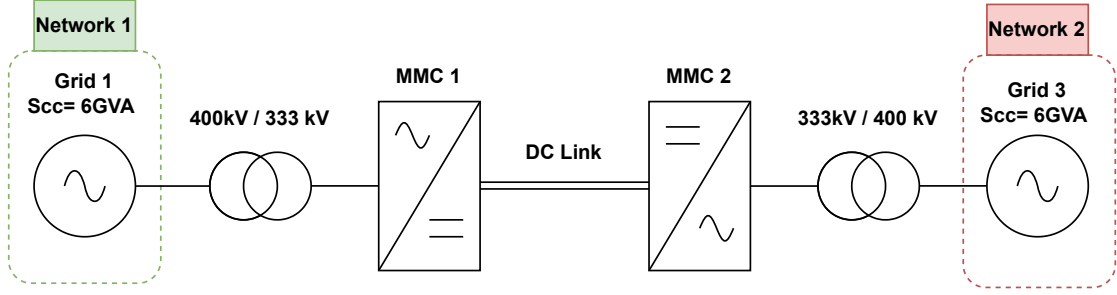


FIGURE 6.8: Schematic of system simulated

6.2.1 Results

Quantities observable on the DC side

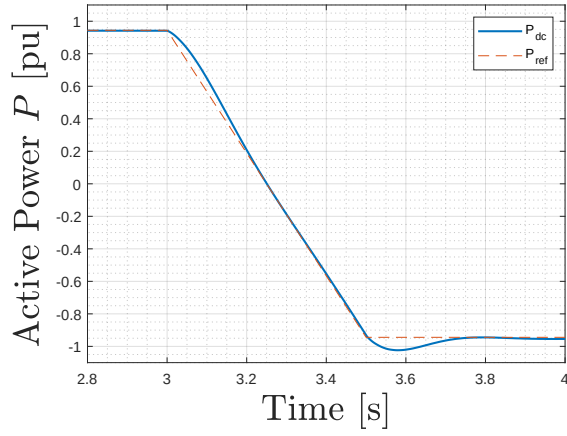


FIGURE 6.9: Active power in the DC link

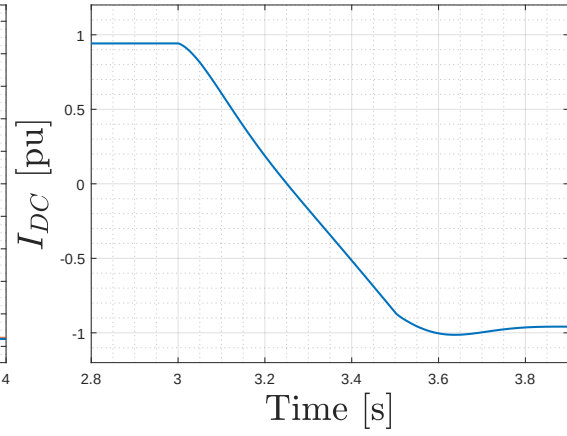


FIGURE 6.10: DC Current in the DC link

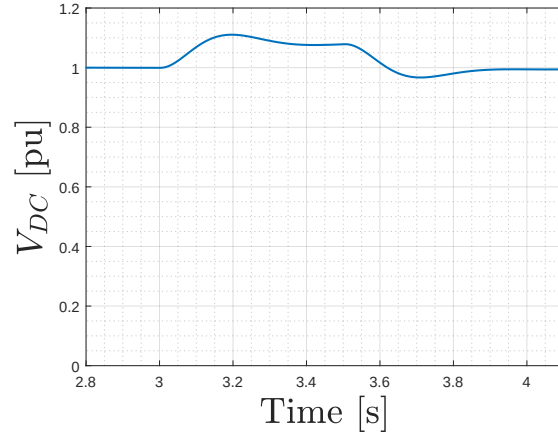


FIGURE 6.11: DC Voltage in the DC link

Quantities observable on the AC side

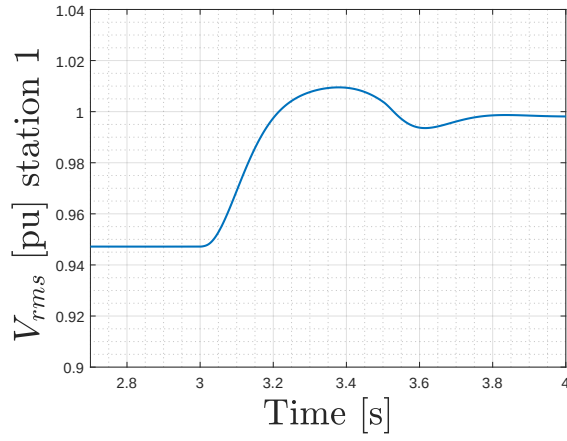


FIGURE 6.12: AC voltage at PCC of station 1 during power reversal (RMS)

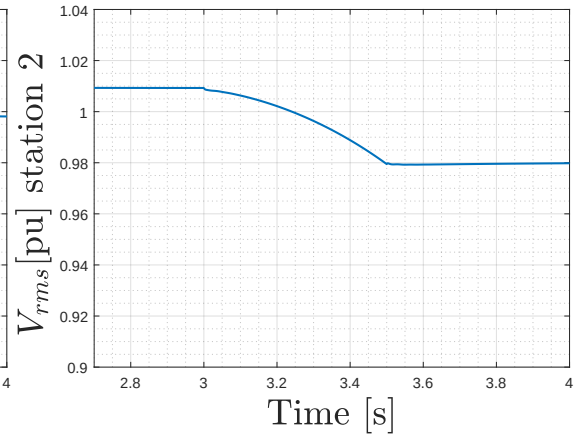


FIGURE 6.13: AC voltage at PCC of station 2 during power reversal (RMS)

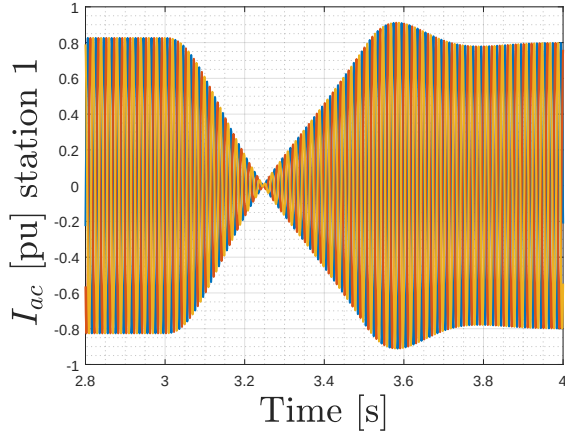


FIGURE 6.14: AC current at PCC of station 1 during power reversal

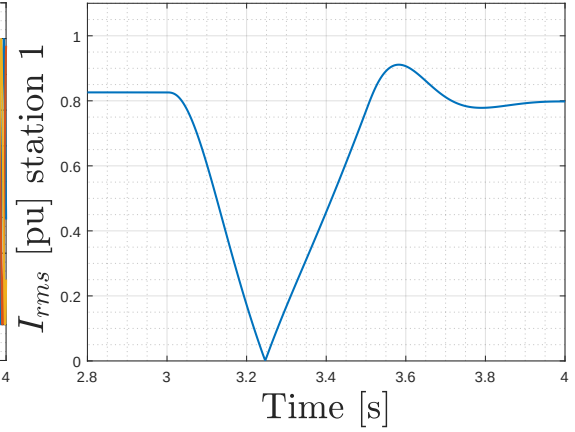


FIGURE 6.15: AC current at PCC of station 1 during power reversal (RMS)

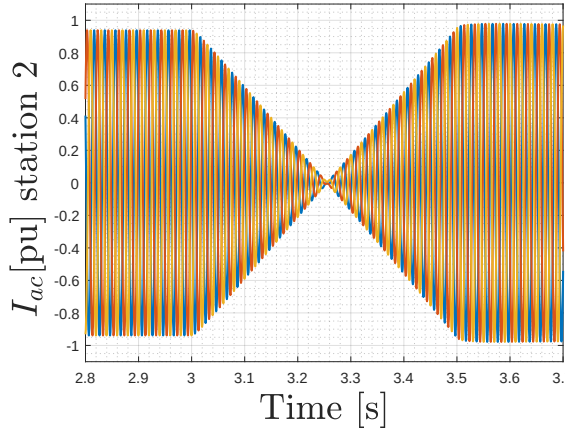


FIGURE 6.16: AC current at PCC of station 2 during power reversal

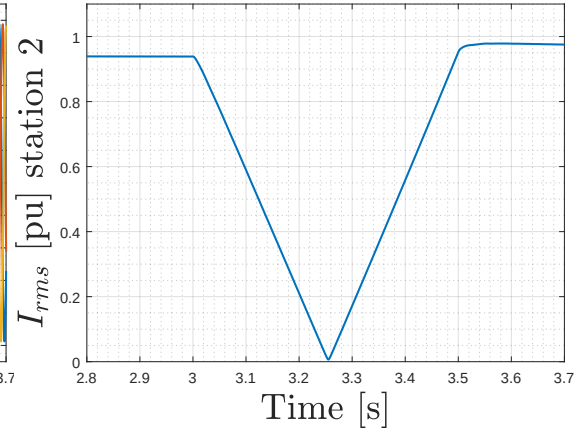


FIGURE 6.17: AC current at PCC of station 2 during power reversal (RMS)

6.2.2 Discussion

The system simulated can handle a power reversal quickly. The inversion is done in 500 [ms] and the active power transmitted becomes stable at $t = 3.7$ [s]. Indeed, the system is moving to a stable steady-state where the observable quantities are not subject to other variations. The extra 200[ms] is the time needed for the controllers to reach the reference values.

In practice, because the power flow can be reversed a few times per day, it is important to be able to change the direction of the active power transported in

the DC-link without creating a lot of transients on the AC side. In FIGURE 6.12, 6.13, the AC voltage is stable shortly after the end of the power flow inversion. It confirms the reliability of the MMC for power reversal. To compensate the voltage drop at station 2, a change of the reactive power set point could be done [31].

In FIGURE 6.11, an overvoltage of 10% can be observed during the reversal. This overvoltage must be acceptable for both the DC cable and the IGBT in the arms of the converter. It is acceptable according to the datasheet of the DC cable [44, 45] and for the IGBT of the arms, according to ABB's datasheet for *StakPak IGBT Module* [55]. The overvoltage could be drastically reduced by increasing the time of the reversal. In FIGURE 6.18, the power reversal lasts 2[s] instead of the previous 0.5[s] and the overvoltage is reduced to 3%.

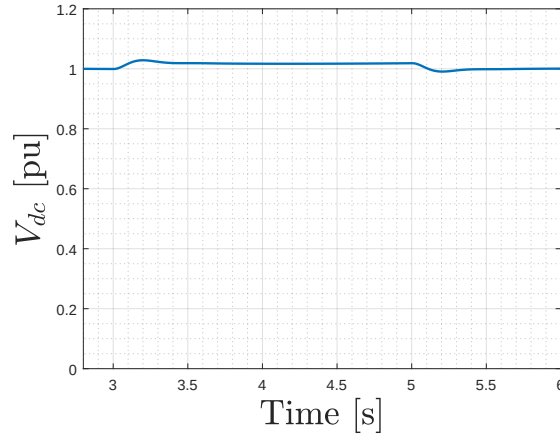


FIGURE 6.18: DC Voltage in the DC link for a 2 [s] power reversal

6.3 Transient stability : Three-phase fault

To investigate the interactions between an HVDC link and the electrical grid under a fault, two AC-sources has been connected in parallel and are feeding the MMC rectifier station. A three-phase fault is then introduced in one of the line between the transformer's primary voltage and the grid at 2.6[s]. The line is then opened at 2.8[s] to clear the fault. The representation of this configuration can be seen in FIGURE 6.19.

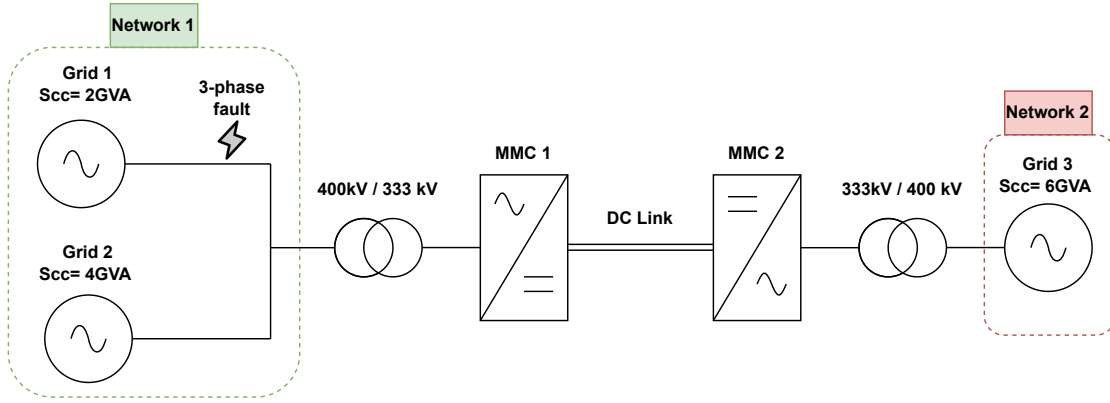


FIGURE 6.19: Configuration of the three-phase fault

6.3.1 Requirements : fault-ride-through capability of an HVDC station

The fault-ride-through profile of an HVDC converter station is depicted in FIGURE 6.20. It represents the evolution of the minimum voltage at the connection point given by *ENTSO-e* [56]. The HVDC is asked to be able to sustain such minimum voltages.

The fault represented in FIGURE 6.20 starts at $t_{fault} = 0[s]$. U_{ret} is the retained voltage at the connection point during a fault, t_{clear} is the moment at which the fault is cleared, U_{rec1} specifies the lower limit of the voltage recovery of the fault at moment t_{rec1} . Similarly, the lower limit of the voltage is up to U_{rec2} after t_{rec2} . The voltage U_{block} is the voltage at the connection point under which the HVDC is allowed to stay connected to the network but with no active nor reactive contribution, until the voltage comes back to a higher value. U_{block} is specified by the *TSO* [56]. The range of parameters that must be considered by the *TSO* can be found in TABLE 6.2.

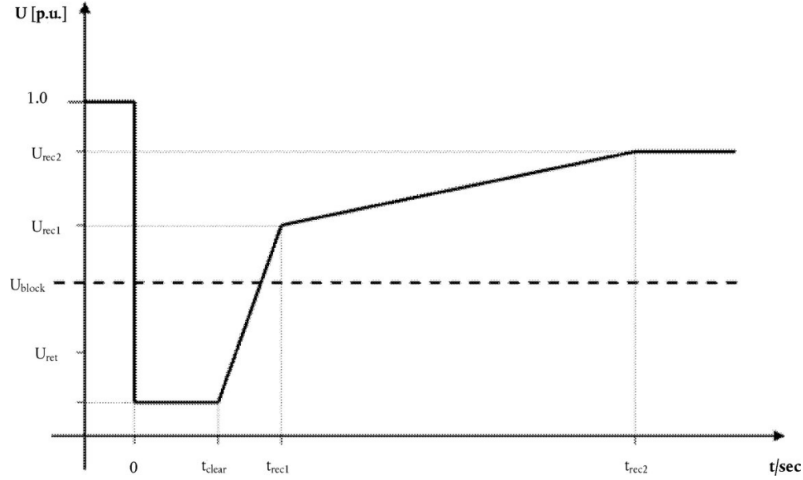


FIGURE 6.20: Fault-ride-through profile of an HVDC converter station [56]

Voltage parameters [pu]		Time parameters [seconds]	
U_{ret}	0 - 0.3	t_{clear}	0.14 - 0.25
U_{rec1}	0.25 - 0.85	t_{rec1}	1.5 - 2.5
U_{rec2}	0.85 - 0.9	t_{rec2}	$t_{rec1} - 10$

TABLE 6.2: Parameters for the fault-ride-through capability curve of an HVDC converter station [56]

6.3.2 Control strategy during the three-phase fault

Two control strategies will be explained in this section. The first one is an original strategy developed in this work to sustain a three-phase fault and in the mean time to transport an active power through the DC link during the fault. This strategy implies that a constant voltage measurement at the PCC of both stations is performed. When the retained voltage U_{ret} is dropping between $0.2[pu] < U_{ret} < 0.3[pu]$ at one of the PCC, the station situated near the fault will need to produce enough reactive power to support the faulted voltage. In the meantime, the station controlling the active power of the link will reduce the reference of the active power. The reduction of active power is needed for two reasons. The first one is to stay within the capability curve if the reactive power needed is high. The second one is to protect the IGBT of the MMC from too high arm fault currents.

A reaction time of 10[ms] after the fault was considered [57]. Once the fault is cleared, the control system will get back to the initial set-point values. The reference of active and reactive powers when $0.2[pu] < U_{ret} < 0.3[pu]$ can be seen in FIGURE

6.21, 6.22. For the voltage values below the threshold of $U_{block} = U_{ret} = < 0.2[pu]$, the control strategy is to block the MMC and therefore to produce neither active nor reactive power during the fault.

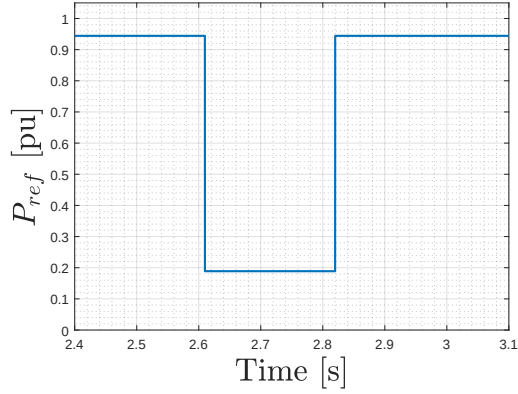


FIGURE 6.21: Active power reference signal, reduced during the fault

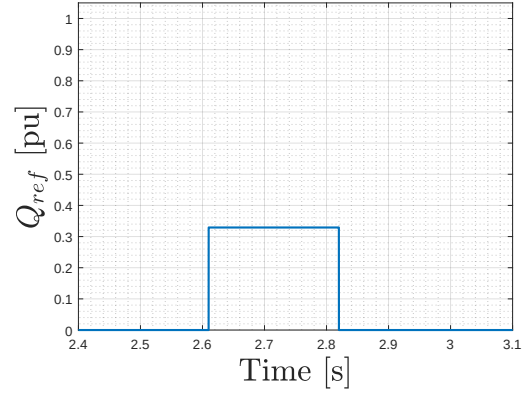


FIGURE 6.22: Reactive power reference signal, increased during the fault

A second control strategy is proposed when the retained voltage drops below $U_{ret} < 0.2[pu]$. This strategy is the most classical and is often used by HVDC stations. The MMC will be blocked and both active and reactive power will be set to 0 during the fault. Similarly to the first strategy, after the fault is cleared, the set points of the power are set back to their previous values.

6.3.3 Results for $U_{ret} \geq 0.2[pu]$

Quantities observable on the AC sides

In FIGURE 6.23, 6.24, the fault happens at 2.6[s] and the AC voltage drops to $U_{ret} = 0.2[pu]$. The fault is cleared $t_{clear} = 0.2[s]$ later. One can observe that, depending on the reactive power, the AC voltage during the fault are different. For the same amount of active power exchanged ($P = 0.75[pu]$) and a high enough reactive power, the AC voltage is stable while for a low reactive power, the AC voltage is fluctuating a lot and is about to collapse. The high active power reference was chosen for these two figures only, to exacerbate the collapse. The other figures are simulated with a $P_{ref} = 0.18 [pu]$.

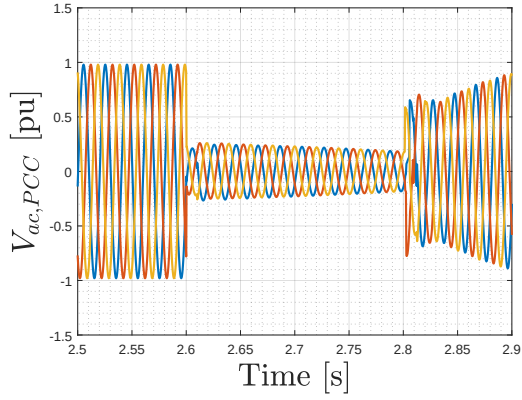


FIGURE 6.23: AC voltage at PCC during the three-phase fault when $P = 0.75[\text{pu}]$ and $Q = 0.33[\text{pu}]$

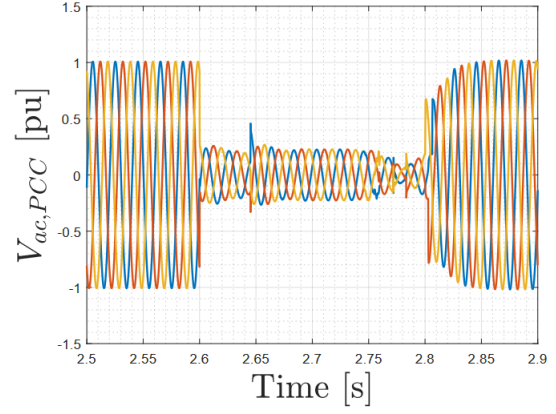


FIGURE 6.24: AC voltage at PCC during the three-phase fault when $P = 0.75[\text{pu}]$ and $Q = 0.14[\text{pu}]$

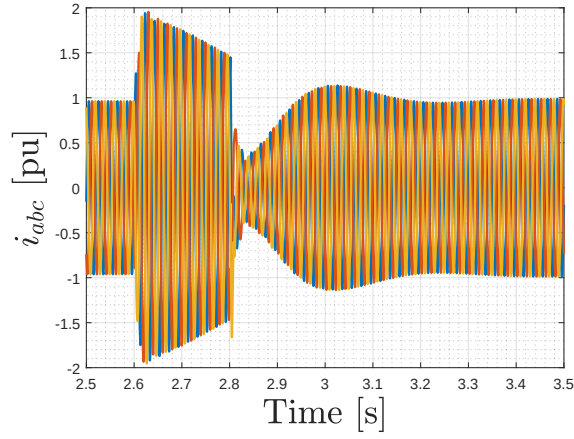


FIGURE 6.25: AC current at rectifier PCC during the three-phase fault with $P = 0.19 [\text{pu}]$

Reactive power

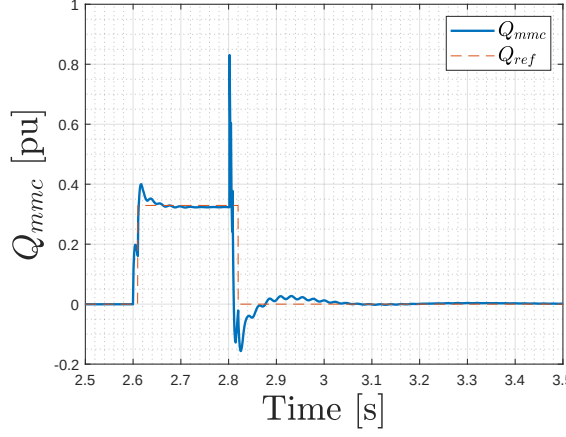


FIGURE 6.26: Reactive power at station 1 with the reference value

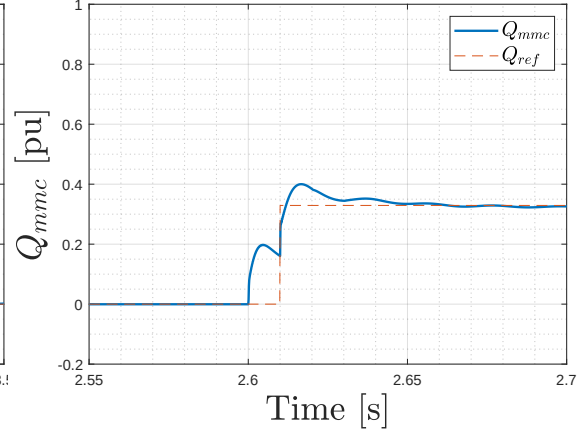


FIGURE 6.27: Reactive power at station 1 - Zoom on the fault time

Quantities observable on the DC side

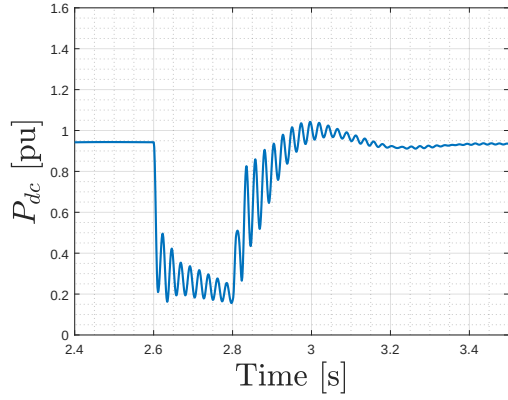


FIGURE 6.28: DC power transmitted from station 1 to the station 2 with $P = 0.19$ [pu]

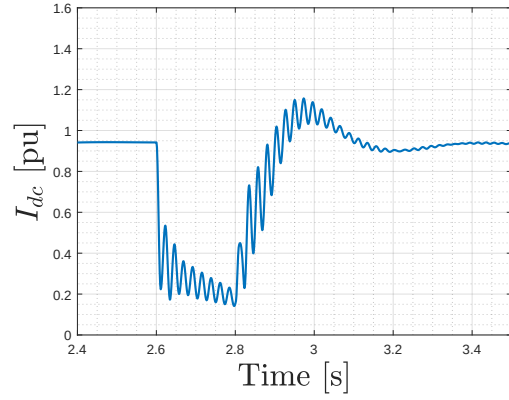


FIGURE 6.29: DC current at DC link during the three-phase fault with $P = 0.19$ [pu]

Arm currents

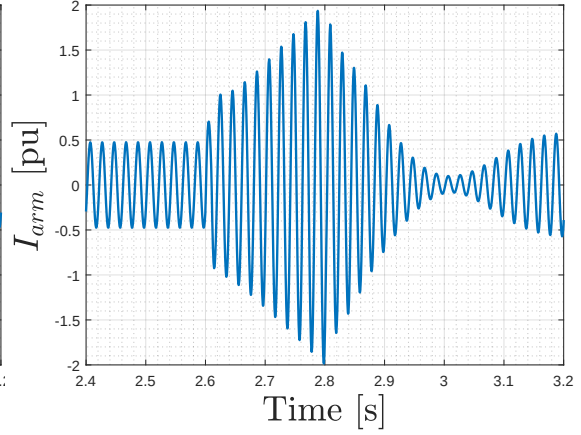
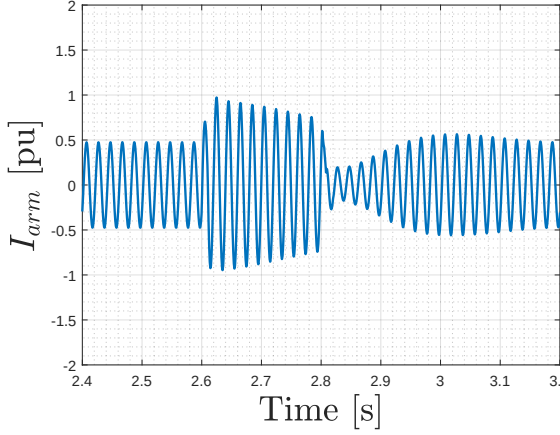


FIGURE 6.30: Arm current in phase A, FIGURE 6.31: Arm current in phase A, with $P=0.18[\text{pu}]$ with $P=0.75[\text{pu}]$

6.3.4 Discussion for $U_{ret} \geq 0.2[\text{pu}]$

Control of reactive power

In FIGURE 6.23, 6.24, it was observed that a minimum amount of reactive power produced by the MMC was needed to sustain the fault while transmitting a lot of active power ($P = 0.75 [\text{pu}]$). In fact, the reactive power produced acts like an energy reserve that provides voltage support during the fault, improving the grid voltage stability [58]. To be able to provide sufficient reactive power, the active power transported in the DC link may need to be reduced to stay in limit of the power capability curve.

The MMC could be very useful in the context of voltage fluctuations and voltage stability because it provides a rapid reactive power regulation. Indeed, the reactive control has a very rapid response time [58]. In FIGURE 6.27 the simulated model confirmed that observation. A few milliseconds after the fault, $Q = 0.33[\text{pu}]$ could be generated by the MMC station to support the voltage.

Actually in practice, the owner of the HVDC system must specify its reactive power capability to the relevant TSO in the context of varying voltage. The HVDC system has to be able to provide reactive power, even when it runs at its maximum active power transmission capacity [56]. It could therefore help the TSO to quickly provide or consume reactive power when it is necessary

When the fault is cleared, there is a peak appearing at 2.8[s] in the produced reactive power as seen in FIGURE 6.26. This can be explained by the sudden increase in the

voltage due to the clearing of the fault, as represented in FIGURE 6.32. This sharp rise in the voltage creates an instability in the values of the dq0-reference frame that are fed to the controllers. As an example, the q-component of the voltage is depicted in FIGURE 6.33. This instability can be due to the PLL that tries to synchronise with an unstable system. The instability lasts $\approx 12[ms]$ after the clearing of the fault, between between 2.801 and 2.813 [s]. After this time, the dq0-components of the voltages and the currents are back to more stable values and are not subjects to other variations, besides a change in the reference values of the controllers. The exact same reasoning can be expressed to explain the increase of reactive power at the fault time $t = 2.6[s]$ in FIGURE 6.27.

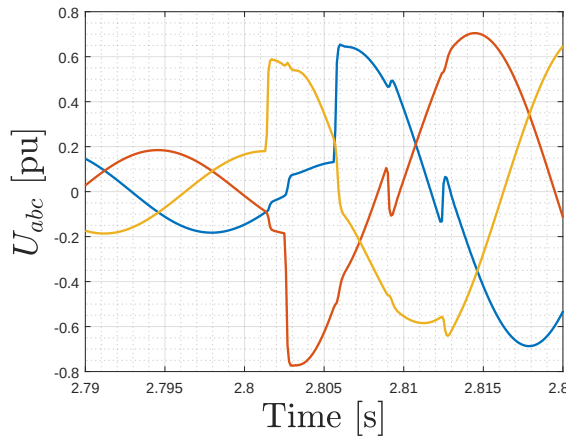


FIGURE 6.32: Three-phase voltage at the PCC of station 1

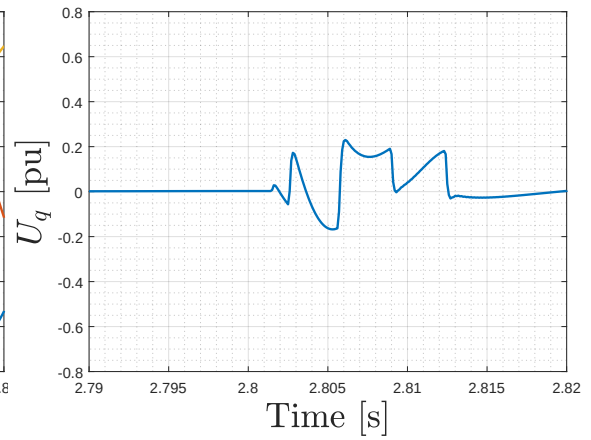


FIGURE 6.33: Q component of the voltage at the PCC of station 1

The DC current and DC power have an overshoot when the fault is cleared and the reference values are set back to the initial set-point values. This overshoot in the DC current is at the limit of acceptable values for the cables ($I_{DC,max} = 1.15[pu]$) [44, 45]. To avoid this overshoot, the return to the initial set-point reference could be done under the form of a ramp, instead of the step used in this simulation depicted in Fig.6.21. It will ensure a smoother transition after the fault.

Control of active power

While it is possible to transmit active power through the HVDC link during a fault when $U_{ret} > 0.2[pu]$, it is important to look after the arm currents of the station situated near the faulted network during the fault. Indeed, the short circuit currents can rapidly become very important and flow through the MMC, causing damage to the IGBTs. FIGURE 6.30, 6.31 show that the arm currents

can rise quickly to high unacceptable values for the arms if the transmitted active power is high during a fault. According to the IGBT's datasheet, the collector current can go up to $I_c = 2000[\text{A}]$ ($0.77[\text{pu}]$) and can support a peak collector current of $I_c = 4000[\text{A}]$ ($1.54[\text{pu}]$) during 1 [ms] [55]. The simulation in FIGURE 6.30 showed that a transmission of active power of $P = 0.19[\text{pu}]$ is acceptable for the arms of the MMC situated near the faulted network if such IGBTs are chosen.

To handle the fault, the station controlling the active power (done by station 2 in the simulated model) must detect when the fault occurs. It has to reduce the reference value of active power in order to protect the IGBTs in the arms of the MMC. A proposed strategy to effectively detect a fault on the other side of the link would be to measure the DC current of the DC link. Indeed, when a fault occurs, the sudden drop of AC voltage leads to a drop in power transmitted at the faulted station. This leads to a drop in the DC current as depicted in FIGURE 6.29.

6.3.5 Results for more severe fault ($U_{ret} < 0.2[\text{pu}]$)

As explained in SECTION 6.3.2, for more severe faults, it is necessary to block the MMC in order to survive from an AC voltage drop close to $U_{ret} = 0[\text{pu}]$. When the AC voltage at the PCC drops below the threshold $U_{block} = 0.2[\text{pu}]$, the second control strategy will be used and the power controllers will both set the active and reactive values to $P_{ref} = Q_{ref} = 0[\text{pu}]$ during the fault.

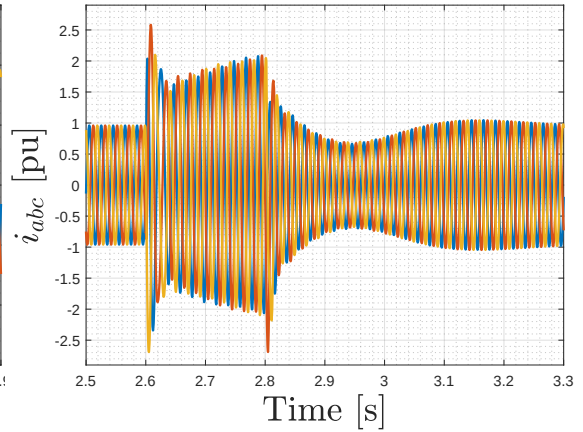
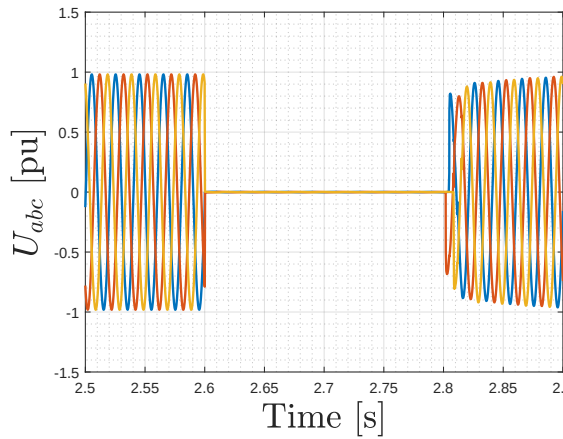


FIGURE 6.34: AC voltage at station 1 PCC during the severe three-phase fault FIGURE 6.35: AC current at station 1 PCC during the severe three-phase fault

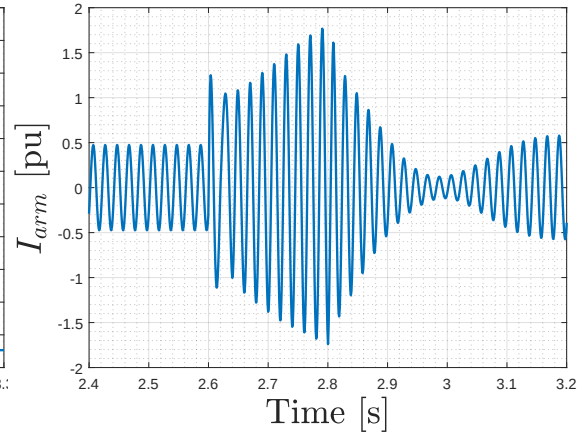
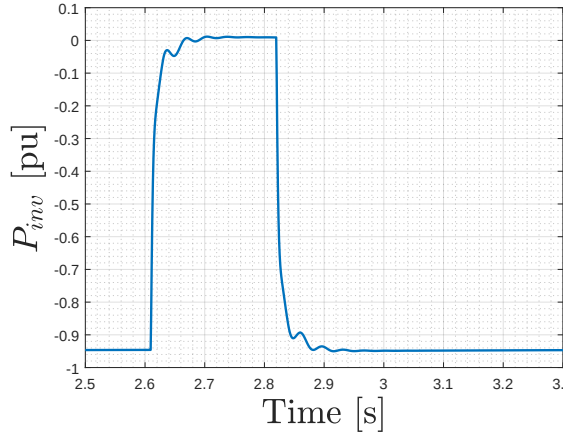


FIGURE 6.36: Active power at station 2 FIGURE 6.37: AC arm current in phase A during the severe three-phase fault

6.3.6 Discussion when $U_{ret} \approx 0$

When the residual voltage $U_{ret} > 0.2[\text{pu}]$, it was still possible to transmit active power during the fault without damaging the arms of the converter if the active power was reduced. However, if the residual voltage drops too low, it is necessary to block the MMC during the fault to avoid damage on the IGBTs because of the excessive fault currents [59]. When the MMC enters in the "blocked" state where no power is transmitted, the faulted currents will not flow through the IGBTs. It was verified by the simulated model that the arm currents become very high during a fault for a very low residual voltage, as represented in FIGURE 6.37.

It is also important to have a fast reaction time to detect the fault in order to block the MMC on the right time. The fault currents quickly rises to $1.25[\text{pu}]$ after the fault, which is close to the peak collector current of $1.54[\text{pu}]$ [55], and would quickly rise to higher values if the active power reference is still high during the fault.

6.4 Connection of a synchronous generator : Interaction with the electrical grid

To deepen the investigation of the impact of an HVDC link using MMC on the transient stability of the electrical power system, a synchronous generator has been connected in parallel to the AC sources which represent the electrical power systems grid. This section aims to understand how does the MMC influence or change the dynamic behaviour of the synchronous machine when the active power transferred

by the MMC is changed. The representation of the simulated configuration is depicted in FIGURE 6.38.

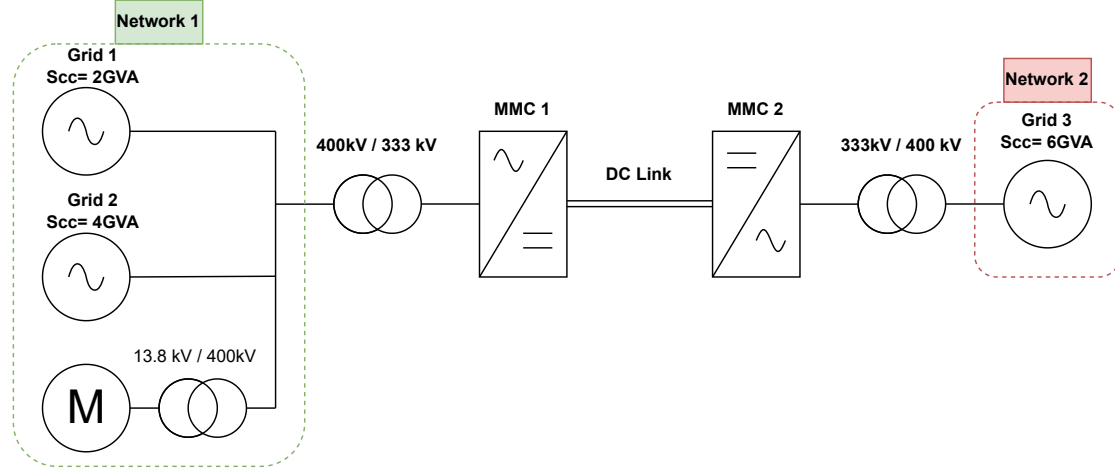


FIGURE 6.38: Schematic with the synchronous machine

6.4.1 Synchronous generator parameters

The synchronous generator connected in parallel represents a production unit with the size of a nuclear power plant or a gas turbine. The nominal power of the connected synchronous generator is equal to $P = 500[\text{MW}]$. The synchronous generator excitation system is the *IEEE ST1A* with a constant stator reference voltage. This excitation system is part of a class of fast static excitation systems and represents systems in which the excitation power is supplied through a transformer from the generator terminals and is regulated by a controlled rectifier [60]. In order to vary the active power produced by the generator, a ramp profile for the mechanical power has been implemented. It will increase the power produced by $\pm 10\%$ from the initial value without using turbine or governor block. Further synchronous generator parameters are gathered in TABLE 6.3. The synchronous machine is acting such as a *PV* node whereas the AC sources are in swing and *PV* node configuration.

Nominal Volt.[kV]	Freq.[Hz]	Inertia Coef.[s]	Poles pair	Type
13.8	50	2	20	Salient pole

TABLE 6.3: Parameters of the synchronous machine

6.4.2 Results

Both the active and reactive powers are following a ramp at 1 s and 0.5 s respectively in order to reach $\simeq -0.56$ [pu] and $\simeq -0.82$ [pu]. The mechanical power of the synchronous generator is increased at 6[s] from 0.9 to 1 [pu] and from 1 to 0.8 [pu] at 10 [s]. The required active power in the DC link is equal to $P_{dc} = 600$ [MW]. The reference set points are summarised in FIGURE 6.39. The results of the simulation are depicted in the different FIGURE 6.40, 6.41 and 6.42. The "Grid 1" and "Grid 2" refer to the two voltage sources that represent the AC network, as depicted in FIGURE 6.38.

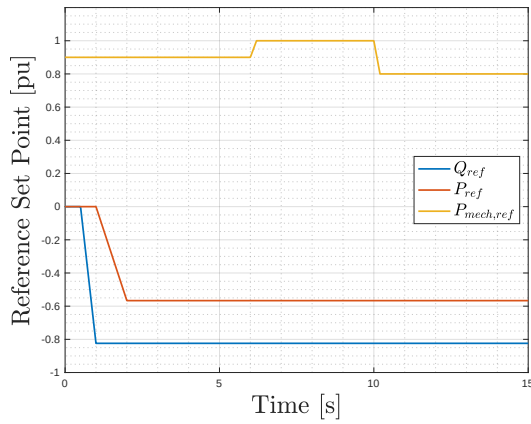


FIGURE 6.39: Reference set points of the simulation

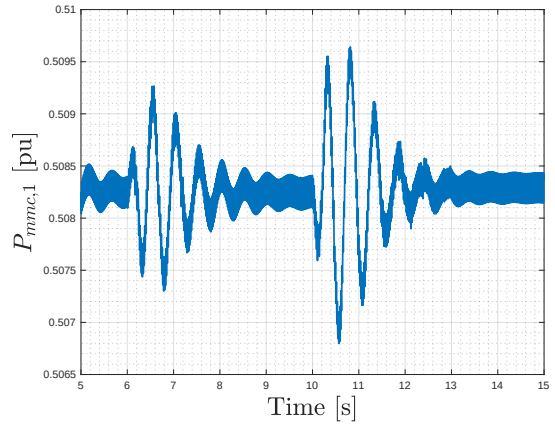


FIGURE 6.40: Active Power at the MMC 1

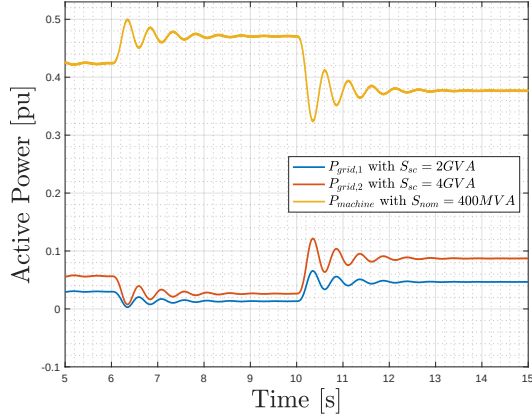


FIGURE 6.41: Active power from the synchronous machine and the grid AC sources

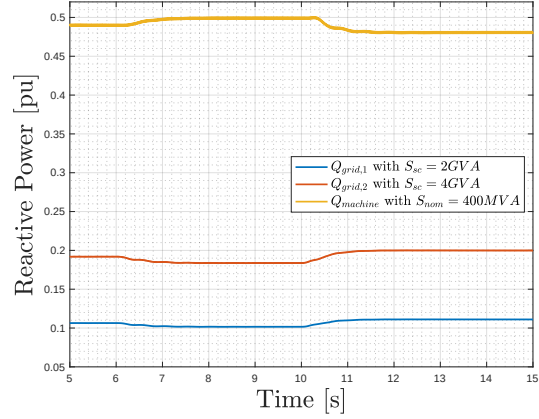


FIGURE 6.42: Reactive power from the synchronous machine and the grid AC sources

6.4.3 Discussion

As mentioned previously, the goal was to analyse the interaction between the MMC and the synchronous generator when a transient is introduced. For this study case, the transient is an increase/decrease of the mechanical power of the synchronous machine and takes place at 6[s] and 10[s]. As depicted in FIGURE 6.40, the active power absorbed by the MMC 1 is slightly perturbed by the transient of the synchronous generator. However, the amplitude of the oscillation is quite small ($\pm 1.5 \times 10^{-3}$ [pu]) and is then negligible. On the primary side of the transformer, one can notice that the increase of the mechanical power increases the active power generated by the synchronous machine. Therefore, the AC source representing the grid have to compensate this increase of active power. This is observable in FIGURE 6.41 where both AC sources work hand by hand in order to adjust the injected amount of active power. It is also notable that when one grid is stronger than the other, this last will contribute more to the compensation than the weaker grid. In the simulation, this is modelled throughout the Short-Circuit Capacity of the AC source.

6.5 Variation of the injected reactive power from the MMC

In this section, the impact of the variation of reactive on the transient of the synchronous generator will be analysed. The transient of the synchronous machine will be introduced through the variation of the mechanical power of the synchronous machine as depicted in FIGURE 6.43. The contribution of active power during the simulation is done by two AC sources and by the synchronous machine. They are able to transfer throughout the HVDC link, a constant amount of active power equal to 0.94[pu]. Finally, three different reference set points for the reactive power have been studied and are represented in FIGURE 6.44. The distance between the synchronous machine and the MMC is equal to 1 [km] and the rated power of the machine is equal to 500[kV]. The simulated situation is depicted in FIGURE 6.38.

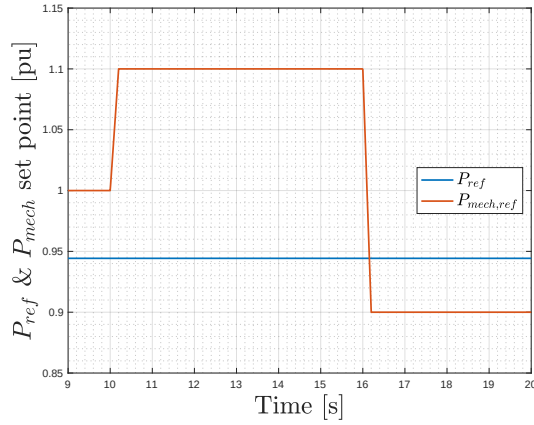


FIGURE 6.43: Mechanical Power and Active Power set point

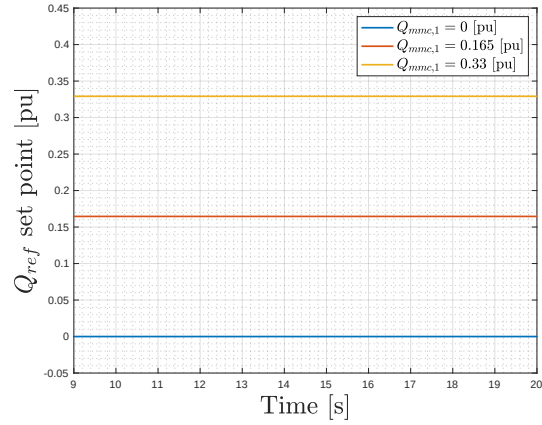


FIGURE 6.44: Reactive Power set point

6.5.1 Results

Electrical quantities observable

The active power produced by the synchronous generator is depicted in FIGURE 6.45. The RMS value of the AC voltage at the PCC on the station 1 is also represented in FIGURE 6.46. The reactive power consumed by the machine is shown in FIGURE 6.47 and the current flowing out the machine can be seen in FIGURE 6.48. Finally, the load angle is represented in FIGURE 6.49.

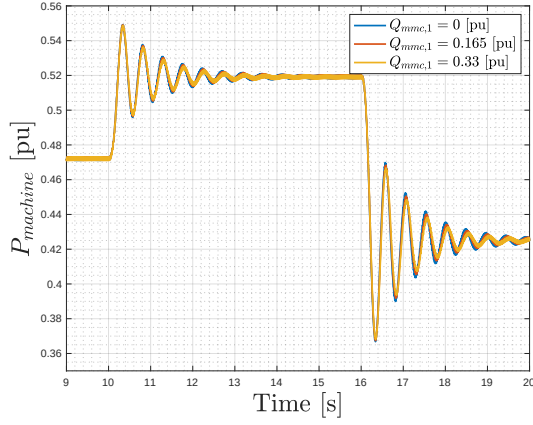


FIGURE 6.45: Active power output of the machine with different reactive powers from the MMC

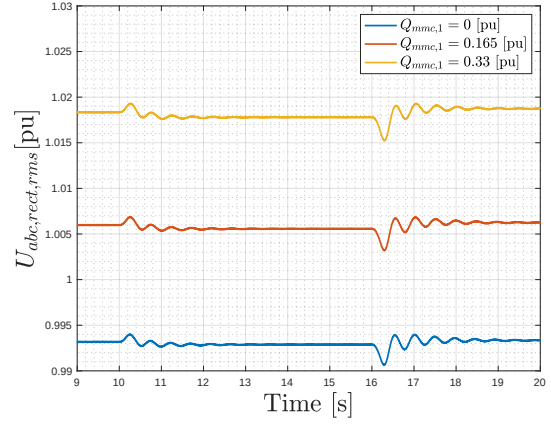


FIGURE 6.46: RMS AC voltage at the PCC of station 1

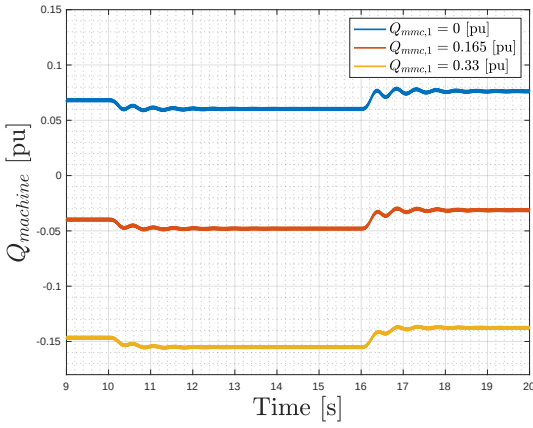


FIGURE 6.47: Reactive power consumed by the machine

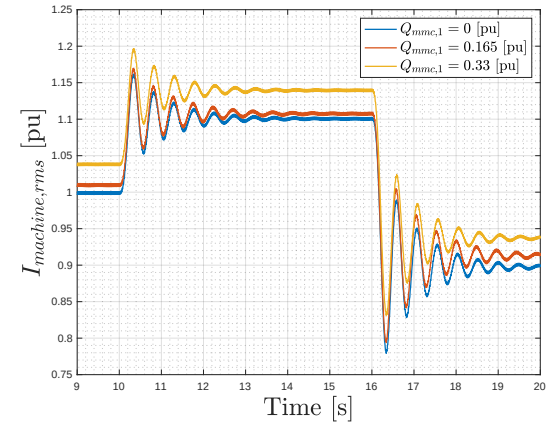


FIGURE 6.48: RMS AC current of the machine with different reactive powers from the MMC

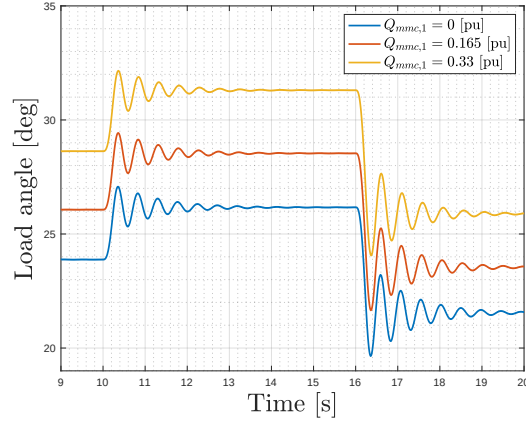


FIGURE 6.49: Load angle of the machine with different reactive powers from the MMC

Mechanical quantities observable

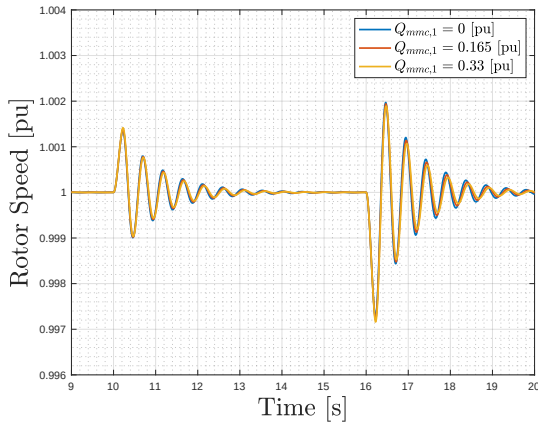


FIGURE 6.50: Rotor Speed of the machine with different reactive powers from the MMC

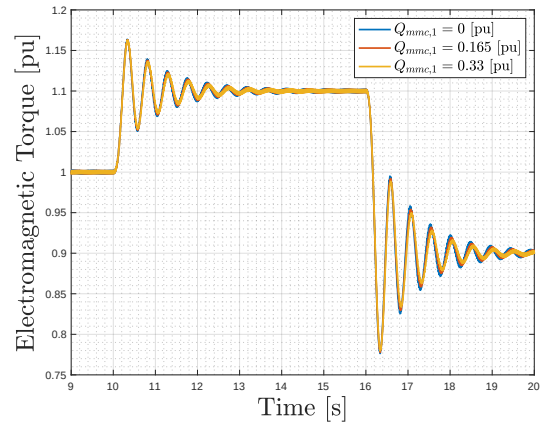


FIGURE 6.51: Electromagnetic Torque of the machine with different reactive powers from the MMC

6.5.2 Discussion

As depicted in FIGURE 6.49, the load angle of the machine naturally increases with the reactive power injection from the MMC while the transient time become smaller. Furthermore, as depicted in FIGURES 6.50 and 6.51, the variation of the reactive power does not have a major impact on the mechanical quantities of the machine.

It is due to the fact that only a small transient is induced here (small variation in the mechanical power of the machine) which is less severe than a three-phase fault (cfr 6.7). The rotor speed of the machine naturally oscillates when the transient takes place but the amplitude is small. Concerning the electromagnetic torque, it is quite similar in the three cases. However, the transient time is reduced with the injection of the reactive power from the MMC.

In conclusion, the reactive power produced by the MMC have an minor impact on the dynamic behaviour of the synchronous machine in case of small disturbances such as mechanical power variation.

6.6 Synchronous generator distance variation from the MMC

The variation of the distance between the synchronous generator and the MMC has been studied in this section. As for the previous SECTION 6.5, the transient is introduced by increasing and decreasing the mechanical power of the synchronous generator as depicted in FIGURE 6.52. The reference active power transmitted throughout the HVDC line is equal to 0.85[pu] whereas the reactive power is equal to 0.52[pu]. The distance has been chosen respectively to 1,30,60 and 90 [km] from the MMC station. The situation is depicted in FIGURE 6.38.

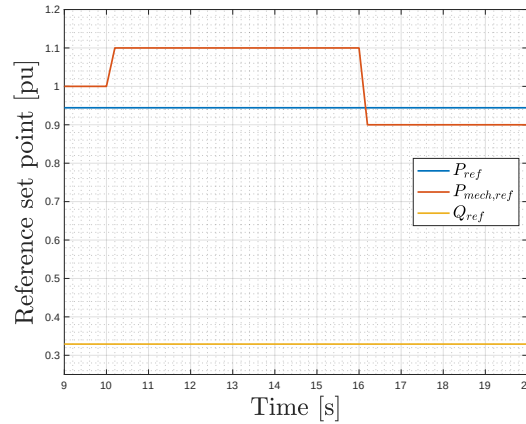


FIGURE 6.52: Reference set points for Q, P and P_{mech}

6.6.1 Results

The active power produced by the synchronous generator and transmitted in the DC link are depicted in FIGURE 6.53 and 6.54. The RMS currents of the machine

and the RMS voltage of the rectifier are shown in FIGURE 6.55 and 6.56.

Electrical quantities observable

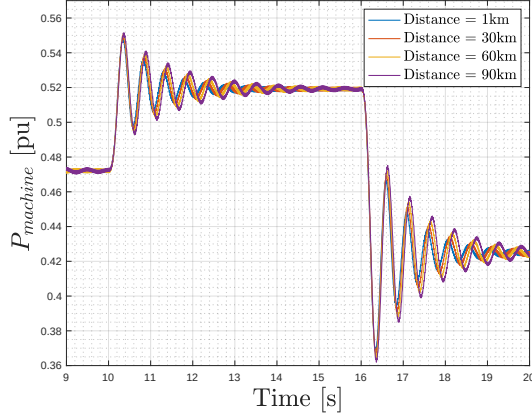


FIGURE 6.53: Active power output of the machine with varying distance and constant Q from the MMC

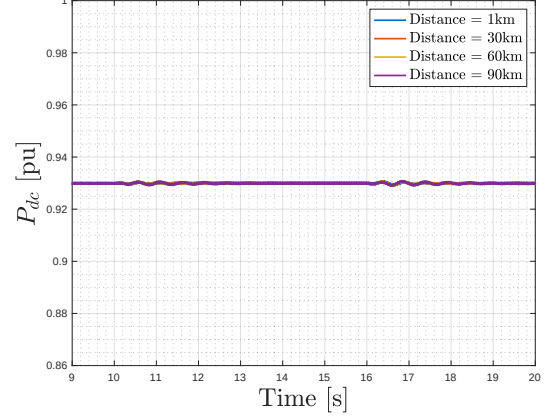


FIGURE 6.54: DC active power transmitted in the DC link

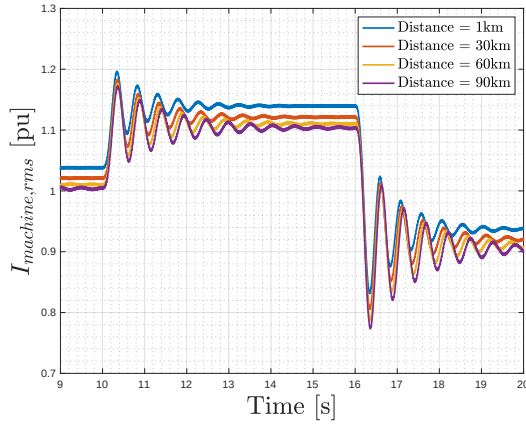


FIGURE 6.55: RMS AC currents of the machine with varying distance and constant Q from the MMC

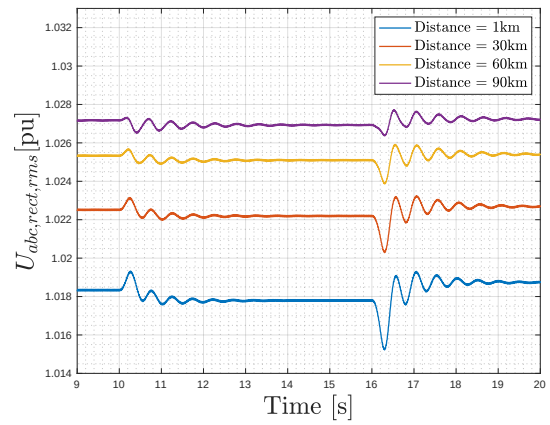


FIGURE 6.56: RMS AC voltage at the PCC of station 1

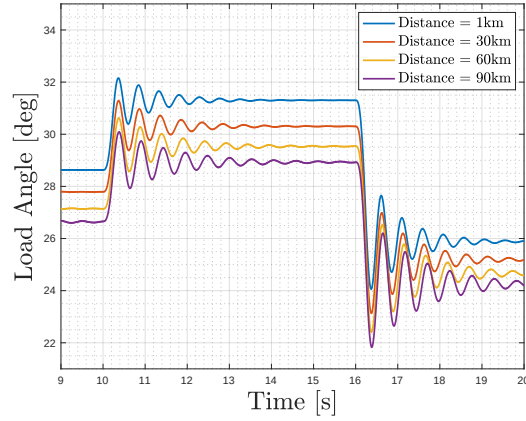


FIGURE 6.57: Load angle of the machine with varying distance and constant Q from the MMC

Mechanical quantities observable

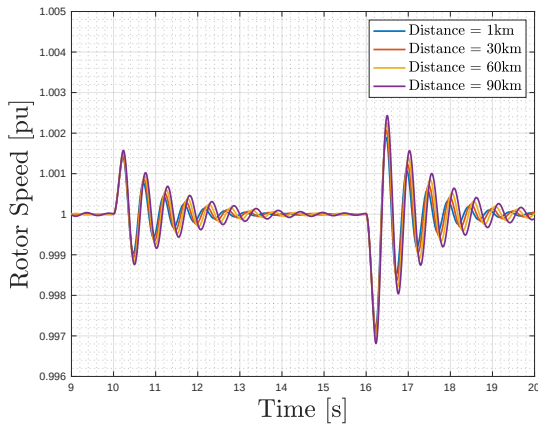


FIGURE 6.58: Rotor Speed of the machine with varying distance and constant Q from the MMC

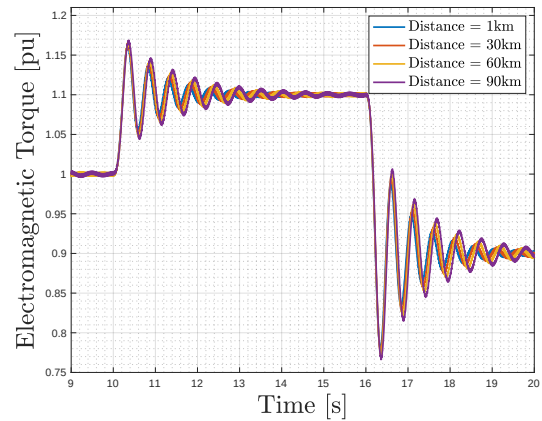


FIGURE 6.59: Electromagnetic Torque of the machine with varying distance and constant Q from the MMC

6.6.2 Discussion

The oscillations after the transients seem to increase when the distance between the synchronous machine and the MMC is increased, as depicted in [FIGURE 6.53](#). In [FIGURE 6.56](#), the RMS AC voltage at the PCC is on the contrary increasing with the distance of the converter. When the distance between the generator and the

MMC increases, the impedance of the line increases as well, and thus the currents will decrease with the distance according to Ohm's law. However, the variation of the distance of the generator does not have a big influence on the MMC. It is confirmed by FIGURE 6.53, where the active power transmitted in the DC link is not changing a lot. The mechanical quantities depicted in FIGURES 6.58 and 6.59 also show that the dynamic behaviour of the machine is improved when it is closer to the MMC. The load angle is also stabilising quicker (see in FIGURE 6.57).

6.7 Three-Phase Fault with a synchronous generator

In order to see if the presence of the MMC can be an opportunity for enhancing the transient behaviour of the synchronous machine, a three-phase fault is introduced between the first generator and the transformer, as represented in FIGURE 6.60. Two different remaining voltages will be studied : $U_{ret} \approx 0.5[\text{pu}]$ and $U_{ret} \approx 0.2[\text{pu}]$.

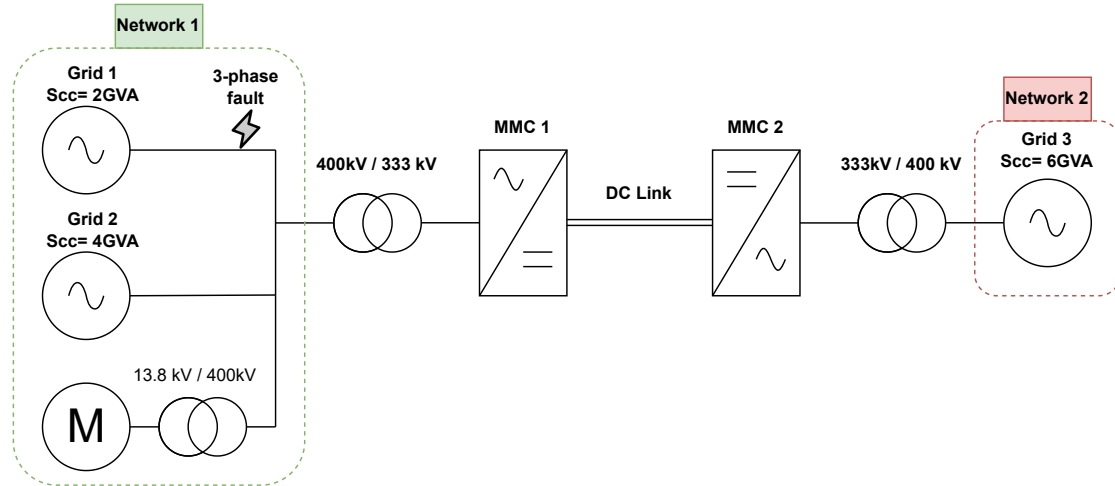


FIGURE 6.60: Schematic with the synchronous machine and the three-phase fault

6.7.1 Three-phase fault with a synchronous generator and $U_{ret} \approx 0.5$

The distance between the MMC and the fault is set to 70[km]. As a consequence, the remaining voltage is $U_{ret} \approx 0.5[\text{pu}]$, as depicted in FIGURE 6.61. The fault occurs at $t = 7[\text{s}]$ and is cleared at $t = 7.4[\text{s}]$ in the simulation.

Control Strategy

Two different strategies will be simulated. The first one is the classical strategy of a constant $\cos \varphi$, with $P_{ref} = 0.94[\text{pu}]$ and $Q_{ref} = 0.33[\text{pu}]$. Following the equation of AC power factor :

$$pf = \cos \varphi = \frac{P}{|S|} = \frac{P}{\sqrt{P^2 + Q^2}} \quad (6.2)$$

$$= \frac{0.94}{\sqrt{0.94^2 + 0.33^2}} = 0.9435 \quad (6.3)$$

The second strategy is to block the MMC, with $P_{ref} = 0 [\text{pu}]$ and $Q_{ref} = 0[\text{pu}]$. The blocking of the MMC will mean that the converter is not helping the machine anymore during the fault time.

For the synchronous machine, it can be noted that no control system is implemented to protect the machine from the fault currents. It is relevant to physical synchronous machines as they are generally not protected, unless by circuit breakers for faults occurring close to the terminals of the machine.

Results

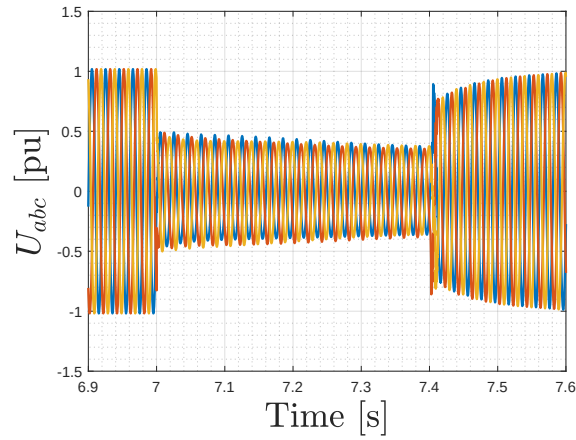


FIGURE 6.61: AC voltage at station 1 PCC during the fault

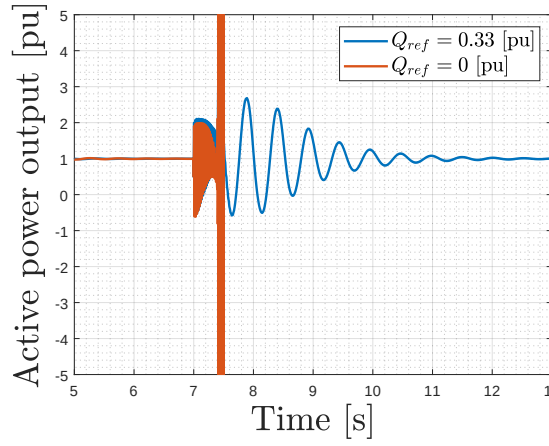


FIGURE 6.62: Active power output of the synchronous machine

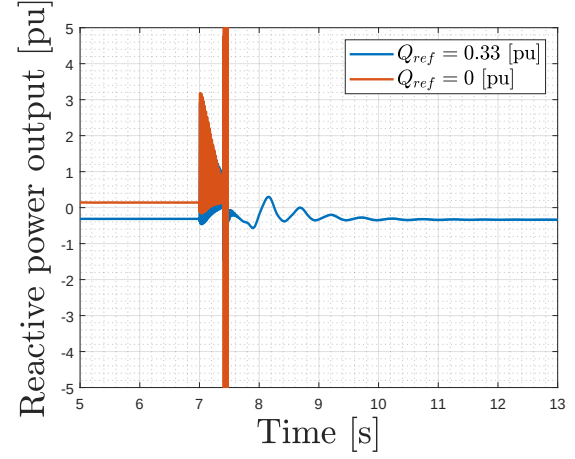


FIGURE 6.63: Reactive power output of the synchronous machine

Mechanical quantities observable

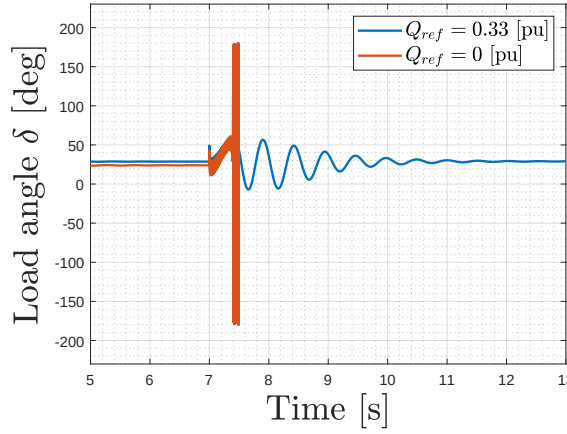


FIGURE 6.64: Load angle with 2 different reactive powers from MMC

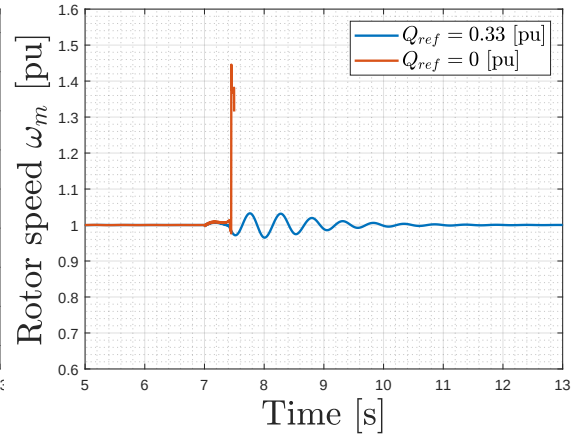


FIGURE 6.65: Rotor speed with 2 different reactive powers from MMC

DC quantities observable

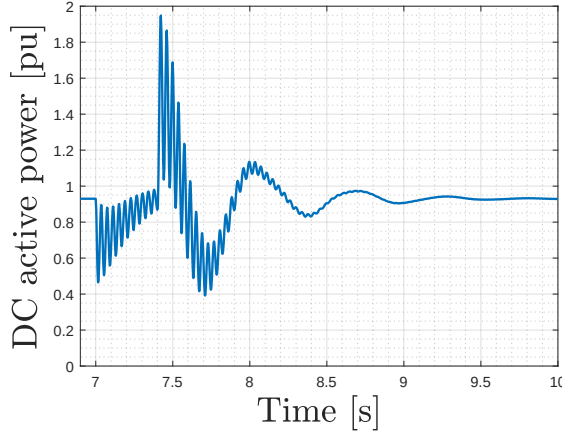


FIGURE 6.66: DC power transmitted from station 1 to the station 2

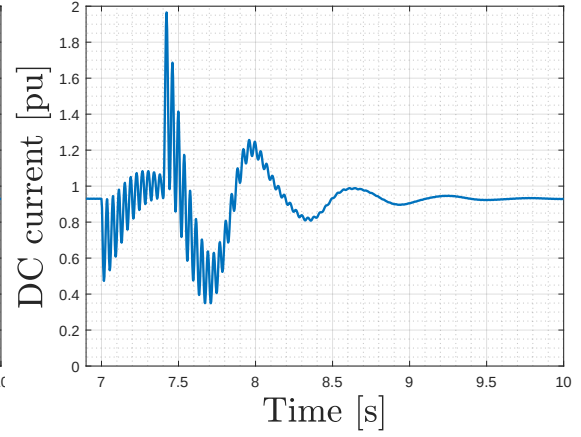


FIGURE 6.67: DC current at DC link during the three-phase fault

Arm currents

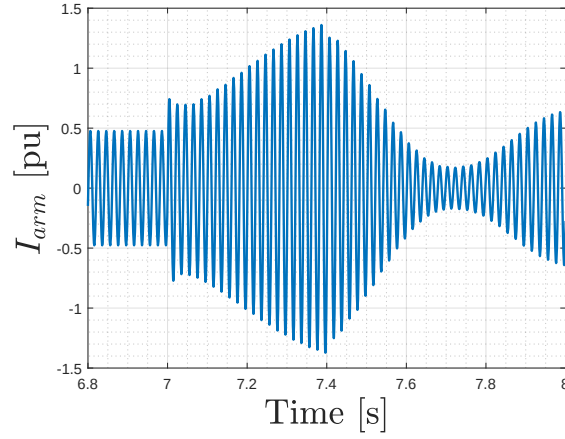


FIGURE 6.68: Arm current in phase A, with $P=0.94[\text{pu}]$ and $Q=0.33[\text{pu}]$

Discussion

The transient stability of the synchronous machine is its capacity to maintain synchronism during disturbances [61]. It can be evaluated with the angle δ , the angle between the terminal voltage and the internal voltage of the synchronous machine. Following a large disturbance, large variations of the rotor angle δ will occur. A stable system will, after the perturbation, see its angle δ pass through a maximum, then oscillate and reach a stable value. An unstable system will have an angle δ that continues to increase, which means that the system has lost the synchronism with the network [62]. In FIGURE 6.64, the phenomenon of the increase of the rotor angle δ and the subsequent loss of synchronism has been illustrated when the MMC is not generating reactive power.

The power of the machine can be expressed as :

$$P = \frac{E \cdot V}{X_s} \sin \delta \quad (6.4)$$

Where E is the internal voltage of the generator, V the terminal voltage, X_s the synchronous reactance of the machine and δ the load angle. Using EQUATION 6.4, it can be said that if the angle δ is very unstable as depicted in FIGURE 6.64, the power will be unstable. This is confirmed in FIGURE 6.63. When the fault is cleared at $t=7.4[s]$, the power fluctuates a lot.

However, when the MMC provides a reactive power, it allows the machine to maintain the synchronism with the network. The behaviour of a stable system is illustrated in FIGURE 6.64, where the angle δ oscillates and becomes stable after 5 [s]. Once the load angle δ is stable, the other mechanical values are also stable. The equilibrium value of the angle δ is kept away from $\delta = 90^\circ$, known as the critical stability point, to bring a margin of stability to the electrical system [63]. In conclusion, the MMC can provide reactive power during a fault, acting like a Static Var Compensator (SVC). It will increase the critical fault elimination time, which is "the maximum time the fault can last without compromising the system's ability to return to equilibrium" [61].

During the fault, the arm currents of the MMC are acceptable according to the IGBT datasheet [55], as depicted in FIGURE 6.68. However, the DC values of the transmitted power and the current reach unacceptable values after the fault has been cleared with the cable used [44, 45]. Therefore, a reduction of the reference active power should be considered, after the elimination of the fault. In the same way as in the SECTION 6.3.4, the station controlling the DC active power can measure the DC current. If it becomes too high, a reduction of the active power reference can be performed to ensure the safety of the DC components. As the control of active power is decoupled from the reactive power control, the reduction of the active power will not have any impact on the control of reactive power

and the discussion in this section regarding the reactive power support during the three-phase fault remains valid.

6.7.2 Three-phase fault with a synchronous generator and $U_{ret} \approx 0.2$

In this section, the configuration of FIGURE 6.60 does not change. A more severe fault will be analysed. The remaining voltage is $U_{ret} = 0.2[\text{pu}]$. The distance between the fault and the MMC is $30[\text{km}]$. The fault is introduced at $7[\text{s}]$ and is cleared after $200[\text{ms}]$. Two control strategies have been used to analyse the transient behaviour of the synchronous machine.

Control strategy

The strategies will be the same as the one explained in SECTION 6.3.2. In the first strategy, the active power reference will be reduced to decrease the arm currents and therefore to protect the IGBTs. It will be set back to its initial set-point value after the fault. Unlike the SECTION 6.3, the reactive power is injected before the fault to simulate a voltage support from the MMC. The second control strategy will be to block the MMC during the fault, thus setting $P_{ref} = Q_{ref} = 0$.

Results

The electrical and mechanical quantities observable on the AC side are depicted in the following figures¹.

¹ $Q_{ref,fault}$ and $P_{ref,fault}$ are representing the reactive and active power set point during the fault

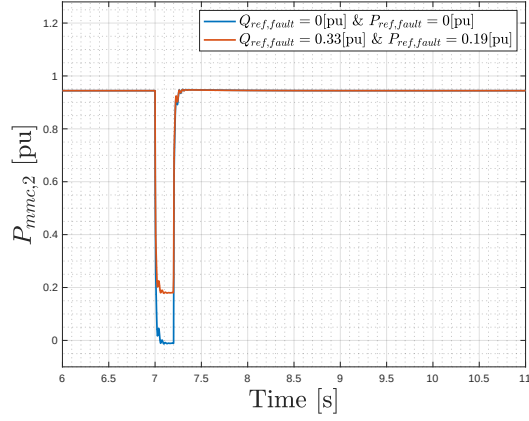


FIGURE 6.69: Active power measured at station 2

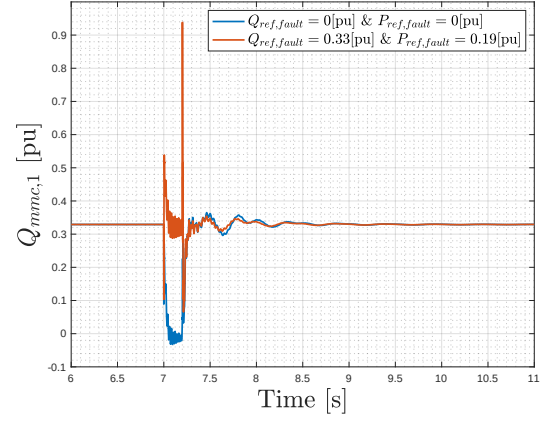


FIGURE 6.70: Reactive power measured at the PCC

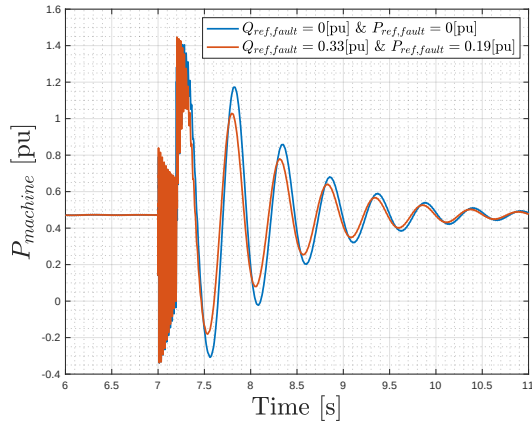


FIGURE 6.71: Active power of the synchronous generator

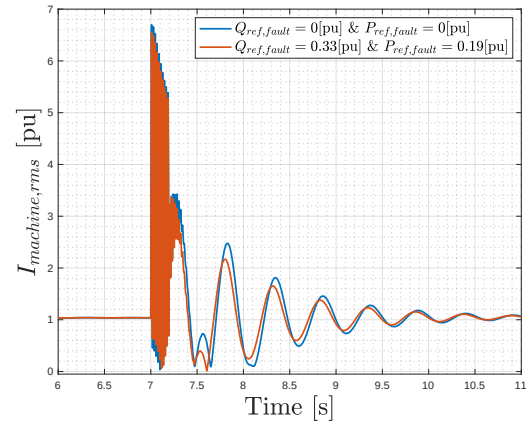


FIGURE 6.72: Currents of the synchronous machine during the fault

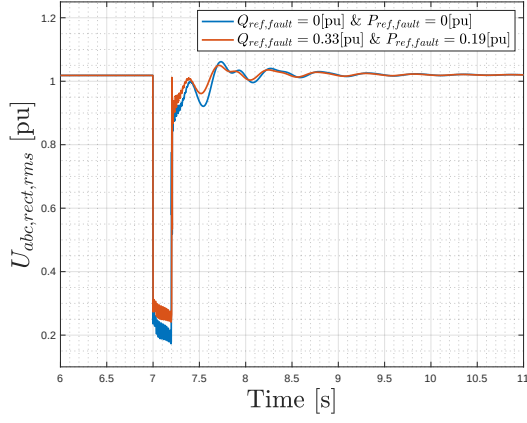


FIGURE 6.73: RMS Voltage at the PCC of station 1

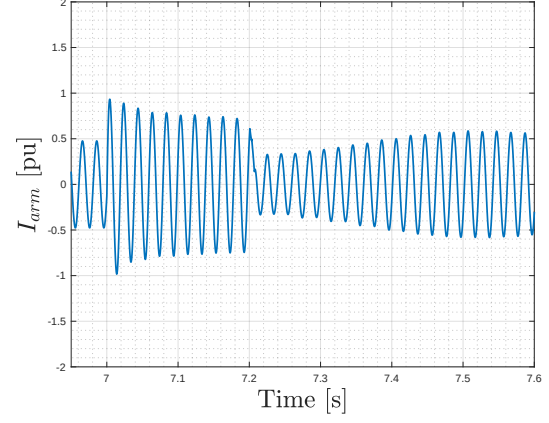


FIGURE 6.74: Arm current with P control to 0.18[pu] during fault

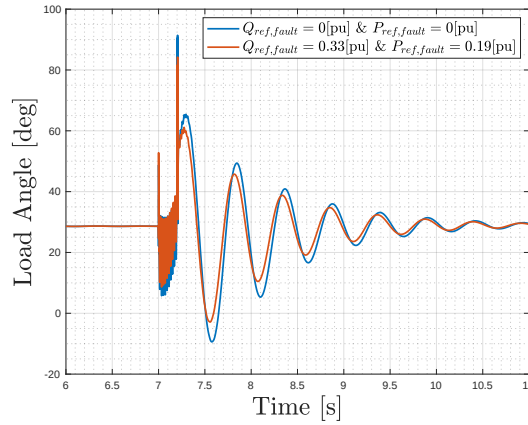
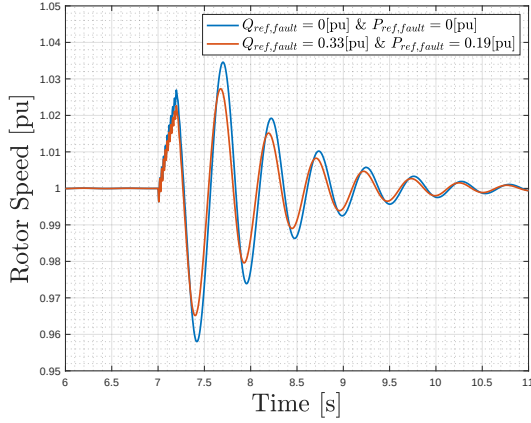
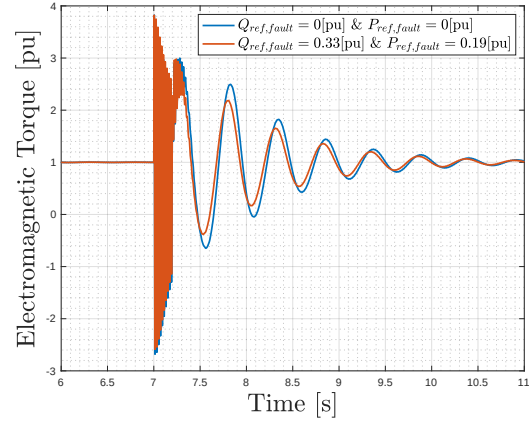


FIGURE 6.75: Load angle during the fault $U_{ret} = 0.2[pu]$


 FIGURE 6.76: Rotor speed during the fault $U_{ret} = 0.2[pu]$

 FIGURE 6.77: Electromagnetic Torque during the fault $U_{ret} = 0.2[pu]$

Discussion

The synchronous generator has a slower transient dynamic than an ideal AC source, which is expected and confirmed by FIGURE 6.71 ($t_{transient} > 4[s]$). The slower transient dynamic has an impact on the time needed to recover from the fault. In FIGURE 6.73, the voltage takes a few seconds to fully return to nominal values, while a simulation without a synchronous machine would see its voltage reverts to nominal values in less than half a second (as depicted in FIGURE 6.23). The transmitted power by the machine in FIGURE 6.71 has oscillations peak at high values. It is explained by the oscillations depicted in FIGURE 6.75, representing the load angle. Indeed, following the EQUATION 6.4, the variation of the load angle directly impacts the active power.

It is depicted in FIGURE 6.76 that without any reactive supply from the MMC (blocked state), the rotor speed oscillations are larger than when a support of reactive power is done by the MMC. The same observation is also done for the load angle and the electromagnetic torque of the machine as represented in FIGURES 6.75 and 6.77. It confirms that the MMC has an impact on enhancing the dynamics behaviour of the synchronous machine.

The arm currents of the MMC are in an acceptable range when the remaining voltage is $U_{ret} \approx 0.2[pu]$ as depicted in FIGURE 6.74. Finally, the case where $U_{ret} \approx 0 [pu]$ has also been investigated. The conclusion is the same as in SECTION 6.3. Conversely, the arm currents are overly high in this case. In order to protect the IGBT from these overly high currents, it is needed to block entirely the MMC during the fault. It means that when $U_{ret} = 0$ (i.e. for extreme disturbances), the MMC would not be able to provide support to a synchronous machine.

Chapter 7

Conclusion

The model developed in this work has been used to simulate different cases and to verify the observations of other publications on HVDC using MMC technology. It was also possible to study the positive impact that MMC can have on the transient stability of the machine during a three-phase fault.

The stability limits of the model when connected to a weak grid were investigated and confirmed. The simulated model was able to perform a power inversion and confirmed its low impact on the AC variables. In case of ideal AC network modelled by AC sources, it was confirmed that the MMC could provide voltage support to the network during a three-phase fault by injecting reactive power if the retained voltage was above 0.2 [pu].

It was possible to evaluate the impact of the MMC on the synchronous machine for small transients such as the variation of mechanical power in different configurations: variation of reactive power or synchronous machine's distance.

In addition, the impact of the MMC on the transient behaviour of the machine could be studied during a more severe disturbance: the three-phase fault. Different remaining voltages were studied with the possibility to illustrate the mutual interactions between the converter and the synchronous machine during such a fault. The slower dynamics and the oscillations of the machine would have an impact on the dynamics of the MMC, in particular on the DC current in the DC link, while the MMC could provide a support to the machine and would increase the critical fault elimination time.

Different control strategies can be simulated and their feasibility assessed.

7.1 Future perspectives

To improve the model presented in this work, it would be interesting to investigate a method to calculate the different controller gains. In this work, a tedious empirical

method was used to find the different values. A proposed method would be to establish a closed-loop transfer function that includes the controllers, the MMC and the DC link, and from this calculate the different values that would make the system stable.

To go further with our model, it is possible to identify a working region for the MMC in the PQ plane under a given fault situation. Indeed, for each set of (P,Q), our model gives the opportunity to assess if the fault currents are in an acceptable range for the IGBTs. It will then be possible to know for each point of the plane if this point is a sustainable point for the MMC and therefore to delimit a working region.

A more detailed study of the stability of the rotor angle could be performed, by evaluating the stability according to the equal-area criterion, and by establishing the robustness index against a disturbance.

The events that would be interesting to analyse are other transient phenomena of the electrical power system, such as a single-phase fault. This would allow to study the behaviour of the MMC unbalance voltage and its impact on the transient behaviour of the machine.

In addition, a fault detection strategy could be properly investigated to ensure coordination between the two stations. The black-start capability of the MMC can also be investigated. It would be interesting to observe its ability to provide sufficient power to a generator so that it can help the grid to restart.

Finally, it would be interesting to connect several MMCs and create a MTDC (Multi-Terminal Direct Current) in order to study their interactions and their reaction to faults.

Part III

Appendix

Appendix A

Simulink Bloc Diagram

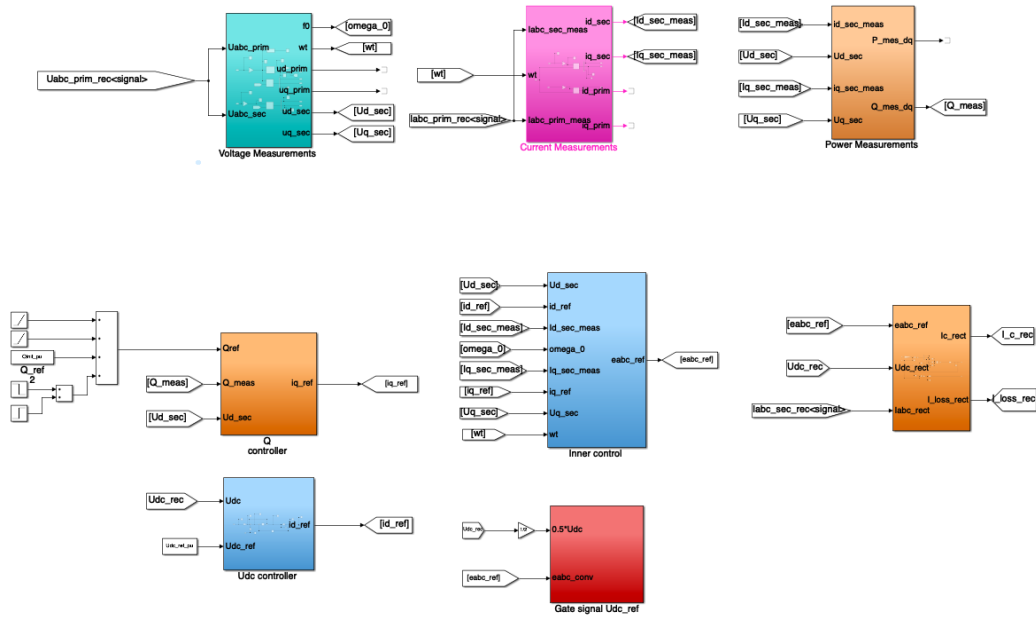


FIGURE A.1: Control blocks of Station 1

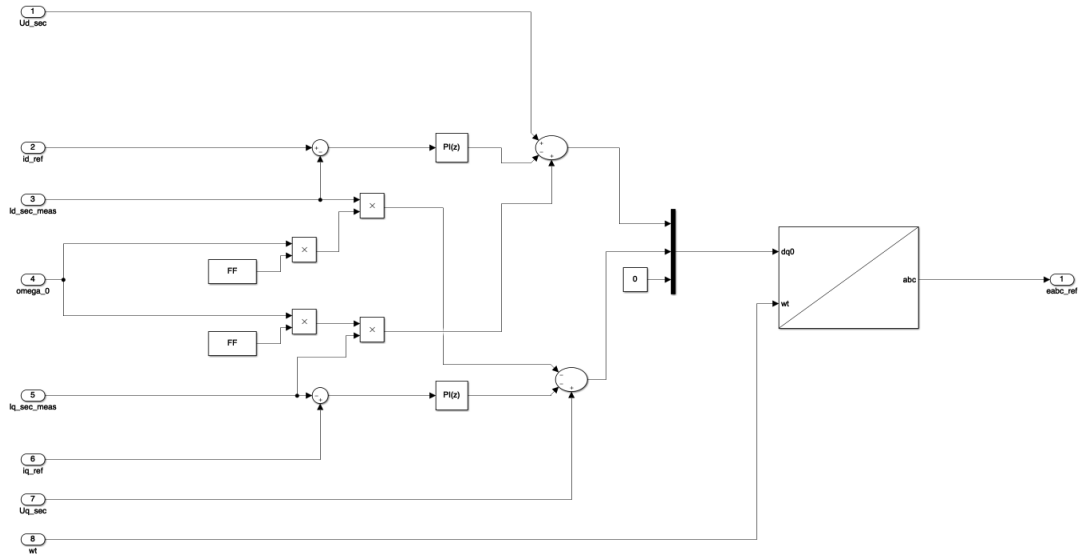


FIGURE A.5: Inner control block diagram

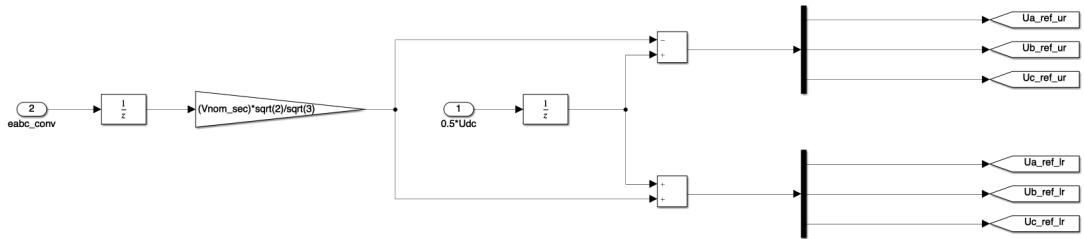


FIGURE A.6: Gate signal generation for controlled voltage sources

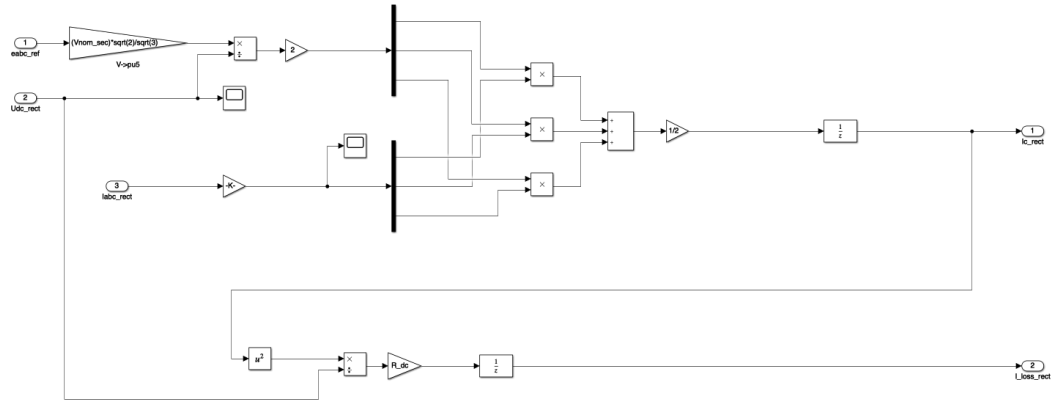


FIGURE A.7: Signal generation for controlled current sources

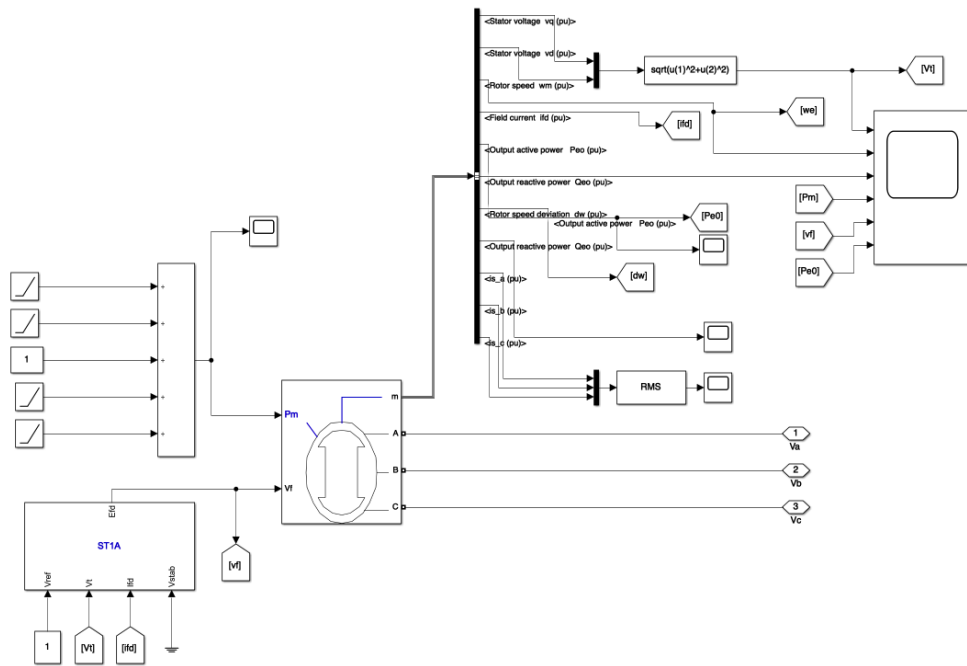


FIGURE A.8: Synchronous machine block diagram

Bibliography

- [1] Nemolink. *Nemo Link announces go-live date*. Last accessed 20 may 2022. 2019. URL: <https://www.nemolink.co.uk/news-news/nemo-link-announces-go-live-date/>.
- [2] Elia. *Elia et Amprion inaugurent ALEGrO, la première interconnexion entre la Belgique et l'Allemagne*. Last accessed 20 may 2022. 2020. URL: https://www.elia.be/fr/actualites/communiques-de-presse/2020/11/20201109_cp-alegro-inauguration.
- [3] Elia. *Elia and Energinet's collaboration is advanced following preliminary study on hybrid interconnector between Belgium and Denmark*. Last accessed 20 may 2022. 2021. URL: https://www.elia.be/-/media/project/elia/shared/documents/press-releases/2021/20211123_hybride-interconnector_en.pdf.
- [4] Hitachi Energy. *The Gotland HVDC link*. Last accessed 24 may 2022. 2018. URL: <https://www.hitachienergy.com/it/it/case-studies/the-gotland-hvdc-link>.
- [5] Hualei Wang and M.A. Redfern. "The advantages and disadvantages of using HVDC to interconnect AC networks". In: *45th International Universities Power Engineering Conference UPEC2010*. 2010, pp. 1–5.
- [6] Hitachi. *Case study : Higashi-Shimizu*. 2019. URL: <https://www.hitachienergy.com/case-studies/higashi-shimizu>.
- [7] S. Du et al. *Modular Multilevel Converters: Analysis, Control, and Applications*. IEEE Press Series on Power and Energy Systems. Wiley, 2018. ISBN: 9781119366300. URL: <https://ieeexplore.ieee.org/servlet/opac?bknumber=8292871>.
- [8] Eurostat. *Energy from renewable sources*. 2017. URL: <https://ec.europa.eu/eurostat/statistics-explained/index.php> (visited on 03/11/2022).

- [9] Thu Win May et al. “Comparative evaluation of power loss in HVAC and HVDC transmission systems; Comparative evaluation of power loss in HVAC and HVDC transmission systems”. In: *2016 IEEE Region 10 Conference (TENCON)* (2016). DOI: [10.1109/TENCON.2016.7848080](https://doi.org/10.1109/TENCON.2016.7848080).
- [10] D M Larruskain et al. “Transmission and Distribution Networks: AC versus DC”. In: ().
- [11] De Jaeger Emmanuel. “Power Lines 1”. In: *LELEC 2520 - Electrical Power Systems* (2022), pp. 1–66.
- [12] De Jaeger Emmanuel. “Flexible AC Transmission Systems(FACTS)”. In: *LELEC2753 - Electrical energy systems: advanced topics and smart grids* (2022), pp. 1–52.
- [13] Michael P. Bahrman and Brian K. Johnson. “The ABCs of HVDC transmission technologies”. In: *IEEE Power and Energy Magazine* 5.2 (2007), pp. 32–44. DOI: [10.1109/MPAE.2007.329194](https://doi.org/10.1109/MPAE.2007.329194).
- [14] N.G. Hingorani. “High-voltage DC transmission: a power electronics workhorse”. In: *IEEE Spectrum* 33.4 (1996), pp. 63–72. DOI: [10.1109/6.486634](https://doi.org/10.1109/6.486634).
- [15] Oluwafemi E. Oni, Innocent E. Davidson, and Kamati N.I. Mbangula. “A review of LCC-HVDC and VSC-HVDC technologies and applications”. In: *2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC)*. 2016, pp. 1–7. DOI: [10.1109/EEEIC.2016.7555677](https://doi.org/10.1109/EEEIC.2016.7555677).
- [16] Silke Allebrod, Roman Hamerski, and Rainer Marquardt. “New transformerless, scalable Modular Multilevel Converters for HVDC-transmission”. In: *2008 IEEE Power Electronics Specialists Conference*. 2008, pp. 174–179. DOI: [10.1109/PESC.2008.4591920](https://doi.org/10.1109/PESC.2008.4591920).
- [17] Gen Li et al. “Power reversal strategies for hybrid LCC/MMC HVDC systems”. In: *CSEE Journal of Power and Energy Systems* 6.1 (2020), pp. 203–212. DOI: [10.17775/CSEEJPES.2019.01050](https://doi.org/10.17775/CSEEJPES.2019.01050).
- [18] Rainer Marquardt. “Modular Multilevel Converters: State of the Art and Future Progress”. In: *IEEE Power Electronics Magazine* 5.4 (2018), pp. 24–31. DOI: [10.1109/MPEL.2018.2873496](https://doi.org/10.1109/MPEL.2018.2873496).
- [19] Entsoe. *Line-Commutated Converters - Current Source Converters*. 2022. URL: <https://www.entsoe.eu/Technopedia/techsheets/line-commutated-converters-current-source-converters> (visited on 03/25/2022).
- [20] Elisabeth N. Abildgaard and Marta Molinas. “Modelling and control of the modular multilevel converter (MMC)”. In: *Energy Procedia* 20 (2012), pp. 227–236. ISSN: 18766102. DOI: [10.1016/J.EGYPRO.2012.03.023](https://doi.org/10.1016/J.EGYPRO.2012.03.023). URL: <http://www.ntnu.edu/>.

- [21] Bjorn Jacobson et al. “VSC-HVDC Transmission with Cascaded Two-Level Converters”. In: (). URL: www.cigre.org.
- [22] Ying Jiang-Hafner et al. “HVDC with voltage source converters - a powerful standby black start facility”. In: *2008 IEEE/PES Transmission and Distribution Conference and Exposition*. 2008, pp. 1–9. DOI: [10.1109/TDC.2008.4517039](https://doi.org/10.1109/TDC.2008.4517039).
- [23] Hans-Joachim Knaak. *Intro : Modular Multilevel Converters and HVDC/FACTS: a success story*. 2011.
- [24] E Spahic et al. *Impact of the DC technology on transmission grids*.
- [25] Phil S Jones and Colin C Davidson. *Calculation of Power Losses for MMC-based VSC HVDC Stations*. URL: <http://www.alstom.com/grid>
<http://www.alstom.com/grid>.
- [26] Dominic Paradis. *Real-time simulation of Modular Multilevel Converters*. 2013.
- [27] Hasnida Saad et al. “Dynamic Averaged and Simplified Models for MMC-Based HVDC Transmission Systems”. In: *Power Delivery, IEEE Transactions on* 28 (July 2013), pp. 1723–1730. DOI: [10.1109/TPWRD.2013.2251912](https://doi.org/10.1109/TPWRD.2013.2251912).
- [28] Hani Saad et al. “Modular multilevel converter models for electromagnetic transients”. In: *2014 IEEE PES General Meeting / Conference Exposition*. 2014, pp. 1–1. DOI: [10.1109/PESGM.2014.6939255](https://doi.org/10.1109/PESGM.2014.6939255).
- [29] Conseil international des grands réseaux électriques. Comité d’études B4. and Impr. Conformes). *Guide for the development of models for HVDC converters in a HVDC grid*. CIGRÉ, 2014. ISBN: 9782858733057.
- [30] G. P. Adam et al. “Generalized switching function model of modular multilevel converter”. In: *2015 IEEE International Conference on Industrial Technology (ICIT)*. 2015, pp. 2702–2707. DOI: [10.1109/ICIT.2015.7125496](https://doi.org/10.1109/ICIT.2015.7125496).
- [31] Jaime Peralta et al. “Detailed and Averaged Models for a 401-Level MMC–HVDC System”. In: *IEEE Transactions on Power Delivery* 27.3 (2012), pp. 1501–1508. DOI: [10.1109/TPWRD.2012.2188911](https://doi.org/10.1109/TPWRD.2012.2188911).
- [32] Maryam Saeedifard and Reza Iravani. “Dynamic performance of a modular multilevel back-to-back HVDC system”. In: *2011 IEEE Power and Energy Society General Meeting*. Vol. 25. 4. 2011, pp. 2903–2912.
- [33] J Peralta Rodriguez. “Dynamic Averaged Models of VSC-Based HVDC Systems for Electromagnetic Transient Programs”. PhD thesis. École Polytechnique de Montréal, 2013.

- [34] Song Ruihua et al. “VSCs based HVDC and its control strategy”. In: *2005 IEEE/PES Transmission Distribution Conference Exposition: Asia and Pacific*. 2005, pp. 1–6. DOI: [10.1109/TDC.2005.1546800](https://doi.org/10.1109/TDC.2005.1546800).
- [35] Sophie Tarbouriech, Isabelle Queinnec, and La Commande Anti-Windup. *Un tour d’horizon sur les techniques anti-windup pour les systèmes saturés Un tour d’horizon sur les techniques anti-windup pour les systèmes saturés An overview of anti-windup techniques for saturated systems-Anti-windup control*. URL: <https://hal.laas.fr/hal-03070178>.
- [36] Steffen Rohner et al. “Analysis and Simulation of a 6 kV, 6 MVA Modular Multilevel Converter”. In: *2009 35th Annual Conference of IEEE Industrial Electronics*. 2009, pp. 225–230. DOI: [10.1109/IECON.2009.5414775](https://doi.org/10.1109/IECON.2009.5414775).
- [37] Qingrui Tu, Zheng Xu, and Jing Zhang. “Circulating current suppressing controller in modular multilevel converter”. In: *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*. 2010, pp. 3198–3202. DOI: [10.1109/IECON.2010.5675048](https://doi.org/10.1109/IECON.2010.5675048).
- [38] Qingrui Tu et al. “Parameter design principle of the arm inductor in modular multilevel converter based HVDC”. In: *2010 International Conference on Power System Technology*. 2010, pp. 1–6. DOI: [10.1109/POWERCON.2010.5666416](https://doi.org/10.1109/POWERCON.2010.5666416).
- [39] Daniel Dinkel, Claus Hillermeier, and Rainer Marquardt. “Direct Multivariable Control of Modular Multilevel Converters”. In: *2018 20th European Conference on Power Electronics and Applications (EPE’18 ECCE Europe)*. 2018, P.1–P.10.
- [40] K. Deepa et al. “A study of comparative analysis of different PWM techniques”. In: *2017 International Conference On Smart Technologies For Smart Nation (SmartTechCon)*. 2017, pp. 1144–1149. DOI: [10.1109/SmartTechCon.2017.8358548](https://doi.org/10.1109/SmartTechCon.2017.8358548).
- [41] Marcos Rejas Haddioui. “Control and modulation strategies for MMC - based HVDC”. MA thesis. Danemark: Alborg University, 2015.
- [42] Qingrui Tu and Zheng Xu. “Impact of Sampling Frequency on Harmonic Distortion for Modular Multilevel Converter”. In: *IEEE Transactions on Power Delivery* 26.1 (2011), pp. 298–306. DOI: [10.1109/TPWRD.2010.2078837](https://doi.org/10.1109/TPWRD.2010.2078837).
- [43] A. Beddard and M. Barnes. “HVDC cable modelling for VSC-HVDC applications”. In: *2014 IEEE PES General Meeting / Conference Exposition*. 2014, pp. 1–5. DOI: [10.1109/PESGM.2014.6939059](https://doi.org/10.1109/PESGM.2014.6939059).
- [44] Entso-E. *Technology Factsheets*. Last accessed 15 may 2022. 2021. URL: https://eepublicdownloads.entsoe.eu/clean-documents/RDC%20documents/2021_Technology%20Factsheet.pdf.

- [45] Entso-e. *HVDC XLPE (Cross-linked Polyethylene)*. 2022. URL: <https://www.entsoe.eu/Technopedia/techsheets/hvdc-xlpe-cross-linked-polyethylene>.
- [46] *Total harmonic distortion*. Last accessed 4 June 2022. URL: https://en.wikipedia.org/wiki/Total_harmonic_distortion.
- [47] C.N. Bhende Jatin K. Pradhan Arun Ghosh. “Small-signal modeling and multivariable PI control design of VSC-HVDC transmission link”. In: *Electric Power Systems Research*. Vol. 144. 2017, pp. 115–126. DOI: <https://doi.org/10.1016/j.epsr.2016.11.005>.
- [48] S. Pavljasevic and F. Dawson. “Synchronization to Disturbed Utility-Network Signals Using a Multirate Phase-Locked Loop”. In: *IEEE Transactions on Industrial Electronics* 53.5 (2006), pp. 1410–1417. DOI: [10.1109/TIE.2006.882002](https://doi.org/10.1109/TIE.2006.882002).
- [49] Zicong Zhang et al. “An Advance Index to Evaluate the Stability of MMC-HVDC and Offshore Wind Power Generation”. In: *2019 IEEE 8th International Conference on Advanced Power System Automation and Protection (APAP)*. 2019, pp. 996–1000. DOI: [10.1109/APAP47170.2019.9225176](https://doi.org/10.1109/APAP47170.2019.9225176).
- [50] Yunfeng Li et al. “Power Compensation Control for Interconnection of Weak Power Systems by VSC-HVDC”. In: *IEEE Transactions on Power Delivery* 32.4 (2017), pp. 1964–1974. DOI: [10.1109/TPWRD.2016.2602890](https://doi.org/10.1109/TPWRD.2016.2602890).
- [51] Jenny Z. Zhou et al. “Impact of Short-Circuit Ratio and Phase-Locked-Loop Parameters on the Small-Signal Behavior of a VSC-HVDC Converter”. In: *IEEE Transactions on Power Delivery* 29.5 (2014), pp. 2287–2296. DOI: [10.1109/TPWRD.2014.2330518](https://doi.org/10.1109/TPWRD.2014.2330518).
- [52] Jiantao Zhao, Meng Huang, and Xiaoming Zha. “Nonlinear Analysis of PLL Damping Characteristics in Weak-Grid-Tied Inverters”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 67.11 (2020), pp. 2752–2756. DOI: [10.1109/TCSII.2020.2978026](https://doi.org/10.1109/TCSII.2020.2978026).
- [53] Heng Wu and Xiongfei Wang. “Design-Oriented Transient Stability Analysis of PLL-Synchronized Voltage-Source Converters”. In: *IEEE Transactions on Power Electronics* 35.4 (2020), pp. 3573–3589. DOI: [10.1109/TPEL.2019.2937942](https://doi.org/10.1109/TPEL.2019.2937942).
- [54] Stefan Kovacevic et al. “Comparative stability analysis of LCC, MMC and dualinfeed HVDC operating with weak AC network”. In: *2020 IEEE Power Energy Society General Meeting (PESGM)*. 2020, pp. 1–5. DOI: [10.1109/PESGM41954.2020.9281570](https://doi.org/10.1109/PESGM41954.2020.9281570).

-
- [55] ABB. *Data Sheet, Doc. No. 5SYA 1431-02 5SNA, 2000K450300 StakPak IGBT Module*. Last accessed 23 may 2022. 2018. URL: <https://library.e.abb.com/public/8d0f218db8df4641a4bf7c978dd2d239/5SNA%202000K450300%205SYA%201431-02%2001-2018.pdf>.
- [56] “COMMISSION REGULATION (EU) 2016/1447, establishing a network code on requirements for grid connection of high voltage direct current systems and direct current-connected power park modules”. In: *Official Journal of the European Union* L 241/1 (6/08/2016), pp. 1–65.
- [57] Xinjia Song et al. “Calculation of AC Short-Circuit Current at MMC-HVDC Converter Station”. In: *2021 6th Asia Conference on Power and Electrical Engineering (ACPEE)*. 2021, pp. 1516–1520. DOI: [10.1109/ACPEE51499.2021.9437003](https://doi.org/10.1109/ACPEE51499.2021.9437003).
- [58] Tianxiao Huang et al. “Research on Reactive Power Control Strategy of MMC HVDC Converter”. In: *2020 IEEE 4th Conference on Energy Internet and Energy System Integration (EI2)*. 2020, pp. 880–884. DOI: [10.1109/EI250167.2020.9346787](https://doi.org/10.1109/EI250167.2020.9346787).
- [59] L. Xiong et al. “Research on the converter temporarily blocking strategy during the AC fault of the MMC-HVDC link”. In: *The 16th IET International Conference on AC and DC Power Transmission (ACDC 2020)*. Vol. 2020. 2020, pp. 1761–1766. DOI: [10.1049/icp.2020.0216](https://doi.org/10.1049/icp.2020.0216).
- [60] *IEEE ST1A Exciter*. Last accessed 4 June 2022. URL: https://www.typhoon-hil.com/documentation/typhoon-hil-software-manual/References/ieee_st1a_exciter.html.
- [61] De Jaeger Emmanuel. “Rotor Angle Stability”. In: *LELEC2595 - Electrical power systems dynamics and quality of supply* (2022), pp. 1–80.
- [62] Fetissi Selwa and Labed Djamel. “Transient Stability Analysis of Synchronous Generator in Electrical Network”. In: *International Journal of Scientific Engineering Research* 5.8 (2014), pp. 55–59. ISSN: 2229-5518.
- [63] Electrical Baba. *Why is Load Angle of Alternator Kept 20°-30°?* Last accessed 3 june 2022. 2016. URL: <https://electricalbaba.com/why-is-load-angle-of-alternator-kept-20-30/>.

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