

École polytechnique de Louvain

Study of a Si_3N_4 passivation layer in Si/SiO_2 -based piezoresistive pressure sensors

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Abstract

Miniaturized pressure sensors are of great interest in many industrial applications such as thermodynamics, biosensors, soil and fluid mechanics as they yield high sensitivity, self sensing abilities and a compact design. Silicon plays a significant part in the production of such sensors, offering dependable micromachining capabilities and delivering excellent sensitivity and accuracy.[1] Silicon-based piezoresistive pressure sensors are typically composed of doped silicon piezoresistances mounted in a Wheatstone bridge configuration which measures the pressure due to a change in the electrical resistances. As piezoresistive pressure sensors are electromechanical devices, enhancing their overall sensitivity can be achieved by optimizing the electrical properties of the piezoresistors in conjunction with the mechanical properties of the membrane.

This work has two main purposes. The first one is to characterize the Si_3N_4/SiO_2 interface with Si by means of MOS capacitor structures to quantify the potential passivation effects related to the Si_3N_4 dielectric layer. This dielectric stack is of particular interest in the context of sensing applications as the residual stress of both material are self-compensating. In this context three stacks are considered : SiO_2/Si as a reference stack, Si_3N_4/Si and $Si_3N_4/SiO_2/Si$, each of which have an aluminium backgate electrode whose post-deposition annealing temperature is investigated. C-V measurements with the mercury probe are performed in order to extract the electrical figures of merit such as the total dielectric stack capacitance C_{ins} , the flatband voltage V_{fb} , the fixed dielectric stack charge Q_f and the interface traps density D_{it} . The second purpose of this work is to propose a stack for piezoresistive pressure sensor designed with a Si_3N_4 passivation layer based on the design from a previous project conducted at UCLouvain with piezoresistors mounted in a Wheatstone bridge configuration. Then to fully characterize the fabricated sensors with mechanical measurements of the membrane deflection with pressure, electrical measurements of the I-V characteristics of the piezoresistors and electromechanical measurements of the full bridge with pressure. Sensors with a balanced bridge with low voltage offset drifts and good normalized sensitivity [ppm/Pa/mm²] are targeted.

The characteristics of the studied MOS stacks which are the total insulator capacitance C_{ins} , the flatband voltage V_{fb} and the fixed charge in the insulator layer Q_f are extracted from C-V measurements. The increase in aluminium annealing temperature showed to reduce the fixed charge density but its limit to 432°C, to prevent silicon nitride delamination and aluminium melting, restrained the improvement of fixed charge density. With regard to the interface trap density D_{it} estimated using both the conductance and high-low frequency method, their estimated values were questioned as no correction was applied to the measured conductance and capacitance.

The deflection with pressure of five n-type sensors showed good agreement with theoretical curves from membrane deflection theory and allowed to estimate a resulting stress on small and large membranes ranging from 50MPa to 70MPa tensile. The balance of the bridge was assessed for three sensors through I-V

measurements and the piezoresistances values ranging from $7.7\text{k}\Omega$ to $21.018\text{k}\Omega$ were extracted from the linear current range. The current and bridge output voltages variation with current were measured with a positive pressure difference applied on the backgate of the membrane. The pressure ranged from 0kPa to 20kPa with 5kPa increments for $0.5\times 0.5\text{mm}^2$ membranes and from 0kPa to 2kPa for $2\times 2\text{mm}^2$ ones with 0.5kPa increments. Both the current and output voltages variation with pressure displayed a linear relation to pressure for positive pressure differences. Finally the maximal sensitivity obtained for a n-type sensor was computed and it reached $2.096\text{ppm}/\text{Pa}/\text{mm}^2$ for an orthogonal $0.5\times 0.5\text{mm}^2$ membrane.

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Acronyms

Acronym	Signification
AC	Alternating Current
BHF	Buffered Hydrofluoric Acid
C-V	Capacitance-Voltage
CVD	Chemical Vapor Deposition
DI	Deionised
DRIE	Deep Reactive Ion Etching
HF	Hydrofluoric Acid
HMDS	Hexamethyl Disilazane
HB	Hard Bake
KITE	Keithley Interactive Test Environment
LPCVD	Low Pressure Chemical Vapor Deposition
MIS	Metal-Insulator-Semiconductor
MOS	Metal-Oxide-Semiconductor
PCB	Printed Circuit Board
PECVD	Plasma Enhanced Chemical Vapor Deposition
PVD	Physical Vapor Deposition
PEB	Post Exposure Bake
RIE	Reactive Ion Etching
SC	Semiconductor
SCS	Semiconductor Characterisation System
SMU	Source-Measurement Unit
TMS	Topography Measurement System
TCR	Thermal Coefficient of the Resistance

Introduction

Miniaturized pressure sensors are of great interest in many industrial applications such as thermodynamics, biosensors, soil and fluid mechanics as they yield high sensitivity, self sensing abilities and a compact design. Silicon plays a significant part in the production of such sensors, offering dependable micromachining capabilities and delivering excellent sensitivity and accuracy.[1] Silicon-based piezoresistive pressure sensors are typically composed of doped silicon piezoresistances mounted in a Wheatstone bridge configuration which measures the pressure due to a change in the electrical resistances. As piezoresistive pressure sensors are electromechanical devices, enhancing their overall sensitivity can be achieved by optimizing the electrical properties of the piezoresistors in conjunction with the mechanical properties of the membrane.

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The first chapter provides an overview of the relevant theoretical aspects which will be used in this work starting with the characterisation of silicon-oxide interface from a basic MOS capacitor through C-V measurements. The selection of silicon nitride Si_3N_4 as part of the insulating layer of the MOS stack is then motivated with both electrical and mechanical considerations. The last section of this theoretical overview covers the silicon-based piezoresistive pressure sensors with the piezoresistive effect, the optimal piezoresistors configuration according to the crystalline orientation and doping type of silicon, the membrane deflection theory and two important figures of merit : the sensitivity and the limit of detection of pressure sensors.

The rest of this work is divided in two parts composed of two chapters each, with a similar structure to present the experimental methodology and results for both the MOS stack and the piezoresistive pressure sensors studied for this work. This in-

cludes an overview of the samples structure followed by the principle of the relevant processing techniques, the fabrication processes which took place in the Winfab facility and a detailed description of the experimental set-ups and measurement sequence used to measure the samples in the Welcome facility. The results for the Si_3N_4/SiO_2 MOS stack give the parameters of each sample extracted from C-V measurements and discusses the conclusions of interest regarding the fabrication of $Si_3N_4/Si/SiO_2$ -based pressure sensors. On the other hand the results for piezoresistive pressure sensors give mechanical, electrical and electromechanical measurements results and discusses further improvements of the latter with fabrication and complementary measurements considerations.

The last chapter concludes with a reminder of the main achievements that were made throughout this work.

Chapter 1

State of the art

1.1 Characterization of silicon-oxide interface

This section introduces the theory behind a MOS capacitor and how one can characterize the interface between its insulator and semiconductor (SC) layers in terms of charges and interface traps densities by means of C-V measurements. The basic structure of the MOS capacitor is first introduced in Section 1.1.1 followed by a thorough description of C-V measurements in Section 1.1.2. Finally the insulator-SC interface quality is discussed in Section 1.1.3.

1.1.1 Structure of MOS capacitor

The typical structure diagram of a metal-insulator-semiconductor (MIS) capacitor is shown in Figure 1.1. The insulator is usually silicon dioxide SiO_2 , as considered in this work, hence the metal-oxide-semiconductor (MOS) capacitor designation. This device is very important in semiconductor device physics because one is able to characterize to a certain extent the oxide-SC interface[2] mainly by performing Capacitance-Voltage measurements, which will be referred as C-V measurements moving forward.

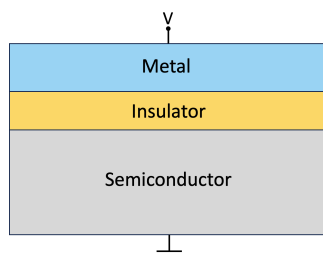


Figure 1.1: MIS structure

the SC is made of p-type silicon with two layers of silicon dioxide and silicon nitride on top, respectively

In this work the SC is made of p-type silicon Si with a layer of silicon dioxide SiO_2 and a layer of silicon nitride Si_3N_4 on top, respectively. Through C-V measurements the objective is to study the surface passivation effects at the oxide-SC interface resulting from the addition of a silicon nitride layer stacked on top of the oxide. In this context the following sections will first describe the expected C-V curves for an ideal MOS capacitor without the presence of defects and the different regimes that can be identified based on these measurements. The interface quality will then be discussed and the two main defect densities, namely the surface density of fixed charges Q_f [cm^{-2}] and the density of interface traps D_{it} [$cm^{-2}eV^{-1}$], will be introduced as well as their influence on the ideal MOS characteristics.

Eventually two approaches on how to extract the aforementioned defect densities from C-V measurements performed on MOS structures will be detailed.

1.1.2 C-V measurements

1.1.2.1 Overview

As mentioned above, C-V measurements play a crucial role in characterizing the SC interface. This technique involves the measurement of capacitance and conductance while varying the voltage bias and frequency. The voltage signal includes a variable DC bias denoted V with respect to a grounded backgate, along with a fixed-amplitude AC superimposed small signal at variable frequency. Although conductance is also measured and the frequency varies, these measurements are commonly referred to as C-V measurements, as is the case in this work. In our specific case, the quantity being measured is the parallel admittance Y , which can be divided into two components shown in Figure 1.2: a capacitive component and a conductive component, denoted C_p and G_p respectively. Note this is an equivalent circuit of the measurements which will subsequently be broken down into an equivalent circuit specific to the measured stack to retrieve the relevant component values.

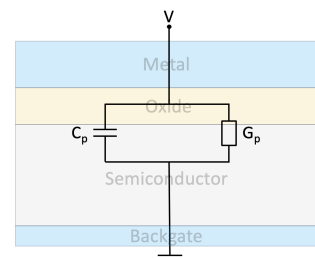


Figure 1.2: C-V measurement small signal equivalent.

An ideal C-V measurement where no defects are present neither within the oxide bulk nor at the interface with the SC when the MOS capacitor is biased with positive or negative voltages would exhibit consistent C-V curves and as one can see in Figure 1.3 three cases can exist at the SC interface with the oxide : accumulation, depletion and inversion. These are detailed in the following sections taking into account the band structure of the materials and are greatly inspired from both [2] and [3].

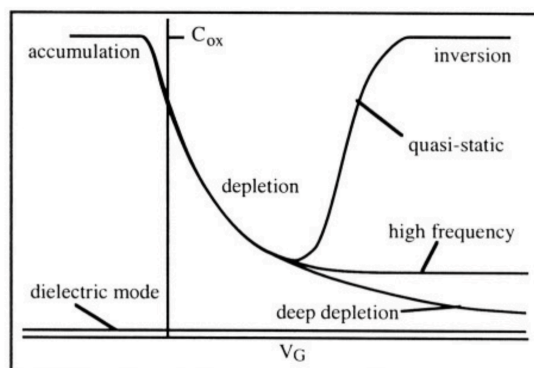


Figure 1.3: Ideal C-V curve of a MOS capacitor on a p-type substrate.[3]

1.1.2.2 Band structure of an ideal MOS capacitor

In order to understand the phenomenons happening at the oxide-SC interface of an ideal MOS capacitor when biased with positive or negative voltages one has to understand the energy band structure of the materials and how they interact. First one can consider the band structure of an ideal p-type SC MOS capacitor under the assumption of flatband conduction, i.e. $V = V_{fb} = 0V$, without neither oxide charges nor defaults which is shown in Figure 1.4 below,

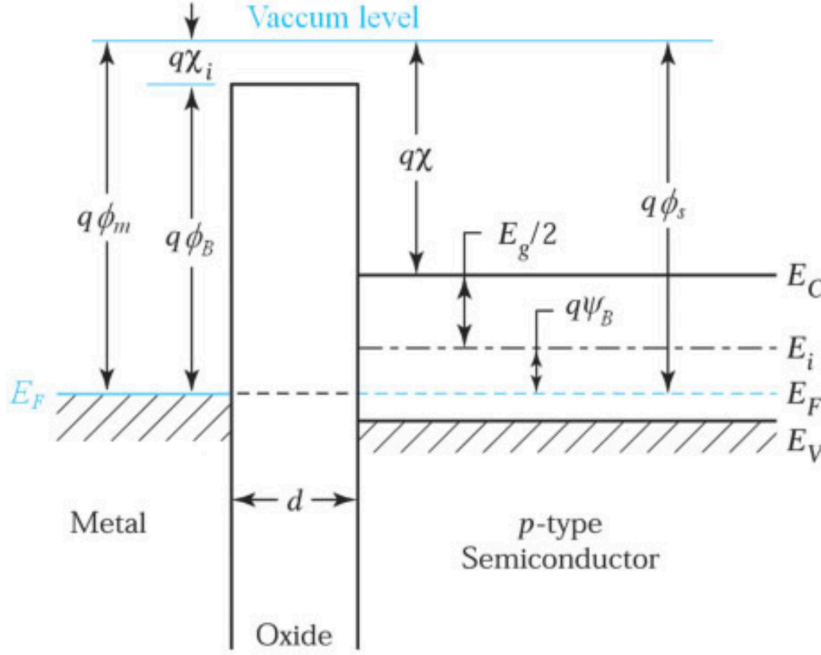


Figure 1.4: Energy band diagram of an ideal MOS capacitor at $V = V_{fb} = 0V$. [2]

where several key parameters are denoted : the Fermi level E_F , the intrinsic Fermi level E_i or midgap energy, the SC bandgap E_g , the electron affinity of the SC $q\chi$, the electron affinity of the oxide $q\chi_i$, the work function of the metal $q\phi_m$ and that of the SC $q\phi_s$. By looking at the energy levels of each material, one can see the metal has no bandgap as it contains a lot of free electrons which will move according to the applied voltage. Its E_F depends on both the metal type and the applied voltage since $E_F = q\phi_m + qV$. For the oxide there is a large bandgap to pass for an electron to be free that causes a high potential barrier between the metal and the SC which makes it a great insulator. For the p-doped SC the E_F will not equal the intrinsic Fermi level, as it is the case in absence of dopants, but instead will lie between the intrinsic Fermi level and the valence band, unlike an n-type SC which E_F would be located between the intrinsic Fermi level and the conductance band. Indeed it is doped with acceptors of electrons and thus holes are the majority carriers. The greater the concentration of dopants, the closer the Fermi level gets to the valence band. It behaves like an insulator which has more free carriers.

Going back to the band structure showcased in Figure 1.4, one can see at zero applied bias that the work function of the SC and that of the metal are equal. In other words the difference between ϕ_s and ϕ_m is zero and the energy band is flat. This is called the "flat-band condition" where the MOS structure is at equilibrium and the E_F difference between the SC and the metal is theoretically equal to the voltage applied to the structure, in this case zero.[2] It is important to consider that in practical structures, the voltage corresponding to the state of flat band, known as the flat band voltage V_{fb} , is not zero.

In an ideal structure, the only charges present in the capacitor, regardless of the biasing conditions, are those within the semiconductor and an equal but opposite charge on the metal surface adjacent to the oxide. Throughout C-V measurements, as the applied bias transitions from negative to positive values, the varying DC voltage carrying an AC small-signal changes the charge distribution within the MOS capacitor and the bands close to the surface of the SC will undergo band bending. Indeed when applying a bias to the metal gate the energy level of electrons moves which changes the whole structure's alignment and the rest of the structure will move accordingly through band bending due to contacts between the materials. However without any charge transport through the oxide ($G_p \approx 0$), the Fermi level in the SC will stay constant. That being said let's see how band bending apply to the three aforementioned regimes.

Accumulation regime For a p-type SC, when a negative voltage is applied to the metal gate, an excess of majority carriers (holes) are attracted at the oxide-SC interface and form an **accumulation** layer. In this case, the bands of the SC are bent upwards as the Fermi level of the semiconductor attempts to align with the one of the metal grid. This accumulation regime is shown in Figure 1.5 below :

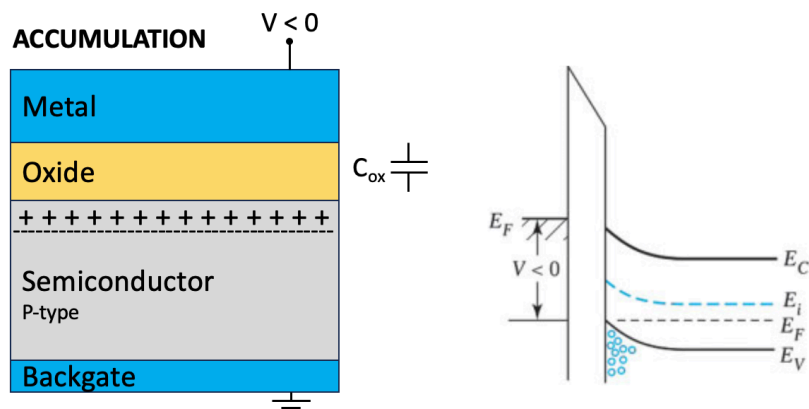


Figure 1.5: MOS capacitor in accumulation regime : (left) MOS structure with negative bias voltage and representation of both the accumulation of majority carriers right below the oxide-SC interface and the oxide capacitance C_{ox} , (right) band bending diagram taken from [2].

Regardless of the type of small AC signal applied to the MOS capacitor, the capacitance measured in the strong accumulation region remains essentially constant, resulting in a flat slope in the C-V curve as previously shown in Figure 1.3. Additionally, the capacitance in the accumulation region remains unchanged across different frequencies and the measured capacitance $C_p = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} [\frac{F}{m^2}]$ in the accumulation region, with C_{ox} the oxide capacitance, t_{ox} the oxide thickness and ϵ_{ox} the oxide dielectric constant.

Depletion region When a small positive voltage is applied to the metal gate, majority carriers (holes) are repelled deeper in the SC which results in a negative charge due to negatively ionized acceptor centers. In that region below the oxide-SC interface the holes are said to be depleted and that's why it is called the **depletion** regime. In this case, the bands of the SC are bent downwards as the Fermi level of the semiconductor attempts once again to align with the one of the metal grid. This depletion regime is shown in Figure 1.6 below :

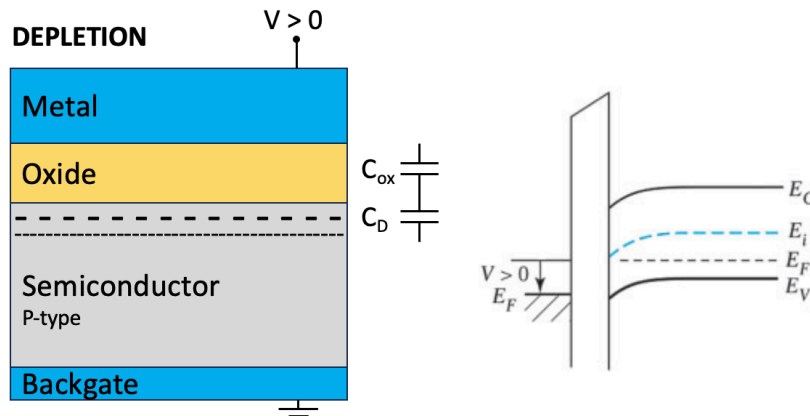


Figure 1.6: MOS capacitor in depletion regime : (left) MOS structure with a small positive bias voltage and representation of the concentration of the negatively-charged acceptor centers right below the oxide-SC interface, the oxide capacitance C_{ox} and the depletion capacitance C_D , (right) band bending diagram taken from [2].

The measured capacitance is now composed of the oxide capacitance C_{ox} in series with a depletion capacitance C_D and thus decreases in the depletion regime as previously shown in Figure 1.3.

Inversion region When the positive voltage applied to the metal gate becomes larger, in addition to negatively-charged acceptor centers, additional electrons are attracted below the oxide-SC interface and it is called the **weak inversion** regime. In this case, the bands of the SC bend downwards even more as the Fermi level of the semiconductor keeps its alignment with the one of the metal grid and is

crossed by the intrinsic Fermi level. This inversion regime is shown in Figure 1.6 below :

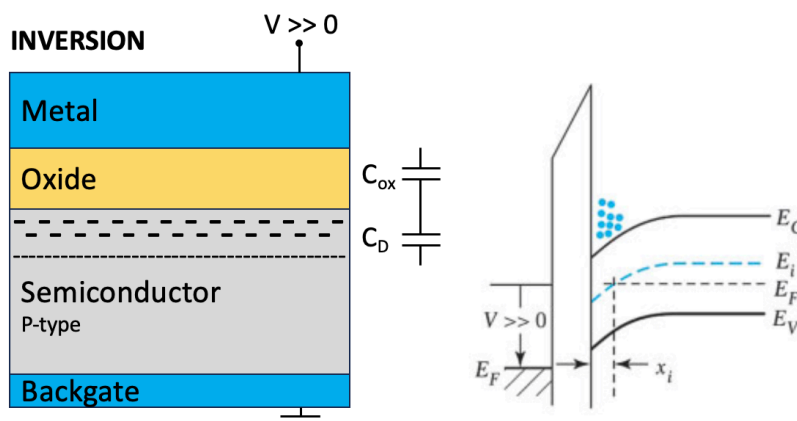


Figure 1.7: MOS capacitor in inversion regime : (left) MOS structure with a larger positive bias voltage and representation of the high concentration of electrons which become majority carriers right below the oxide-SC interface, the oxide capacitance C_{ox} and the depletion capacitance C_D , (right) band bending diagram taken from [2].

The measured capacitance is still composed of the oxide capacitance C_{ox} in series with an even smaller depletion capacitance C_D , as the depleted region becomes thicker, and it keeps decreasing until the depletion region below the oxide-SC interface reaches a maximum depth and the minimum total capacitance is measured. The concentration of electrons then reaches the negatively-charged acceptor centers concentration and the structure is said to be in a **strong inversion** regime. The inversion part of the C-V measurement shown in Figure 1.3 for further increased bias voltage displays different curves depending on the frequency used. Indeed at low frequency the total measured capacitance corresponds to C_{ox} again (quasi-static curve). For a higher frequency, due to the rapid variations of the voltage small-signal, certain electrons in the inversion layer are unable to keep pace, leading to an additional increase in the depletion capacitance. As a result, the total capacitance progressively decreases below the value of C_{ox} as the frequency rises and even reaches a deep depletion state. If a very high-frequency AC signal is used then even majority carriers have no time to react with the varying gate voltage and the structure ends up behaving like a dielectric (dielectric mode).

1.1.3 Interface quality

In realistic MOS structures the C-V curve profiles will differ from the ones detailed in previous sections due to interface trapped charges which are defects located at the oxide-SC interface and to defects inside the oxide bulk. Regarding the latter there exist fixed oxide charges, oxide-trapped charges and mobile ionic charges but

only fixed oxide charges are commonly studied in literature in order to analyse the interface quality.[4][5] Consequently the two defects of interest which will be studied in this section are the density of fixed oxide charges Q_f [cm^{-2}] along with the density of interface traps D_{it} [$cm^{-2}eV^{-1}$]. The following section draws significant inspiration from the ideas and concepts presented in the previously referenced article [2].

1.1.3.1 Density of fixed charges Q_f

The volumetric density of fixed charged defects found within the bulk of the oxide layer can be approximated as a charge sheet with a charge density of Q_f located at the bottom surface of the oxide layer. Indeed let's assume x_0 denotes the vertical position along the oxide thickness d with $x_0 = d$ being located at the oxide-SC interface and $\rho_f(x)$ is the volumic fixed charge density distribution along that same axis then the total charge contained in a charge sheet with a charge density of Q_f located at the oxide-SC interface can be expressed as follow :

$$Q_f = \frac{1}{d} \int_0^{x_0=d} x \cdot \rho(x) \cdot dx \quad [cm^{-2}] \quad (1.1)$$

For a given work function of the metal grid, the electrostatic potential associated with Q_f causes a horizontal voltage shift shown in Figure 1.8(b) of the C-V curves directed leftwards in the case of positive charges (resp. rightwards for negative charges) when compared to the ideal scenario where there are no defects and $V_{fb} = 0V$ also shown in Figure 1.8(a).

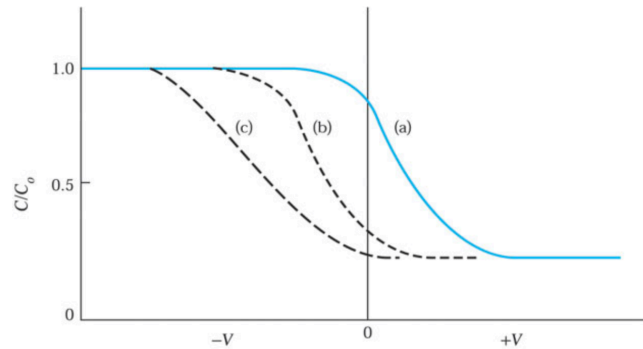


Figure 1.8: (a) The C-V characteristics of an ideal MOS capacitor with a p-type SC. (b) Parallel shift along the voltage axis due to positive fixed-oxide charges. (c) Nonparallel shift along the voltage axis due to interface traps.[2].

The flatband voltage is thus influenced by two factors: the density of the sheet charge density Q_f and its position x_0 within the oxide layer. To make it clear when the sheet charge is located very close to the metal ($x_0=0$) it will induce no charges and therefore have no effect on the flat-band voltage whereas it will exert its maximum influence and give impact the flatband voltage when located very

close to the oxide-SC interface ($x_0=d$). The voltage shift ΔV_f can be expressed as follow :

$$\Delta V_f = \frac{-q \cdot Q_f}{C_{ox}} \cdot \frac{x_0}{d} = \frac{-q Q_f}{C_{ox}} \quad [V] \quad (1.2)$$

with $C_{ox} [\frac{F}{cm^2}]$ the oxide capacitance and $q = 1.602 \cdot 10^{-19} [C]$ the elementary charge. Since realistic structures are considered here the difference between the work functions of the metal and the SC is not null as mentioned in 1.1.2.2 and has an influence on the flatband voltage. In fact it induces a potential that contributes to shifting the C-V curve as well. Ultimately the expression for the updated value of the flat-band voltage V_{fb} that takes into account not only the influence of fixed charges in the oxide but also the built-in potential difference inherent in the MOS structure can be written as follow :

$$V_{fb} = \Delta V_f + \phi_{ms} = \frac{-q \cdot Q_f}{C_{ox}} + \phi_{ms} \quad [V] \quad (1.3)$$

The above equation can be reformulated to provide an alternative expression for Q_f :

$$Q_f = \frac{\phi_{ms} - V_{fb}}{q} \cdot C_{ox} \quad [cm^{-2}] \quad (1.4)$$

Later on in this work this equation will be used in order to compute the magnitude of Q_f . The typical order of magnitude for fixed-oxide charge densities $10^{10} cm^{-2}$. [2] but more importantly it is crucial to get the sign of Q_f which gives the direction of the electrical field created by fixed charges within the oxide layer.

The second derivative method was chosen to extract the flatband voltage V_{fb} from C-V measurements and will be used later on in this work when computing the density of fixed charges. It is descibed in detail in [6] and is based on the inflection point of C-V curves measured at any selected frequency. Furthermore this method remains valid when determining V_{fb} in MOS structures with high interface densities. It consists in plotting the second derivative of the measured capacitance as a function of the metal-gate voltage V and taking the bias value of the first point of intersection of the second derivative with the V-axis as the flatband voltage.

1.1.3.2 Density of interface traps D_{it}

The presence of interface trapped charge is linked to the existence of dangling bonds at the interface between the insulator and the SC.[7] These interface trapped charges exhibit a distinct behavior compared to the oxide bulk defects discussed above, particularly in terms of their dependence on bias voltage and frequency. This is due to their ability to rapidly adjust their charge state and their dependence

with E_F at the interface which implies a dependence to the voltage applied at the metal-gate as well. Indeed as it is described Section 1.1.2.2 when varying this voltage band bending occurs in the SC close to the interface with the insulator and the state of interface trapped charges fluctuates. As a result the total capacitance value also changes. Moreover some charges which would normally contribute to band bending when the structure attempts to align with the new E_F of the metal when the applied voltage changes will have a tendency to become trapped at the interface instead. This actually reduces the band bending and causes an horizontal stretch of C-V curves as one can see in Figure 1.8(c).

Now that the influence of interface traps on the total capacitance is established, one can use an improved equivalent circuit suggested in [7] to represent their effect. As shown in Figure 1.9(a) a capacitance C_{it} in series with a resistance R_{it} that represents the lossy process of capture-emission of carriers by the D_{it} can be added in parallel of the depletion capacitance C_S which corresponds to C_D in our previous notations. The capacitance of the dielectric layer denoted C_i which corresponds to C_{ox} in our previous notations remains unchanged. Through these additional components one can estimate the density of interface traps when measuring the parallel capacitance and conductance also shown in Figure 1.9(c) obtained with C-V measurement for several voltages and frequencies. The middle equivalent circuit aims at simplifying the matching between equivalent circuit in (a) and (c).

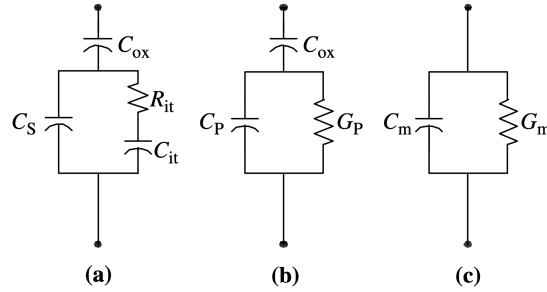


Figure 1.9: Equivalent circuit including the components related to interface traps. (a) MOS capacitor with interface trap time constant $\tau_{it} = R_{it}C_{it}$, (b) simplified circuit of (a), (c) measured circuit. 1.9

The following equations taken from [7] links C_P and G_P to the resistance R_{it} and C_{it} , ultimately linking them to the density of interface traps :

$$\begin{cases} C_P &= C_S + \frac{C_{it}}{1+\omega^2\tau_{it}^2} \\ \frac{G_P}{\omega} &= \frac{q\omega\tau_{it}D_{it}}{1+\omega^2\tau_{it}^2} \end{cases} \quad (1.5)$$

with $C_{it} = q^2D_{it}$, $\omega = 2\pi f$ the angular frequency with the measurement frequency f and $\tau_{it} = C_{it}R_{it}$ the interface trap time constant which governs the frequency response of the interface states.

Now that the relations between the density of interface traps which needs to be estimated for the purpose of this work and the evolution of both parallel capacitance and conductance is established, let's review two methods that will be used later on to extract the value of D_{it} . The typical order of magnitude for interface traps density is $10^{-11} [cm^{-2}eV^{-1}]$ for a good quality oxide and $10^{-12} [cm^{-2}eV^{-1}]$ or even $10^{-13} [cm^{-2}eV^{-1}]$ for a low quality oxide.[7] The exact value of the D_{it} is less relevant than the order of magnitude especially since the methods to estimate it remains approximative.

Conductance method The conductance method is considered the most sensitive approach for determining the density of interface traps of the order of $10^9 cm^{-2}eV^{-1}$ and lower.[7] This method involves measuring the equivalent parallel conductance G_p of a MOS capacitor as a function of the applied voltage at various frequencies. The conductance, which is related to the loss mechanism caused by the capture and emission of carriers by interface traps, is measured as a function of frequency and plotted as G_P/ω versus ω . The next step is to identify the maximum of this curve which is a priori located at $\omega = \frac{1}{\tau_{it}}$ and at that maximum an approximate expression giving the interface trap density in terms of the measured maximum conductance derived from Equation 1.5 and taken from [7] is used :

$$D_{it} = \frac{2.5}{q} \cdot \left(\frac{G_P}{\omega} \right)_{max} \quad (1.6)$$

High-low frequency capacitance method The high-low frequency method allows to compute the interface traps density by means of the high and low frequency C-V curves. By comparing the measured capacitance C_p response at high and low frequency ideally at the minimum C_{lf} where this technique is most sensitive[7], one is able to isolate C_{it} in the equivalent circuit given in Figure 1.9 (a). Indeed at low frequency C_{it} dominates such that R_{it} can be neglected and at high frequency the $R_{it}-C_{it}$ branch disappears as interface traps are not able to follow the voltage variations at such frequencies. This implies that the frequency must be sufficiently high for the D_{it} not to respond anymore.[7] The formula used to estimate D_{it} is given below :

$$D_{it} = \frac{C_{ox}}{q^2} \cdot \left(\frac{C_{lf}/C_{ox}}{1 - C_{lf}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}} \right) \quad (1.7)$$

1.2 Selection of silicon nitride as passivation layer

The linear permittivity of a given material is often given relative to that of free space, as a relative permittivity ϵ_R also called the dielectric constant k of the material which has no unit. The actual permittivity can be computed as follow :

$$\epsilon = \epsilon_R \cdot \epsilon_0 \quad (1.8)$$

with $\epsilon_0 = 8.854 \cdot 10^{-12} [F \cdot m^{-1}]$ the intrinsic permittivity of free space. Silicon nitride is a dielectric with a high dielectric constant k , accordingly called a high- k dielectric, which can serve many purposes. Indeed silicon nitride thin films are widely used as passivation films in integrated circuits, offering a combination of chemical resistance and mechanical scratch protection, it is also used for suspended membrane since residual stress in such films can be made small and tensile, or it can be used as a capacitor dielectric.[8] This section first discusses the use of silicon nitride as a capacitor dielectric then motivates the use of this material for sensing devices.

Two out of the three capacitor stacks considered in this work contain a thin silicon nitride layer. In the first one, the silicon dioxide is fully replaced by silicon nitride whereas in the second one it is stacked with the latter on top. There are several requirements for a replacement of a dielectric layer which need to be taken into account :

- The dielectric must have a high dielectric constant which is the case for Si_3N_4 whose dielectric constant is $k_{Si_3N_4}=7.5$ which is almost two times higher than that of SiO_2 , $k_{SiO_2}=3.9$.
- Ideally the dielectric must have a large band gap in order to provide a good insulation therefore low leakage currents. For Si_3N_4 the band gap is 5.3eV which is smaller than that of thermally grown SiO_2 equal to 9eV.[9] See Table 1.1 for comparison with other high- k dielectrics.
- Literature also indicates that the conduction band offset ΔE_c has to be over 1eV to avoid large tunneling current since it is the barrier preventing electrons to travel from the gate to the silicon substrate. For Si_3N_4 , $\Delta E_c=2.4$ and for SiO_2 , $\Delta E_c=3.2$ which is 33% higher.[9] See Table 1.1 for comparison with other high- k dielectrics.
- The dielectric must have a good chemical and thermal stability, which is the case for Si_3N_4 [10].
- Another important aspect is the ability to grow high purity, either totally crystalline or totally amorphous films on Si with a clean interface. In this work the silicon nitride film is totally amorphous and remains amorphous in all typical microfabrication processes.[8]

- Last but not least it needs to be compatible with the substrate, the top electrode and moreover with the CMOS technology used.

Dielectric	k	E_g	ΔE_c	ΔE_v
SiO_2	3.9	9	3.2	4.7
Si_3N_4	7	5.3	2.4	1.8
Al_2O_3	9	8.8	2.8	4.9
HfO_2	25	5.8	1.4	3.3
TiO_2	80	3.5	0	2.4

Table 1.1: Several high-K materials available in Winfab with their parameters : k the dielectric constant, E_g [eV] the band gap, ΔE_c [eV] the conductance band offset and ΔE_v [eV] the valence band offset. Numerical values are taken from [9].

As one might expect, the quality of the dielectric and its thickness are critical because these parameters have a strong impact on the tunneling transmission of carriers through the dielectric.[11] If silicon dioxide is replaced by a high-k dielectric such as silicon nitride, one can obtain the high-k thickness which yields smaller leakage while maintaining similar capacitance value [12] :

$$t_{Si_3N_4} = \frac{t_{SiO_2} \cdot k_{Si_3N_4}}{k_{SiO_2}} \quad (1.9)$$

with t_{SiO_2} [m] the equivalent oxide thickness, $k_{Si_3N_4}$ the high-k dielectric constant and k_{SiO_2} the equivalent oxide dielectric constant. As a relevant example for the continuation of this work, for a 300nm thick oxide layer, a 538nm thick silicon nitride layer would yield an equivalent capacitance value for replacement.

When replacing silicon dioxide with any high-k dielectric the main goal is to achieve a good interface quality at the dielectric-silicon interface. As already explained in Chapter 1.1, the quality of the interface mainly depends on fixed charge Q_f and interface charge density D_{it} . In amorphous silicon nitride the main defects are silicon and nitrogen dangling bonds which density varies with composition and deposition conditions. These dangling bonds within the nitride are energetically below the silicon conduction band [13] Consequently, there is a relatively efficient injection of negative charge from the silicon to the nitride. Injected electrons pass through the insulating layer by hopping through silicon dangling bond defects. The removal of charge from the nitride can be achieved by thermal treatments.[13] However in an ideal case, for a p-type silicon substrate, the fixed charge would have the same sign as the inversion layer which precisely prevents channel electrons tunneling the dielectric to the gate. Even if an additional silicon dioxide layer is added between the high-k dielectric and the silicon the total fixed charge should remain negative. For this reason there is a significant demand for alternative dielectric materials with negative fixed charge, as they are crucial for efficiently passivating p-type semiconductor surfaces.[4]

As for the use of silicon nitride as a passivation layer in sensing devices there are also several requirements which depends on the environment. First of all it needs to have a good adhesion with the underlying material even during stressing, it is usually chemically inert and corrosion-resistant. The high-k dielectric commonly used as passivation layers are silicon dioxide, aluminum oxide and silicon nitride.[14] The latter is often used in integrated circuits and micro-mechanical structures. It offers superior diffusion resistance to water and sodium compared to silicon dioxide. Moreover, silicon nitride serves as a dielectric material in microelectronic and photonic applications. The most common form of silicon nitride used in microfabrication is Si_3N_4 , typically formed through either Low Pressure Chemical Vapor Deposition (LPCVD) or Plasma-Enhanced Chemical Vapor Deposition (PECVD) processes.[15] Another advantage of silicon nitride used together with silicon dioxide for sensing applications such as pressure sensing with micromechanical diaphragms is the possibility to achieve small and tensile residual stresses on the membrane of the sensor and on the metal lines since they form a stress-compensating dielectric stack with opposite sign stresses, compressive for silicon dioxide films and tensile for silicon nitride ones.[11]

1.3 Silicon-based piezoresistive pressure sensors

The foundation of almost all micromechanical pressure sensors relies on thin diaphragms that bend under pressure differences. This diaphragm displacement is subsequently converted into an electrical signal, either through direct capacitive sensing or indirectly via piezoresistive sensing.[16] The latter is the focus of this work and will be discussed in this section starting with a detailed explanation of piezoresistivity, the important equations and the origin of piezoresistive coefficients, followed by the piezoresistors configuration considered in this work and the membrane deflection theory with theoretical models to express the maximal deflection and stresses when a pressure difference is acting on a circular or square membrane. Finally the two main figures of merit, the sensitivity and the limit of detection, will be discussed.

1.3.1 Overview of piezoresistivity

Please note this section is greatly inspired from chapter 6.1 in [17] and chapter 9.2 in [18]. Let's first consider a SC bar of length L and cross section S along which flows an electrical current I . According to Ohm's law the electrical conductivity σ can be expressed as a function of the current density $[A/cm^2]$, given by the current I divided by the cross-section of the bar, and the electrical field in the bar along the current flow direction $[Volts/cm]$, given by the voltage drop along the bar and the length of the latter. The electrical conductivity is also reciprocal to the electrical resistivity denoted ρ $[\Omega \cdot cm]$ and writes as follow :

$$\sigma = \frac{1}{\rho} = \frac{1}{R} \cdot \frac{L}{S} \quad (1.10)$$

with $R = \frac{V}{I}$ the resistance. From the above equation one can express the resistance as a function of either the conductivity or resistivity and the physical dimensions of the bar as follow :

$$R = \rho \cdot \frac{L}{S} = \frac{1}{\sigma} \cdot \frac{L}{S} \quad (1.11)$$

The resistivity ρ can also be re-expressed knowing that the conductivity σ is the product of the electronic charge of carriers e , the number of charge carriers n and the average mobilities of these carriers μ which gives the following expression :

$$\rho = \frac{1}{e \cdot n \cdot \mu} \quad (1.12)$$

When a tensile (or compressive) force F is applied to the SC bar it creates a tensile (or compressive) stress in it which induces a change in all elements constituting Equation 1.11 simultaneously. The relative resistance change is given below :

$$\frac{\Delta R}{R} = \frac{\Delta \rho}{\rho} + \left(\frac{\Delta L}{L} - \frac{\Delta S}{S} \right) \quad (1.13)$$

where $\frac{\Delta \rho}{\rho}$ is the relative resistivity change and $(\frac{\Delta L}{L} - \frac{\Delta S}{S})$ is the relative geometric change of the bar. From Equation 1.12, the relative resistivity change of a SC bar under stress can be expressed as :

$$\frac{\Delta \rho}{\rho} = -\left(\frac{\Delta n}{n} + \frac{\Delta \mu}{\mu} \right) \quad (1.14)$$

This equation shows that the magnitude and polarity of the relative resistivity change depend on the SC type, its crystallographic orientation with respect to the current flow, its carriers concentration and the working temperature. In particular a shift in the material's band structure is induced by the applied stress and consequently the effective mass of holes and electrons changes, leading to variations in carrier mobility and thus influencing the resistivity of the material.[19] This relative resistivity change is proportional to the applied stress and can be expressed as follow :

$$\frac{\Delta \rho}{\rho} = \pi_L \cdot \tau = \pi_L \cdot E \cdot \epsilon_L \quad (1.15)$$

with π_L the longitudinal piezoresistive coefficient and τ the applied stress equal to the product of the Young's modulus of the SC and the longitudinal strain mentioned previously, denoted E and ϵ_L respectively. Then assuming a and b are the lateral dimensions of the bar with the crossed section $S = a \cdot b = a^2 \cdot \frac{b}{a}$, the relative cross section variation can be expressed as follow :

$$\frac{\Delta S}{S} = \frac{2 \cdot \frac{b}{a} \cdot a \cdot \Delta a}{a \cdot b} = 2 \cdot \frac{\Delta a}{a} = 2 \cdot \epsilon_S \quad (1.16)$$

where ϵ_S is the lateral strain $\frac{\Delta a}{a}$ of the bar. As for the longitudinal strain of the bar $\frac{\Delta L}{L}$, also denoted ϵ_L , it can be expressed as a function of the lateral strain and the Poisson's ratio ν as follow :

$$\epsilon_S = -\nu \cdot \epsilon_L \quad (1.17)$$

where the minus sign denotes the case where $\Delta S < 0$ and $\Delta L > 0$, and vice versa. Finally combining Equations 1.16, 1.17 and 1.14 with 1.13 one can obtain the following expression for the relative resistance change :

$$\frac{\Delta R}{R} = [\pi_L \cdot E + (1 + 2\nu)] \cdot \epsilon_L \quad (1.18)$$

This equation describes the SC piezoresistivity and the factor $[\pi_L \cdot E + (1 + 2\nu)]$ is called the sensitivity coefficient of the SC bar, also known as the gauge factor. Under stress, the relative geometric change has a contribution to the relative resistance change of less than 1% [17] and can be ignored. As a result, the relative resistivity change $\frac{\Delta \rho}{\rho} = \pi_L \cdot E \cdot \epsilon_L$ is the predominant term often used to describe the piezoresistivity of SC. The resistivity ρ is actually a second-order tensor represented by a 3 by 3 matrix which links the three-components electric field vector $\mathbf{E}$ and the three-components current density vector $\mathbf{I}$ and can be written as follow using matric notation :

$$\begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} = \begin{bmatrix} \rho_{11} & \rho_{12} & \rho_{13} \\ \rho_{21} & \rho_{22} & \rho_{23} \\ \rho_{31} & \rho_{32} & \rho_{33} \end{bmatrix} = \begin{bmatrix} J_1 \\ J_2 \\ J_3 \end{bmatrix} \quad (1.19)$$

According to Onsager's reciprocity theorem[20], the resistivity tensor is symmetrical and only 6 of the nine resistivity components are unique, ρ_{xx} , ρ_{yy} , ρ_{zz} , ρ_{yz} , ρ_{xz} and ρ_{xy} and can be numbered by a single index ρ_i in the following manner :

$$\boldsymbol{\rho} = \begin{bmatrix} \rho_{11}\rho_{12}\rho_{13} \\ \rho_{21}\rho_{22}\rho_{23} \\ \rho_{31}\rho_{32}\rho_{33} \end{bmatrix} = \begin{bmatrix} \rho_1\rho_6\rho_5 \\ \rho_6\rho_2\rho_4 \\ \rho_5\rho_4\rho_3 \end{bmatrix} = \begin{bmatrix} \rho_1 \\ \rho_2 \\ \rho_3 \\ \rho_4 \\ \rho_5 \\ \rho_6 \end{bmatrix} \quad (1.20)$$

The relative resistivity change expressed in Equation 1.15 thus writes[18]:

$$\frac{\Delta\rho_i}{\rho} = \sum_{k=1}^6 \pi_{ik} \tau_k \quad (1.21)$$

or in matrix notation :

$$\begin{bmatrix} \frac{\Delta\rho_1}{\rho} \\ \frac{\Delta\rho_2}{\rho} \\ \frac{\Delta\rho_3}{\rho} \\ \frac{\Delta\rho_4}{\rho} \\ \frac{\Delta\rho_5}{\rho} \\ \frac{\Delta\rho_6}{\rho} \end{bmatrix} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{13} & \pi_{14} & \pi_{15} & \pi_{16} \\ \pi_{21} & \pi_{22} & \pi_{23} & \pi_{24} & \pi_{25} & \pi_{26} \\ \pi_{31} & \pi_{32} & \pi_{33} & \pi_{34} & \pi_{35} & \pi_{36} \\ \pi_{41} & \pi_{42} & \pi_{43} & \pi_{44} & \pi_{45} & \pi_{46} \\ \pi_{51} & \pi_{52} & \pi_{53} & \pi_{54} & \pi_{55} & \pi_{56} \\ \pi_{61} & \pi_{62} & \pi_{63} & \pi_{64} & \pi_{65} & \pi_{66} \end{bmatrix} \cdot \begin{bmatrix} \tau_1 \\ \tau_2 \\ \tau_3 \\ \tau_4 \\ \tau_5 \\ \tau_6 \end{bmatrix} \quad (1.22)$$

where the fourth-order piezoresistance coefficient tensor for crystals with cubic symmetry, such as silicon, only has 3 non-zero independent coefficient [21] and its simplified form is given below:

$$\pi_{ik} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \quad (1.23)$$

The piezoresistivity of SC such as silicon is highly dependent on the crystal direction and for cubic SC the material properties are defined in a coordinate system aligned with the (100) directions of the crystal unit cell.[18] The transformation from the crystal axes, visible in Figure 1.10 for a (100) silicon wafer, to a Cartesian system of arbitrary orientation is given below by direction cosines expressed in terms of Euler's angles in Figure 1.11 :

$$\begin{bmatrix} l_1 m_1 n_1 \\ l_2 m_2 n_2 \\ l_3 m_3 n_3 \end{bmatrix} = \begin{bmatrix} c\phi c\theta c\psi - s\phi s\psi & s\phi c\theta c\psi + c\phi s\psi & -s\theta c\psi \\ -c\phi c\theta s\psi - s\phi c\psi & -s\phi c\theta s\psi + c\phi c\psi & s\theta s\psi \\ c\phi s\theta & s\phi s\theta & c\theta \end{bmatrix} \quad (1.24)$$

where c and s are writing shortcuts for cosinus and sinus.[22] Considering axes 3 and 3' remains combined ($\theta=0$) and the rotation only occurs in the 1-2 plane, two typical piezoresistance effects are considered when uniaxial stress is applied in the material : a longitudinal piezoresistance coefficient π_l when both the current and field are in the direction of the stress, and a transverse piezoresistance coefficient π_t when both the current and field are perpendicular to the stress. These two coefficient can be expressed as a function of the components of the tensor π_{ik} taking into account the transformation :

$$\pi_l = \pi_{11} - 2 \cdot (\pi_{11} - \pi_{12} - \pi_{44}) \cdot (l_1^2 m_1^2 + m_1^2 n_1^2 + n_1^2 l_1^2) \quad (1.25)$$

and

$$\pi_t = \pi_{12} + (\pi_{11} - \pi_{12} - \pi_{44}) \cdot (l_1^2 l_2^2 + m_1^2 m_2^2 + n_1^2 n_2^2) \quad (1.26)$$

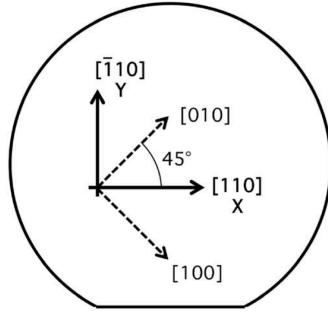


Figure 1.10: Crystalline orientations in a (100) silicon wafer. Figure taken from [23].

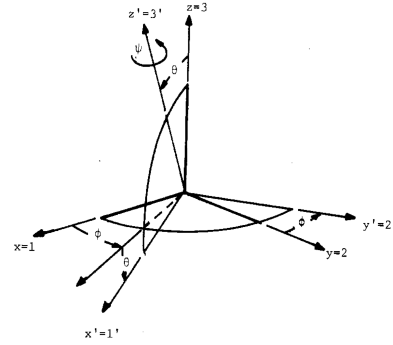


Figure 1.11: Euler's angles. Figure taken from [22]

Using the values of piezoresistance coefficients summarized in Table 1.2 one can obtain the values of the longitudinal and transverse coefficient, π_l and π_t , as a function of crystal direction in a polar plot for a rotation angle varying from 0 to 180 degrees. The plots for orientations in the (100) plane for both p- and n-type silicon are shown in units of $[10^{-11} Pa^{-1}]$ in Figure 1.12. The upper halves of the graphs exhibit positive values of the piezoresistance coefficient which implies that the mobilities decrease and the resistivities increase with tensile stress whereas the lower halves show negative values for the piezoresistance coefficient which implies that the mobilities increase and resistivities decrease with tensile stress. The occurrence of comparable and opposite polarity π_l and π_t in the $\langle \bar{1}10 \rangle$ direction for (100) p-type silicon and in the $\langle \bar{1}00 \rangle$ for (100) n-type silicon is a key feature regarding the design for piezoresistive sensor bridge application[18].

	$\pi_{11}[10^{-11} Pa^{-1}]$	$\pi_{12}[10^{-11} Pa^{-1}]$	$\pi_{44}[10^{-11} Pa^{-1}]$
n-Si	-102.2	53.7	-13.6
p-Si	6.6	-1.1	138.1

Table 1.2: Piezoresistance coefficient for bulk silicon given in [18].

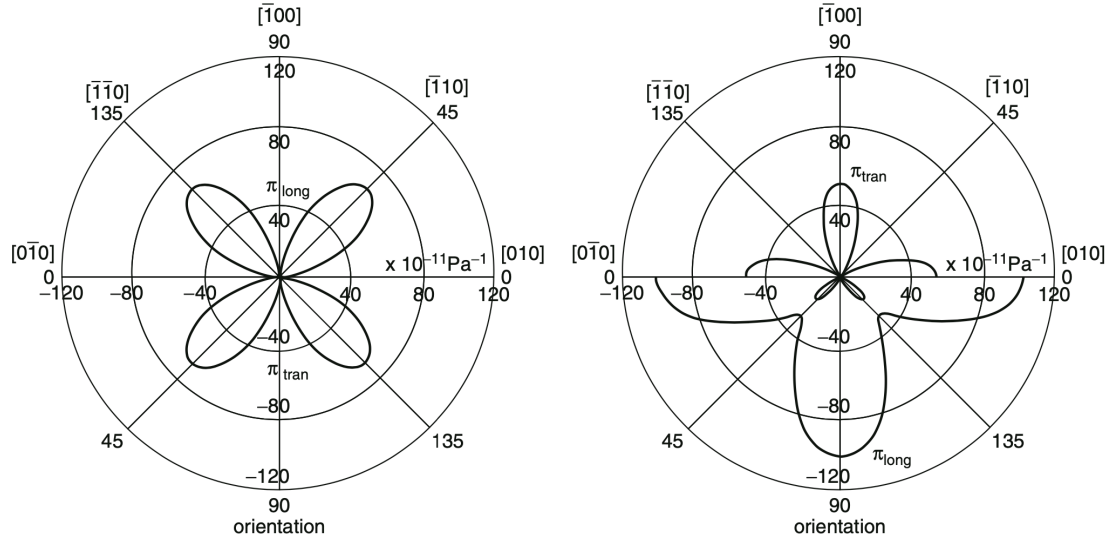


Figure 1.12: Plots of the longitudinal and transverse piezoresistance coefficient in the (100) plane for a p- (left) and n-type (right) Si. Plots reproduced by [24] from [22].

1.3.2 Piezoresistor configurations

If there exist a specific crystalline direction where π_l and π_t are comparable but have opposite sign, the piezoresistors can be arranged in a bridge circuit. In this configuration, the bridge ideally exhibits zero offset voltage, and the output voltage is directly proportional to the input force applied.[18] From the previous section, one can deduce the optimal piezoresistor configurations for a (100) p- or n-type silicon shown in Figure 1.13 with their bridge representation.

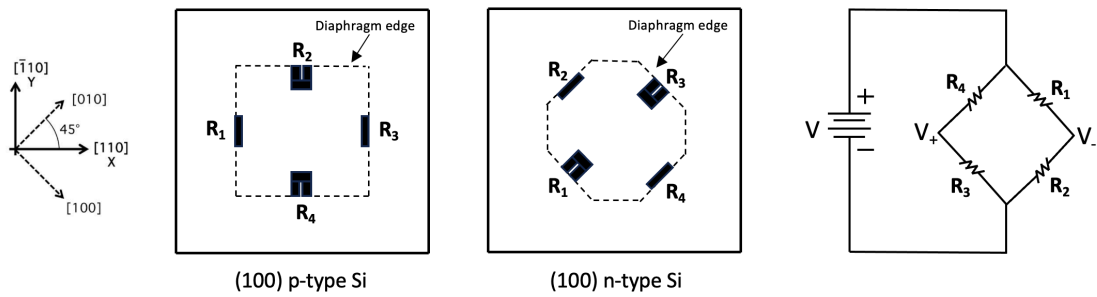


Figure 1.13: Top view of (left) a piezoresistive sensor for (100) p-type silicon and (middle) a piezoresistive sensor for (100) n-type silicon, both example with a square membrane. (Right) Representation of their Wheatstone bridge circuit. The four piezoresistors are placed on the membrane and form the resistance of the Wheatstone bridge. Illustrations inspired from [25]

For the (100) p-type silicon, the piezoresistors are placed on the membrane such that R_1 and R_3 experience transverse stresses whereas R_2 and R_4 experience longi-

tudinal stresses. On the other hand for the (100) n-type silicon, the piezoresistors are placed on the membrane such that R_1 and R_3 experience longitudinal stresses whereas R_2 and R_4 experience transverse stresses. As a consequence of these stresses on the resistors the resistance of R_1 and R_3 decreases while the one of R_2 and R_4 increases.[25] When the piezoresistors are connected in a Wheatstone bridge configuration the output of the bridge is given by the following equation :

$$V_{out} = V_+ - V_- = \left[\frac{R_2 R_4 - R_1 R_3}{(R_1 + R_2) \cdot (R_3 + R_4)} \right] \cdot V \quad (1.27)$$

where V_{out} and V represent the measured output and supply voltages. Under ideal conditions, when the piezoresistors are in an unstressed state, they all have equal resistances and opposite polarity, resulting in a zero output voltage. However, in practical scenarios, an offset voltage can be present even without pressure due to mismatches in resistor values and built-in stresses.[25]

Regarding the shape of the diaphragm, also called membrane, whose edges are visible for both configurations in Figure 1.13, they are designed to deform under applied pressure and induce maximal bending stresses at its borders expressly where piezoresistances are located which results in variation in the resistance due to the piezoresistive effect described previously. Numerous studies exist regarding the stress distribution depending on the shape of the diaphragm and corroborate the optimal diaphragm shapes depicted in Figure 1.13.

1.3.3 Membrane deflection theory

This section covers the of membrane deflection theory and is mainly based on the Practical MEMS book [26] for the analytical expressions of maximum deflection and stresses when a pressure difference is acting on a circular or a square diaphragm. Several hypothesis are made when it comes to this analysis : it is assumed that the deflection is small in comparison to the diaphragm thickness, the diaphragm itself is typically made of polycrystalline silicon or silicon nitride and it does not take into account any residual stress already present in the material or any additional component superposed to the membrane.

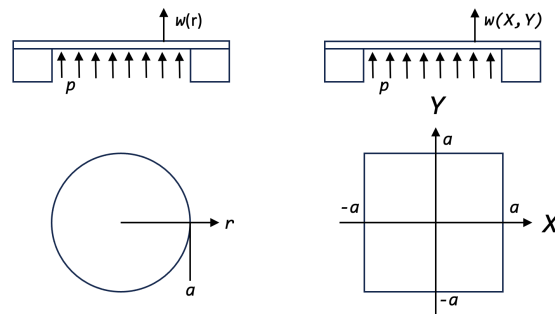


Figure 1.14: Pressure sensors geometries for a circular and a square membrane.

Circular membrane Considering the circular diaphragm of radius a shown in Figure 1.14 (left), the maximum deflection occurs at the diaphragm's center ($r=0$) and can be expressed as follow :

$$w(0) = \frac{3(1 - \nu^2)pa^4}{16Eh^3} \quad (1.28)$$

with ν the Poisson's ratio, p the pressure difference acting on the diaphragm, E the Young's modulus and h the diaphragm thickness. One can distinguish two stresses : the radial stress and the transverse stress on the diaphragm surface. Maximum stresses are obtained at the diaphragm edges ($r=a$) and are expressed below :

$$T_{radial} = \pm \frac{3}{4} \cdot \frac{pa^2}{h^2} \quad (1.29)$$

where the positive sign is for the lower surface whereas the negative sign is for the top surface, and

$$T_{transverse} = \pm \frac{3}{4} \cdot \nu \cdot \frac{pa^2}{h^2} \quad (1.30)$$

where the positive sign is for the top surface whereas the negative sign is for the lower surface.

Square membrane Now considering the square diaphragm centered at the origin ($X,Y=0,0$) of side length $2a$ shown in Figure 1.14 (right), the maximum deflection also occurs at the diaphragm's center located at the origin and can be expressed as follow :

$$w(0,0) \approx \frac{12(1 - \nu^2)pa^4}{47Eh^3} \quad (1.31)$$

the approximation sign denotes the fact that unlike for the circular membrane, the analysis of the square shaped membrane's deflection and stresses is only an approximation. Maximum stresses are obtained at the diaphragm edges : (X,Y) = ($a,0$), ($-a,0$), ($0,a$), ($0,-a$). For example at (X,Y) = ($a,0$) they are expressed as follow :

$$T_{XX}(a,0) \approx \pm \frac{48pa^2}{47h^2} \quad (1.32)$$

where the positive sign accounts for the upper surface and the negative sign is for the lower surface.

As mentioned above these equations assume that the diaphragm displacement is small in comparison to the diaphragm thickness which is not correct when considering thin film deflection, as is the case in this work. Indeed a membrane is called thin when its maximum deflection is larger than its thickness.[27] Furthermore it doesn't take into account residual stresses already present in the material. The exact equation for thin circular membranes with a radius a which takes into account the residual stresses can be found by finite elements method and is given below [27] :

$$p = 4 \frac{wh}{a^2} \left(\tau_0 + \frac{2}{3} \cdot \frac{w^2}{a^2} \cdot \frac{E}{1.026 - 0.793\nu - 0.233\nu^2} \right) [Pa] \quad (1.33)$$

with τ_0 the residual stress and w the deflection. Similarly the equation for thin square membranes with an edge length $2a$ is :

$$p = 13.6 \frac{wh}{(2a)^2} \left(\tau_0 + 1.61 \cdot \frac{w^2}{(2a)^2} \cdot \frac{(1.446 - 0.427\nu)E}{1 - \nu} \right) [Pa] \quad (1.34)$$

1.3.4 Sensitivity and limit of detection

Please note this section which discusses the sensitivity and the limit of detection of silicon-based piezoresistive pressure sensors is greatly inspired by a reference article [28] on figures of merit of such devices.

Sensitivity The sensitivity of the system is determined by the slope of the relationship between the output signal and the applied pressure. It can be expressed as the product of three components: the mechanical sensitivity, which is influenced by the membrane's characteristics (composition, topology), the piezoresistive effect, which depends on the materials and positions of the resistors on the membrane, and electrical sensitivity, which is associated with the circuit used, here the Wheatstone bridge. The sensitivity of a small and uniform silicon membrane of thickness h and area A , assuming small changes introduced by the pressure, is computed as follow :

$$S = \frac{\delta V_0}{\delta p} = \frac{(1 - \nu)(\pi_l - \pi_t)}{2} \cdot 0.25 \cdot \frac{A}{h^2} \cdot V_s [\mu V / Pa] \quad (1.35)$$

with V_0 the output voltage and V_s the supply voltage. Usually the sensitivity for piezoresistive pressure sensors is normalized to bias voltage, expressed as follow :

$$\frac{\delta V_0 / V_s}{\delta p} = \frac{(1 - \nu)(\pi_l - \pi_t)}{2} \cdot 0.25 \cdot \frac{A}{h^2} \cdot [\mu V / V / Pa] \quad (1.36)$$

It can be deduced that the thinner the membrane, and the wider the area, the greater the sensitivity. However this theoretical model seems to overestimate the

sensitivity of small-size membranes and underestimate it for larger ones. Apart from the membrane dimensions, the selection of the top electrode coverage area enhances the performance of the device in terms of deformation and the separation distance between the two metal electrodes also impacts the sensitivity of the device [29] but those design choices won't be discussed here.

Limit of detection The limit of detection, denoted LoD, is defined as three times the ratio between the standard deviation N of the output signal with a constant pressure input and the sensor sensitivity S . In other words it's the minimal change of pressure that induces a measurable output voltage change, hence the signal-to-noise ratio is higher than 10dB. The LoD of a small and uniform silicon membrane of thickness h and area A , with four piezoresistors place in the middle of the membrane edges, is computed as follow :

$$LoD = 3 \cdot \frac{\sqrt{\int_{1Hz}^B (S_{th} + S_{1/f}) df}}{\frac{\delta V_0}{\delta p}} [Pa] \quad (1.37)$$

considering that thermal noise with spectral density S_{th} and flicker noise with spectral density $S_{1/f}$ are the two main noise sources in silicon resistors.

Based on what has been covered so far and taking into account the previous section 1.3.3 and existing literature one can conclude that circular diaphragms display the maximum deformation while square diaphragms demonstrate higher sensitivity for the same surface area of membranes. As for the hexagonal (and by extension orthogonal) diaphragms, they exhibit more deformation than the square diaphragm and greater sensitivity when compared to the circular diaphragm which makes them a trade-off choice for sensing applications.[29] Other optimisation design exist such as pairs of peninsula-island distributed evenly around the edge center of the diaphragm and connected to silicon pedestal which creates a stiffness mutation at the gap region along the length direction of the peninsula-island to concentrate more strain energy in this region[30], but are not part of the scope of this work.

Chapter 2

Experimental methodology for MOS stack

This chapter first describes the fabrication of the four full-plate MOS stacks fabricated in order to assess the influence of Si_3N_4 at the oxide-SC interface and its annealing temperature. Therefore the structure of each sample is presented in Section 2.1 followed by the working principle of the devices used during this process that are relevant when it comes to charges induced in the materials in Section 2.2. Then each step of the fabrication process strictly speaking is detailed in Section 2.3 with dedicated section on the annealing sequence. Secondly, residual stress measurements are summarized in Section 2.4 before diving into C-V measurements of the samples and their characterization in Section 2.5.

2.1 Overview of samples structure

A schematic representation of the structure of each samples is shown in Figure 2.1 below where one can notably see the cross sections of each full-plate sample with the material of each layer and their desired thickness.

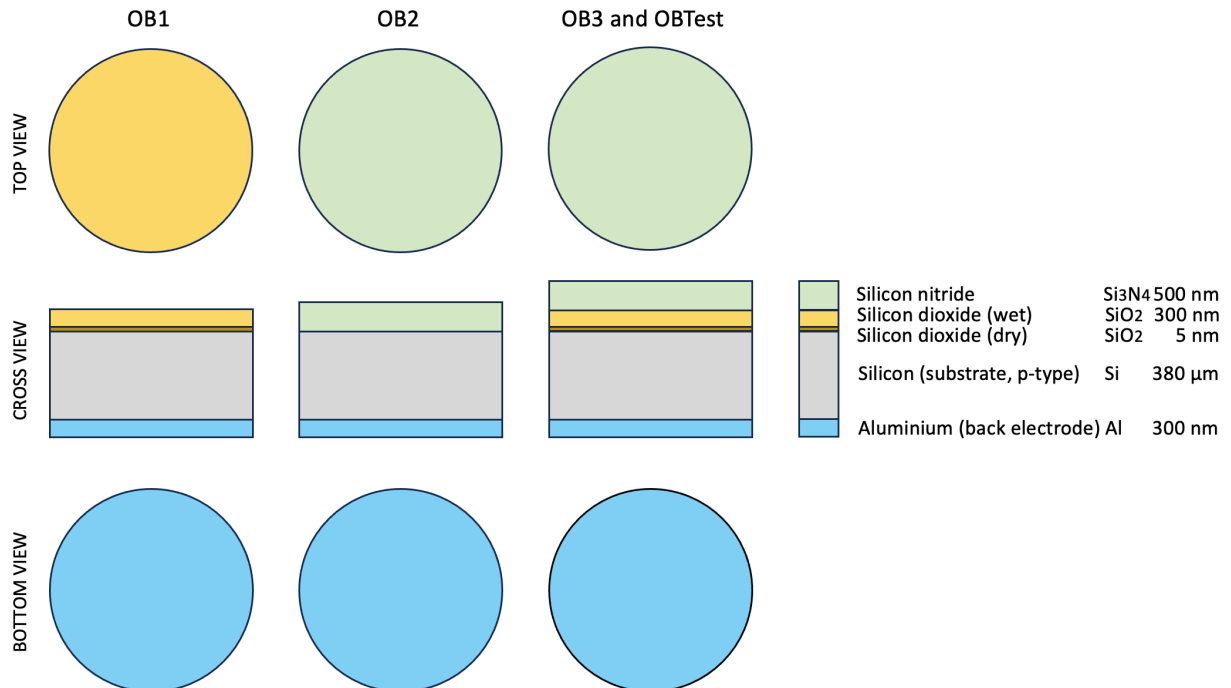


Figure 2.1: Schematic representation of the samples structure with their corresponding views, composition material and desired thickness for each layer. The four samples are denoted OB1, OB2, OB3 and OBTest.

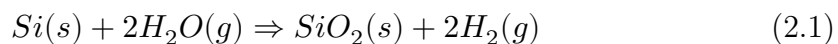
Each sample is composed of a standard 380 μ m thick p-type silicon substrate with a 300nm thick backside electrode in aluminium needed for the measurement set-up described later in Section 2.5. The first capacitor, named OB1, serves as a reference stack and has a 300nm layer of silicon dioxide grown with wet thermal oxidation on top of a thin 5nm layer of silicon dioxide grown through dry thermal oxidation. The second one, named OB2, only has a 500nm thick layer of silicon nitride deposited on top of the silicon substrate. Finally two identical samples, named OB3 and OBTest, have the same stack as OB1 with a 500nm layer of silicon nitride deposited on top of the oxide layers. The OBTest duplicate is mainly used to determine the rate of silicon nitride deposition in order to adjust the recipe according to the desired thickness.

2.2 Principle of processing techniques

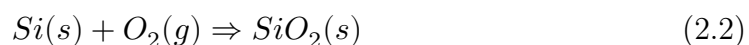
As mentioned earlier this section describes the working principle of the processing techniques used in during this fabrication which are relevant regarding charges induced in the materials and their resulting quality. Of course there are additional processing techniques used for this process which are equally important however to maintain a clear focus around the main topic of this work, the full description of their working principle is incorporated in the appendices and will be referred to in the following section when used.

2.2.1 Thermal oxidation

Thermal oxidation is a furnace operation (900-1100°C) that refers to the formation of a silicon dioxide film on the surface of a silicon wafer. This film is grown by using silicon from the bulk of the wafer itself. In contrast, deposited films acquire silicon from external sources rather than the wafer itself.[31] The differentiation is important because the characteristics of resulting Si- SiO_2 interface are greatly influenced by the method of oxide film formation. Indeed grown oxides typically exhibit a significantly lower density of electronic defects. The oxidation can either occur with dry oxygen which is called **dry thermal oxidation**, in which case the reaction is [8]:



or water, referred as **wet thermal oxidation** corresponding to the reaction below :



Since the oxidation consumes silicon atoms one has to anticipate that around 45% of the desired oxide thickness will be consumed at the surface of the silicon layer.

Moreover as the oxide layer begins to form, the oxidation rate is linearly dependant on time but starts to depend on the square root of time when the oxide thickness increases. This is because the oxygen of water molecules need more time to reach the silicon surface as the forming oxide layer becomes a barrier to oxidants. The Deal–Grove model predicts a linear oxidation rate for thin layers, followed by a parabolic behavior for thicker oxides and gives the following expression for the time as a function of the oxide thickness as a [8]:

$$t = \frac{Z}{KC_s\nu} + \frac{Z^2}{2DC_s\nu} \quad (2.3)$$

with Z [m] the oxide thickness, K , C_s [$\frac{mol}{m^3}$] the oxygen molar concentration and ν [$\frac{m^3}{mol}$] the the molar volume of silicon dioxide. The oxidation rate is much higher for wet thermal oxidation and is thus preferred for thicker films. Indeed one can produce an oxide of 130nm thick in one hour at 900°C whereas only 30nm can be grown using the dry alternative in the same amount of time.[8] Since the reactants must diffuse through the oxide layer to reach the interface where silicon atoms are available, this rate difference can be attributed to the fact that water molecules find it easier to penetrate silicon dioxide layers. However dry oxygen results in slightly denser films with better interface properties.[31]

2.2.2 Plasma Enhanced Chemical Vapor Deposition

Plasma Enhanced Chemical Vapor Deposition (PECVD) is a common process used for thin film deposition based on Chemical Vapor Deposition, referred as CVD. The underlying concept of the latter revolves around introducing the material to be deposited into the reactor in the form of a gas. However, this gas is not the direct vapor of the desired deposition material but instead serves as a precursor.[8] Through a chemical reaction occurring at the surface of the wafer, this precursor transforms into the desired final material. Figure 2.2 shows the path taken by the reactant and the extraction of the undesired products of the reaction.

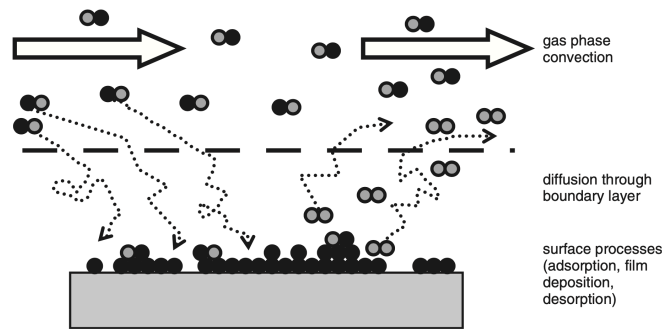
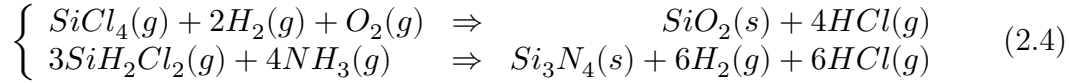


Figure 2.2: Chemical vapor deposition working principle taken from [8].

One can see hereafter typical reactions used to deposit silicon dioxide at 900°C and silicon nitride at 800°C :



CVD processes rely on a combination of chemical reactions and flow dynamics. The key variables that significantly influence the process are pressure, temperature, flow rate, and flow rate ratio. There are 2 distinct scenarios regarding the deposition defined below [8]:

- **Surface reaction limited** : Case where a high flow rate is used which ensures an ample supply of reactants for the process and the film deposition becomes limited by slow surface chemical reactions.
- **Mass transport limited** : fast surface reaction consumes source gas rapidly and the deposition rate is limited by gas supply

Since the high temperatures mentioned above are not compatible with many processes[8] low temperature alternatives have been considered among which Plasma Enhanced CVD. As indicated by the name of this technique the source gas decomposition is enhanced via plasma which ensures a sufficient quantity of reactive species even at low temperatures usually scaled down to 300°C or less. By utilizing a combination of precursor gases, such as silane, nitrous oxide, and ammonia, it is possible to deposit oxynitride (SiOxNy) films with adjustable ratios of nitrogen and oxygen. This allows for a wide range of compositions from oxide to nitride.

The PECVD system is shown in Figure 2.3 with a parallel-plate diode reactor. The reactant enters the chamber through the top electrode and it's energy is enhanced when forced through plasma before reaching the wafer positioned on a heated electrode.

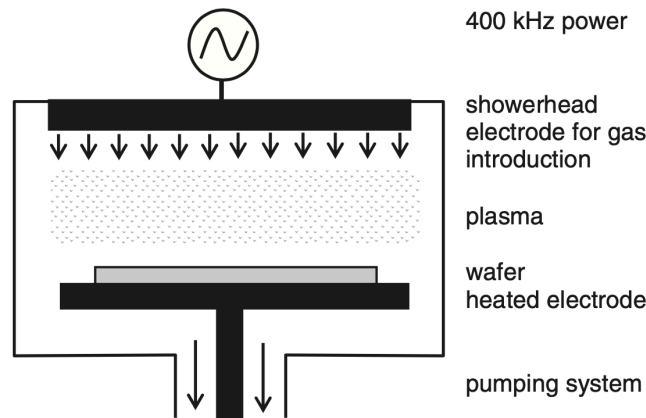


Figure 2.3: PECVD system representation taken from [8].

The typical operating frequency is 400kHz, which allows ions to effectively track the electric field due to its relatively slow pace. As a result, heavy ion bombardment occurs in the process which adds undesired openings or defects in the material.[32] Hydrogen is also incorporated in the deposited film because silane radicals are unable to give away their hydrogen due to the low temperature of the substrate resulting in a high concentration of bonded hydrogen in the form of Si-H and N-H in the case of silicon nitride.[33] Localized states can be formed within the energy bandgap of silicon nitride due to the presence of Si-H and SiNH groups. In this situation, these localized states are located more than approximately 1eV away from either of the band edges. As a result, they can function as active deep trapping or recombination centers. The density of trapping centers in silicon nitride is highly dependant on the film composition and deposition temperatures.[32] Silicon dioxide films deposited by reacting silane and nitrous oxide also contain bonded hydrogen in the form of H_2O SiOH and SiH and the resulting film properties are also highly dependant on deposition conditions.[34]

2.2.3 Plasma barrel cleaning

A barrel essentially consists in a non-directional oxygen plasma generator and is primarily used for the removal of resist or polymer layers, making it highly effective in eliminating organic materials. This dry etching is achieved through the mechanical bombardment of ions generated in the plasma onto the wafer. It selectively removes the unwanted material without affecting the silicon, silicon dioxide or metal layers present on the wafer. The procedure is sequential and that lasts 10 minutes where the operator has to increase manually the active power of the plasma. It is worth noting that a higher RF power does not always result in a higher plasma density, especially at low pressures. In fact, the additional power often leads to increased ion bombardment and the generation of hot electrons, rather than promoting ionization.[35][36]

For unmetallized Si- SiO_2 structures the extent of electrical damages due to O_2 plasma treatment depends on the exposure time, substrate temperature and the pressure of gas. A study[37] on these parameters for a planar reactor shows that most radiation damages occurs during the first 10 minutes of exposure and the ion bombardment of the samples at low pressure creates a trapping layer at the surface of the oxide which once charged will cause a shift of the C-V curves. Positive and negative charging effects also occurs as a result of the plasma treatment. It was concluded that a plasma treatment for a substrate temperature of 20°C and pressure in the range of 0.1-2Torr is less critical considering that all damages can be annealed afterwards by a low temperature annealing in H_2 . A higher temperature annealing is needed to remove the defects induced by a treatment with higher parameter value.[37]

2.2.4 Annealing metal in forming gas

Furnace annealing under forming gas refers to a heat treatment in which a material, typically a metal or SC, is heated at a defined temperature in a furnace environment containing a mixture of nitrogen N_2 and hydrogen H. This process is used to modify the properties of the annealed materials for electrical or mechanical properties improvement purposes. Indeed performing an annealing step during a process at a higher temperature than the deposition temperature has shown improvements in the film properties to a great extent.[32] In the case of an annealing of aluminium deposited on the backside of the substrate, such as silicon, performed at typical temperatures around 400-450°C the forming gas will improve the Al-Si contact by breaking any native oxide present at the interface. Hence this step ensures a good contact of the aluminium backgate.[8] The furnace operation sequence followed in the Winfab facility is described below :

1. **Furnace heating** To begin with the furnace is heated to a given temperature.
2. **N_2 flow** Once the furnace has reached the command temperature, a nitrogen flow set to 2L/min is activated in the furnace tube.
3. **Sample introduction** The samples are then placed on a glass trail and introduced horizontally in the furnace entrance. A long glass stem is used to push the trail in the back of the furnace down 57.5cm and left hanging on the trail as the doors are closed.
4. **H flow** A hydrogen flow of 10% is activated together with the nitrogen flow for the entire 30' annealing duration. It is important to note that while the N_2 flow is active during any manipulation of the trail in the furnace, the H flow cannot be active alone.
5. **Reverse steps** Once the annealing is done, the hydrogen flow is deactivated, the trail is brought back to the furnace entrance and the trail is removed carefully. The N_2 flow is then deactivated as well.
6. **Cooling** The wafers are left on the trail during 5' to cool down before undergoing any further processing.

Although the primary purpose is to anneal the metal, other composition materials will exhibit changes in properties when annealed in the Al furnace in forming gas. Indeed by exposing silicon nitride or silicon dioxide to forming gas anneals out defects at the Si_3N_4/Si or SiO_2/Si interface which helps to prevent charges from becoming trapped at the interface. However good surface passivation following a forming gas anneal is observed for high temperatures in the 700°C to 1000°C range.[38]

2.3 Fabrication process of MOS capacitor stack

This section describes the fabrication process of the 4 full plate MOS capacitors done in the Winfab facility at UCLouvain. The equipment and the relevant parameters for each step are given in Table 2.1 as well as the related samples, also named wafers hereafter. Considering this process only includes full plate layers with no pattern, the metrology measurements results of this fabrication are presented in the next section 2.4 for the residual stress assessment.

Step	Sequence	Parameters	Sample
1	Initial thickness measurement - Palmer	-	All four
2	Profilometer - Dektak	60", 524µm range, 12.5µm stylus	All four
3	Ellipsometer - Sentech	spectral range 400-900nm	All four
4	Standard cleaning - Wet bench	-	OB1/3/Test
5	Dry thermal oxidation - Koyo1 furnace	950°C, 5nm, 2H	OB1/3/Test
6	Wet thermal oxidation - Koyo1 furnace	1000°C, 300nm, 3H04'	OB1/3/Test
7	Ellipsometer - Sentech	spectral range 400-900nm	OB1/3/Test
8	Protective blue resist coating	4000rpm, 120", 130°C	OB1/3/Test
9	SiO_2 wet etching - BHF bath	84nm/min	OB1/3/Test
10	Plasma barrel cleaning	10', 200-500W	OB1/3/Test
11	Profilometer - Dektak	60", 524µm range, 12.5µm stylus	OB1/3/Test
12	Standard cleaning - Wet bench	no HF bath	OB2/3/Test
13	Silicon nitride PECVD - Oxford	300°C, 500nm, 40'	OB2/3/Test
14	Profilometer - Dektak	60s, 524µm range, 12.5µm stylus	OB2/3/Test
15	Ellipsometer - Sentech	spectral range 400-900nm	OB2/3/Test
16	Standard cleaning - Wet bench	no HF bath	All four
17	PVD thermal evaporation - VST	Al/Si 1%, 2e-7 Pvacuum, 5A/s rate, 300nm	All four
18	Profilometer - Dektak	60", 524µm range, 12.5µm stylus	All four
19	Nitric acid cleaning - Wet bench	700ml HNO_3 , 10'	All four
20	Dicing - Diamond tip	-	All four
21	Annealing - Al furnace	N2:H2=9:1, 30'	All four
22	Profilometer - Dektak	60", 524µm range, 12.5µm stylus	All four
23	Ellipsometer - Sentech	spectral range 400-900nm	All four

Table 2.1: Process sheet

To begin with four bulk silicon wafers ((100) p-type, 380µm thick, 3inch diameter) are marked on the unpolished side, which is referred to as the backside, using the diamond tip in order to be able to distinguish them throughout the process and three metrology measurements are performed to see the initial state of the wafers : thickness measurement with the Palmer, curvature measurement perpendicular to the flat edge of the wafer using the Dektak profilometer (cfr. 7.5.2) and ellipsometric scans to identify a potential layer of native oxide of a few nanometers formed on the surface of the substrate (cfr. 7.5.1). Sample OB1, OB3 and OBTest then go through a standard cleaning (cfr. 7.3.1) before being placed inside the Koyo 1 furnace trail for a succession of two thermal oxidations (cfr. 2.2.1). Firstly a thin layer of silicon dioxide SiO_2 is grown on the substrate at 950°C to essentially

improve the quality of the oxide layer at the interface. While the wafers are still in the furnace a second layer of 300nm thick silicon dioxide SiO_2 is grown with a wet thermal oxidation recipe at 1000°C. Metrology measurements are performed before the same three samples are coated at 4000rpm with a blue resist on the frontside in order to protect it while the backside oxide layer is etched away in a BHF bath with an etch rate of 84nm/min. The resist is cured for 3 minutes at 130°C. The removal of the resist is done in a barrel (cfr. 2.2.3) where the samples undergo a 10min cleaning with variable plasma power : 1min at 200W, 2min at 300W, 2min at 400W and 5min at 500W. No heating is used at this step and the pressure of the gas is roughly 0.75Torr. The resist removal is verified with the ellipsometer.

Afterwards a standard cleaning without the HF bath is performed on OB2, OB3 and OBTest and the latter is placed in the Oxford chamber to test the recipe for the deposition of 500nm of PECVD silicon nitride Si_3N_4 (cfr. 2.2.2). After adjustments, samples OB2 and OB3 are processed as well and the final parameters are the following : pressure = 1Torr, SiH_4 flux = 600sccm, NH_3 flux = 21sccm, N_2 flux = 700sccm, power = 30Watt, temperature = 300°C, duration = 40min. A careless mistake was made at this stage and the sample OB1 was processed in the Oxford chamber together with OB2 and OB3 resulting in the loss of the reference stack and the production of two identical stacks with both 300nm thick oxide and 500nm thick silicon nitride. Metrology measurements are performed and all four wafers are cleaned with a standard cleaning without the HF bath. Directly after their exit of the blue fountain each of them are placed upside down in the VST equipment and a PVD thermal evaporation (cfr. 7.4.1) is done to deposit a 300nm thick layer of aluminium Al which serves as a backgate electrode.

Finally after measuring the curve of the wafers they are cleaned with a nitric acid bath (cfr. 7.3.2) and diced using the diamond tip in order to obtain 4 rectangular strips of approximately 5x1cm per wafer with the length in the same direction as the perpendicular to the flat edge. They are numbered according to annealing temperatures as one can see in Figure 2.4 and their shape allows to still measure the curvature of the stack once diced as discussed in Section 2.4. The next section details the annealing sequence done with the Al furnace (cfr. 2.2.4) as well as the parameters for each strip set.

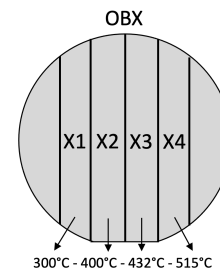


Figure 2.4: Dicing outline for sample OBX with strips numbering with regard to annealing temperature.

2.3.1 Aluminium annealing

This step is constrained by the Al furnace pre-calibrated recipes for specific annealing temperatures : 250°C, 250°C, 300°C, 400°C, 432°C, 515°C, 950°C, 1000°C. The selection of annealing temperatures for this process was based on the silicon nitride deposition temperature 300°C and the melting temperature of aluminium 660°C. Hence strip X.1 of each wafer are placed on the furnace trail and annealed at 300°C for 30 minutes with $N_2 : H_2=9:1$ gas ratio, then strip X.2 of each wafer was annealed at 400°C with the same gas ratio and so on. As visible in Figure 2.5 the trail's notches are not designed to hold strips and one had to be extra cautious for manipulation. Let's note that the rounded pieces on the edges of the wafer are not annealed but will be of use for C-V measurements, more on that in Section 2.5.1.1.

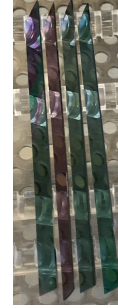


Figure 2.5: Strips X.1 positioned on the Al furnace trail for annealing.

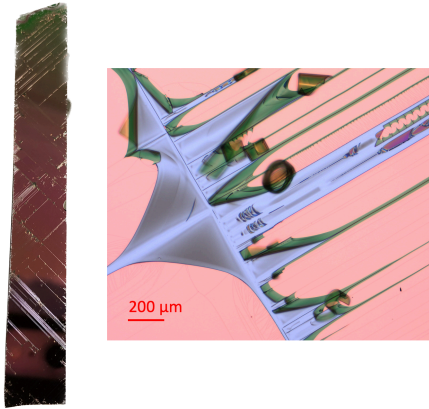


Figure 2.6: OB3.4 strip annealed at 515°C. (Left) Nitride shearing visible on frontside and (right) observations under microscope.

The strips annealed at 515°C presented linear cracks visible to the eye oriented at 45° to the orientation of the length of the strip that propagated on the entire sample until reaching another perpendicular cracks as one can see in Figure 2.6. The little strips are free to move in the x and z axis because they are no longer stuck on the substrate and not held at their ends. Delamination wrinkles were observed under microscope but no delamination blisters.[39] Apart from this qualitative analysis no further investigations were done regarding the shearing on the frontside of this batch but the residual stress is measured in the next section.

2.4 Residual stress measurements

This section aims at estimating the film stress at each step of the process especially for the annealing sequence which greatly influence the residual stress of the stack. The results of the fabrication in terms of obtained thicknesses are also included here. The residual stress within a material arises from variations in the thermal expansion coefficients among the different layers stacked on top of one another during deposition.[40] As mentioned the deposition technique has a significant influence on the residual stress and the latter can be altered through post-deposition

thermal treatments.[41] In order to have a compressive layer one will use silicon dioxide which has a compressive stress of around 300MPa regardless of the deposition technique whereas silicon nitride is usually used to obtain a tensile layer which stress can reach up to 1GPa eventhough both compressive and tensile stresses can be obtained for SiN_x layers.[42]

To assess the stress in the stack throughout the process the curvature of the wafer was measured at each step using the Dektak profilometer with the following parameters : 55mm length, 60s, 524 m range, 12.5 m stylus type. The measurements were systematically taken perpendicular to the flat edge of the wafer for reproducibility, frontside up, with the wafer suspended on three small balls for support. This measure together with the one performed at the previous step enables the assessment of the stress evolution. A commonly used equation to estimate the stress is the Stoney formula given below[43][44]:

$$\sigma = \frac{E_s h_s^2}{6 \cdot (1 - \nu_s)} \cdot \frac{1}{h_f} \cdot \left(\frac{1}{R} - \frac{1}{R_0} \right) \quad (2.5)$$

which not only depends on the radius of the measured wafer $R = \frac{(L/2)^2}{2h_{max}}$ and the previous measured wafer curvature R_0 but also on the length of the Dektak L, the thickness of the film h_f , the thickness of the substrate h_s , the Young modulus of the substrate E_s equal to 180GPa[23] for silicon and its Poisson coefficient ν_s equal to 0.27. considering this reliable formula remains an estimation the results are compared to a polynomial fitting for better accuracy of residual stresses. By fitting a second-order polynomial to the measurement data, the curvature of the wafer can be adjusted to align with the polynomial curve. Similarly, fitting a second-order polynomial to the point-by-point delta between the two reference measurements results in a polynomial where the second-order term represents the change in curvature and is used in the following equation to estimate the stress :

$$\sigma = \frac{E_s h_s^2}{6 \cdot (1 - \nu_s)} \cdot \frac{1}{h_f} \cdot \frac{d^2 P}{dx^2} \quad (2.6)$$

with P the fitted polynomial function and x the axis along which the measurement was taken. Regarding the stress measurements on the strips, the Stoney formula remains valid as long as the length of the shortest side is big against the total thickness of the film. Indeed the formula is independent of the concrete aspect ratio L/W of the rectangular strip as long as the condition $h_s \ll W$ (smaller edge of rectangular strip) is respected.[45] The results are given in Table 2.2 where both values using the curvature radius estimation and the fitted polynomial method are given for comparison. Both estimations give similar results which can be evaluated to fall within the range defined previously although the thermal oxide exhibits a stress closer to 400MPa compressive than 300MPa compressive. Measurements for the PVD thermal evaporation step are erroneous and not included below.

Step name	Measured film	Expected thickness [nm]	Measured thickness [nm]	Maximum deflection [μm]	Est. stress Stoney [MPa]	Fitted pol. stress [MPa]
OB1						
Initial measurement	-	380 μm	384.880 μm	0.537	-	-
Thermal oxidations	O	305	308.74	-7.947	-442.462	-442.460
Si_3N_4 PECVD	N	500	508.67	1.756	307.110	305.492
Anneal 300°C	NO	800	817.410	-4.093	-115.191	-104.389
Anneal 400°C	NO	800	817.410	5.808	79.814	85.540
Anneal 432°C	NO	800	817.410	12.038	202.520	205.863
Anneal 515°C	NO	800	817.410	27.500	507.060	511.506
OB2						
Initial measurement	-	380 μm	387.184 μm	0.030	-	-
Si_3N_4 PECVD	N	500	515.720	9.514	299.600	303.541
Anneal 300°C	N	500	515.720	6.369	-99.348	-106.877
Anneal 400°C	N	500	515.720	14.200	148.053	139.923
Anneal 432°C	N	500	515.720	21.300	372.360	364.800
Anneal 515°C	N	500	515.720	44.850	1116.360	1107.696
OB3						
Initial measurement	-	380 μm	390.879	-1.226	-	-
Thermal oxidations	O	305	309.130	-9.546	-446.917	-447.727
Si_3N_4 PECVD	N	500	511.390	0.349	321.287	323.996
Anneal 300°C	NO	800	820.520	-3.568	-72.855	-74.859
Anneal 400°C	NO	800	820.520	4.096	82.246	77.935
Anneal 432°C	NO	800	820.520	11.255	227.127	222.897
Anneal 515°C	NO	800	820.520	33.890	685.205	679.436
OBTest						
Initial measurement	-	380 μm	385.995	0.921	-	-
Thermal oxidations	O	305	308.190	-7.844	-460.533	-442.509
Si_3N_4 PECVD	N	500	397.070	0.204	328.167	error
Anneal 300°C	N0	800	705.89	-3.765	-84.034	-84.493
Anneal 400°C	N0	800	705.89	2.826	67.296	64.082
Anneal 432°C	N0	800	705.89	8.484	197.206	197.297
Anneal 515°C	N0	800	705.89	27.522	634.322	633.380

Table 2.2: Layer thicknesses and residual stress measurements.

2.5 C-V measurements and characterization

2.5.1 Experimental set-up

The capacitance-voltage measurements are carried out in the Welcome facility at UCLouvain by means of a Keysight B1500 Semiconductor Device Parameter Analyzer and a mercury probe station connected according to the schematic in Figure 2.8.

The mercury probe is a probing device to make rapid, non-destructive contact to a sample for electrical characterization using a concentric dot of 907 μ m diameter and ring of mercury which serves as the top electrode and a small chuck in contact with the bottom electrode of the sample ensures the backgate contact. In addition a ring vacuum system also holds the test wafer securely in position to avoid spillage of mercury. The vacuum regulator is set to 10inch Hg or 0.3Bar. The primary application for mercury probe is semiconductor measurements, without performing the time consuming metallization and photolithographic processing replaced by the mercury dot and ring. The voltage range available is limited to [-100V, 100V] which is the highest range used for this work's measurements and need to be performed with the interlock "ON". The parallel connection C_p - G_p mode is used to measure the C-V curves.

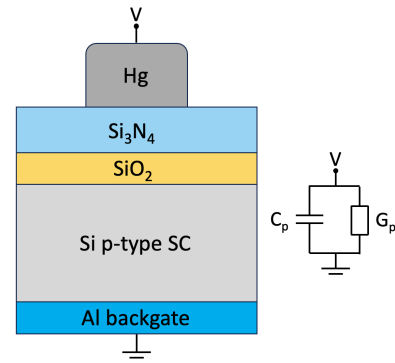


Figure 2.7: (Left) Schematic representation of the mercury probe measurement contacts with MOS capacitor OB3 : mercury dot as top electrode and aluminium layer as bottom electrode. (Right) Measurement small signal equivalent circuit.

As far as optical aspect is concerned it is not considered nor studied and therefore all measurements are performed in a dark environment obtained by lowering the lid of the mercury probe which prevents photogeneration phenomenons.

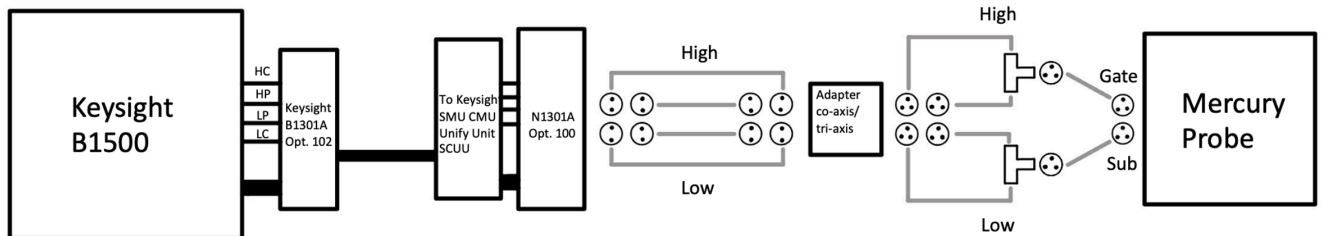


Figure 2.8: Experimental set-up schematic and cable connections of the Keysight B1500 analyser and the mercury probe.

2.5.1.1 Vacuum control for thin strips

It is important to note that some strips were too thin to fully cover the inner vacuum ring and thus were measured with their neighbouring strips on each side to ensure a proper contact. Similar measurements were performed with larger strips to make sure the neighbouring strips had a negligible impact if any on C-V measurements and it was concluded that thin strips could be measured using this set up alternative since no effects related to the neighbouring strips were observed.

2.5.2 Measurement sequence and conditions

As previously mentioned, C-V measurements with the C_p - G_p model yield two resulting parameters : the parallel conductance (G_p) and the capacitance (C_p), referred as G_m and C_m respectively. These measurements are taken for each sample across a bias range which vary according to the sample being measured but with a constant step of 200 mV. Indeed it is necessary to perform a measurement on the range full voltage range in order to be able to precisely identify the relevant range for each sample. After the completion of the voltage sweep at a specific frequency with an alternating current (AC) amplitude set to 30mV, the frequency is incremented to the subsequent step, initiating a new cycle of bias sweeps. The frequency used for this work are 1kHz, 10kHz, 100kHz and 1MHz, in increasing order. To obtain reliable values through C-V measurements, several measurement conditions must be taken into consideration :

- **Parasitic capacitance** An open circuit correction with the B1500 analyzer must be done to remove the set-up parasitic capacitance. This is all the more important in our case as there are many interconnected cables in the set-up to be able to extend the voltage range from -100V to 100V, initially limited from -42V to 42V by default.
- **Equilibrium conditions** Attaining equilibrium conditions requires an adequate hold and delay time, t_{hold} and t_{delay} respectively. A proper way to identify these timing parameters is to perform a C-V measurement with a dual voltage sweep to assess the emergence of a hysteresis characteristic. By adjusting t_{hold} and t_{delay} one is able to mitigate hysteresis effects and ensure accurate results. For this work t_{hold} is set to 10" and t_{delay} to 100m".
- **Series resistances** The maximum capacitance value observed in the stabilized accumulation region may vary with frequency. In that case a notable fluctuation becomes apparent as the capacitance consistently decreases as the frequency rises, leading to non-constant capacitance values. This phenomenon arises due to the presence of series resistances in the dielectric layers or substrate which must be de-embedded from the measured data. As these series resistances are not incorporated within the basic C_p - G_p model, a six element reconstruction model shown in Figure 2.9 is used to correct the C-V curves which suffers from frequency dispersion in the accumulation regime[46].

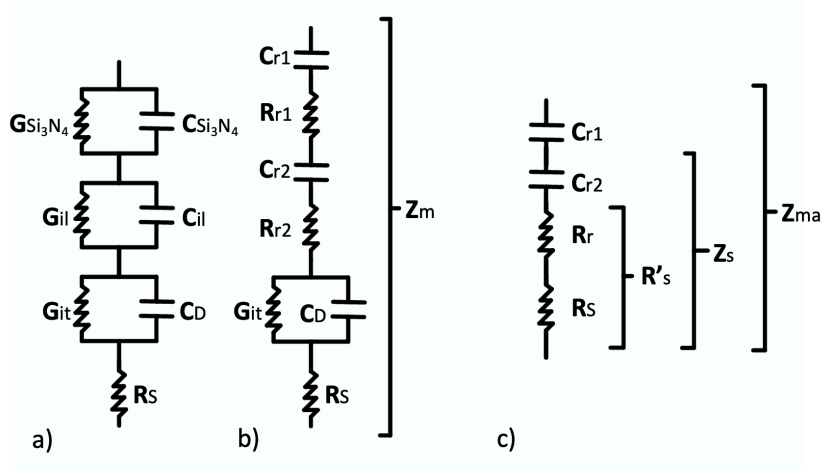


Figure 2.9: Six element reconstruction model inspired from [47] and [46] : (a) the equivalent circuit for a MOS capacitor with Si_3N_4/SiO_2 dielectric stack, (b) the simplified circuit of (a) and (c) the simplified circuit in the strong accumulation regime.

In this reconstruction model, the total series resistance is represented by R_s , G_{it} is the conductance of interface traps between the silicon substrate and the dielectric stack, C_D is the capacitance of the depletion layer, G_{il} and C_{il} model the conductance and capacitance of interfacial layer SiO_2 , $G_{Si_3N_4}$ and $C_{Si_3N_4}$ are the conductance and capacitance of the silicon nitride layer. Z_m is the simplified version of Figure 2.9 (a) and can be expressed as follow :

$$Z_m = \frac{1}{G_m + j\omega C_m} \quad (2.7)$$

where G_m and C_m denotes the **measured** conductance and capacitance. This circuit can be further simplified in strong accumulation as C_d and G_{it} can be neglected which gives the equivalent circuit in Figure 2.9 (c), where Z_s is the actual correction made to the C-V measurements. Indeed Z_c is the corrected impedance written as follow :

$$Z_c = \frac{1}{G_c + j\omega C_c} = Z_m - Z_s \quad (2.8)$$

The corrected values G_c and C_c can be obtained by identification of the real and imaginary parts of the above equations. Although this model has proven to be robust for the corrections of high accumulation frequency dispersion for a 10nm thick insulating stack composed of Al_2O_3 , a high-k dielectric, and SiO_2 [47], it failed to correct the measured C-V and G-V curves of this work. The next section discusses the hypotheses that explain why the reconstruction model proposed above does not apply for the stack of this work as well as the approach taken to extract the important parameters as accurately as possible given the absence of series resistance correction.

2.5.2.1 Impedance dynamic in measured stacks

Let's recall Equation 1.3 derived from Section 1.1.3.1 that expresses the flatband voltage V_{fb} as a function of the metal work function ϕ_m , the SC work function ϕ_s and the voltage due to the charge of the insulating stack referred as $V_{ins.}$:

$$V_{fb} = q\phi_m - q\phi_s - V_{ins.} = \phi_{ms} - \frac{Q_{ins.}}{C_{ins.}} \quad (2.9)$$

In an ideal case where no charges are present in the insulating layer, the flatband voltage is equal to the metal-SC work function difference, which absolute value typically lies between 0 and 1V. The value of the work function difference between mercury and silicon is equal to -0.435V. When charges are present in the insulating layer, the flatband voltage of the structure is shifted according to the amplitude and sign of these charges. As seen in Chapter 3, large shifts of the flatband voltage towards negative values for each measured sample is observed and indicates that a large amount of positive charges are present in the insulation layer. They might originate from the Si_3N_4/SiO_2 interface for samples OB3 and OBTest, from the Si_3N_4/Si interface for sample OB2, as well as fixed charges within the bulk of the Si_3N_4 layer and the related capacitance probably dominates every other capacitance from the stack which makes it very difficult to approximate and to correct. This means that even a small error on the estimation of this large capacitance can distort the corrections applied to the other elements of the model.

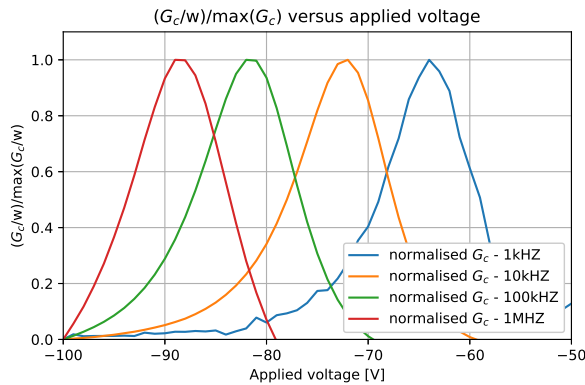


Figure 2.10: Normalized (G_c/w) as a function of the applied voltage at different frequencies for sample OB2 without annealing.

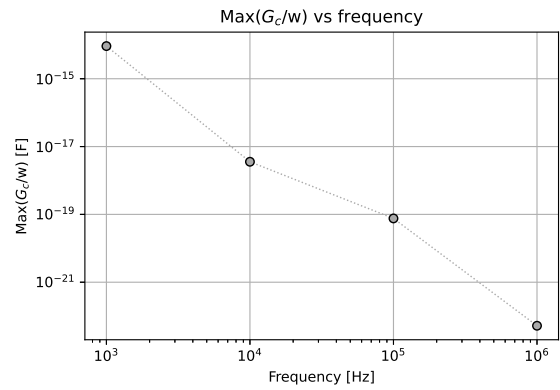


Figure 2.11: Peak amplitude of (G_c/w) as a function of the frequency for sample OB2 without annealing.

That being said, the contribution to the measured impedance at low frequency of this capacitance measured through C_m in Equation 2.7 is limited and the as-

sumption is made that the measured conductance G_m at 1kHz is the most reliable available measured data. As frequency increases, even by a small amount from 1kHz to 10kHz, C_m increases considerably which induces a drop of the conductance. This assumption is correlated by measurements of the corrected conductance over the angular which is shown in Figure 2.10 where each conductance curve is normalized by its peak value in order to see clearly how the shape of the curve is maintained and how the peak values drop exponentially as one can see in Figure 2.11. In addition the curve is shifted towards lower negative values as the frequency increases.

2.5.2.2 Flatband voltage extraction

The flatband voltage is extracted from C-V measurements using the second derivative method described in Section 1.1.3.1 applied on the raw measured capacitance at 1kHz. A practical example of this extraction is shown in Figure 2.12 where one can see the evolution with voltage of the capacitance from sample OB2 annealed at 515°C. Both the first derivative and the second derivative with regard to voltage of this measured capacitance is superimposed on the graph of C_m to illustrate the method where one can identify the bias value of the first point where d^2C_m/d^2V is zero. In the given example, the intersection point is framed and corresponds to a flatband voltage $V_{fb} = -59.35V$.

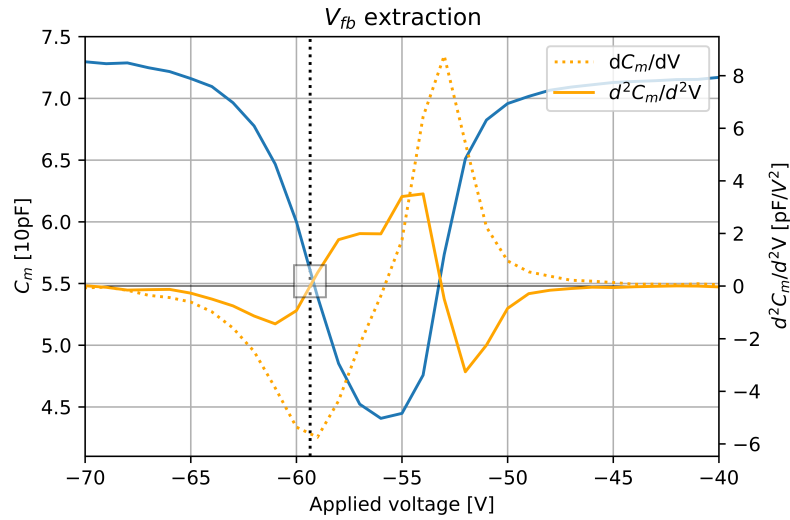


Figure 2.12: Flatband voltage extraction using the second derivative method from C-V measurement at 1kHz of sample OB2 annealed at 515°C.

2.5.2.3 Fixed charge Q_f [cm^{-2}] estimation

The total fixed charges of the dielectric stack, either composed of Si_3N_4 for sample OB2 or composed of $\text{Si}_3\text{N}_4/\text{SiO}_2$ for samples OB1, OB3 and OBTest, can be estimated with Equation 1.4 derived in Section 1.1.3.1 which is given below for reference :

$$Q_f = \frac{\phi_{ms} - V_{fb}}{q} \cdot C_{ins.} \quad [\text{cm}^{-2}] \quad (2.10)$$

where $\phi_{ms} = -0.435\text{V}$ is the metal-semiconductor work function difference between mercury and silicon, V_{fb} is the flatband voltage extracted according to the second derivative method, $C_{ins.}$ [F cm^{-2}] is the total capacitance of the insulating layer of dielectric taken as the maximum value in the stable part of the accumulation regime at 1kHz normalized by the mercury probe surface area and $q = 1.602\text{e}-19$ C is the elementary charge. Although the above equation gives an exact value of the fixed charge amplitude the relevant information to retrieve from this estimation is the sign of this total fixed charge as it gives the direction of the electrical field created by these charges within the insulating layer.

2.5.2.4 Interface traps density D_{it} [$\text{cm}^{-2}\text{eV}^{-1}$] estimation

Both methods described in Section 1.1.3.2 are used to estimate the value of the interface traps density between the insulating layer and the silicon SC. As discussed in this section, the occupation of interface traps mainly undergoes changes due to the capture and emission of majority carriers in the depletion region of the SC, where the density of minority carriers is significantly low. The presence of interface trap levels becomes evident through the alterations in their occupancy which are stimulated with the small alternating AC voltage of 30mV applied via the mercury contact. This voltage variation leads to shifts of the band edges toward or away from the Fermi level. Consequently, the capture or emission of majority carriers takes place, inducing changes in the occupancy of the interface trap levels located within a narrow energy range centered around the Fermi level.

Conductance method As an energy loss caused by these mechanisms is measured as the equivalent parallel conductance G_p , one can extract an estimation of the interface traps density using the Equation 1.6

$$D_{it} = \frac{2.5}{q \cdot A} \cdot \left(\frac{G_m}{\omega} \right)_{max} \quad (2.11)$$

where $\omega = 2\pi f$ is the angular frequency, A is the mercury electrode area equal to 0.00646 cm^2 and $(G_m/\omega)_{max}$ is the maximum value of the measured conductance peak normalized by the angular frequency. The measured conductance normalized by the angular frequency for sample OB2 without annealing is shown in Figure 2.13

where one can see the conductance peak above the flatband voltage of -65V at 1kHz and the shift of the peaks towards lower negative values for higher frequencies.

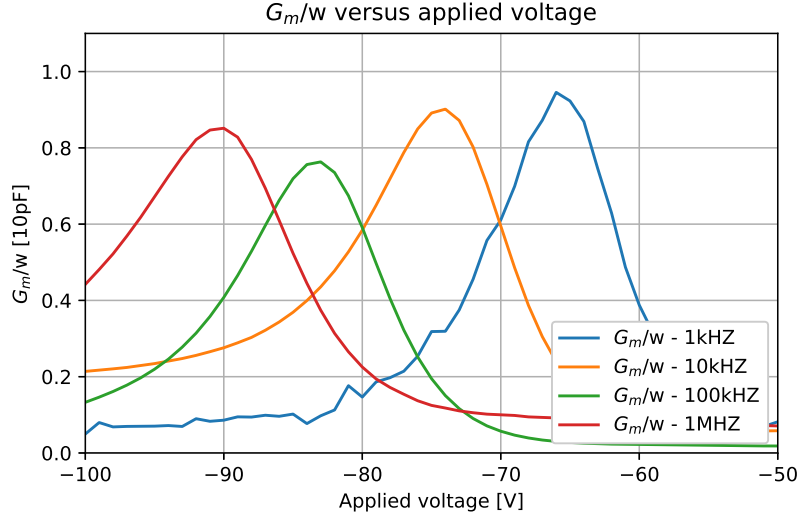


Figure 2.13: (G_m/w) as a function of the applied voltage at different frequencies for sample OB2 without annealing.

The peaks dispersion with frequency occurs for each measured samples with or without annealing and the maximal value of (G_m/w) for 1kHz is selected to estimate the D_{it} through the conductance method.

High-low frequency method The high-low frequency method is also used to estimate the interface traps density as to compare it with the previous estimation using Equation 1.7 :

$$D_{it} = \frac{C_{ins.}/A}{q^2} \cdot \left(\frac{C_{lf}/C_{ins.}}{1 - C_{lf}/C_{ins.}} - \frac{C_{hf}/C_{ins.}}{1 - C_{hf}/C_{ins.}} \right) \quad (2.12)$$

where C_{lf} is taken as the minimum value of C_m at 1kHz in the depletion regime and C_{hf} being the C_m value at 1MHz at the same voltage. However, given the uncertainty on the capacitance data measured, these estimations are less reliable.

Chapter 3

Results of C-V measurements for the MOS stacks

This chapter presents the results obtained for C-V measurements described in Section 2.5 as well as the relevant conclusions for pressure sensors.

3.1 Parameters extraction

The strips from samples OB2, OB3 and OBTest were measured using the set-up described in Section 2.5 with the corresponding measurement conditions and the insulator capacitance $C_{ins.}$, either composed of Si_3N_4 for OB2 or Si_3N_4/SiO_2 for OB3 and OBTest, the flatband voltage V_{fb} , the fixed charge of the insulating layer Q_f and the interface traps density D_{it} for each sample were extracted from the C-V measurements. These results are gathered in Table 3.1 below. Note that the strips annealed at 515°C for OB3 and OBTest could not be measured due to all the delamination wrinkles which are crumbling and could easily contaminate the mercury probe.

Anneal [°C]	Ins. layer [nm]	$C_{ins.}$ [F]	V_{fb} [V]	Q_f [cm ⁻²]	$D_{it,cond.}$ [cm ⁻² eV ⁻¹]	$D_{it,HLE}$ [cm ⁻² eV ⁻¹]
OB2						
-	Si_3N_4 - 515.72	6.997e-11	-65	5.534e12	4.975e10	0.566e10
300	Si_3N_4 - 515.72	6.812e-11	-84	5.503e12	1.934e10	0.383e10
400	Si_3N_4 - 515.72	6.905e-11	-77.7	5.160e12	3.282e10	0.585e10
432	Si_3N_4 - 515.72	7.131e-11	-72.05	4.939e12	1.515e10	1.376e10
515	Si_3N_4 - 515.72	7.392e-11	-59.35	4.291e12	2.938e10	2.336e10
OB3						
-	Si_3N_4 - 511.39 SiO_2 - 309.13	3.861e-11	-32.5	1.026e12	1.031e10	5.144e10
300	Si_3N_4 - 511.39 SiO_2 - 309.13	3.737e-11	-35.7	1.275e12	0.862e10	7.868e10
400	Si_3N_4 - 511.39 SiO_2 - 309.13	3.836e-11	-27.9	9.487e11	0.863e10	5.970e10
432	Si_3N_4 - 511.39 SiO_2 - 309.13	3.852e-11	-26	1.027e12	error on G_m	6.921e10
OBTest						
-	Si_3N_4 - 398.07 SiO_2 - 308.190	4.265e-11	-24.8	1.005e12	1.210e10	3.142e10
300	Si_3N_4 - 398.07 SiO_2 - 308.190	4.335e-11	-25.3	1.043e12	1.458e10	2.805e10
400	Si_3N_4 - 398.07 SiO_2 - 308.190	4.276e-11	-24.1	1.043e12	0.672e10	3.681e10
432	Si_3N_4 - 398.07 SiO_2 - 308.190	4.316e-11	-14.55	5.893e11	0.114e10	2.198e10

Table 3.1: Parameters extraction results from C-V measurements performed on OB2, OB3 and OBTest.

Before discussing the obtained results, it is important to note that these measurements were taken on one point of each strip and additional identical C-V measurements one more than one point per strip would ensure repeatability of these results.

A typical C-V measurement obtained is shown in Figure 3.1 for sample OB2 annealed at 515°C where the three voltage regimes are clearly visible. In accumulation one can observe a mild frequency dispersion where the capacitance value tends to decrease as frequency increases. The presence of interface traps densities is supported as one can see a kink in the depletion bias voltage regime at high frequency which is a typical characteristic of D_{it} . [4] In the inversion regime one can see the total measured capacitance corresponds to $C_{ins.}$ again (quasi-static curve) at low frequency. On the other hand for higher frequency, due to the rapid variations of the voltage small-signal, carriers in the inversion layer are unable to keep pace, leading to additional increase in the depletion capacitance C_D . As a result, the total capacitance progressively decreases below the value of $C_{ins.}$ as the frequency rises. If a very high-frequency AC signal is used then even majority carriers have no time to react with the varying gate voltage anymore.

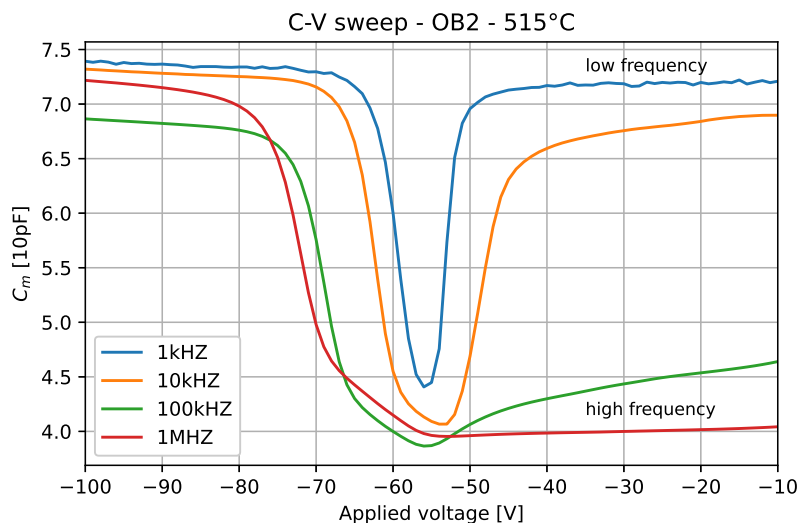


Figure 3.1: C-V sweep as a function of the applied voltage at different frequencies for sample OB2 with a 515°C annealing.

High density of positive fixed charges are present in the insulating layer as indicated by the large negative flatband voltage values. The exact densities of each defects are not defined for every sample, and it's also improbable that all defect types share identical individual densities. Nevertheless one can say that silicon nitride Si_3N_4 induces a lot of fixed charges in the insulating layer and this could be confirmed with measurements of the reference stack which is no longer available. Another behaviour confirmed through C-V measurements is the decrease of fixed charges within the insulating layer as the annealing temperature increases as one

can see in Figure 3.2 which shows the shift of the C-V sweeps for sample OBT with no anneal performed in the Al furnace on the left (dashed lines) and with an annealing at 432°C on the right. This shift is even more pronounced for sample OB2 where the insulating layer is composed of Si_3N_4 only.

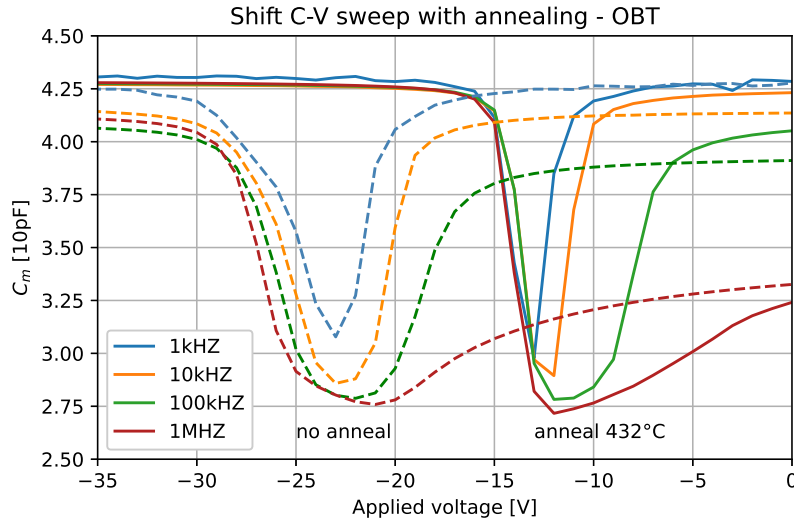


Figure 3.2: Shift of the C-V sweep as a function of the applied voltage after annealing for sample OBT.

With regard to the D_{it} estimated using both the conductance and high-low frequency method, as no correction was applied to the measured conductance and capacitance as explained in 2.5.2.1, renders the resulting values questionable although most of them lie in the $1e10 - 1e12$ [$cm^{-2}eV^{-1}$] range.

3.2 Relevant conclusions for pressure sensors

Several considerations should be taken into account for the fabrication process of the $Si_3N_4/SiO_2/Si$ -based piezoresistive pressure sensors detailed in the next Chapter 4. The backside aluminium annealing performed in the Al furnace should be done at the second highest available temperature 432°C so that the aluminium itself doesn't melt, the silicon nitride doesn't delaminate especially since the passivation layer is patterned unlike the full plate layer studied here and the fixed charges within the insulating layer are reduced as much as possible even-though the mechanical aspects have a greater impact than charges which could influence the conductivity through recombination mechanisms with the interface traps. Indeed the order of magnitude of these charges remain under the ones of the dopants dose and the piezoresistive properties of the silicon bar will still originate from the intrinsic silicon properties. In terms of the residual stress of the strips annealed at 432°C, it remains within an acceptable range for pressure sensors and a similar thickness ratio between silicon nitride and silicon dioxide should be considered.

Chapter 4

Experimental methodology for piezoresistive pressure sensors

This chapter follows a similar structure as Chapter 2 beginning with a description of the design layout and the fabrication of the dies in Section 4.1 followed by the working principle of the important devices used during this process in Section 4.2. Then each step of the fabrication process strictly speaking is detailed in Section 4.3 with intermediary results of the fabrication steps included as well. Secondly mechanical and electrical measurements and their characterization are detailed in Section 4.4 and 4.5, respectively.

4.1 Overview of samples structure

This process is a variant of an existing sample structure shown in Appendix 7.1 which was designed by Nicolas André and Thibault Delhayé as part of the project called "Biocloud". This project was started five years ago at UCLouvain and notably involved 8 unfinished wafers namely p-ONO1, p-ONO2, n-ONO1, n-ONO2, p-ON1, p-ON2, n-ON1, n-ON2. The prefix p- or n- refers to the dopant type of the silicon bars constituting the piezoresistors and the letters refer to the stack of silicon dioxide (O) and silicon nitride (N). Each wafer was located and five of them left hanging at the same stage were recovered for this work : p-ONO2, n-ONO1, n-ONO2, p-ON1, n-ON1. For a matter of convenience regarding the existing process sheets, markings on the wafers and traceability of the steps carried out on each of them, the previous names were kept even though they don't reflect the proper stack of the wafers which composition material and thicknesses were altered for this work. Nevertheless the prefix related to the dopant type is accurate since doping steps were already done as it will be discussed at the beginning of Section 4.3. As for the design layout of the piezoresistive pressure sensors processed in this work all the existing masks from "Biocloud" were used and an additional mask denoted "PASSIVATION" was designed to create openings on the metal pads through the silicon nitride passivation layer.

Element	Thickness [nm]	Length [μm]	Width [μm]
Membrane	1650	2/1/0.5mm	2/1/0.5mm
Si bar (rectangular mesa)	200	104	20
Si bar (u-shaped mesa)	200	≈ 176	20
Contact hole (mesa)	260	3	3
Al Pad	500	250	250
Al lines (on membrane)	500	-	≤ 20
Contact pad	1000	240	240

Table 4.1: Main dimensions of the design layout elements for a typical die.

The design layout is given below in Figure 4.1 with the 3inch wafer outlines visible in black. The pattern of interest which is repeated sixteen times within the layout contains thirty-two $3 \times 3 \text{ mm}^2$ dies. On the upper part one can find the design optimized for n-type silicon piezoresistors connected in a Wheatstone bridge, denoted with a "N" in the specific name of the design, with three intermediary membrane sizes : "BIG" $2 \times 2 \text{ mm}^2$, "MED" $1 \times 1 \text{ mm}^2$, "SMALL" $0.5 \times 0.5 \text{ mm}^2$. The membranes are typically squares or octagons (indicated with a "0" in the name). The design optimized for p-doped silicon piezoresistors are on the lower part of the pattern and has the same characteristics indicated before. One can also see a small column located in the middle of the layout in Figure 4.1 (left) which is another repeated pattern composed of four dies that will not be studied in this work but can be found in Appendix 7.4 for completeness.

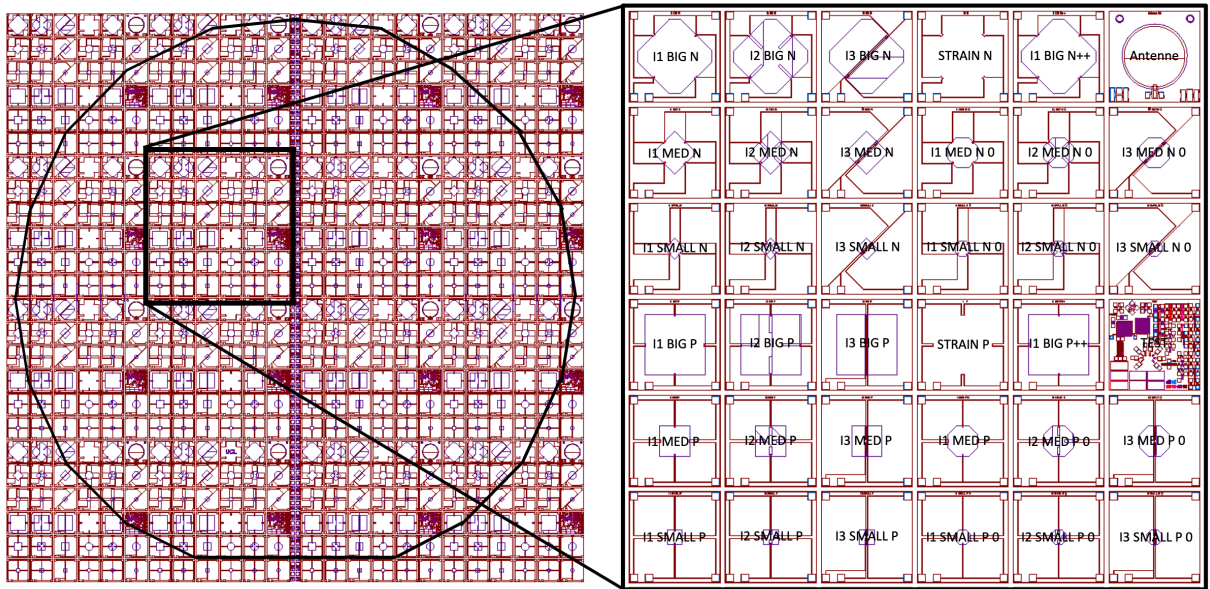


Figure 4.1: Biocloud design layout from Klayout with all masks superposed, (left) full layout and (right) layout of the repetitive patterns which includes 36 $3 \times 3 \text{ mm}^2$ dies.

The 6 masks used for this process are listed in Figure 4.2 with the die "I1 SMALL P" taken as an example and the dimensions of the main components of the design are given in Table 4.1 above. The "PASSIVATION" mask designed specifically for this work using Klayout included square-shaped openings centered above each metal pad with a $5 \mu\text{m}$ margin on each side, a quality marker to assess the quality of both the mask exposition and the etching that follows, an alignment marker to ensure a proper alignment of the mask with the existing patterns on the wafer and finally alignment windows to facilitate the alignment of the mask as well.

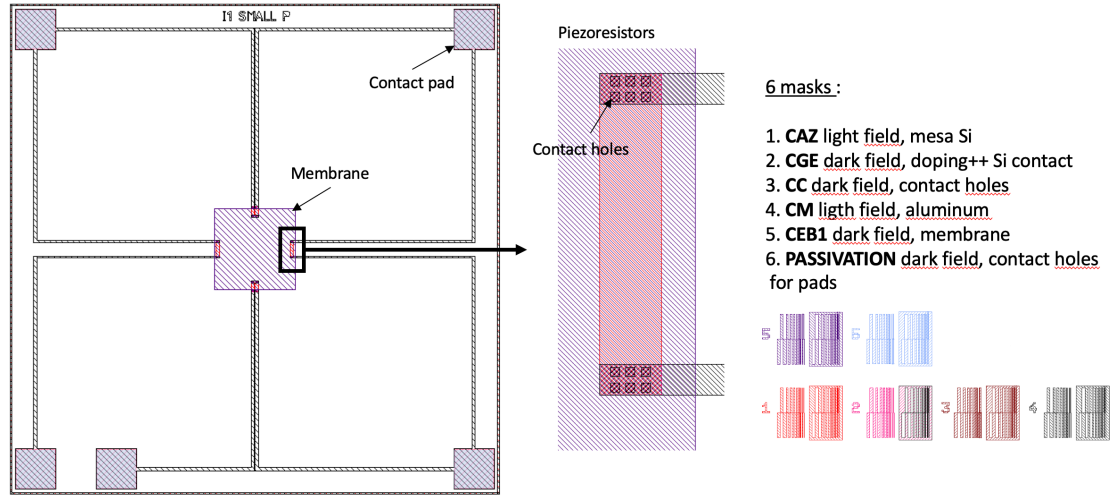


Figure 4.2: Identification of each mask based on the design layout of "I1 SMALL P" as a reference example and the quality marks located in the "Test" die, numbered and colored according to the mask.

An unscaled schematic representation of the structure of one die is shown in Figure 4.4 below where one can notably see the cross section of the die in Figure 4.3 taken vertically across the membrane through two piezoresistors (red arrow) with the material of each layer and its desired thickness. The stack is identical from one die to another (except for dies with islands and those which are not designed as membrane based sensors such as "Test", "Antenne", "Strain") and each wafer undergoes the same process steps planned as part of this work to complete their fabrication.

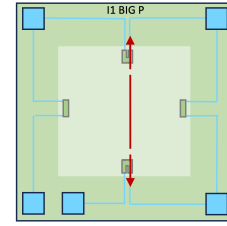


Figure 4.3: Schematic representation of the top view from a die "I1 Big P" with red arrow corresponding to the cross-section in Figure 4.4.

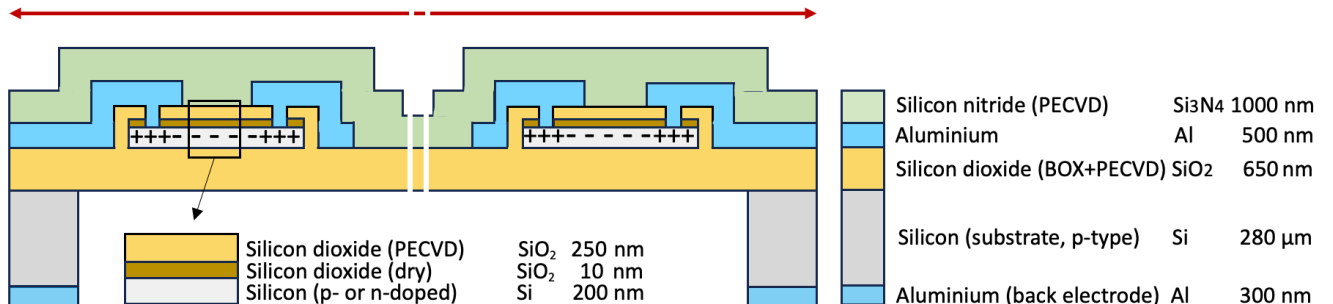


Figure 4.4: Schematic representation of the cross section of a die with composition material and desired thickness for each layer. The red arrow locates the cross-section on the schematic representation of the top view from a die in Figure 4.3.

Each finished wafer is composed of a grinded 280 μm thick p-type silicon substrate with a 300nm thick backside mask in aluminium needed for the membrane etching at the end of the process. On top of the silicon substrate lies a 400nm thick BOX of silicon dioxide stacked with a 250nm thick PECVD silicon dioxide between which lie 200nm thick silicon bars, or mesas, patterned in the stack of the initial wafer. They are doped with either p- or n-type dopants, boron or phosphorus respectively, and a small 10nm thick dry thermal silicon dioxide is grown above them. The aluminium contacts are created by patterning twelve contact holes per mesa through the oxide layers on top of the highly doped regions and depositing a 500nm thick aluminium layer that fills in the holes and reaches the silicon bar. Eventually a 1000nm thick passivation silicon nitride layer is deposited over the stack. The suspended membrane is therefore composed of silicon dioxide (650nm) stacked with silicon nitride (1000nm) for a total membrane thickness of 1650nm.

4.2 Principle of processing techniques

This section describes the working principle of the processing techniques which are relevant with regard to the fabrication of pressure sensors with a suspended membrane. Please note this section is greatly inspired from the "Introduction to microfabrication" reference book [8]. The additional processing techniques used for this process are described either in the appendices or in Section 2.2 and will be referred to in the next section when used.

4.2.1 Photolithography

Photolithography is a process used in microfabrication to create patterns on a substrate which involves the use of light to transfer a mask pattern onto a light-sensitive material called a photoresist. The latter is applied to the substrate and exposed to ultraviolet (UV) light through a photomask which contains the desired pattern. The light exposure causes a chemical change in the photoresist, either making it more soluble in a developer solution (positive photoresist) or less soluble (negative photoresist), as one can see in Figure 4.5. After the exposure, the photoresist is developed, revealing the patterned areas on the substrate. This patterned photoresist serves as a protective layer during subsequent processes, such as etching or deposition, to define specific features or circuits on the substrate. There are a few parameters which are reviewed here after to consider : the type of resist, the design of the mask and the photolithography resolution.

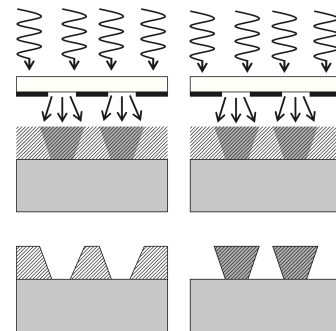


Figure 4.5: (Left) positive resist with exposed parts developed away and (right) negative resist with exposed parts hardened. Illustration taken from [8].

4.2.1.1 Photoresist type

As mentioned above the photoresist can either be positive or negative. In both scenarios, the incident light causes alterations in the polymer bonds of the resist. For positive resist, exposure leads to the breakdown of bonds, making the resist more soluble in the exposed areas. On the other hand, negative resist behaves differently and creates new polymeric bonds when illuminated which renders the resist less soluble in the exposed regions. The exposure dose, measured in $[mJ/cm^2]$, denotes the amount of light and energy necessary to bring about a sufficient modification in the resist's chemistry. This value is provided by the manufacturer and varies depending on the type of resist being used. Additionally, the range of exposure doses fluctuates based on the specific resist and its spin-coated thickness. Thicker layers of resist demand higher energy levels for effective modification. Moreover perfectly vertical resist walls are hard to achieve and positive resists usually have a slightly positive slop whereas negative resists have opposite but similar negative profile. This occurs as a direct consequence of the exposure light intensity through the mask. The phenomenon of diffraction causes certain areas of the resist to be exposed even under the opaque portions of the mask. A positive photoresist, AZMIR 701, is used in this work.

4.2.1.2 Photomask design

Photomasks are glass plates covered with an approximately 100nm thick chromium layer patterned using beam writers. Optical lithography using photomasks remains the prevailing patterning technology due to its swift performance. Indeed illumination through a photomask enables exposure of up to ten billions pixels in less than 1 second. There are several elements found on the photo-masks such as quality markers, alignment marks which are designed to allow a proper alignment with the pre-existing designs on the substrate which also come from a previous mask. In darkfield masks one can also find alignment windows which allows to see the substrate underneath the mask since chromium is fully opaque. Regarding the polarity of the mask it can either be a light of a dark-field mask. The first one is fully transparent except for the chromium patterns while the second one is fully covered with chromium with the exception of the patterns which are transparent. The choice depends on the process step and the photoresist type should be chosen accordingly as well.

4.2.1.3 Resolution

The resolution of a photolithographic process step refers to the minimum feature size that can be reliably patterned or resolved on a substrate. In other words it's a measure of the level of precision achievable during the photolithography step. The resolution depends on several parameters :

- **Wavelength of the light source λ** : in conventional photolithography, the energy driving the polymeric reaction in the photoresist is derived from

incident photons. Usually, UV wavelengths are used, with the most common being 365 nm. Proximity lithography minimum resolvable linewidth is calculated based on Fresnel's diffraction expression and approximated by the following formula :

$$"linewidth" \approx \sqrt{\lambda \cdot (g + \frac{d}{2})} \quad (4.1)$$

with g [m] the air gap between the substrate and the photomask, λ [m] the wavelength of the UV light and d [m] the photoresist thickness.

- **Working distance** : it is the exposure position selected among various options that define the distance between the substrate and the photomask. Hard vacuum, hard contact, and soft contact are common approaches used in photolithography. The highest resolutions are typically achieved when the wafer is brought into close contact with the mask using a hard vacuum. However, this method may result in mask contamination due to resist or resist peeling from the wafer if adhesion is not adequately promoted.
- **Mask quality** : the quality of the photomask used in the process affects the ability to accurately transfer patterns to the substrate.
- **Exposure dose** : the amount of light energy applied during exposure impacts the development of patterns and, therefore, resolution. Indeed over or under-exposition needs to be avoided.
- **Alignment accuracy** : the final exposition is obviously impacted by the precision with which different masks are aligned during multiple exposures.
- **Resist thickness and uniformity** : a typical resist thickness typically falls within the sub-micrometer to one-micrometer range. This ensures that the resist layer is sufficiently thick to withstand ion bombardment during most dry etching processes. Although reducing the thickness could potentially enhance resolution, it would come at the expense of a less durable resist mask, which might be more susceptible to damage during the etching process. The uniformity of the resist layer is crucial to avoid unwanted contact between the resist and the mask and to ensure a uniform exposure.

4.2.1.4 Typical process flow

Here is the typical sequence for a photolithography step :

1. **Adhesion promotion** : to promote adhesion between the wafer and the resist, the wafer is placed in an oven where it is Hexamethyl disilazane vapor (HMDS) is applied at reduced pressure on the substrate.
2. **Spin coating** : the resist is spin coated on the wafer the desired thickness can be achieved with parameters given in its datasheet. In this work either a 2.2 μm thick layer of AZMIR positive resist spin coated at 2000rpm or a 1.6 μm thick layer of AZMIR positive resist spin coated at 4000rpm is used.

3. **Soft bake (SB)** : the resist which still contains solvent is then baked to allow further processing and remove almost all solvent. A 60 seconds baking on a hot plate at 90°C are the typical parameters for this step.
4. **Exposure** : the wafer is placed on a holder and specific regions of the resist defined by the photomask are exposed to UV light.
5. **Post exposure bake (PEB)** : this baking step is intended to make the resist regions that must stay on the substrate to become more resistant during the development step afterwards. A 90 seconds baking on a hot plate at 110°C are the typical parameters for this step.
6. **Development** : the development is a very visual step during which the soluble resist is stripped away using a mild base before rinsing and drying the wafer.
7. **Hard bake (HB)** : afterward, a hard bake is performed typically for 120 seconds at 130°C to fully cure the resist by eliminating any remaining solvent. This makes the resist more robust for subsequent processing steps, including wet or dry etching.

4.2.2 Dry etching

Dry etching is a fabrication technique used to pattern and remove material from a substrate without the use of a liquid chemical etchant. Indeed a high-energy gas containing ions, also referred to as plasma, is used to react with the material and to remove it from the substrate. Plasma etching takes place within a vacuum chamber, where reactive gases are excited by RF fields. In this process, both excited and ionized species play essential roles. For instance, excited molecules exhibit high reactivity, while ionic species are accelerated by the RF field, imparting directional energy to the surface. As a result, plasma etching is a combination of both chemical (reactive) and physical (bombardment) processes, effectively removing material from the substrate. The process can be either isotropic or anisotropic, depending on the etching method used. The two main techniques are Reactive Ion Etching (RIE) and Deep RIE, which are reviewed hereafter.

4.2.2.1 RIE

In RIE, reactants are introduced into the plasma chamber. Upon ionization in the plasma, these reactants generate highly reactive radicals that have the capability to etch the targeted material. Typical RIE rates are on the order of 0.1 to 1 $\mu\text{m}/\text{min}$. It's also important to note that pure RIE barely relies on ion bombardment and is mainly chemical. This results in isotropic etching, meaning material is removed equally in all directions from the substrate. This can lead to rounded sidewalls and less well-defined features compared to anisotropic etching techniques like DRIE.

4.2.2.2 DRIE

DRIE is an extension of the RIE process designed to make deep structures with high etch rates in many materials such as silicon. The reactors have two power generators, one for generating a high-density plasma and another one for biasing the wafer electrode. This configuration allows for the use of high powers to generate active species, while enabling separate and independent control of ion bombardment using the second power source. In the chamber a combination of chemical and physical etching mechanisms occur to achieve highly anisotropic etch profiles, resulting in vertical sidewalls and well-defined features. The basic steps of DRIE involve alternating cycles of etching and passivation. Firstly, a few micrometers of silicon are chemically etched by reactive ions such as sulfur hexafluoride (SF_6). However, this is not completely anisotropic which is why a passivation layer such as octafluorocyclobutane (C_4F_8) is applied. The latter allows the deposition of a fluoropolymer protective film all over the exposed wafer. Then the second pulse of SF_6 removes the coat of fluoropolymer at the bottom and then continues to etch the substrate, while sidewalls are still protected. The two gases mentioned here, SF_6 and C_4F_8 , are well known reactant gases for silicon etching. Typical DRIE etching rates are 2 to 20 $\mu\text{m}/\text{min}$ and the etch depth can reach up to 500 μm . With regard to masks no resists can be used and one must create a hard mask such as silicon dioxide or aluminium as this process can be very demanding on the selectivity towards the mask material due to long processing time. For instance aluminium in fluorine plasmas gives very high etch selectivity because AlF_3 is nonvolatile.[48]

4.3 Fabrication process of piezoresistive pressure sensors

This section describes the fabrication process of piezoresistive pressure sensors done in the Winfab facility at UCLouvain. The equipment and the relevant parameters for each step are given in Table 4.2 for the steps already completed in the Biocloud project and in Table 4.4 for those made during this work. A full process schematic for a typical die "I1 BIG P" is given in Section 4.3.4 with a top, bottom and cross view at each step numbered according to the process sheets with the corresponding materials and their thickness. As a reminder, each wafer is intended to have the same stack except for the dopant type and concentration, and they are named p-ONO2, n-ONO1, n-ONO2, p-ON1, and n-ON1, respectively. The final results of this fabrication process are given in Section 4.3.3.

4.3.1 Process limitations - Biocloud project

As mentioned above, this process follows an unfinished production of 5 wafers taken from the Biocloud project samples hence several steps were already done and it had to be taken into account for the rest of the fabrication. Based on the data sheet recovered with the help of Nicolas André, the implantation forms as well

as metrology measurements performed on each wafer, it was possible to identify the steps performed on the samples which are given below in Table 4.2.

Step	Sequence	Parameters	Sample
1	Wafer edges polishing	3" SOI	All five
1	Diamond tip marking	-	All five
1	Ellipsometer - Sentech	Si,spectral range 400-900nm	All five
2	Standard cleaning - Wet bench	-	All five
2	Dry th. oxidation - Koyo1 furnace	950°C,25nm,45'	All five
3	External implant frontside - IBS	p-,Boron,40keV,6e12at/cm ²	p-ONO2/ON1
3	External implant frontside - IBS	n-,Phosphorus,60keV,5e12at/cm ²	n-ONO1/ONO2/ON1
4	Standard cleaning - Wet bench	no HF bath	All five
4	Degassing nitrogen - Tempress	vacuum,170mJ/cm ² ,800°C,20'	All five
4	Lithography ⊕ frontside - MA6	mask CAZ,vacuum contact,160mJ/cm ²	All five
4	<i>SiO₂</i> wet etching - BHF bath	25nm,1'	All five
4	Etching doped Si - STS- <i>SiCl₄</i>	190nm	All five
4	Ellipsometer - Sentech	Si,spectral range 400-900nm	All five
5	Standard cleaning - Wet bench	no HF bath	All five
5	Degassing nitrogen - Tempress	800°C,15'	All five
5	Lithography ⊕ frontside - MA6	mask CGE,vacuum contact,160mJ/cm ²	All five
5	External implant frontside - IBS	p++,Boron,40keV,2x2.5e15at/cm ²	p-ONO2/ON1
5	External implant frontside - IBS	n++,Phosphorus,60keV,2x2.5e15at/cm ²	n-ONO1/ONO2/ON1
5	Diffusion doped silicon - Tempress	850°C,30'	All five

Table 4.2: Process sheet - part 1

The starting wafers are 3inch SOI wafers with a 780µm thick silicon layer stacked with 400nm of silicon dioxide on top of which lies a 200nm thick silicon layer. Their thickness is assessed with the help of an ellipsometer and a standard cleaning (cfr. 7.3.1) is performed to prepare them for a thermal oxidation (cfr. 2.2.1) in the Koyo furnace. There a 25nm thick silicon dioxide layer is grown to serve as a sacrificial layer to protect the silicon underneath for the implantation step. The silicon layer is reduced of approximately 15nm during the oxidation step. Afterwards the wafers are sent to IBS for the first implantation which is done on the entire surface. For p-type wafers, p-ONO2 and p-ON1, a boron species is implanted with a 40keV energy and a dose of 6e12at/cm². For n-type wafers, n-ON01, n-ON02 and n-ON1, a phosphorus species is implanted with a 60keV energy and a dose of 5e12at/cm². Once the wafers are doped, they get cleaning through a standard cleaning without the final HF bath again and they are put in the Tempress for 20 minutes at 800°C to undergo a nitrogen degassing (cfr. 7.4.3). Right after this step, a lithography 4.2.1 is done using the "CAZ" mask with a vacuum contact and a dose of 160J/cm² which patterns the silicon piezoresistors, or mesa. First the thin dry silicon dioxide layer is etched in a BHF bath (cfr. 7.4.2) then the 185nm thick silicon is etched away using silicon tetrachloride *SiCl₄* which is a colorless, fuming liquid that is decomposed by water to form hydrochloric acid. An ellipsometer measurement is performed to ensure the silicon is removed everywhere except for the mesa. A third standard cleaning with no HF bath is done on each wafer followed by another nitrogen degassing (cfr. 7.4.3) step for 15 minutes at 800°C to prepare the wafers

for a photolithography (cfr. 4.2.1) with the "CGE" mask that patterns the highly doped regions on the borders of each mesas. Indeed one can see in Figure 4.6 the typical doping regions defined on the design layout for both rectangular and u-shaped silicon mesas. There also exist 2 die design, namely "I1 BIG N++" and "I1 BIG P++" whose highly doped regions cover the entire mesa as one can see Figure 4.7. These specific designs are supposedly less sensitive to temperature, have smaller piezoresistive coefficients and have no n+/n- or p+/p- junctions.[49]

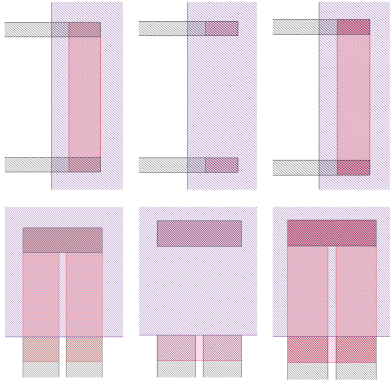


Figure 4.6: Typical doping regions for both piezoresistor structures with (left) p/n- doping regions, (center) p/n++ doping regions and (right) superposed doping regions with both masks visible.

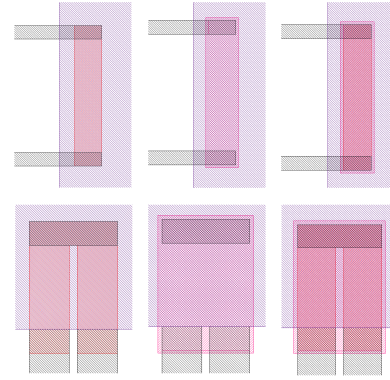


Figure 4.7: Special doping for I1 BIG N/P++ with (left) p/n- doping regions, (center) p/n++ doping regions and (right) superposed doping regions with both masks visible.

The lithography is done with a vacuum contact and a dose of $160\text{J}/\text{cm}^2$. Afterwards the wafers are sent to IBS for the second implantation. For p-type wafers, p-ONO2 and p-ON1, a boron species is implanted with a 40keV energy and a dose of $2 \times 2.5 \times 10^{15} \text{at}/\text{cm}^2$. For n-type wafers, n-ONO1, n-ONO2 and n-ON1, a phosphorus species is implanted with a 60keV energy and a dose of $2 \times 2.5 \times 10^{15} \text{at}/\text{cm}^2$.

Measured film	Expected thickness [nm]	Measured thickness [nm]				
		p-ONO2	n-ONO1	n-ONO2	p-ON1	n-ON1
SiO_2 BOX	400	401	402	402	402	400
Si	200	207	201.5	204.5	204	208
SiO_2 dry	25	26	26	26	26	26
Si post dry oxidation	190	$175 \leq t \leq 192$				

Table 4.3: Layers thickness measurements throughout the process.

Silvaco simulations for the diffusion step Based on the knowledge of the process steps performed on the wafers, it was unclear if the last step was the second implantation or the diffusion in the tempres (cfr. 7.4.3) at 850°C for 30 minutes. Considering the modified process given in Table 4.4 begins with a dry thermal

oxidation (cfr. 2.2.1) at 950°C for one hour which was not part of the previous process sheet, simulations were done using Silvaco to assess the dopants diffusion in one of the silicon bar and the resulting simulated resistance for three case study : 1 diffusion step at 850°C for 30' (base case of the initial process), 1 diffusion step at 950°C for 60' (diffusion step only in the second part of the process), 1 diffusion step at 850°C for 30' followed by 1 diffusion step at 950°C for 60' (both diffusion occur).

First let's discuss the limitations of the Silvaco software that must be taken into account and simplifying assumptions regarding the design and simulated process :

- It's not possible to distinguish a dry or a thermal silicon dioxide in the deposition process of thermal oxidation. Furthermore there is no PECVD silicon dioxide available in the material library and it was replaced by thermal oxide.
- The thickness of each material corresponds to the theoretical desired thickness as one can see in Figure 4.9 (left) but the default width of any stack is $1\mu m$ as silvaco is a 2D simulator tool. This information is crucial for the estimation of the silicon bar later on.
- For the aluminium contacts, instead of having a 2 by 3 array of $3 \times 3\mu m^2$ square contact holes, a rectangular shaped contact hole is designed with a $6\mu m$ length centered in the highly doped region as one can see in Figure 4.8.

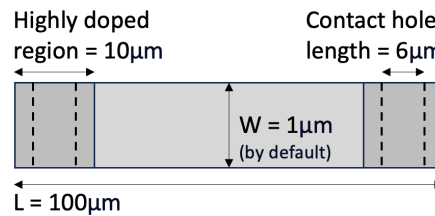


Figure 4.8: Top view representation of the simulated silicon bar with its relevant dimensions.

- For the **highly** doped regions, they have the proper theoretical dimensions and the correct doping parameters but they are doped in one step instead of 2.

The structure of the simulated stack is shown in Figure 4.9 with the doping regions shown on the right part including 4 numbered cutlines on which the absolute net doping was plotted to assess the doping levels of the silicon bar in each region of interest both vertically and horizontally. These results are shown for a n-doped silicon bar for each case study in Figures 4.11, 4.12 and 4.13. In addition to these graphs, the visual doping diffusion for each case is available in Appendix 7.2.1. The same results were produced for a p-doped silicon bar taking the same considerations into account and they are available in Appendix 7.2.2.

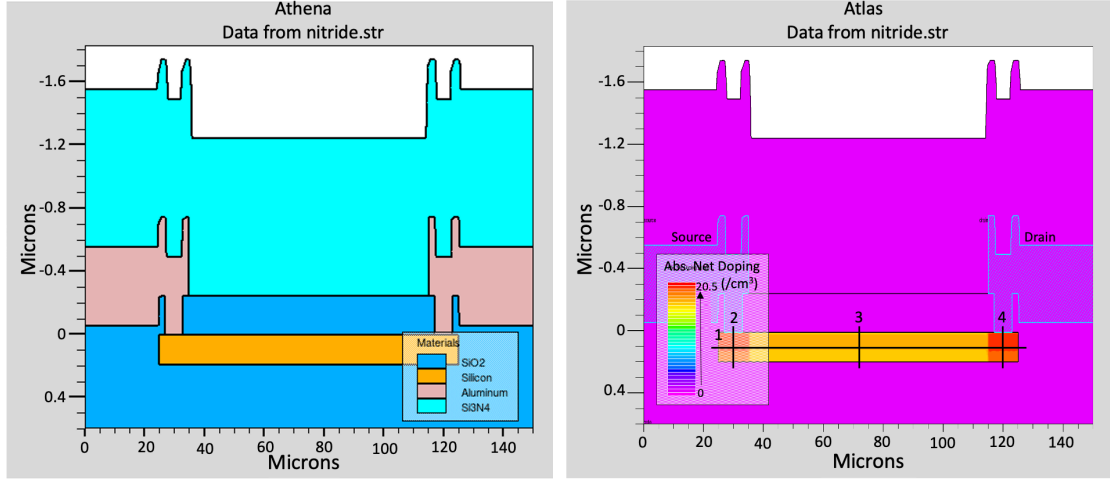


Figure 4.9: Silvaco figures of (left) the stack representation and (right) the doped regions with the numbered cutline positions of the absolute net doping graphs and the aluminium electrodes highlighted in blue.

Based on the results obtained for both doping types, one can observe the dopants tend to diffuse slightly deeper with a 60 minutes diffusion step at 950°C but the orders of magnitude of the absolute net dopings are the same. By defining the aluminium layer as two electrodes, namely source and drain, the evolution of the drain current as a function of the gate voltage sweeping from 0V to 1V was plotted and the resulting simulated resistance in the actual 20μm width silicon bars could be obtained by first computing the resistivity of the simulated bar and recompute the resistance with a 20μm width using the following formula :

$$R = \frac{\rho \cdot L}{S} \quad (4.2)$$

where ρ is the resistivity of the material, S the cross-section equal to $0.2 \times 1 \mu\text{m}^2$ in the silvaco simulation and $0.2 \times 20 \mu\text{m}^2$ in the actual bar, and L the length of the silicon bar equal to 100μm.

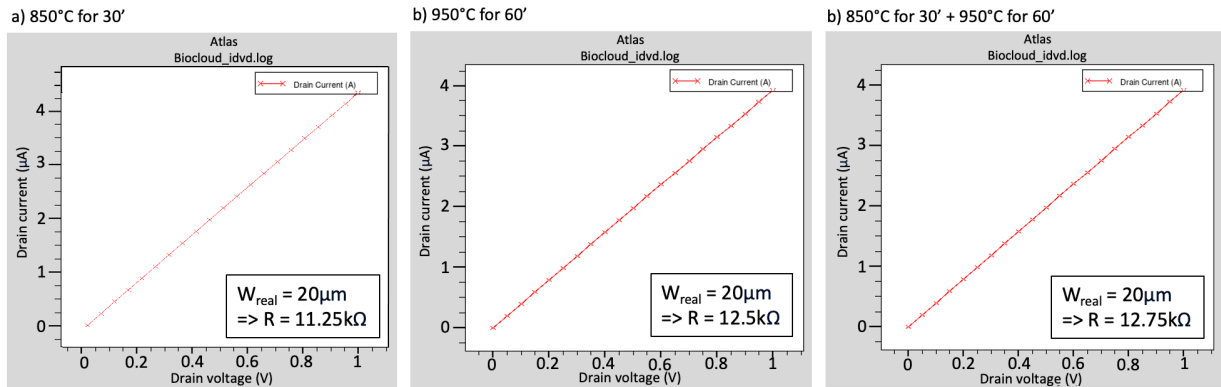


Figure 4.10: I-V plots for each case study and the resulting resistance.

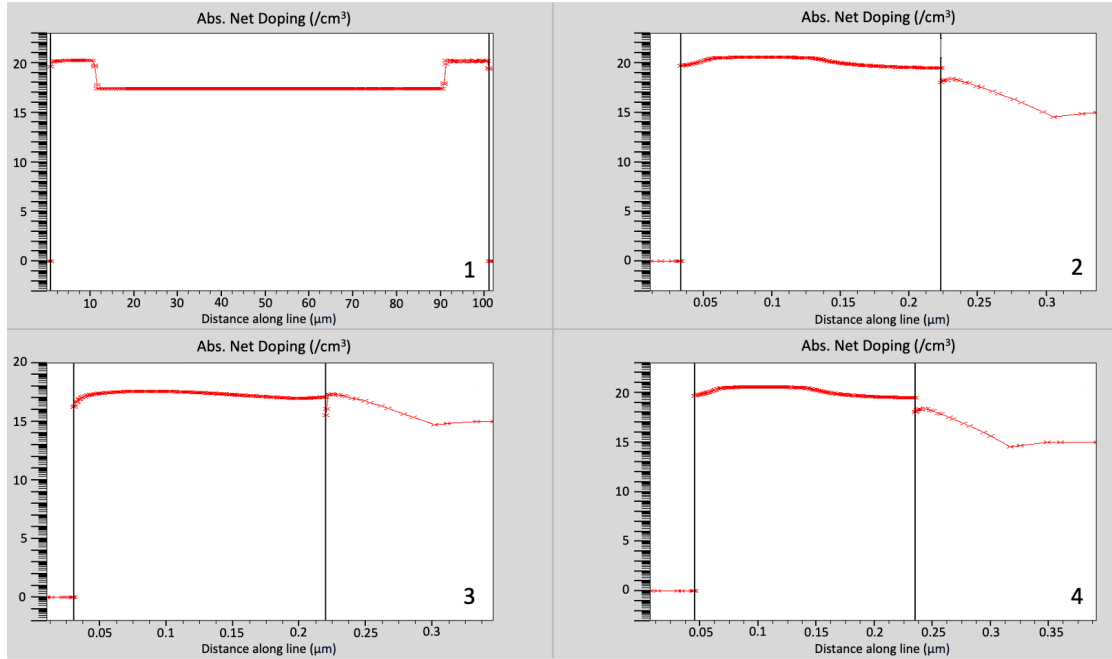


Figure 4.11: Silvaco absolute net doping simulated graphs for a n-doped silicon bar with one diffusion step at 850°C for 30 minutes. The numbers correspond to the cutlines in Figure 4.9 (right).

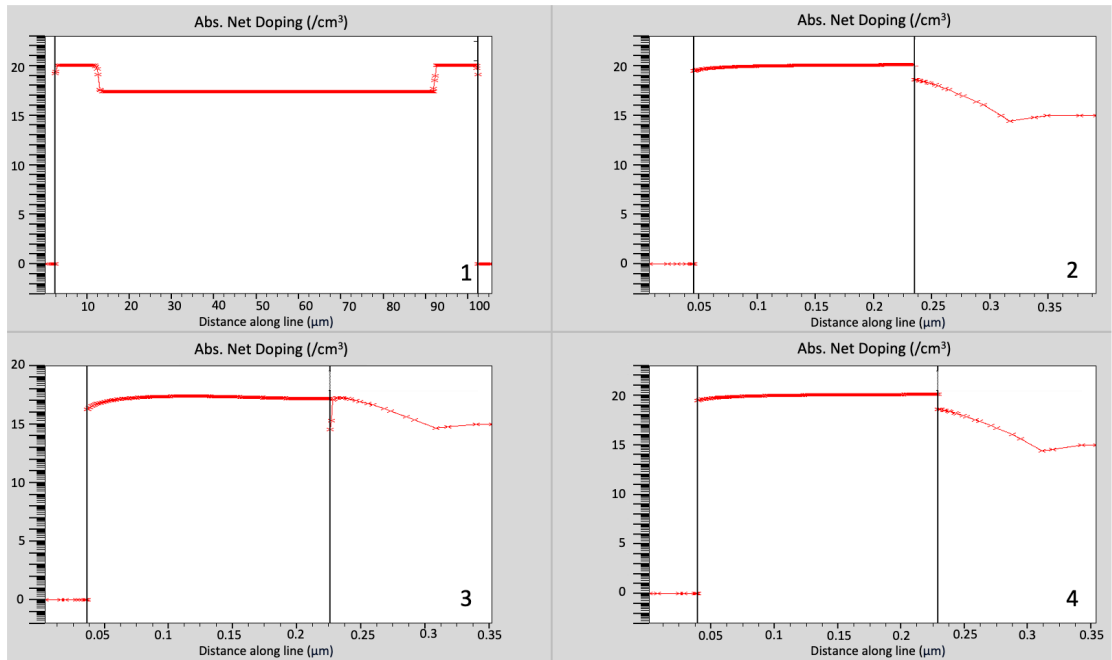


Figure 4.12: Silvaco absolute net doping simulated graphs for a n-doped silicon bar with one diffusion step at 950°C for 60 minutes. The numbers correspond to the cutlines in Figure 4.9 (right).

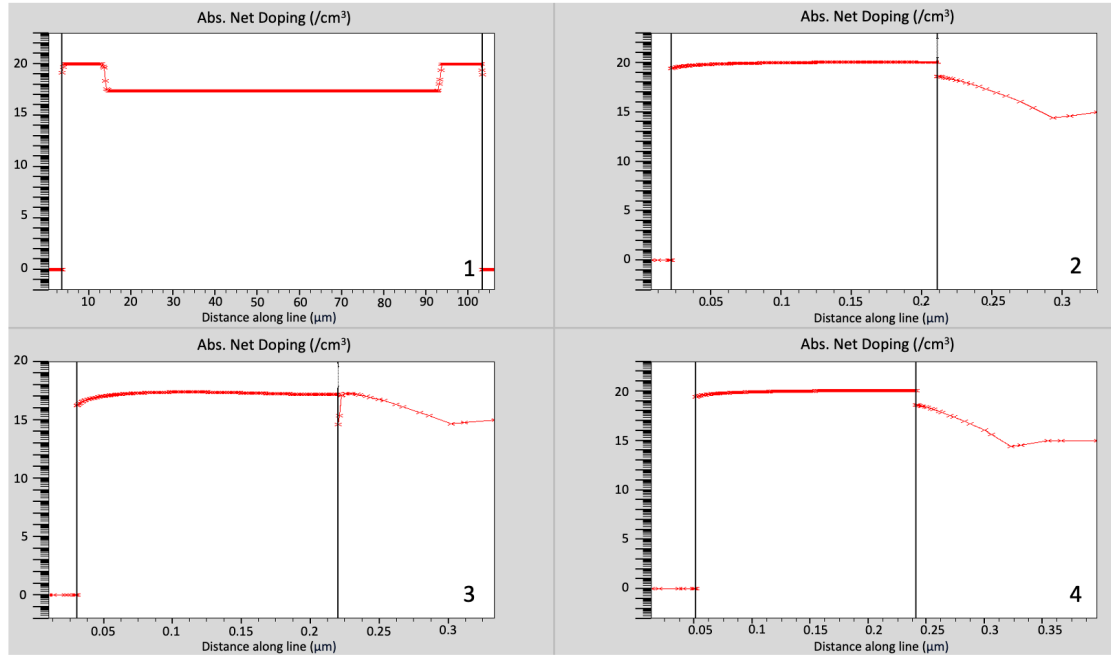


Figure 4.13: Silvaco absolute net doping simulated graphs for a n-doped silicon bar with one diffusion step at 850°C for 30 minutes followed by another one at 950°C for 60 minutes. The numbers correspond to the cutlines in Figure 4.9 (right).

According to the computed resistance values given in Figure 4.10 based on the I-V curves for each case study and to the previous diffusion results it was concluded that the process could go on as planned knowing that the diffusion in the silicon is minimal compared to the reference diffusion step at 850°C for 30 minutes and that the simulated resistance increases by less than $1\text{k}\Omega$ for both alternatives and remains in the $[1\text{k}\Omega, 50\text{k}\Omega]$ expected value range.

4.3.2 Continuation of the process

Considering this process is slightly longer then the previous ones, it includes a more extensive description of the step by step continuation of the fabrication and its intermediary results, from step 6 to 18 (cfr. 4.3.4). The full process sheet is given in Table 4.4 below.

4.3.2.1 Step 6 - Dry thermal oxidation

The five wafers were firstly submerged in a BHF bath with 87.5% ammonium fluoride and 12.5% $\text{HF}_{50\%}$ for 30 seconds in order to remove native oxide grown on the samples over time and this etched away around 80nm of the silicon dioxide BOX as well. They were then rinsed for 10 minutes in water.

After this first step observations under a microscope were made to see the doped silicon bars created during the previous part of fabrication, as one can see in Figure 4.14. Then they were all cleaned through a standard cleaning (cfr. 7.3.1) before being placed inside the Koyo 1 furnace trail for dry thermal oxydation (cfr. 2.2.1) for 2H09 at 950°C in order to obtain a 10nm thick silicon dioxide layer on top of the silicon mesas. A previous trial of the recipe on a test wafer gave a dry oxide layer of 10.26nm thick.

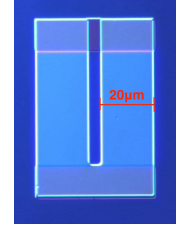


Figure 4.14: Microscope observations of a mesa on sample "n-ON1".

Step	Sequence	Parameters	Sample
6	<i>SiO₂</i> wet etching - BHF bath	native oxide,30"	All five
6	Standard cleaning - Wet bench	-	All five
6	Dry th. oxidation - Koyo1 furnace	950°C,10nm,1H	All five
7	Silicon dioxide PECVD - Oxford	300°C,250nm,6'30"	All five
7	Ellipsometer - Sentech	<i>SiO₂</i> ,spectral range 400-900nm	All five
8	Standard cleaning - Wet bench	no HF bath	All five
8	Degassing nitrogen - Tempres	600°C,15'	All five
8	Lithography ⊕ frontside - MA6	mask CC,hard contact,170mJ/cm ²	All five
8	<i>SiO₂</i> wet etching - BHF bath	th. oxide 260nm,40"	n-ON01/p-ON1 /n-ON1/p-ONO2
9	Standard cleaning - Wet bench	-	n-ON01/p-ON1 /n-ON1/p-ONO2
9	PVD thermal evaporation - VST	Al/Si 1%,500nm,40',306W,0.8A,382V,250°C	n-ON01/p-ON1 /n-ON1/p-ONO2
10	Lithography ⊕ frontside - MA6	mask CM,vacuum contact,190mJ/cm ²	n-ON01/p-ON1 /n-ON1/p-ONO2
10	Al wet etching - <i>H₃PO₄</i> bath	500nm,55°C	n-ON01/p-ON1 /n-ON1/p-ONO2
10	Test contact - [Polytec+K4200]	-	n-ON01/p-ON1 /n-ON1/p-ONO2
10	Nitric acid cleaning - Wet bench	700ml <i>HNO₃</i> , 5'	n-ON01/p-ON1 /n-ON1/p-ONO2
10	Annealing - Al furnace	N ₂ :H ₂ =9:1,432°C,30'	n-ON01/p-ON1 /n-ON1/p-ONO2
11	Silicon nitride PECVD - Oxford	300°C,1000nm,44'	p-ON1/n-ONO1
12	Lithography ⊕ frontside - MA6	mask PASS.,vacuum contact,220mJ/cm ²	p-ON1/n-ONO1
12	<i>Si₃N₄</i> dry etching - Oxford	1000nm,13'	p-ON1/n-ONO1
12	Ellipsometer - Sentech	<i>Si₃N₄</i> ,spectral range 400-900nm	p-ON1/n-ONO1
13	Resist coating - Suus Gamma 80	130°C,120"	p-ON1/n-ONO1
14	Grinding - Grinder G&N MPS 2R 300S	backside,500μm	p-ON1/n-ONO1
15	PVD thermal evaporation - VST	Al/Si 1%,300nm,24',306W,0.8A,382V,250°C	p-ON1/n-ONO1
15	Degassing oven	N ₂ ,120°C,2H30	p-ON1/n-ONO1
16	Lithography ⊕ backside - MA6	mask CEB1,vacuum contact,200mJ/cm ²	p-ON1/n-ONO1
16	Al wet etching - <i>H₃PO₄</i> bath	300nm,55°C	p-ON1/n-ONO1
17	Dicing - Tempres 602 Dicing	blue tape backside,3x3mm ² dies	p-ON1/n-ONO1
17	Si dry etching backside - Oxford	chiller -10°C, <i>SF₆</i> 120sscm, <i>C₄F₈</i> 140sscm	p-ON1/n-ONO1
18	Resist removal - Wet bench	acetone,methanol	p-ON1/n-ONO1

Table 4.4: Process sheet - part 2

4.3.2.2 Step 7 - Silicon dioxide PECVD

The next step was to deposit a 250nm thick layer of silicon dioxide PECVD (cfr. 2.2.2) in the Oxford chamber for deposition with the following parameters : 300°C, 30W, SiH_4 100 sccm, N_2O 700 sccm, N_2 1000 sccm. After a try of the recipe on a test wafer, the duration of the deposition was set to 6'30". Ellipsometer measurements indicated the resulting thicknesses given in Table 4.5. This layer serves as a stop layer for the aluminium etching later on.

Measured film	Expected thickness [nm]	Measured thickness [nm]				
		p-ONO2	n-ONO1	n-ONO2	p-ON1	n-ON1
SiO_2 BOX	400	317	332	321	326	320
SiO_2 dry	10	10.26				
SiO_2 PECVD	250	262				

Table 4.5: Layers thickness measurements for step 6.

4.3.2.3 Step 8 - Lithography $\oplus$ frontside [mask CC]

After a standard cleaning without the final HF bath the wafers were placed in the Tempress to undergo a nitrogen degassing (cfr. 7.4.3) for 15 minutes at 600°C. The following lithography (cfr. 4.2.1) sequence was then performed in the yellow room to pattern the frontside of the wafers with the contact holes on the mesas :

Step	Equipment	Parameters
Adhesion promotion	HMDS, LPIII oven	25minutes
Spin coating	SUUS Gamma 80	azmir, 4000tr/min
SB	SUUS Gamma 80	90°C, 90"
Exposure	SUUS MA6 aligner	hard-vacuum contact, 170-190-220mJ/cm ²
PEB	SUUS Gamma 80	110°C, 90"
Development	SUUS Gamma 80	180"
HB	SUUS Gamma 80	130°C, 120"

Table 4.6: Lithography $\oplus$ frontside with mask CC sequence.

After a first lithography on the wafer "p-ON1", observations under a microscope were made and diamond-shaped patterns were discovered instead of the expected $3 \times 3 \mu m^2$ square, with what appears to be small interference closer to the borders of the wafer. A first hypothesis was that the samples were under-exposed so the exposure dose was increased to 190mJ/cm² and a vacuum contact was selected for the next lithography of sample "n-ONO1" but it didn't change the shape of the observed pattern so a final increase of the dose to 220mJ/cm² was tried on sample "n-ON1" the diamond-shape pattern still remained as one can see in Figure 4.15. The pre- and post-baking temperatures didn't alter the observed shape either so it was concluded with Michael Coulombier that it was caused by the contact between the sample and the mask which was thoroughly cleaned with wipes wetted with acetone, rinsed for several minutes with isopropanol and dried with a air gun. The

masks of the following lithographies were systematically cleaned in this way to avoid such problems.

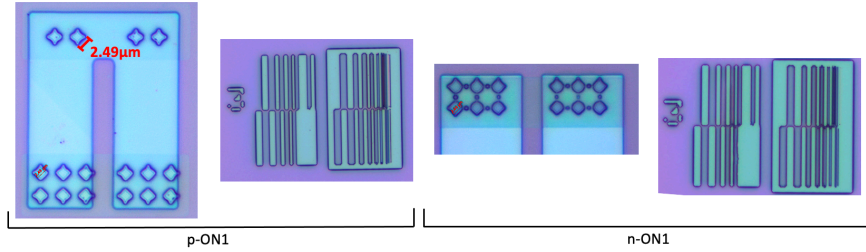


Figure 4.15: Microscope observation on sample (left) "p-ON1" with contact holes patterns close to the flat and exposure at $170\text{mJ}/\text{cm}^2$ and (right) "n-ON1" with contact holes patterns close to the alignment window and exposure at $220\text{mJ}/\text{cm}^2$. The quality mark is also shown for both sample.

The next step was to wet etch the 260nm of silicon dioxide PECVD and the underlying 10nm thick layer of dry oxide over the entire depth of the holes with a BHF bath (cfr. 7.4.2) to reach the silicon mesas. A first try was done on sample "n-ONO1" with a 40 seconds plunge to ensure the duration was sufficient to reach the silicon and didn't etch over the region defined for the holes knowing that they size only $3 \times 3 \mu\text{m}^2$. Then the rest of the samples except "n-ON1" and "n-ONO2", which was kept as a back-up wafer, were dipped in the BHF bath for 40 seconds as well. An underetch of $1.5 \mu\text{m}$ on average was observed underneath the resist as one can see in Figure 4.16.

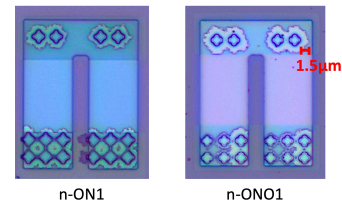


Figure 4.16: Under-etch after BHF bath shown on sample (left) "n-ON1" and (right) "n-ONO1".

4.3.2.4 Step 9 - PVD thermal evaporation frontside

The four samples together with a test wafer were then cleaned through a standard cleaning (cfr. 7.3.1) and put in the VST for a PVD thermal evaporation (cfr. 7.4.1) at 250°C for 40 minutes to deposit a 500nm thick layer of an alloy of $\text{Al}/\text{Si}_{1\%}$ on the frontside of the samples. They were placed in an oven at 120°C to degas overnight. An alloy was used to avoid aluminium spiking in the mesas.

4.3.2.5 Step 10 - Lithography $\oplus$ frontside [mask CM]

After a calibration of the parameters on the test wafer, the following lithography (cfr. 4.2.1) sequence was performed in the yellow room to pattern the frontside aluminium layer of the wafers with the aluminium contacts, lines and pads :

Step	Equipment	Parameters
Adhesion promotion	HMDS, LPIII oven	25minutes
Spin coating	SUUS Gamma 80	azmir, 2000tr/min
SB	SUUS Gamma 80	90°C,90"
Exposure	SUUS MA6 aligner	vacuum contact,220mJ/cm ²
PEB	SUUS Gamma 80	110°C,90"
Development	SUUS Gamma 80	180"
HB	SUUS Gamma 80	130°C,120"

Table 4.7: Lithography $\oplus$ frontside with mask CM sequence.

The 500nm thick aluminium was removed through an isotropic wet etching (cfr. 7.4.2) using H_3PO_4 heated at 55°C. The duration is defined by the visual aspect of the wafer which changes color as the aluminium is etched away and no more bubbles are visible in the liquid. Observations of the mesas and quality mark for each sample are shown in Figure 4.17.

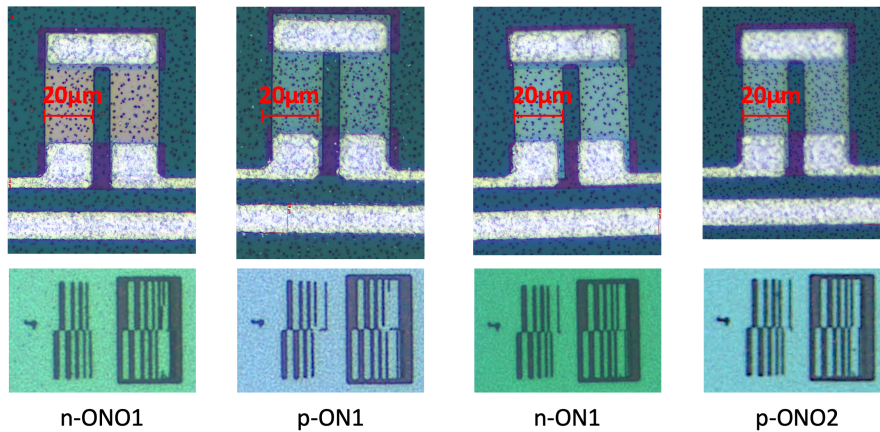


Figure 4.17: Microscope observation of the metal lines and quality mark for each sample.

Afterwards the resist was removed using acetone and isopropanol and the wafers were carried in individual Petri containers to the Welcome facility to test the aluminium contacts using the Polytec equipment together with a K4200 analyzer. Five quarter-bridge measurements which are not included here were done in different regions of each wafer : center, flat, right, left, top. Once it was established that the contacts were guaranteed on each sample, they were brought back in the Winfab facility and cleaned by plunging them in a nitric acid HNO_3 bath (cfr. 7.3.2) for 5 minutes and rinsed in deionized water for 10 minutes. The aluminium was then annealed at 432°C for 30 minutes in the Al furnace (cfr. 2.2.4).

4.3.2.6 Step 11 - Silicon nitride PECVD

At this stage of the fabrication it was decided to only process 2 wafers, "n-ONO1" and "p-ON1", for the rest of the work to still have the opportunity to change

the nitride thickness later on. A 1000nm thick silicon nitride PECVD (cfr. 2.2.2) layer was deposited on the frontside of a test wafer to adapt the recipe according to the desired thickness then of the two samples in the Oxford with the following parameters : 300°C, 44', 1Torr pressure, 600sccm SiH_4 flux, 21sccm NH_3 flux and 3Watt power. The thickness of this layer was chosen to have a similar Si_3N_4/SiO_2 ratio as for the first process of this work to ensure a resulting stress of the order of 50 to 150MPa tensile and to ease the comparison with other piezoresistive pressure sensors produced at UCLouvain which silicon nitride thickness was either 500nm or 1500nm.

4.3.2.7 Step 12 - Lithography $\oplus$ frontside [mask PASSIVATION]

After a calibration of the parameters on the test wafer, the following lithography (cfr. 4.2.1) sequence was performed in the yellow room to pattern the frontside silicon nitride PECVD layer of the wafers with the contact pad over the aluminium pads :

Step	Equipment	Parameters
Adhesion promotion	HMDS, LPIII oven	25minutes
Spin coating	SUUS Gamma 80	azmir, 4000tr/min
SB	SUUS Gamma 80	90°C, 90"
Exposure	SUUS MA6 aligner	vacuum contact, 190mJ/cm ²
PEB	SUUS Gamma 80	110°C, 90"
Development	SUUS Gamma 80	180"
HB	SUUS Gamma 80	130°C, 120"

Table 4.8: Lithography $\oplus$ frontside with mask PASSIVATION sequence.

The 1000nm thick silicon nitride layer was removed to uncover the aluminium contact pads through dry etching (cfr. 4.2.2) in the Oxford chamber using the following parameters : 5'+5'+3' successively, 10mTorr pressure, 30sccm SF_6 flux and 30Watt power. One had to be extra cautious with the timing since the resist was also damaged in the process. Observations of the pads and quality mark for each sample are shown in Figure 4.18 below.

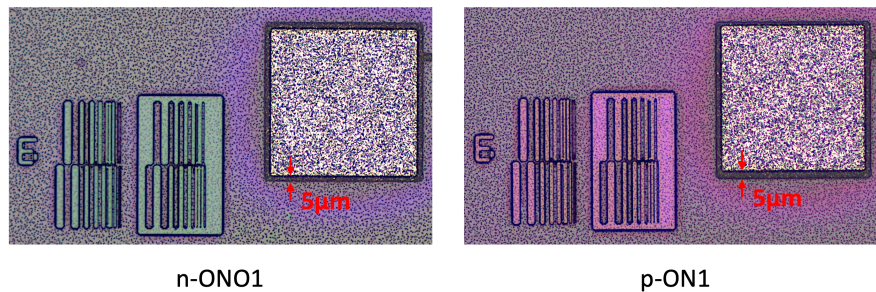


Figure 4.18: Microscope observation of the pad aperture after dry etching of the silicon nitride with the quality mark for both sample. Note the resist is not yet removed here.

Ellipsometer (cfr. 7.5.1) measurements were done on the big rectangular test zones to ensure that silicon nitride was etched all the way through and the resist was kept as an additional frontside protective layer for the following steps.

4.3.2.8 Step 13 - Resist coating frontside

Both samples were coated with a blue resist baked at 130°C for 120 seconds in the SUUS Gamma 80 to protect the frontside for the next steps of the process.

4.3.2.9 Step 14 - Grinding Si backside

The preparation of the samples for the grinding (cfr. 7.4.4) step included the previous resist coating and a blue tape covering the frontside of the samples which was placed using water to efficiently remove any air bubbles. The backside silicon layer of both samples was then successfully grinded using the GRinder G&N MPS. Thickness measurements with the Palmer before and after the grinding step allowed to deduce that a thickness of about 500µm had been successfully removed from the backside of both wafers.

4.3.2.10 Step 15 - PVD thermal evaporation backside

The two samples together with a test wafer were then put in the VST for a PVD thermal evaporation (cfr. 7.4.1) at 250°C for 24 minutes to deposit a 300nm thick layer of an alloy of Al/Si_{1%} on the backside of the samples. They were placed upside-down in an oven at 120°C to degas for 2H30.

4.3.2.11 Step 16 - Lithography ⊕ backside [mask CEB1]

The following lithography (cfr. 4.2.1) sequence was performed in the yellow room to pattern the backside aluminium layer of the wafers with the membranes :

Step	Equipment	Parameters
Adhesion promotion	HMDS, LPIII oven	25minutes
Spin coating	SUUS Gamma 80	azmir, 4000tr/min
SB	SUUS Gamma 80	90°C,90"
Exposure	SUUS MA6 aligner	vacuum contact,220mJ/cm ²
PEB	SUUS Gamma 80	110°C,90"
Development	SUUS Gamma 80	180"
HB	SUUS Gamma 80	130°C,120"

Table 4.9: Lithography ⊕ backside with mask CEB1 sequence.

The 300nm thick aluminium was removed through an isotropic wet etching (cfr. 7.4.2) using H_3PO_4 heated at 55°C. The duration is once again defined by the visual aspect of the wafer which changes color as the aluminium is etched away and no more bubbles are visible in the liquid. Observations of the membrane pattern for sample "n-ON1" are shown in Figure 4.19 where one can see streaks on

the surface materials caused by the grinding. On average the underetch observed was 750nm and the resist was left on the wafers for the following step.

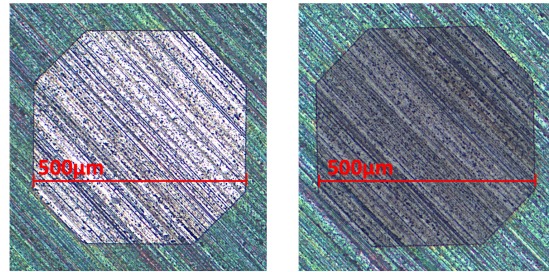


Figure 4.19: Microscope observation of the membrane patterns (left) after the lithography and (right) after the aluminium wet etching for "n-ON1" wafer.

4.3.2.12 Step 17 - Silicon dry etching backside

For the release of the membranes it was decided to proceed with 4 to 6 dies at a time to increase the control of this critical step and have higher success rates, instead of releasing the whole wafer in one go. Consequently the wafers were first diced (cfr. 7.4.5) then small batches of dies were processed in the Oxford to release their membranes. Let's recall only small sensors ($0.5 \times 0.5 \text{ mm}^2$ membrane) and big ones ($2 \times 2 \text{ mm}^2$ membrane) without islands are processed here. Nevertheless they are processed up to the releasing stage and could be subject to further processing.

Dicing In addition to the two resist layers left on the backside of the wafer, a blue tape was placed on top of it using water to remove any remaining bubbles between the resist and the tape. This tape is necessary to keep the $3 \times 3 \text{ mm}^2$ dies grouped in their initial position after they are diced using the Tempres 602 dicing equipment (cfr. 7.4.5). Note this step was exclusively done by Miloud Zitout in his technical workshop and an example of the resulting alignment of the cutouts is shown in Figure 4.20.

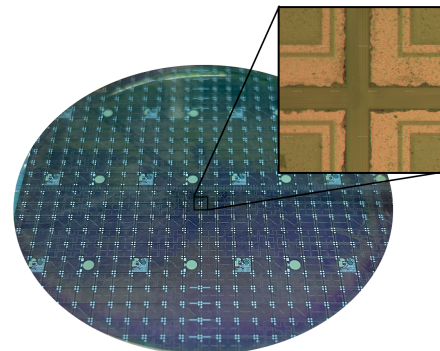
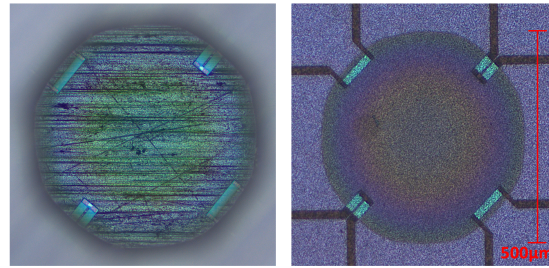


Figure 4.20: Wafer "n-ONO1" after dicing with microscope zoom on the alignment of an intersection of two cutouts.

Batch preparation First the two resist layers on the frontside of the die are removed using a small beaker filled with acetone in which they lie for approximately 1 minute before being submerged in isopropanol and rinsed with deionised (DI) water. The dies are then observed under a microscope to evaluate if the die is viable for further processing. Indeed the continuity of each aluminium line is check

as well as the overall quality of the membrane surface and the piezoresistances. Several dies are discarded at this stage because defects are identified. Afterwards an aluminium square-shaped support plate from the Oxford chamber is cleaned as well and 4 to 6 drops of blue resist are placed in the center region of the metallic support using a small pipette. The only criterion regarding the resist quantity is to put enough so that the sides of the die are covered to avoid peeling-off of the die during etching but not so much that it comes back on the back surface of the die or, even worse, on the membrane itself. The dies are dropped one by one on the resist dots upside down and the outside borders of the membrane are pressed down gently with a clamp. The support is then placed in a vacuum chamber and cycled three times from atmospheric pressure (down to 200mbar) to remove air bubbles from the resist that might be in contact with the die. Finally the resist is baked at 120°C for 180 seconds to harden it.

DRIE of the membranes Around 280 μ m of silicon must be etched to release the membrane which is done using a DRIE (cfr. 4.2.2.2) recipe from the Oxford Plasmalab System 100 equipment in the Winfab facility. This recipe has 3 phases : isotropic etching (or initial etch) of 10 seconds with a 120sccm flux of SF_6 which aims at removing any grass formation, a deposition step of 10 seconds with a flux of 140sccm of C_4F_8 which is a RIE loop for passivation, and an etching step of 14 seconds with a flux of 120sccm of SF_6 which is a RIE loop for etching. These successive steps are done with the chiller set at -10°C beforehand (20'), after a complete cleaning of the chamber with the metallic support alone (40'). The chamber cleaning is performed 1 to 3 times a day depending on the number of rounds and a conditioning is performed after each cleaning with the etching recipe for around 10cycles. The etch rate deduced from Dektak measurements was around 1.2 μ m/cycle, each cycle during approximately 25 seconds. The number of cycles per batch is not fixed but rather depends on the size of the membrane (same size membranes per batch), the presence of grass on the bottom silicon surface being etched. The typical sequence for this work was to start with 100 cycles followed with 140 cycles if no grass was observed during the intermediary microscope measurements and continue with rounds under 50 cycles until reaching the membrane. to limit overetching and avoid damaging the stop layer of SiO₂. For the few last rounds of etching the number of cycles is adapted to limit overetching and avoid damaging the stop layer of silicon dioxide. The total number of cycles for each batch won't be detailed here but it varied between 290 and 377 cycles. For an ideal etching of the membrane the uniformity of the membrane has to be assured and the best etching results obtained through this step are shown in Figure 4.21 where one can see a 11 small N 0 die from sample "n-ONO1" with the transverse piezoresistances slightly overetched and a uniform membrane surface.



n-ONO1 I1 SMALL N 0 – 301 cycles

Figure 4.21: Microscope observations of (left) the backside of a membrane from sample "n-ONO1" and (right) the qualitative aspect of the resulting membranes surface after 301 cycles.

In practice some membranes end up with an irregular surfaces because grass columns that usually grow increasingly after the last 240 cycles remain attached to the backside of the membrane or get etched in the last few cycles of the etching but it leaves numerous traces on the backside of the membrane as well. A typical grass evolution is shown in Figure 4.22 for a batch of 4 $0.5 \times 0.5 \text{ mm}^2$ membranes with different grass density and the resulting frontside membrane surface. Etching columns of grass require more cycles and lead to an overetching of the piezoresistances as shown in Figure 4.23. One can limit the development of grass in the following ways :

- Increasing the initial etch of SF_6 , set by default in the recipe to 10 seconds, up to 25 seconds. A disadvantage of this measure are more rounded corners as one can see in Figure 4.24.
- Performing an oxygen etching during 1 minute at 100Watt which removes teflon in the grass column and prevents any further growth.
- Cleaning the Oxford chamber completely both with the cleaning recipe and with a vacuum in the entry compartment of the Oxford.
- Plasma barrel cleaning of the dies which was excluded for this work due to charge introduction.

Almost every grass columns growth was successfully controlled using the three first solutions above and scanning electron microscope (SEM) (cfr. 7.5.3) observations were made to assess the quality of the DRIE etching and remaining defaults such as grass columns after the resist removal step. An example of these observations are given in Figure 4.26.

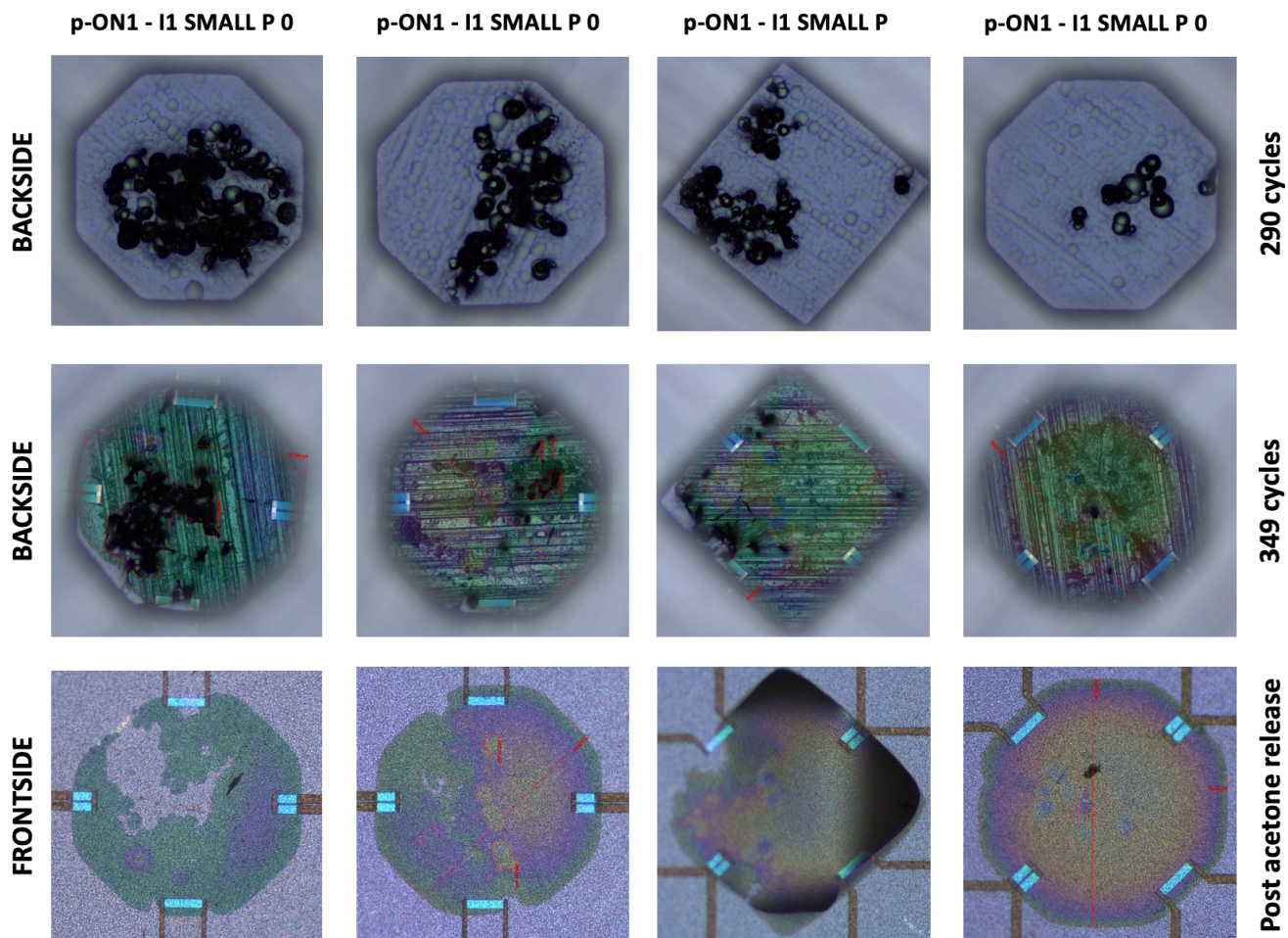


Figure 4.22: Microscope observations of the grass evolution with the number of cycles on four $0.5 \times 0.5 \text{ mm}^2$ membranes released simultaneously from sample "p-ON1" and the qualitative aspect of the resulting membranes surface.

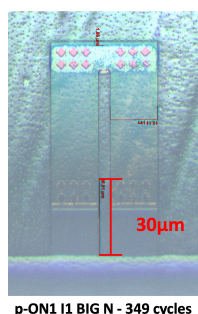


Figure 4.23: Microscope observations of the overetching done on a "p-ON1" piezoresistor after 349 cycles.

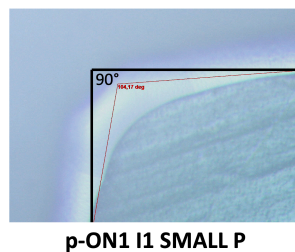


Figure 4.24: Microscope observations of the rounded corner obtained on a "p-ON1" piezoresistor after 335 cycles.

4.3.2.13 Step 18 - Resist removal frontside

The final step of this process is to release the dies from the metallic support without breaking the fragile membranes that have just been freed from the silicon substrate. Here is the list of needed material : a beaker large enough to contain the metal support on which are etched the dies, half a bottle of acetone, two watch glass (one for isopropanol and one for DI water), two cleanroom napkins (one to collect the released dies and one to dry them off after they are rinsed in DI water). The metallic support was firstly placed in the beaker filled with acetone and a cleanroom napkin at the bottom for 45 minutes to 1 hour depending on the batch as shown in Figure 4.25. While still submerged in acetone, the dies were flipped so that the frontside faces up. The napkin was then removed from the beaker and each die were placed in isopropanol for 30 seconds then in DI water for the same amount of time using the watch glasses and dried carefully with a clean napkin. Note that any contact with the frontside and more specifically the membrane surface must be avoided from the moment they detach from the metallic support. Some of the microscope observations of the membrane surface after the resist removal are available in Figure 4.21 and 4.22.

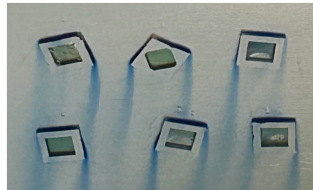


Figure 4.25: Resist removal on 6 dies submerged in acetone.

See below some of the SEM images of the backside of the die which showcase both grass columns and the signature mark of DRIE etchings : scalloped walls.

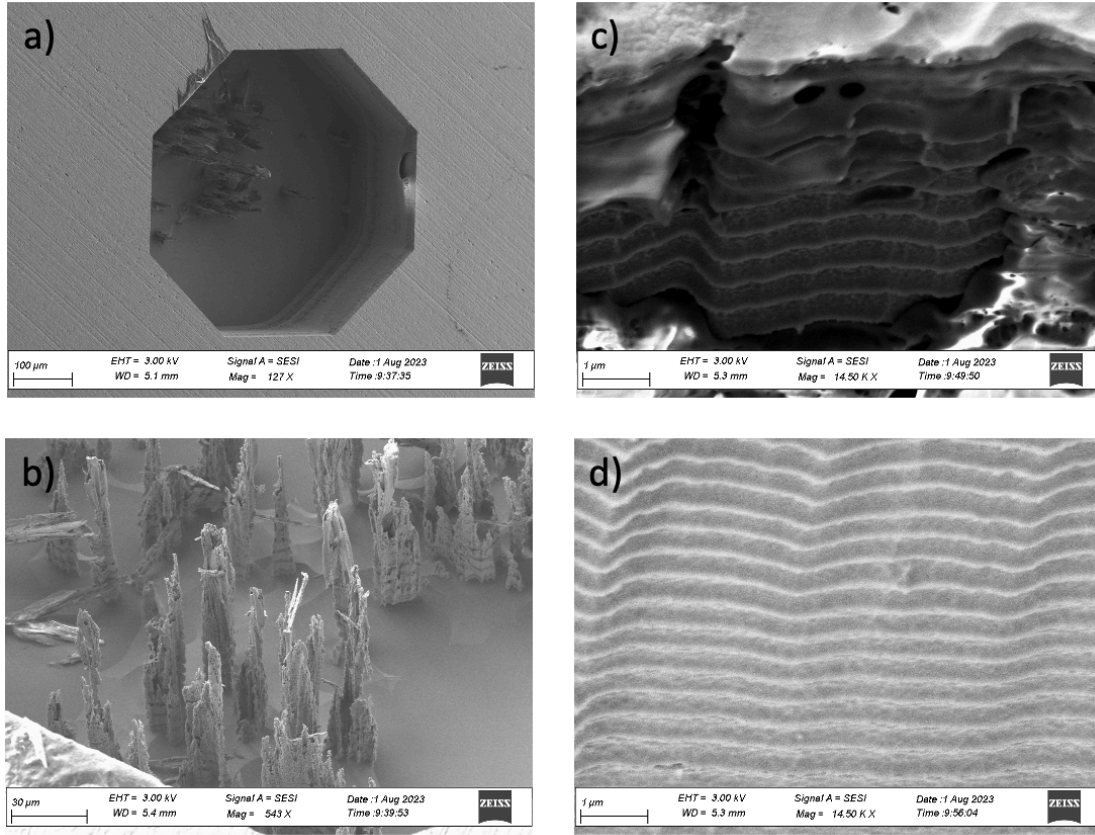


Figure 4.26: SEM observations on a "p-ON1" die (I1 SMALL P 0) : a) side-way view of the backside of the die, b) zoom from a) on the remaining grass columns still attached to the backside of the membrane, c) zoom from a) on the passivation C_4F_8 layer peeling off the sidewalls which reveals the scalloped wall surface right below the thin aluminium layer, d) zoom from c) on the scalloped sidewalls.

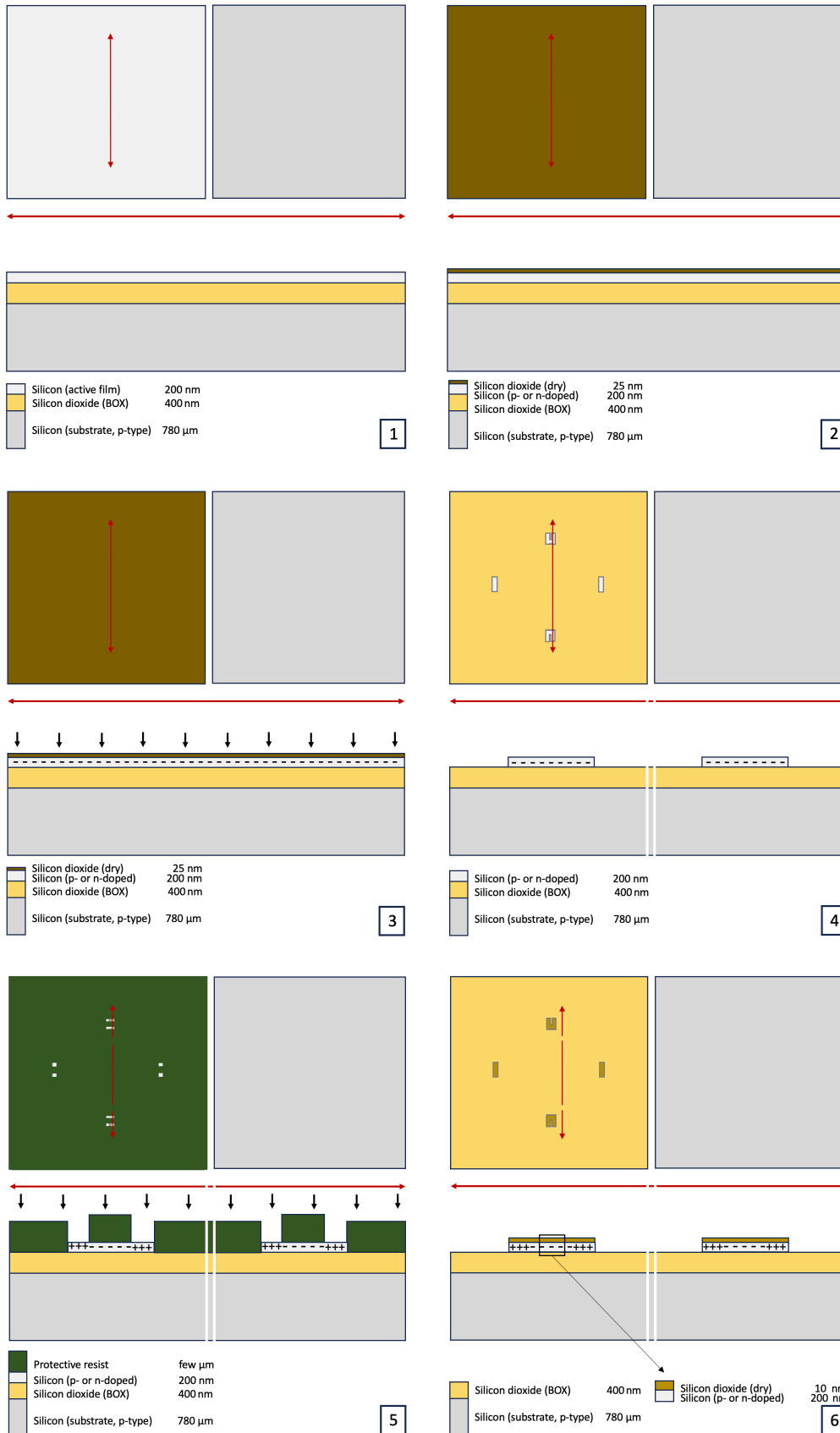
4.3.3 Process production report

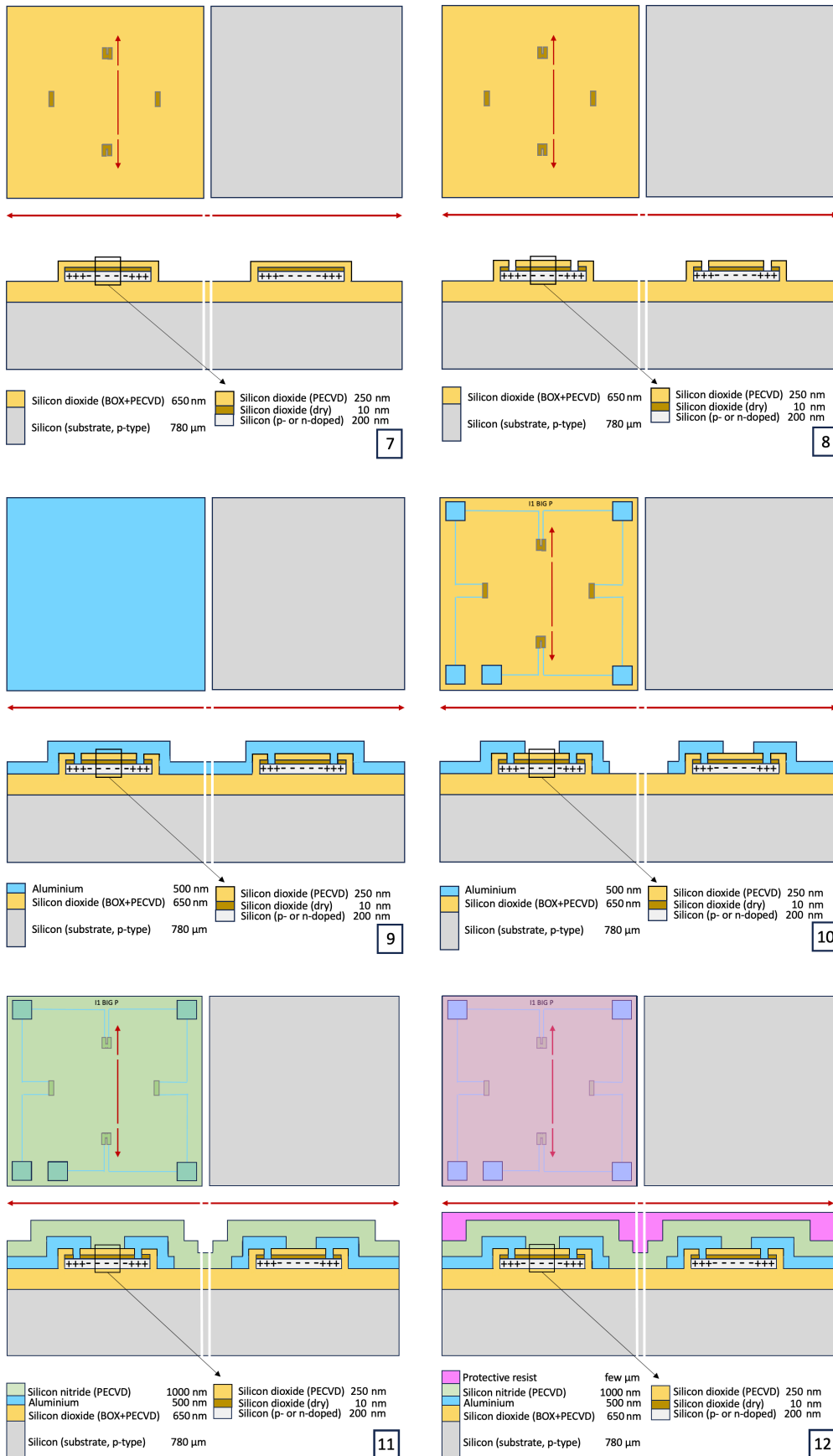
At the end of this process a total of 24 piezoresistive pressure sensors were produced which represent >85% of success rate considering only 4 dies were broken during the last step 4.3.2.13. The production was focused on the $0.5 \times 0.5 \text{ mm}^2$ and $2 \times 2 \text{ mm}^2$ membranes without islands, and each die from both samples available for measurements are listed below in Table 4.10.

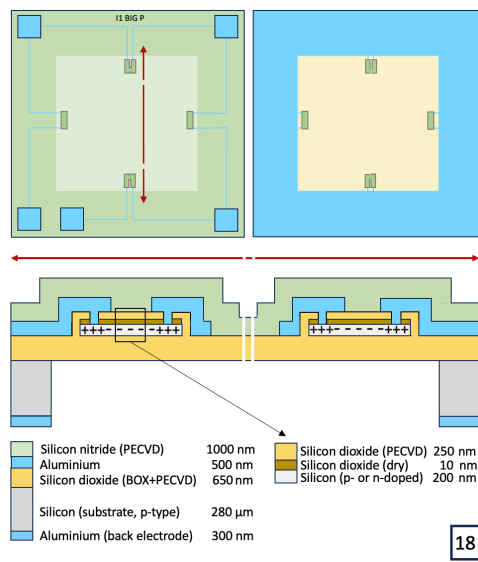
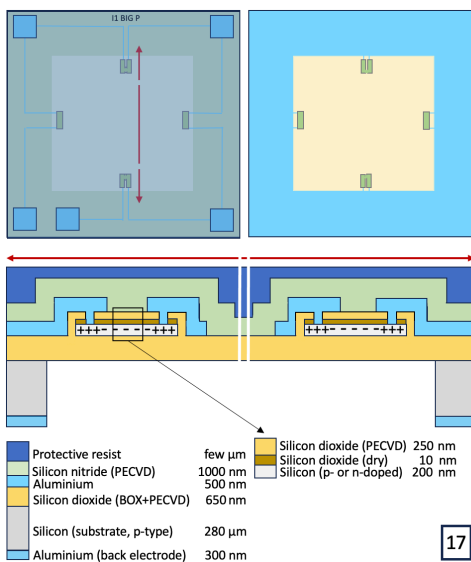
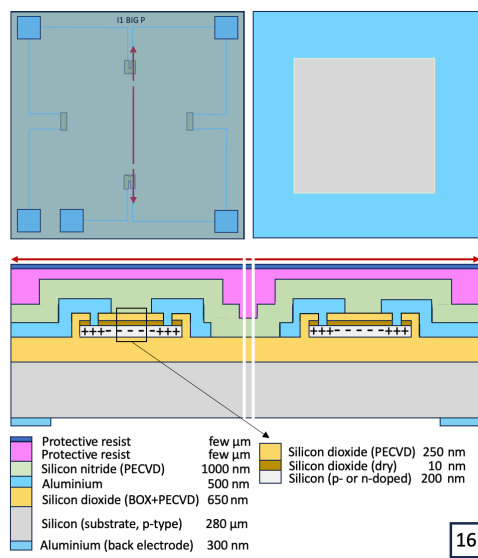
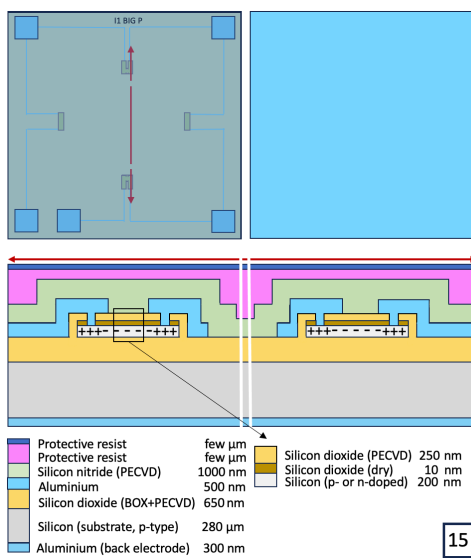
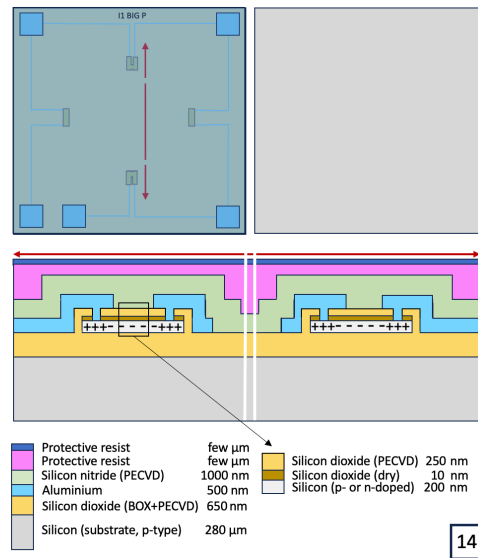
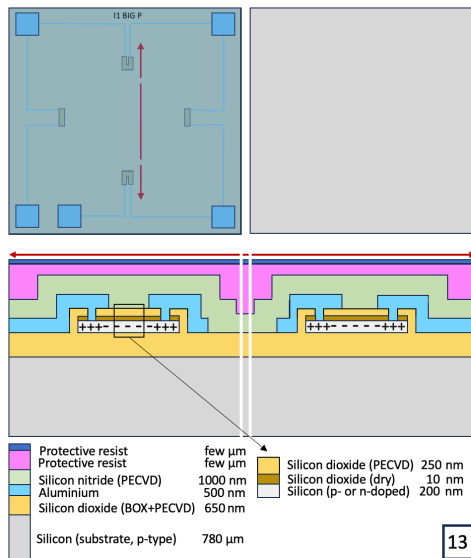
	I1 BIG N	I1 SMALL N 0	I1 SMALL N	I1 BIG P++	I1 BIG P	I1 SMALL P 0	I1 SMALL P
n-ONO1	x1	x2	x1	x2	x2	x3	x1
p-ON1	x1	x2	x1	x2	x1	x3	x2

Table 4.10: Process production report.

4.3.4 Process schematic for "I1 BIG P" die







4.4 Mechanical measurements and characterization

4.4.1 Experimental set-up

Topography measurements of the membrane are done with the Polytec MSA-500 Micro System Analyzer probe station. It uses the Polytec white-light interferometer which enables to evaluate the curvature of the membranes and assess if the residual stress in the film is tensile or if its compressive considering that tensile films give flat membranes whereas compressive ones induce buckling. Together with the Halstrup KAL100 used as a pressure generator and a pressure chamber used to connect the Halstrup tube to the backside of the membrane in a confined space, one is able to measure the deflection of the membrane with regard to positive and negative pressure variations from the backside of the membrane.

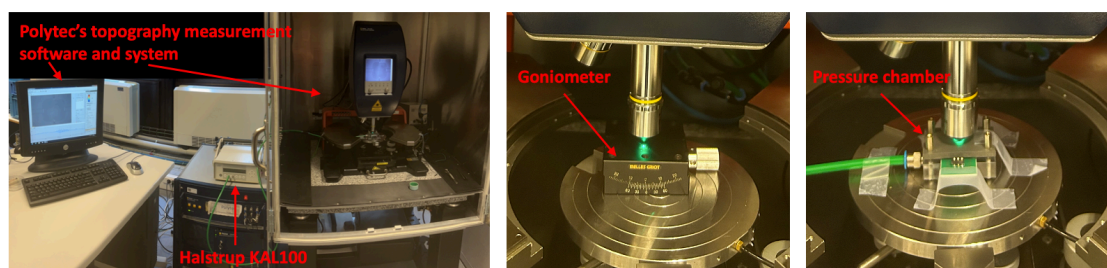


Figure 4.27: Experimental set-up for topography measurements : (left) overview, (center) initial measurement with a goniometer and (right) measurement with the pressure chamber for dies mounted on PCBs.

The polytec white-light interferometer is based on the principle of Michelson interferometry, utilizing an optical configuration shown in Figure 4.28 with a light source having a coherence length in the micrometer range. The light beam is divided into a measurement beam and a reference beam by a beam splitter. The measurement beam is directed towards the sample, while the reference beam is directed towards a mirror. After reflecting from the mirror and the sample, the light is recombined at the beam splitter and then focused onto a camera. When the optical path for an object point in the measuring arm matches the optical path in the reference arm, constructive interference occurs for all wavelengths in the light source's spectrum, resulting in maximum intensity at the corresponding camera pixel. This is then monitored by the camera and post-processed to give the topology of the sample's surface.[50]

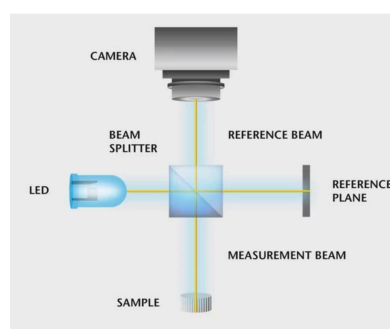


Figure 4.28: Polytec configuration taken from [50].

4.4.1.1 Mounting sensors on printed circuit boards

In order to perform both mechanical and electrical measurements with pressure on the sensors it is necessary to mount them on printed circuit boards (PCB) which provides a secure contact to the metal pads, eases manipulation of the device and gives a safe access to the backside of the membrane through a small hole in the PCB. An order was placed at Multi-cb for a $366 \times 144 \text{ mm}^2$ plate including 36 PCBs which design is shown in Figure 4.29 (left). The contacts have a chemical gold finish, the backside contact is a $4 \times 4 \text{ mm}^2$ square with a $300 \mu\text{m}$ diameter hole in the center which allows to apply pressure on the backside of the membrane. In addition, markings on the side of the PCB allow to specify the dopant type of the piezoresistors and the membrane size.

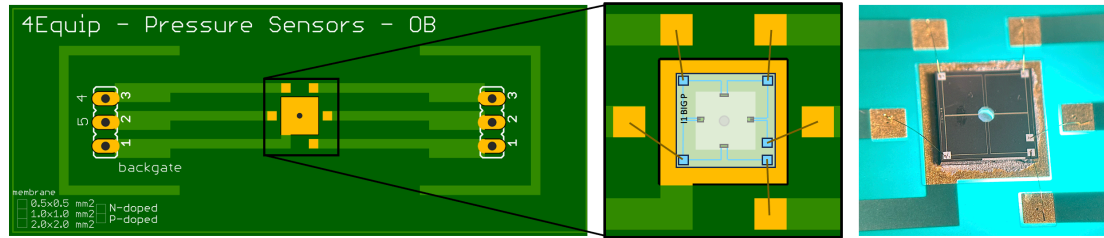


Figure 4.29: (Left) PCB design, (center) wirebonding schematic representation, (right) Microscope observations of I1 SMALL P 0 die after the wirebonding.

First a conductive gluing paste is spread on the borders of the back contact pad and the die is centered above the hole. After 48 hours of drying, the pads are connected with a thin gold wire 7.4.6 using the 4500 Digital Series Manual Wire Bonder in the Winfab workshop according to the schematic representation shown in Figure 4.29 (center). PCB connectors are then soldered in the Welcome workshop to allow the insertion of small standard cables. In total seven dies were mounted on the PCBs : I1 BIG N, I1 SMALL N 0 (2x), 1 SMALL N, 1 BIG P, I1 SMALL P 0, I1 SMALL P. One of them is shown in Figure 4.29 (right). The topography of the membranes was measured for each die before and after being glued on to the PCB to ensure no additional constraints are induced in the membrane by this step.

4.4.1.2 Pressure chamber set-up

The pressure chamber set-up used for every measurements that include pressure variations with the Halstrup equipment is shown in Figure 4.30. The confined space below the PCB is hermetically sealed with a rubber band centered below the hole through the PCB and 4 screw allow to press down the PCB thanks to another wider rubber band placed on top of the PCB.

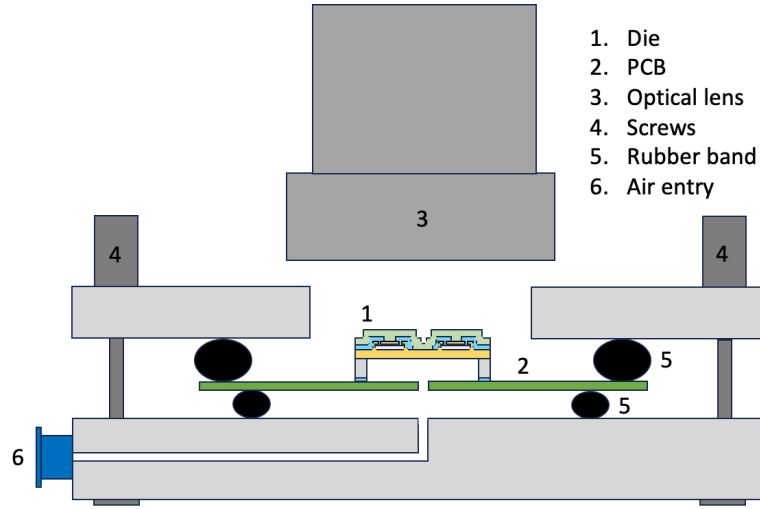


Figure 4.30: Schematic representation of the pressure chamber set-up cross-section.

4.4.1.3 Air leakage correction with UV glue

With the first preliminary measurements performed at a 5kPa pressure for small membranes and 1kPa for larger ones, significant air leaks were discovered on some of the samples caused by the non-uniform conductive gluing paste. Indeed leaks arbitrarily ranging from less than 1% of the Halstrup generated pressure up to 90% were measured. To cope with this problem, UV glue was manually placed exclusively on the borders of the leaky dies and cured for 60 seconds in the Welcome workshop. One had to be extra cautious not to touch the gold wires, avoid placing glue on the frontside of the die or on the inner back walls of the membrane cavity as the glue spread under the membrane. The equipment used for this step as well as a photo of die "I1 BIG P" after leakage correction is shown in Figure 4.31. Note any leakage under 1% were considered acceptable and every other leakages were fully corrected using this method and topology measurements performed after this step and compared to those after the mounting on the PCBs showed no additional constraints were induced in the membrane.



Figure 4.31: Welcome workshop set up for air leakage corrections.

4.4.2 Measurement sequence

4.4.2.1 Procedure for topology scanning

Topography scanning of the membranes is done to assess their curvature and check for any abnormalities that could come from both the sample's fabrication and preparation. The first measurements performed without additional pressure are done to check the resulting stress type on the membranes which must be in tensile stress for this sensing application. Secondly, the deflection with pressure is assessed for the dies mounted on PCBs with pressure levels ranging from 0kPa to 35kPa with the following steps [0, 2.5, 5, 7.5, 10, 15, 20, 25, 30, 35] [kPa] for small $0.5 \times 0.5 \text{ mm}^2$ membranes and pressure levels ranging from 0kPa to 2.5kPa with the following steps [0, 0.5, 1, 1.5, 2, 2.5] [kPa] for big $2 \times 2 \text{ mm}^2$ membranes. The pressure levels applied with the Halstrup were defined based on trial measurements performed on one of the I1 SMALL P 0 die available to identify some relevant electrical pressure responses for which the membrane didn't break.

An interferometric lens set to interferometric mode with a x10 zoom is chosen for small membranes whereas a x2.5 zoom is chosen for big ones. The zoom type is chosen in order to have a sufficient scanned amount of die space around the membrane which is used to level out the measurement during post-processing. Under the microscope, the samples which are not mounted on a PCB are placed on a goniometer which allows to correct the sample's orientation in one direction in order to make it as flat as possible. For dies mounted on a PCB in the pressure chamber there is less room for an inclination correction and it is done manually using transparent adhesive band to place the chamber in a fixed position. Since each die has a different inclination as the glue paste is not uniformly placed on the PCB, this inclination correction must be done for each measurement and the die surface is considered flat enough when the fringes of the diffracted beam can be seen distinctively.[51]

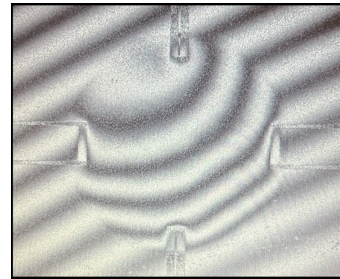


Figure 4.32: Interference fringes on a "n-ONO1" I1 SMALL P 0 die during a topography measurement.

Afterwards the Polytec's topography measurement system (TMS) software can be set up in the measurement setting window starting with the zoom size which is either set to x2.5 or x10, and the measurement precision which is directly proportional to the scanning duration. Then the scan's starting and ending points can be established. To achieve this, the measurement position is reset to zero, and the focus is adjusted to center the fringes in the region of interest. The software is then used to manipulate the fringes by actuating the mirror in the interferometer. When the fringes are just beyond the region of interest, the mirror's displacement is halted, and the configuration can be saved as either the start or end point. The exposure and threshold settings can be customized for each configuration. These

settings are determined based on the intensity of the reflection display. To ensure the object is measurable, the reflection intensity should fall within the limits of 100 and 200, as indicated on the graph. Achieving this can be done by adjusting the exposure time and threshold accordingly.[51] The ideal set of these parameters for this work's topography measurements was 1/1250 exposure time, a threshold of 6 and a $3\mu\text{m/s}$ speed. The raw measurement of a "n-ONO1" I1 SMALL N die with a 20kPa pressure obtained following the procedure described above is given in Figure 4.34 (left) with the topography profile plotted along a cutline through both transversal piezoresistances.

4.4.2.2 Post-processing and artefacts

The first step for post-processing is to level out the measurement data by defining mask boundaries on the die outside the membrane area which, upon a sufficiently flat inclination of the die, are at the same level. These regions are then masked and a linear regression filter is applied on the unmasked regions. The masked regions are then unmasked and the resulting die surface is now leveled out.[51]

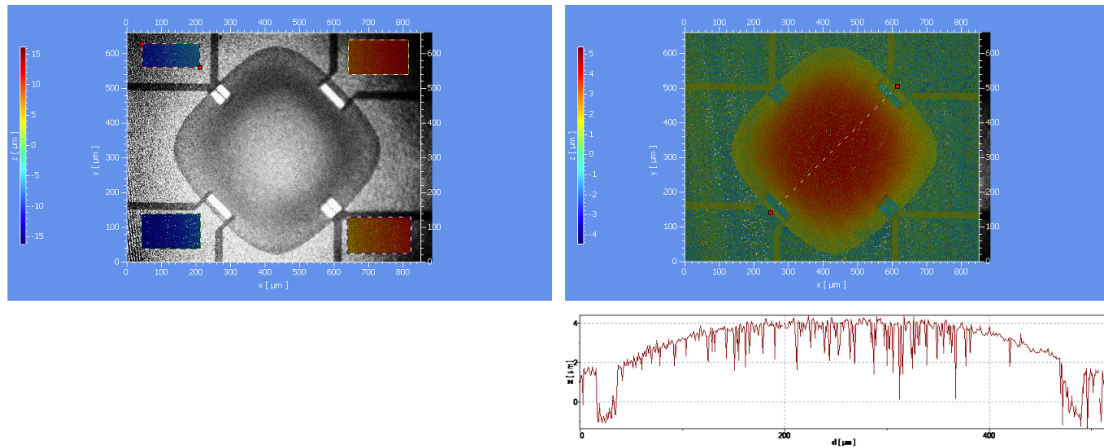


Figure 4.33: Topography measurement leveling for a "n-ONO1" I1 SMALL N die with a 20kPa pressure generated from the Halstrup equipment : (left) masked regions and (right) leveled measurement.

Finally, several filters available in the post processing filter library of the TMS can be applied to reduce the impact of artefacts and interferences. Among them one can use a spike removal filter which removes data over a defined pixel area that exceeds a given threshold and a median filter which is a noise reduction technique whereby the median pixel value is chosen from the neighbouring pixel values.[51] The spike removal filter (pixel width and height of 3, $1\mu\text{m}$ threshold) was used as well as the median filter (pixel width and height of 9, upper threshold set to $7.903\mu\text{m}$ and lower threshold set to $-7.903\mu\text{m}$ by default, fill-only mode, 1 iteration) are systematically used for the topography measurements post-processing and the resulting measurement is given in Figure 4.34 (right). Using a differential cursor,

one is able to average the data values over an x-range and retrieve the maximal deflection of the membrane.

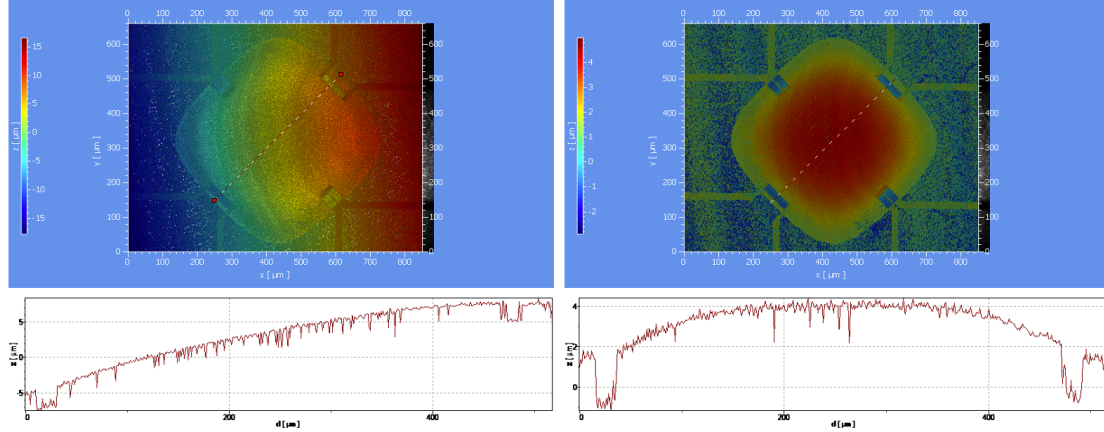


Figure 4.34: Topography measurement obtained with the Polytec's TMS software for a "n-ONO1" I1 SMALL N die with a 20kPa pressure generated from the Halstrup equipment : (left) raw measurement, (right) post processed measurement.

4.5 Electrical and electromechanical measurements and characterization

4.5.1 Experimental set-up

Electrical and electromechanical measurements of the membrane are done with the Keithley 4200 Semiconductor Characterisation System (SCS), a tri-axis to co-axis converter with maximum leakages ranging from 25fA at 1V to 80fA at 100V, small standard cables ports, the sample (cfr. 4.4.1.1) clamped in the pressure chamber set-up (cfr. 4.4.1.2) and the Halstrup KAL100 which generates a pressure difference on the backgate of the membrane via the tube plugged in the pressure chamber. With this set-up one is able to perform I-V measurements without pressure, I-P measurements with a fixed supply voltage on each single piezoresistances, V_1/V_2 -t half or full-bridge measurements with or without pressure.

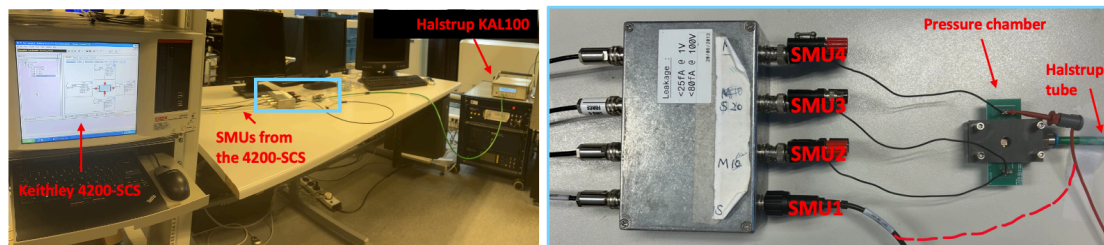


Figure 4.35: Experimental set-up for electromechanical measurements : (left) overview and (right) SMUs connections with the PCB clamped in the pressure chamber and the Halstrup tube plugged in.

4.5.2 SMUs configurations and measurement sequence

Two SMUs configurations are considered for this work : a configuration to measure the output voltages of a full Wheatstone bridge composed of the four piezoresistances numbered according to the schematic representation in Figure 4.36 (left) as a function of time when supplying it with a fixed bias voltage with and without pressure, and a configuration shown in Figure 4.36 (right) to either measure the current through each piezoresistance individually as a function of the supplied swept voltage without pressure or measure the variation of current through each piezoresistance with pressure over time with a fixed bias voltage.

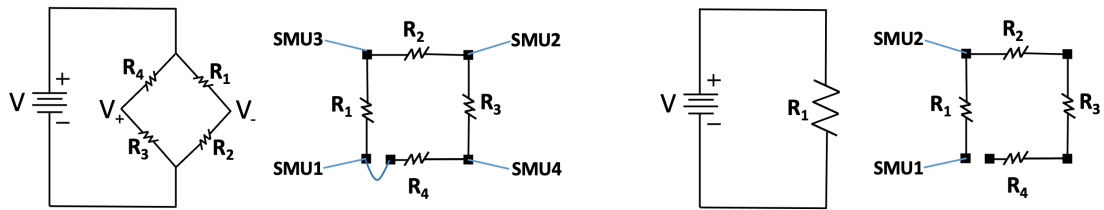


Figure 4.36: Probe contacts and SMUs configuration for (left) a full-bridge measurement and (right) a quarter-bridge measurement with R_1 taken as an example. The blue lines represent the connections between the pads of the measured die and the associated SMU.

The configuration for each source-measurement unit (SMU) set in the Keithley Interactive Test Environment (KITE) for each measurement configuration is given in Table 4.11 below. Note these configurations are valid for any design of the die to be measured for this work.

Full-bridge - measurement with and without pressure	
SMU1	Fixed voltage 0.5V for 0.5x0.5mm ² membranes or 1V for 2x2mm ² membranes, compliance 0.1A, current measured (max. 100pA)
SMU2	Fixed voltage common 0V, compliance 0.1A, current measured (max. 100pA)
SMU3	Fixed current 0A, compliance 0.1A, voltage measured
SMU4	Fixed current 0A, compliance 0.1A, voltage measured
Timing	Delay factor 0.01, Filter factor 0.01, A/D aperture time 0.01, sampling mode : max. 4000 samples, interval 1e-8", hold time 5"

Quarter-bridge - measurement without pressure	
SMU1	Sweep voltage [-5V;5V] (linear), step 0.01V, 1002 points, compliance 0.001A, current measured (max. 100pA)
SMU2	Fixed voltage common 0V, compliance 0.1A, current measured (max. 100pA)
Timing	Delay factor 1, Filter factor 1, A/D aperture time Auto, sweeping mode : sweep delay 0", hold time 0"

Quarter-bridge - measurement with pressure	
SMU1	Fixed voltage 0.5V for 0.5x0.5mm ² membranes or 1V for 2x2mm ² membranes, compliance 0.1A, current measured (max. 100pA)
SMU2	Fixed voltage common 0V, compliance 0.1A, current measured (max. 100pA)
Timing	Delay factor 0.01, Filter factor 0.01, A/D aperture time 0.01, sampling mode : max. 4000 samples, interval 1e-8", hold time 0"

Table 4.11: KITE model with SMUs configuration for full and quarter-bridge measurements with and without pressure pressure.

The following sequence of measurements is performed :

- Quarter-bridge I-V measurement on each piezoresistance without pressure with a supply voltage swept from -5V to 5V and the backgate of the die left floating to determine the linear range of the I-V curve and estimate the piezoresistance value in that linear range.
- Quarter-bridge I-t measurement with a positive pressure difference ranging from 0 to 20kPa applied on the backside of the membrane with a fixed supply voltage of 1V for small 0.5x0.5mm² membranes and 0.5V for 2x2mm² membranes, and the backgate of the die left floating to determine the current response of each piezoresistance to pressure.
- Full-bridge V_-/V_+ -t, or V_1/V_2 -t, measurement with a positive pressure difference ranging from 0 to 20kPa applied on the backside of the membrane with a fixed supply voltage of 1V for small 0.5x0.5mm² membranes and 0.5V for 2x2mm² membranes, and the backgate of the die left floating to assess how the full-bridge is balanced and to determine the bridge output voltages response to pressure. This measurement allows us to compute the piezoresistive sensor's sensitivity.

Among the parameters listed in Table 4.11 which are reminded in the measurement sequence above, the fixed supply voltage for quarter and full-bridge measurements with pressure together with the hold time of 5" for full-bridge measurements with pressure and the measurement condition that consists of leaving the backgate floating are critical when it comes to the readability of the results presented in Chapter 5 due to the presence of a voltage drift on the bridge output voltages. Indeed this voltage drift can reach an order of magnitude more than the response to pressure in specific measurement conditions and is studied in the next section 4.5.3. As for the data post-processing, it was carried out using Python and the description of this post-processing is provided alongside the obtained results.

4.5.3 Bridge output voltages drift analysis

This section aims to evaluate the drift in bridge output voltages for the samples intended for electromechanical measurements. It seeks to investigate the underlying causes of this drift and identify the parameters that restrict its behavior.

4.5.3.1 Initial observations

The bridge response to pressure variations for sample I1 SMALL P 0 during the preliminary phase of electromechanical measurements is shown in Figure 4.37 where one can see the evolution over time of both output voltages of the bridge, V_1 and V_2 , with a supply voltage of 2V and a two consecutive 10kPa positive pressure variations, in increments of 50% and 20% respectively.

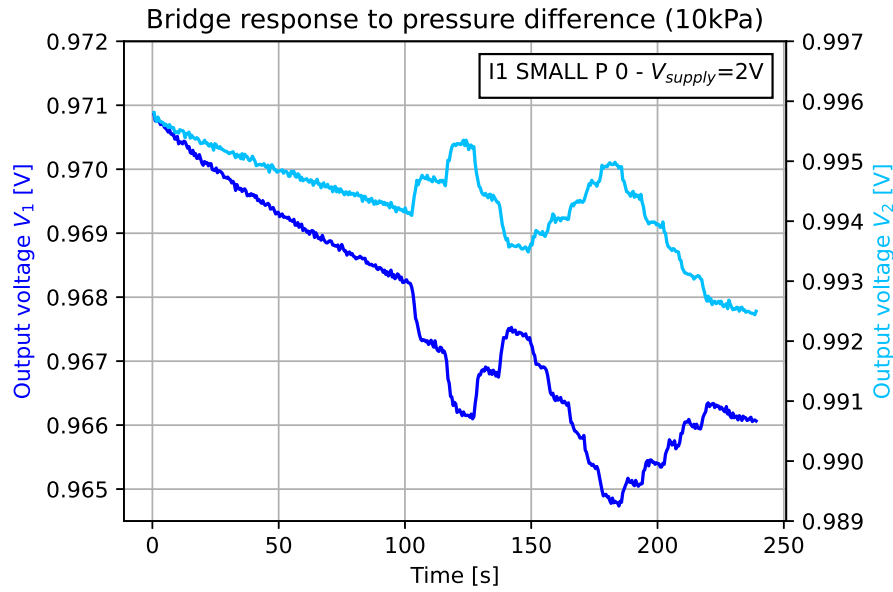


Figure 4.37: Preliminary bridge output voltages response to pressure difference for sample I1 SMALL P 0.

Without considering the quantitative pressure response, one can observe a drift, whose order of magnitude is greater than the one of the 10kPa pressure response, is experienced by the two bridge output voltages. Indeed over this 240" time interval the voltage drift on V_1 is 4.791mV and the one over V_2 is 3.312mV. A first intuition relating to the shape of the drift curvature suggests that a stabilisation of both output voltages of the bridge is reached after a period greater than 250". Figure 4.38 shows a stabilisation period of 1010" of the previous measurement without pressure where the drift on V_1 is 9.931mV and the one on V_2 is 6.091mV. The stabilisation period of the two output voltages drift is therefore greater than 15' which is constraining in terms of measurement time and makes the analysis of the drift, its origin and the limiting parameters all the more relevant in order to be able to carry out measurements with a limited drift before the stabilisation is reached.

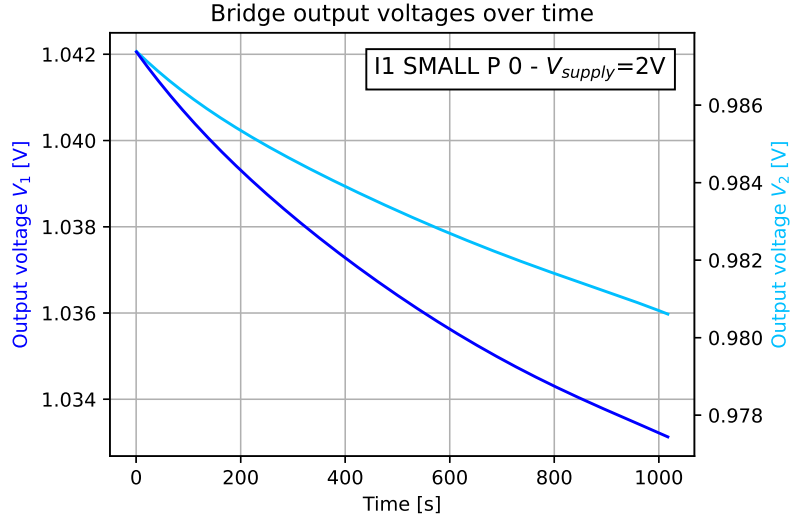


Figure 4.38: Bridge output voltages stabilisation over time for sample I1 SMALL P 0.

Several hypotheses listed below have been made regarding the parameters or experimental conditions that may have an impact on this drift :

1. Set-up cables and SMUs
2. Hold time
3. Backgate of the die
4. Luminosity
5. Supply voltage
6. Temperature and humidity

All hypotheses are investigated hereafter, except for the impact of temperature and humidity due to the full booking of the ESPEC SH-261 Temperature and Humidity Chamber during the measurement period of this work.

4.5.3.2 Set-up cables and SMUs

To begin with the current leakage related to the SMUs, the tri-axis to co-axis converter is measured one branch at a time with the standard leakage current measurement KITE model to confirm it is in the range of 25 to 80fA. As expected the order of magnitude of the leakage currents is of the order of 10^{-15} A. The same measurement is then performed with the standard cables connected to the tri-axis to co-axis converter as well to quantify leakage related to all serial measurement connections and the order of magnitude of the leakage currents is of the order of 10^{-12} A which is 10^6 times smaller than the currents subsequently measured through the piezoresistances. Switching the cables did not have an impact on the bridge output voltages drift and the configuration given in Figure 4.36 was set as a reference configuration for this work.

4.5.3.3 Hold time influence

The bridge output voltages variation over time with a supply voltage of 5V without pressure for sample I1 SMALL P 0 is shown in Figure 4.39 for increasing values of the hold time, denoted t_{hold} , ranging from 0" to 5". Please note the y-axis were not scaled for better visibility of the 4 pairs of output voltages.

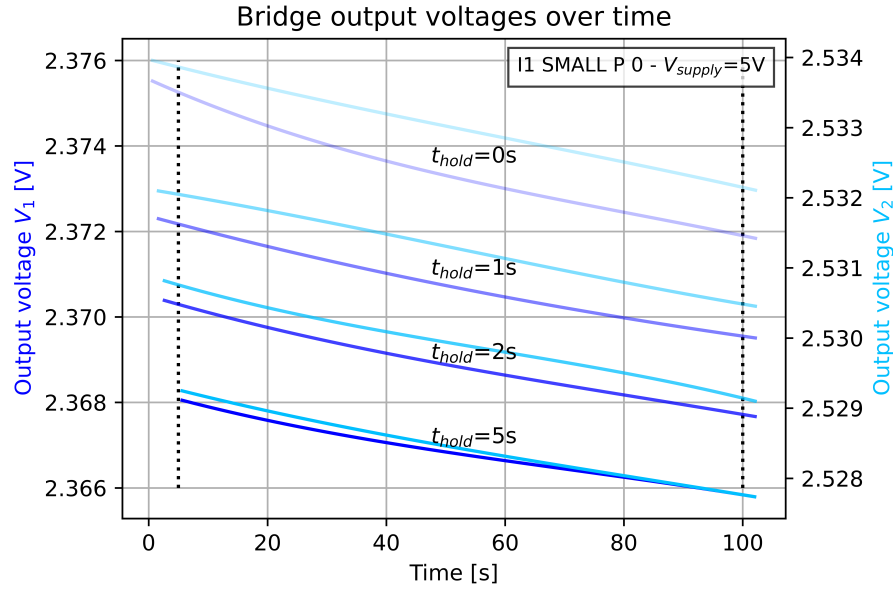


Figure 4.39: Bridge output voltages over time for different hold time values for sample I1 SMALL P 0.

The drifts on both output voltages are measured over a 95" time period delimited by the vertical black dotted lines and plotted as a function of t_{hold} in Figure 4.40. With a drop of 1.41mV for the drift on V_1 and a drop of 0.33mV for the drift on V_2 between extreme values of t_{hold} , a trend can be inferred that the drift tends to decrease with increasing values of t_{hold} . One can also see a change in the balance of the bridge in Figure 4.39, but it won't be discussed here.

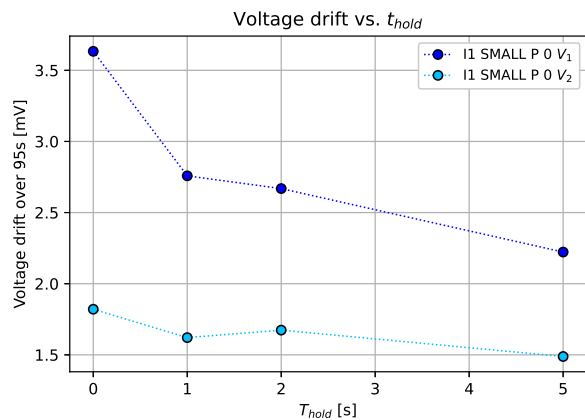


Figure 4.40: Bridge output voltages drift as a function of the hold time value for sample I1 SMALL P 0.

4.5.3.4 Backgate influence

As a reminder, the backside of the die is connected to a pad on the PCB via a conductive gluing paste and this backgate can either be grounded, supplied with a bias voltage or left floating. In order to study the influence of the backgate on the piezoresistances and by extension on the bridge's output voltages, the backgate leakage current was first measured with the configuration 4.11 and an additional SMU for the backgate with a fixed voltage of 0V, a compliance of 0.1A and the current as the quantity being measured.

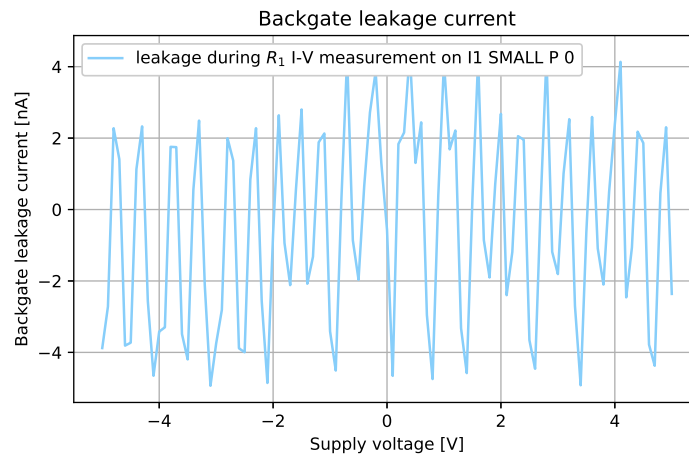


Figure 4.41: Backgate leakage current measured in parallel of an I-V measurement with a swept supply voltage for sample I1 SMALL P 0.

Knowing that the current in the resistor R_1 is of the order of μA , a leakage current of the order of nA is not negligible and is around 10^3 times higher than the leakage currents in the set-up cables measured previously. However this noisy leakage current is relatively constant and does not show a trend that could be related to drift. Grounding the backgate with the same ground as the bridge with SMU1 using an additional cable soldered to the one closing the bridge and using SMU2 as the supply voltage didn't alter the drift on the output voltage either. The next experiment carried out to assess the influence of the backgate was to perform I-V measurements with a dual voltage sweep from -5V to 5V with different fixed backgate voltages to see if there was a transient current response. A backgate voltage of -1, 0V common, 1V and 3V was supplied through SMU3 successively and no transient response were observed considering the maximal current gap measured was $0.5\mu\text{A}$ for currents of the order of a hundred micrometers on sample I1 SMALL P 0. Lastly I-V measurements were performed on R_1 and R_2 of I1 SMALL P 0, I1 BIG P and I SMALL N 0 with a single supply voltage sweep from 0V to 5V and a backgate voltage ranging from 0V to 10V by increments of 2.5V to assess any transistor like behaviour. The results of these measurements are shown for R_1 in Figures 4.42, 4.43 and 4.44.

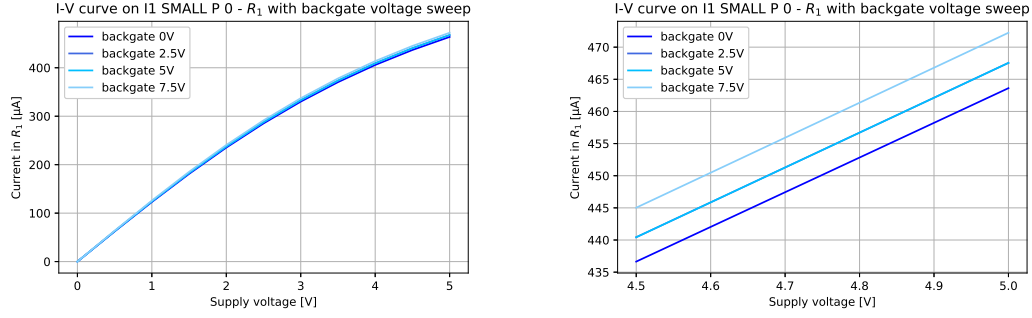


Figure 4.42: I-V measurements with varying backgate voltage on I1 SMALL P 0 - R_1 : (left) supply voltage sweep from 0V to 5V and (right) zoom for supply voltage ranging from 4.5V to 5V.

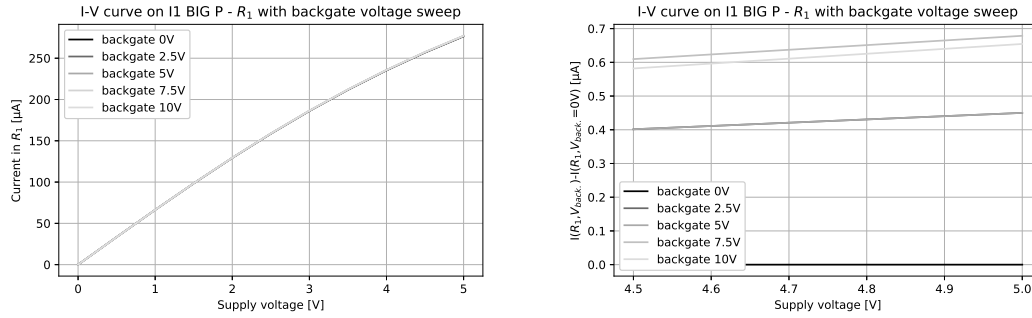


Figure 4.43: I-V measurements with varying backgate voltage on I1 BIG P - R_1 : (left) supply voltage sweep from 0V to 5V and (right) zoom for supply voltage ranging from 4.5V to 5V with each current curve subtracted with the reference 0V backgate current curve for better visibility.

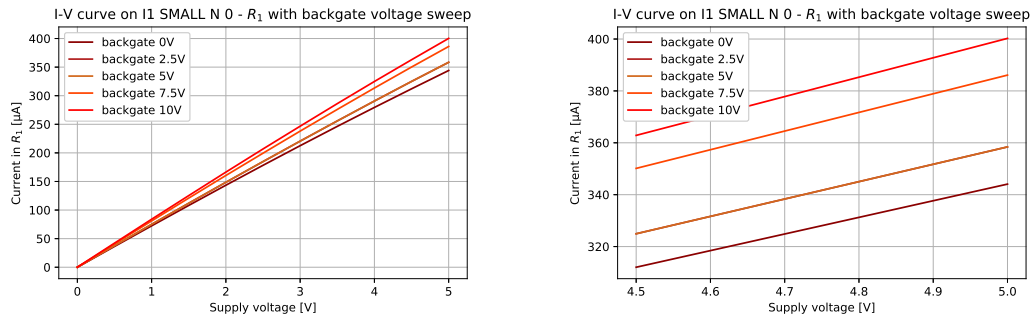


Figure 4.44: I-V measurements with varying backgate voltage on I1 SMALL N 0 - R_1 : (left) supply voltage sweep from 0V to 5V and (right) zoom for supply voltage ranging from 4.5V to 5V.

Please note that the current curves for a backgate voltage of 2.5V and 5V appear superimposed on the graph but are distinguishable with zoom at higher supply voltage values. The maximum current difference measured at a supply voltage of 5V between the curve for a backgate at 10V, or 7.5V for I1 SMALL P 0, and that for a backgate at 0V is 8.62μA, 0.655μA and 56.176μA for I1 SMALL P 0, I1 BIG

P and I1 SMALL N 0 respectively. No conclusions are drawn from these results regarding the influence of the backgate on the bridge output voltages drift and the backgate is left floating for the rest of the measurements for this work.

4.5.3.5 Luminosity influence

The bridge output voltages variation over time with a supply voltage of 5V without pressure for sample I1 SMALL P 0 is shown in Figure 4.45 for three different set-up conditions : no light shield over the pressure chamber, a cardboard box with a small hole for the gas tube placed over the pressure chamber and an additional opaque black cloth placed on top of the cardboard box. The idea behind this experiment is to see if the bridge output voltage drift is impacted by the ambient light.

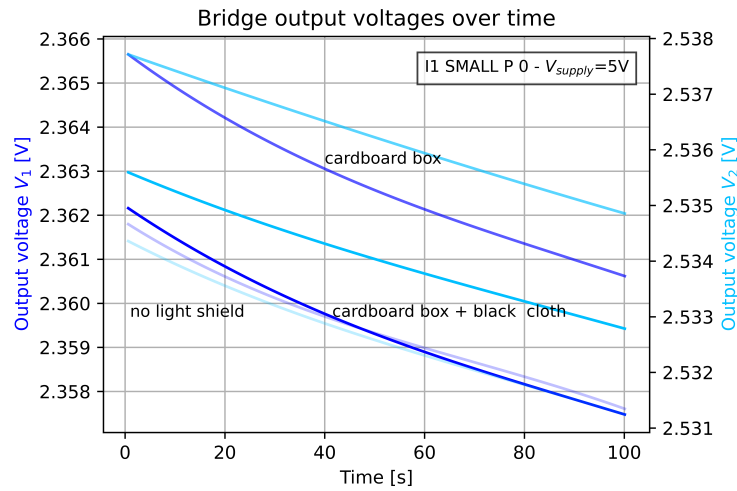


Figure 4.45: Bridge output voltages over time in different luminosity conditions for sample I1 SMALL P 0.

Additional measurements on more samples would be necessary to be able to draw conclusions regarding the impact of luminosity on the measurements carried out in this work. Nevertheless the rest of the measurements were made with the cardboard box placed over the pressure chamber in order to have a measurement set-up identical to that of the samples of another project referred to as project A for confidentiality reasons which will be compared to the samples measured in this work later on.

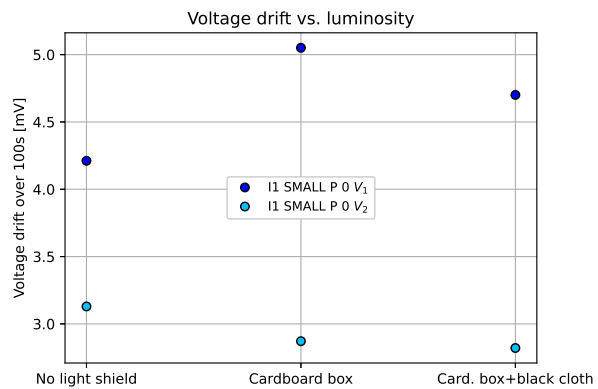


Figure 4.46: Bridge output voltages drift in different luminosity conditions for sample I1 SMALL P 0.

4.5.3.6 Supply voltage influence

The last parameter studied with respect to its influence on the drift is the supply voltage of the bridge. The bridge output voltages drift over 100" with the backgate left floating, the blackbox over the pressure chamber and a fixed voltage supplied through SMU1 of 0.5V, 1V, 2V, 2.5V, 5V, 10V is successively measured for each die mounted on a PCB. The resulting voltage drifts as a function of the supply voltages are shown in Figure 4.47. Note the bridge output voltages for sample I1 SMALL N 0 are superimposed which is why V_1 is not visible on the graph and sample I1 SMALL P 0 was only measured for a supply voltage of 0.5V, 1V and 2V due to a piece of cable stuck inside a connector on the PCB.

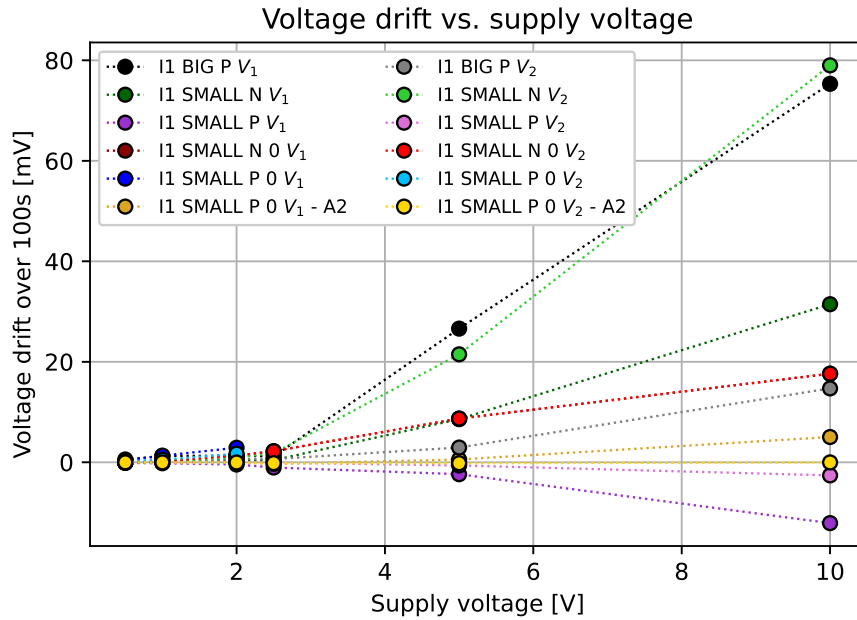


Figure 4.47: Bridge output voltages drift over a 100" period as a function of the supply voltage value for each die mounted on a PCB. A zoomed in version of this graph for supply voltages ranging from 0.5V to 2.5V is given in Figure 4.48.

One can also see an additional sample denoted "I1 SMALL P 0 - A2" which was measured for this supply voltage analysis as it has the same design as I1 SMALL P 0 with a different stack and a p-doped 1 μ m thick silicon mesa. Indeed it has a 500nm thick BOX silicon dioxide with an additional 500nm thick thermal silicon dioxide lying on top and a 1.5 μ m thick silicon nitride passivation layer which makes it a good candidate for comparison purposes for the study of the bridge output voltages drift. One can see this sensor exhibits a maximal drift of 5.034mV on V_1 when its bridge is supplied with 10V whereas almost all the measured sensors from this work exhibit higher drifts for any supply voltage reaching up to 79mV for V_2 on sample I1 SMALL N. Based on the above results the conclusion can be drawn that there is a strong non-linear dependence between the drift on the output

voltages of the bridge and its supply voltage. A supply voltage of 1V is chosen for 0.5x0.5mm² membranes for the rest of the measurements to limit the drift on both bridge output voltages to less than 1.5mV. As for the 2x2mm² membranes, a 0.5V supply voltage is chosen to have less than 1mV of drift since the bridge response to pressure is smaller due the limited pressure range of 0kPa to 2.5kPa determined in Section 4.4.2.

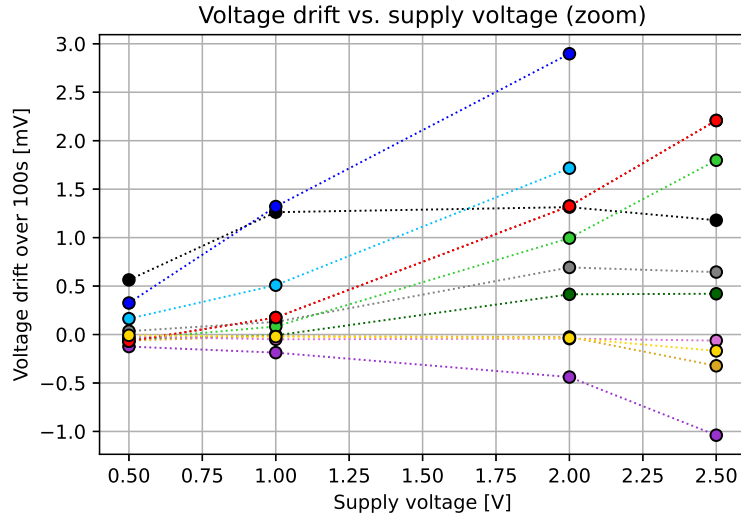


Figure 4.48: Bridge output voltages drift over a 100” period as a function of the supply voltage value ranging from 0.5V to 2.5V for each die mounted on a PCB.

The presence of the output voltages drift can be due to different phenomena like design and temperature. In the case of this work the bridge configuration together with the membrane is rather symmetrical which seems to indicate that the drift isn’t related to any asymmetry in the design although small variations related to the etching step 4.3.2.12 in the different lateral dimensions in horizontally and vertically placed piezoresistances may influence this drift. Another possible cause could be an implanted dose loss caused by a shadowing effect of the resist mask when implanting the highly doped regions on the borders of the silicon mesas which limits the effective implanting area.[19] The most plausible cause given the strong dependence of the drift on the supply voltage, is a thermal drift of the bridge output voltages which depends on the difference between each thermal coefficient of the resistance (TCR).[19] A mismatch between these TCR could explain the presence of the drift and the difference in drift observed from one branch to another. A potential explanation for this behavior could be rooted in the emergence of thermomechanical stress at the interface between the membrane and substrate, arising from variations in thermal coefficient of expansion. Considering that the piezoresistances are located close to the clamping region, it’s plausible that this stress predominantly impacts this area, which might be further compounded by the challenge of precisely controlling the actual clamping point due to imperfections in the etching process.[19]

Chapter 5

Results for piezoresistive pressure sensors

5.1 Mechanical results

This section presents the results obtained for the mechanical measurements and characterisation described in Section 4.4 starting with the initial deflection of 6 dies of each doping type followed by the deflection with pressure of those which are mounted on PCBs together with a comparative analysis with theoretical estimations.

5.1.1 Initial deflection

The initial maximal deflection measurement is given in Table 5.1 below for six "n-ONO1" dies and six "p-ON1" dies while none of them are mounted on PCBs. These dies are selected based on the resulting quality of the membrane after its release. Each of them display a maximal initial deflection under 1 μ m and there is no trend that emerges from these preliminary measurements neither with respect to the shape of the membrane nor with its size.

	Initial maximal deflection [nm]						
	I1 BIG N	I1 SMALL N 0	I1 SMALL N	I1 BIG P++	I1 BIG P	I1 SMALL P 0	I1 SMALL P
n-ONO1	704	874	447	-	138	749	626
p-ON1	307	639	186	198	-	118	330

Table 5.1: Initial maximal deflection of 13 produced membranes.

5.1.2 Deflection with pressure

The maximal deflection with a positive pressure difference applied on the backside of the membrane of 5 "n-ONO1" dies mounted on PCBs grouped by membrane shape and size is given hereafter in Figure 5.1 for 0.5x0.5mm² square membranes, in Figure 5.2 for 2x2mm² square membrane and in Figure 5.3 for 0.5x0.5mm² circular membranes. Note sample I1 BIG N was broken during manipulation with the pressure chamber and could not be measured. The theoretical deflection estimations confronted with the experimental measurements are based on the Equation 1.34 for square membranes and Equation 1.33 for circular membranes. Indeed one can rewrite these equations to obtain a third order polynomial in w , for thin square membranes :

$$w^3 \cdot \left(\frac{13.6 \cdot 1.61h}{(2a)^4} \cdot \frac{(1.446 - 0.427v)E}{1 - v} \right) + w \cdot \left(\frac{13.6h\tau_0}{(2a)^2} \right) - p = 0 \quad (5.1)$$

and for thin circular membranes,

$$w^3 \cdot \left(\frac{8h}{3a^4} \cdot \frac{E}{1.026 - 0.793v - 0.233v^2} \right) + w \cdot \left(\frac{4h\tau_0}{a^2} \right) - p = 0 \quad (5.2)$$

which can be solved using the `numpy.roots()` function that provides three roots per equation, two of which are discarded because they are complex numbers. The values taken for each parameter are given in Table 5.2 below. The membrane Young's modulus is computed with the Young's modulus of its composition materials using the following formula [43]:

$$E = \frac{E_{SiO_2} \cdot h_{SiO_2} + E_{Si_3N_4} \cdot h_{Si_3N_4}}{h_{Si_3N_4} + h_{SiO_2}} \quad (5.3)$$

and the membrane Poisson's ratio is also computed with the Poisson's ratio of its composition materials as follow [43]:

$$v = \frac{v_{SiO_2} \cdot h_{SiO_2} + v_{Si_3N_4} \cdot h_{Si_3N_4}}{h_{Si_3N_4} + h_{SiO_2}} \quad (5.4)$$

As for the side length of the small square membranes, a 10 μ m overetch is taken into account as well as a 30 μ m overetch for small circular membranes radius.

Variable name	Notation	Value	Variable name	Notation	Value
Silicon nitride thickness	$h_{Si_3N_4}$ [nm]	1000	Silicon nitride Poisson's ratio[52]	$v_{Si_3N_4}$ [/]	0.2
Silicon dioxide thickness	h_{SiO_2} [nm]	590	Silicon dioxide Poisson's ratio[23]	v_{SiO_2} [/]	0.27
Membrane thickness	h [μ m]	1.59	Membrane Poisson's ratio	v [/]	0.226
Silicon nitride Young's modulus[52]	$E_{Si_3N_4}$ [GPa]	290	Small square membrane half-length	$a_{smallsquare}$ [μ m]	260
Silicon dioxide Young's modulus[23]	E_{SiO_2} [GPa]	180	Big square membrane half-length	$a_{bigsquare}$ [mm]	1
Membrane Young's modulus	E [GPa]	249.182	Circular membrane radius	$a_{circular}$ [μ m]	280

Table 5.2: Initial maximal deflection of 13 produced membranes.

With the above fixed parameters only the residual stress τ_0 is unknown and can be estimated thanks to the good agreement between the theoretical and experimental curves. Using this approach, it becomes possible to estimate tensile residual stresses below 100MPa, aligning well with the anticipated residual stress levels. By looking at the graphs one can see the theoretical curve is dotted for deflection under 1.590 μ m quite simply because it estimates the maximal deflection for thin membranes which imply that the deflection must be greater than the thickness of the membrane itself. Besides the experimental points for maximal deflection of small membranes under this threshold don't fit the dotted line although it seems to remain a good estimation for maximal deflection under the membrane thickness of larger membranes.

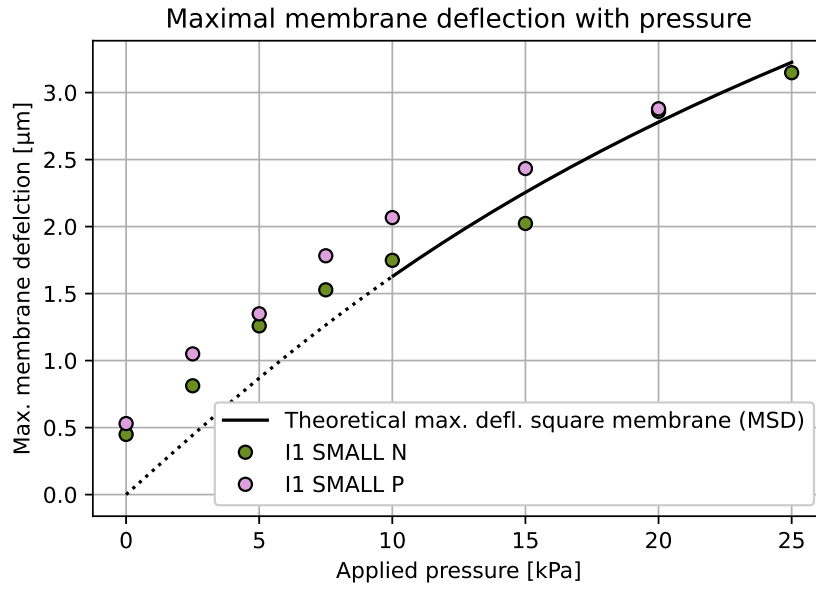


Figure 5.1: Maximal membrane deflection with pressure for $0.5 \times 0.5 \text{ mm}^2$ square membranes together with a theoretical estimation where τ_0 set to 70MPa tensile.

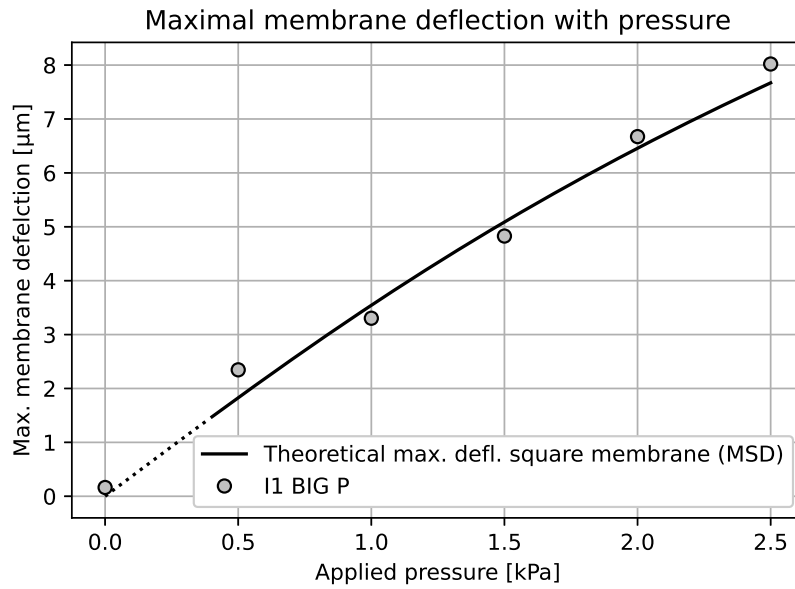


Figure 5.2: Maximal membrane deflection with pressure for $2 \times 2 \text{ mm}^2$ square membrane together with a theoretical estimation where τ_0 set to 50MPa tensile.

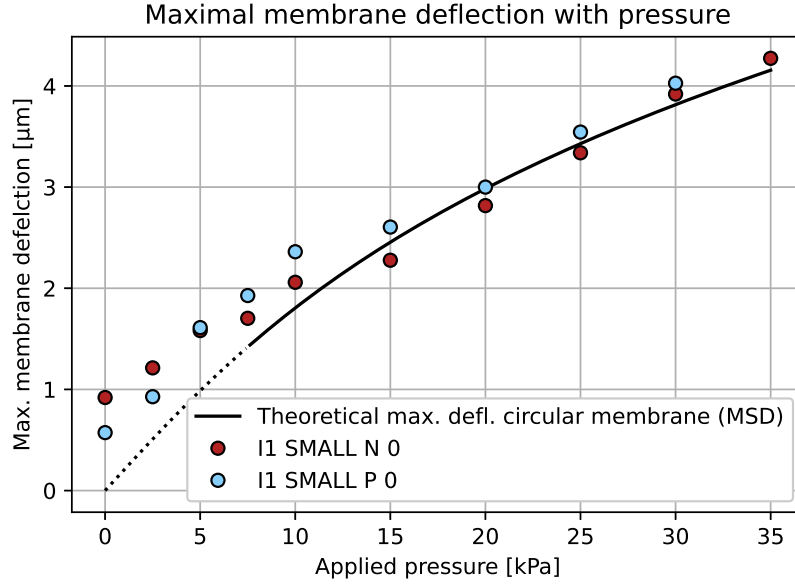


Figure 5.3: Maximal membrane deflection with pressure for $0.5 \times 0.5 \text{ mm}^2$ circular membranes together with a theoretical estimation where τ_0 set to 60MPa tensile.

One can also see that the orthogonal membranes exhibit a higher deflection than square ones for a same configuration of the piezoresistances. In the case of an N configuration for which the piezoresistances are oriented at a 45° angle to the flat, the orthogonal membranes exhibit an average deflection that is 260nm greater than the square ones with the same configuration. This variation is calculated using the average of the deviations at the same pressure, for each pressure points. For a P configuration for which the piezoresistances are oriented at a 90° angle to the flat, the orthogonal membranes exhibit an average deflection of 130nm greater than the square ones with the same configuration. These results support the theory that orthogonal membranes deflect more than square membranes.

5.2 Electrical and electromechanical results

This section presents the results obtained for the electrical and electromechanical measurements described in Section 4.5 performed on three samples : I1 SMALL P 0, I1 BIG P and I1 SMALL N 0. Considering only n-doped samples were mounted on PCBs, this implies piezoresistance configurations which are not optimal for n-doped silicon mesas are also measured here and even if a lower sensitivity is to be expected for these samples, their measure remains interesting in the context of this work. To begin with the linear range of each piezoresistance is extracted from I-V measurements as well as their value within this range. The current variation with pressure on each piezoresistance is then measured at a fixed voltage and finally the

sensitivity of each sensor is extracted from the bridge output voltages variation with pressure.

5.2.1 I-V curves on piezoresistances

The linear range approximation extracted from I-V measurements performed on each piezoresistance with a supply voltage sweep from -5V to 5V using a first order polynomial fitting on the current is given in Table 5.3 together with the piezoresistance value computed within the corresponding linear range with the inverse of the `np.slope()` function. Note no results are given for R_3 and R_4 for sample I1 SMALL P 0 due to a data retrieval error although the linear range is also estimated to be from -1V to 1V for these two piezoresistances based on raw plots extracted directly from the KITE measurements. The piezoresistances values are in good agreement with the estimated values from Silvaco simulations in Section 4.3.1 but one can say the bridges are unbalanced.

	I1 SMALL P 0		I1 BIG P		I1 SMALL N 0	
	Linear range [V]	Value [k Ω]	Linear range [V]	Value [k Ω]	Linear range [V]	Value [k Ω]
R_1	[-1,1]	8.296	[-1.5,1.5]	15.2	[-5,5]	13.954
R_2	[-1,1]	7.7	[-2,2]	16.956	[-2,2]	21.018
R_3	-	-	[-1.5,1.5]	16.062	[-1.5,1.5]	17.282
R_4	-	-	[-1,1]	14.223	[-1,1]	18.211

Table 5.3: Linear range and piezoresistance value of the full-bridge for I1 SMALL P 0, I1 BIG P and I1 SMALL N 0.

5.2.2 Current variation with pressure

The four graphs shown in Figure 5.4 shows the raw current variation over time of each piezoresistance from sample I1 SMALL P 0 when a positive pressure difference of 20kPa is applied gradually with 5kPa increments before being decreased back to 0kPa. A remaining current drift despite the measurement conditions aimed at limiting this drift, particularly evident in R_1 and R_3 in the given example in Figure 5.4, prompted the implementation of a systematic correction which involves using a first-order polynomial generated from the initial current value at 0kPa and the final value at 0kPa. This polynomial is subtracted from the raw curves to rectify the current drift. In addition to this correction, the initial current value at 0kPa was subtracted to each measured point in order to visualise the differential current variation over time of each piezoresistance in one graph per sample. These graphs are shown in Figure 5.5, 5.6 and 5.7 for I1 SMALL P 0, I1 BIG P and I1 SMALL N 0 respectively. Note the horizontal offsets of the current differences for a sample result from pressure changes which is done manually every 10”.

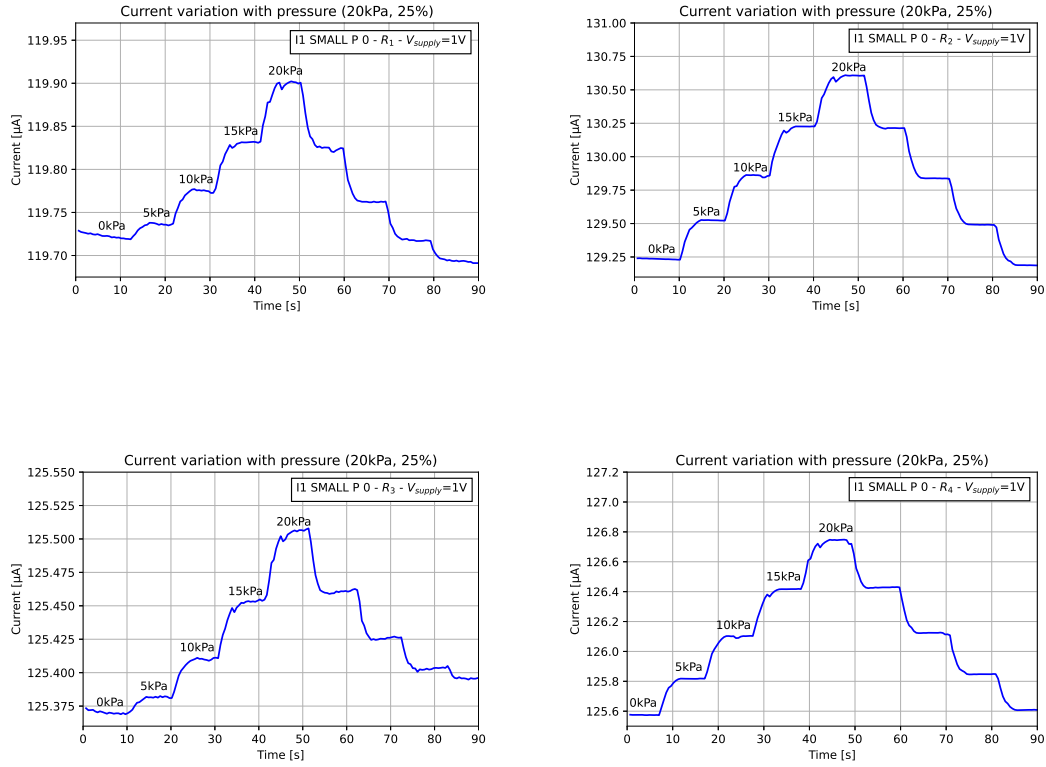


Figure 5.4: Current variation over time with positive pressure differences and fixed supply voltage on each piezoresistance from sample I1 SMALL P 0.

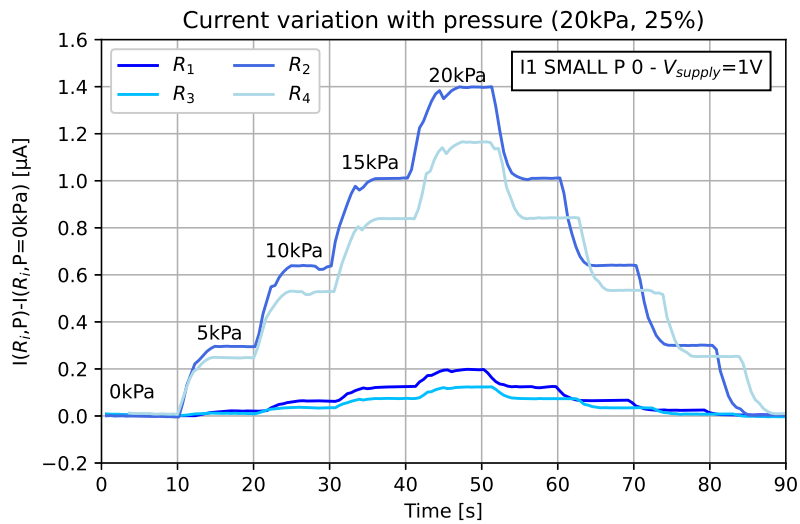


Figure 5.5: Differential current variation over time with positive pressure differences and fixed supply voltage on each piezoresistance from sample I1 SMALL P 0.

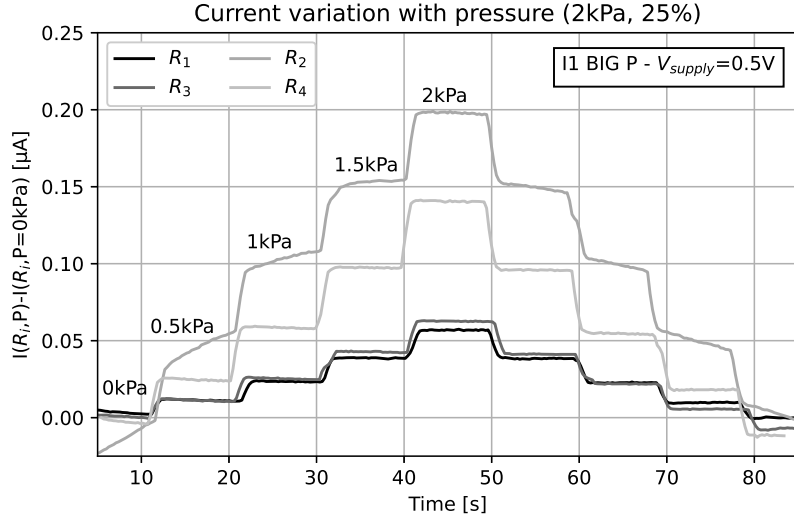


Figure 5.6: Differential current variation over time with positive pressure differences and fixed supply voltage on each piezoresistance from sample I1 BIG P.

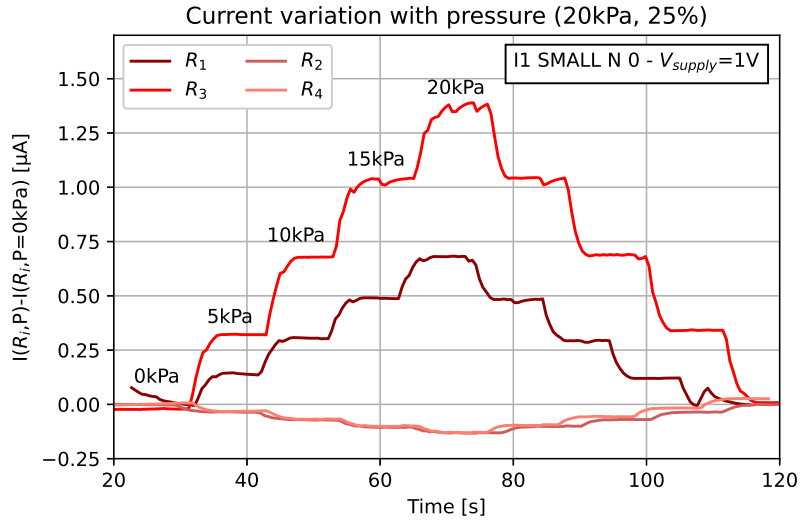


Figure 5.7: Differential current variation over time with positive pressure differences and fixed supply voltage on each piezoresistance from sample I1 SMALL N 0.

The differential current variations with pressure of each measured sample are gathered in Figure 5.8 and Figure 5.9 for the rising pressure flank and one can see the linear relationship that exists between the variation in current of the piezoresistances and the positive pressure applied to the backside of the membrane. This suggests the bridge output voltages response to positive pressure differences is also

linear. Note the curves of I1 SMALL N 0 R_2 and R_4 are superimposed on the graph which prevents seeing R_2 . Regarding the sign of the current variations for each piezoresistance of the samples, they are in good agreement with the theory. Indeed I1 SMALL N 0 has an optimal configuration for n-doped silicon mesas for which the resistivity of R_1 and R_3 is decreased when they experience tensile stress which amounts to an increase of their current over time with positive pressure differences as one can see in Figure 5.7. On the contrary the resistivity of R_2 and R_4 is increased when they experience tensile stress which amounts to a decrease of their differential current over time with positive pressure differences. As for I1 SMALL P 0 and I1 BIG P, all their piezoresistances value decrease with tensile stress since both longitudinal and transverse piezoresistive coefficients are negative for (100) n-doped silicon oriented according to the p-type design which amounts to an increase of their current over time with positive pressure differences as one can see in Figure 5.5 and 5.6.

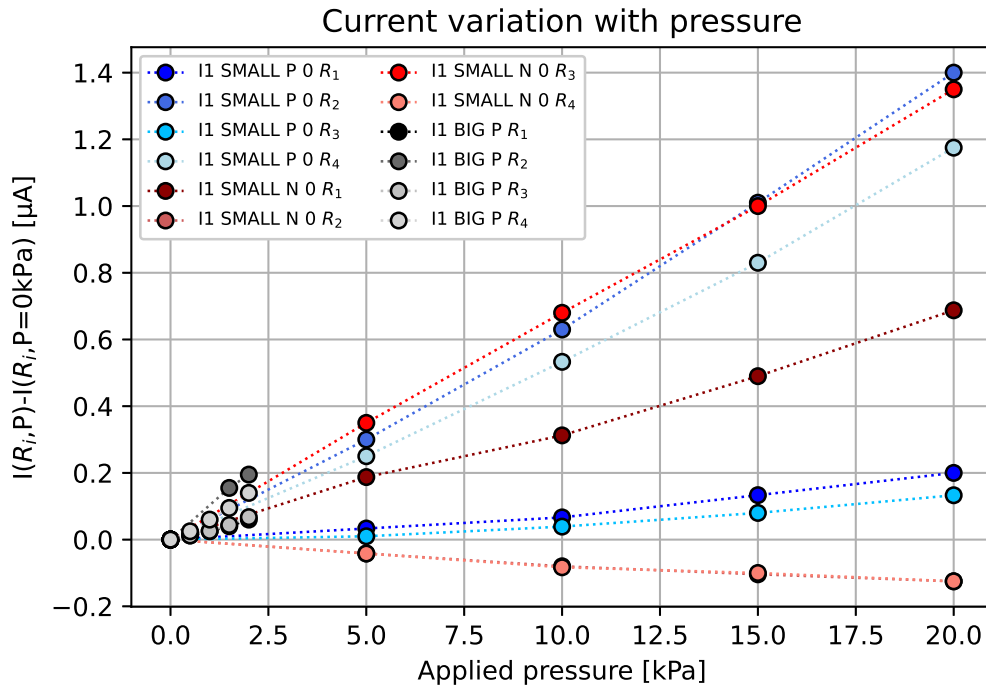


Figure 5.8: Differential current variations with pressure for each piezoresistance of the measured samples.

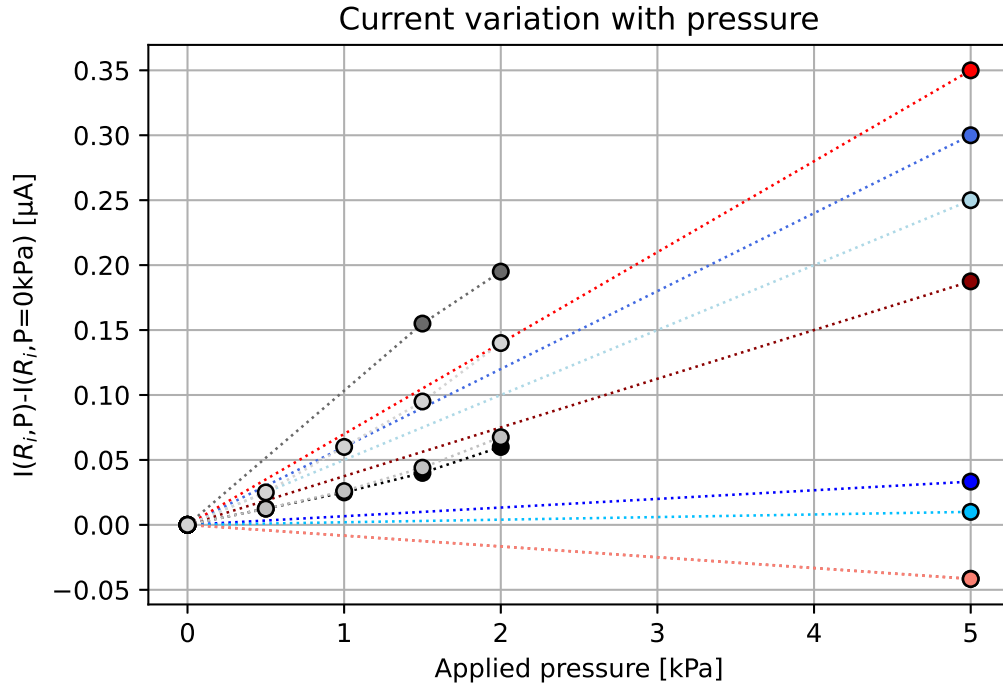


Figure 5.9: Differential current variations with pressure zoom from Figure 5.8 for each piezoresistance of the measured samples.

5.2.3 Bridge output voltages variation with pressure

The three graphs shown in Figure 5.10, 5.11 and 5.12 show the raw bridge output voltages variation over time for sample I1 SMALL P 0, I1 BIG P and I1 SMALL N 0 respectively, when a positive pressure difference of 20kPa is applied gradually with 5kPa increments before being decreased back to 0kPa. Apart from the fact that the bridge is unbalanced as it was already mentioned before, one can see a small voltage drift still remaining despite the measurement conditions aimed at limiting this drift. Thus an identical correction as the one implemented for the current drift in the previous section with a first order polynomial subtracted to the curve was applied in order to extract the bridge output voltages variation with pressure given in Figure 5.13 for sample I1 SMALL P 0 and I1 SMALL N 0, as the measurement on I1 BIG P was too noisy to extract values with the same reliability than the two other samples. Once again the values are taken on the rising pressure flank.

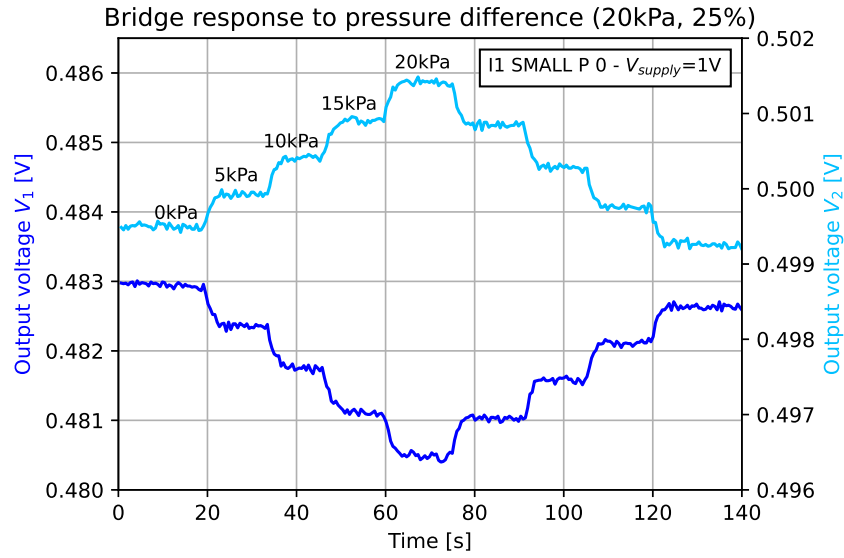


Figure 5.10: Bridge output voltages variation over time with positive pressure differences and fixed supply voltage for sample I1 SMALL P 0.

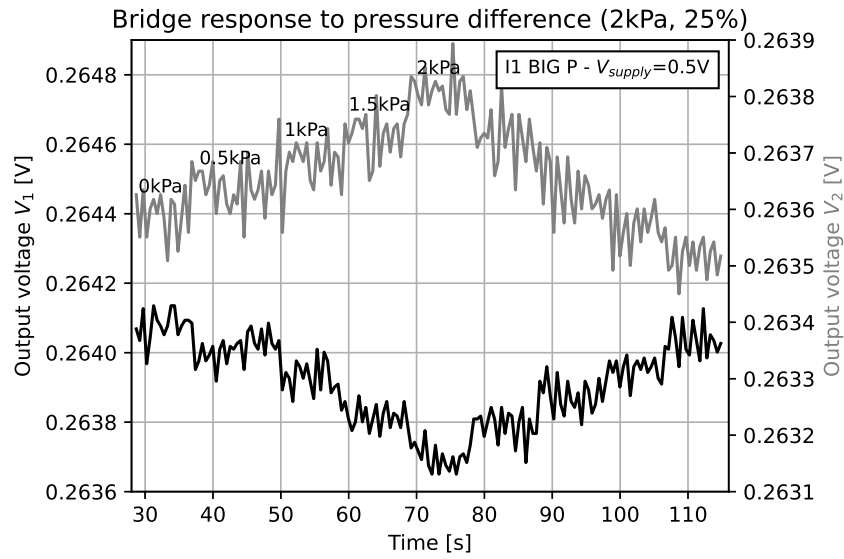


Figure 5.11: Bridge output voltages variation over time with positive pressure differences and fixed supply voltage for sample I1 BIG P.

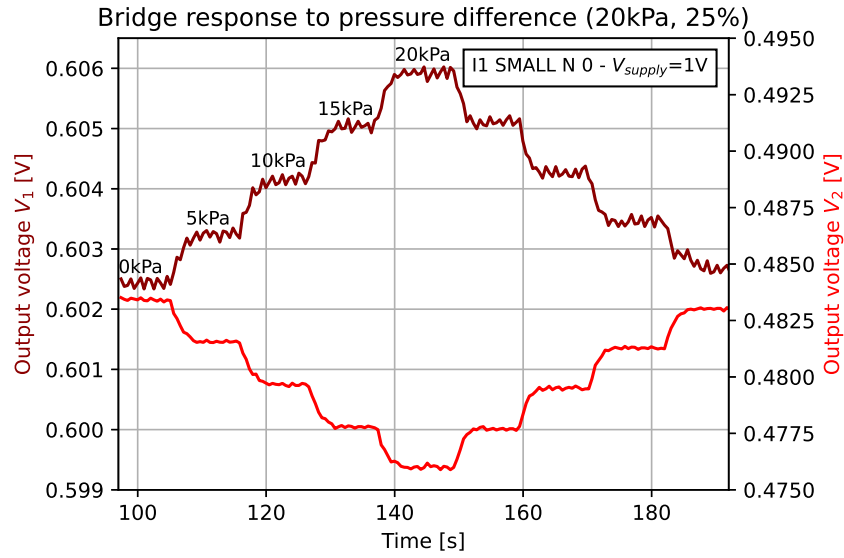


Figure 5.12: Bridge output voltages variation over time with positive pressure differences and fixed supply voltage for sample I1 SMALL N 0.

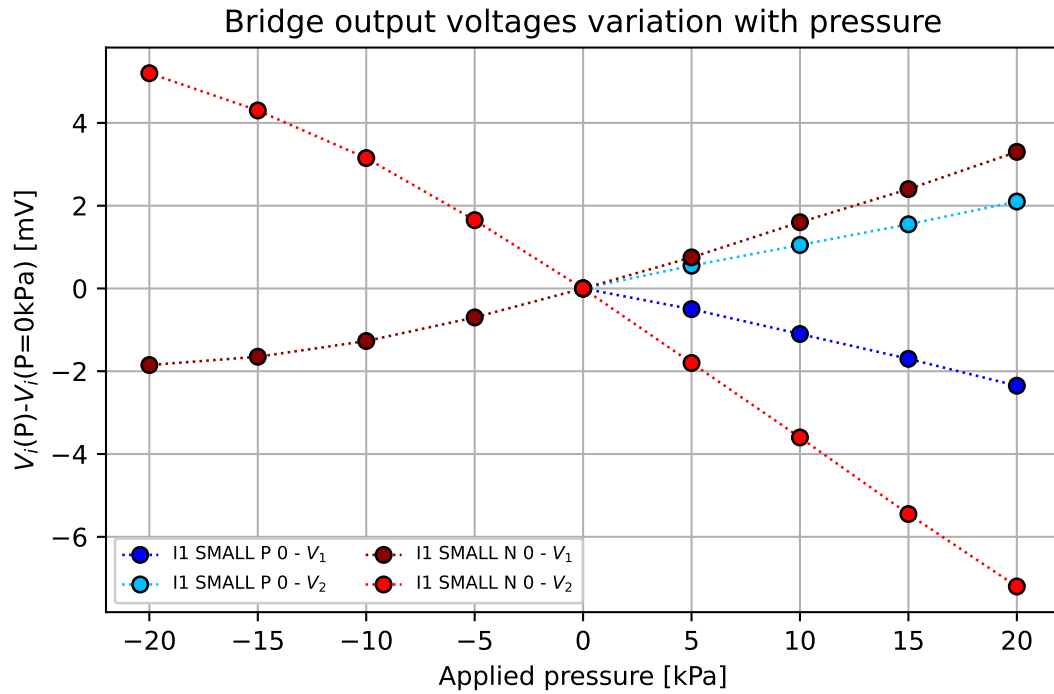


Figure 5.13: Bridge output voltages variation with pressure differences for each measured samples.

As expected with respect to the existing linear relationship between the current in the piezoresistances and pressure, the output voltages variation with pressure display a linear relation to pressure although both voltages don't necessarily vary symmetrically around y-axis=0V. The sign of the voltage V_1 and V_2 variations are in good agreement with respect to the piezoresistances orientation and doping type for both samples. In addition to the measures announced in Section 4.5.2, the output voltages variation with pressure from 0kPa to -20kPa was measured to get a first glance at the bridge response to negative pressure differences and the shape of the curve for sample I1 SMALL N 0 which appears to indicate that the response is not linear and requires full-fledged experimental and theoretical study. Finally the sensitivity of the two samples is calculated once the curves of the above graph are approximated by a first order polynomial for positive pressure values and is given in Table 5.4 below together with the sensitivity obtained for other sensors produced through several projects at UCLouvain and an industrial sensor for performance comparison. It is too early to draw any conclusions on the performance of the sensors from this work as a very limited number of designs were measured but an interesting improvement in sensitivity compared to the Biocloud sensor can already be noticed.

Name	Origin	Membrane area [mm ²]	Membrane shape	Membrane stack	Output response	Measurements conditions	Normalised sensitivity
Acuity - P[53]	Industrial	4	square+guard ring	Si - 3 μ m SOI - 0.25 μ m	105 μ V	4V,1Pa	6.5ppm/Pa/mm ²
A1 - P	UCL	0.25	orthogobal	Si_3N_4 - 500nm SiO_2 - 1000nm	5.9mV	1V,4kPa	5.9ppm/Pa/mm ²
I1 SMALL N 0	UCL	0.25	orthogonal	Si_3N_4 - 1000nm SiO_2 - 590nm	10.479mV	1V,20kPa	2.096ppm/Pa/mm ²
A2 - P	UCL	0.25	orthogonal	Si_3N_4 - 1500nm SiO_2 - 1000nm	-	-	1ppm/Pa/mm ²
I1 SMALL P 0	UCL	0.25	square	Si_3N_4 - 1000nm SiO_2 - 590nm	4.4mV	1V,20kPa	0.88ppm/Pa/mm ²
Biocloud	UCL	1	-	SiO_2 - 250nm Si_3N_4 - 300nm SiO_2 - 450nm	2 μ V	4V,1Pa	0.5ppm/Pa/mm ²

Table 5.4: Sensitivity comparison between UCL and Industrial pressure sensors whose measurements were taken at UCL.

5.3 Improvements on the present results

This section presents several prospects for improvement, both in terms of improving the results from the previous section as well as further expanding the study that was carried out on the silicon-based piezoresistive pressure sensors of this work.

5.3.1 Fabrication process

The main step that needs improving in the current fabrication process is the DRIE 4.3.2.12 of the membranes. Indeed the current produced membranes exhibit an overetching of 30 μ m and 10 μ m for orthogonal and square 0.5x0.5mm² diaphragms, respectively. This is due to the apparition of grass columns that need to be fully etched away in order for the membrane to be properly released which increases the number of etching cycles the die has to go through and eventually overetches the membrane sizes. In addition to the overetching reduction, a better control of the apparition of the grass in the first place would allow to maintain a 10'' initial etch and avoid rounding each corner of the diaphragm.

Regarding the stack itself, since two wafers have not been processed in the Oxford chamber for the deposition of the PECVD silicon nitride, numerous dies with an altered stack could be processed later on for further experimental studies. Another wafer without the frontside aluminium layer left on hold even earlier in the process is also available if the silicon dioxide layer were to be changed.

5.3.2 Complementary measurements

This section provides additional measurements that would complement the ones reviewed previously and improve the understanding of the observed phenomenons such as the bridge output voltages drift, the non-linear sensitivity for negative pressure differences and the bridge output signals noise.

Bridge asymmetry compensation Considering the design of the pressure sensors designed for this work is an open bridge, one could easily compensate the bridge output voltage offset on each branch with a calibration of the supply voltage with known values of the piezoresistances.

Additional designs and p-doped pressure sensors Measurements of the two n-doped designs, I1 SMALL N and I1 SMALL P, that were not measured but are already mounted on PCBs could allow to draw conclusions regarding the sensitivity difference between square and orthogonal membranes as square diaphragms are expected to exhibit a higher sensitivity for identical doping conditions. Speaking of doping conditions, six p-doped dies are waiting to be mounted on PCBs in order to enlarge the experimental study with p-type sensors which are expected to display sensitivity higher than 2ppm/Pa/mm² for their optimal P design with square membranes.

Climatic chamber measurements The measurement conditions could be improved with the use of a climatic chamber which was unfortunately booked during the entire measurement period of this work in order to measure the bridge output voltages thermal offset variation with temperature, the bridge output voltages thermal drift variation with temperature and the sensitivity to temperature [V/°C].

Topography measurements for negative pressure differences In addition to a study of the maximum pressure differences that can be imposed on the back side of the membranes produced without breaking, it would be interesting to define the bridge output voltages response to negative pressure differences for additional samples. A theoretical model that estimates the maximal deformations under the membrane thickness which take into account residual stresses would also be interesting for further researches.

Noise measurements The noise observed on the output signals (voltage and currents) which were not discussed previously manifests as small random fluctuations of the signal and are induced by various components within the circuit.[28] As introduced in the theory, the two main sources of noise in silicon resistors are the thermal noise which is proportional to the resistance value, and the flicker noise which is conversely proportional to the frequency and is the main limiting component for low-frequency measurements. This holds significance because piezoresistances find prominent usage in low-frequency static measurements.[54] By performing noise measurements with the Prober MPI 300mm together with a VNA 37369A 40 GHz in the Welcome facility, one could be able to discuss the shape of the noise curves to check which noises dominate at which frequency, their evolution with the supply voltage as well as identify specific signatures of default related noises.

The LoD could also be computed using Equation 1.37 with a simple method that consists of measuring the standard deviation of the noise of the output signals at a constant pressure, knowing the sensitivity of the sensor.

Chapter 6

Conclusion

The first chapter covered all the theoretical material gathered from literature needed for the purpose of this work. To effectively passivate p-type semiconductor surfaces, it was discovered that the fixed charge of the insulator stack should have the same sign as the inversion layer to prevent channel electrons tunneling the dielectric to the gate. In terms of mechanical properties, silicon nitride used together with silicon dioxide is of particular interest for sensing applications such as pressure sensing with micromechanical diaphragms. Indeed one is able to achieve small and tensile residual stresses using the Si_3N_4/SiO_2 stress-compensating dielectric stack.

In the second chapter, the fabrication of the four MOS stacks processed in order to assess the influence of Si_3N_4 at the oxide-SC interface was described and the residual stress measurement of each sample was estimated using curvature measurements. It was shown that residual stress in the Si_3N_4/SiO_2 increased with the aluminium annealing temperature and reached 679MPa tensile for sample OB3 annealed in forming gas at 515°C. The impedance dynamic of the measured stacks is discussed as the six-elements model used to correct the frequency dispersion of the measured capacitance in accumulation fails to properly correct the measured data of the samples.

The characteristics of the studied MOS stacks are given in the third chapter where the total insulator capacitance $C_{ins.}$, the flatband voltage V_{fb} and the fixed charge in the insulator layer Q_f are extracted from C-V measurements. The increase in aluminium annealing temperature showed to reduce the fixed charge density but its limit to 432°C, to prevent silicon nitride delamination and aluminium melting, restrained the improvement of fixed charge density. With regard to the interface trap density D_{it} estimated using both the conductance and high-low frequency method, their estimated values were questioned as no correction was applied to the measured conductance and capacitance.

The fourth chapter gave a thorough description of the experimental methodology for piezoresistive pressure sensors beginning with the design layout and fabrication process of the dies with a process adapted to the steps already performed on the wafers when this work took place. It was found that the main parameter which influences the drift is the supply voltage which was set to 1V for 0.5x0.5mm² membranes and to 0.5V for 2x2mm² ones. The most plausible cause given the strong dependence of the drift on the supply voltage, is a thermal drift of the bridge output voltages which depends on the difference between each thermal coefficient of the piezoresistances. Moreover, a mismatch between these TCR could explain the presence of the drift and the difference in drift observed from one branch to another.

The final chapter of this work included the results of each category of measurements performed on the sensors. The deflection with pressure of five n-type sensors showed good agreement with theoretical curves from membrane deflection theory and allowed to estimate a resulting stress on small and large membranes ranging from 50MPa to 70MPa tensile. The balance of the bridge was assessed for three sensors through I-V measurements and the piezoresistances values ranging from $7.7\text{k}\Omega$ to $21.018\text{k}\Omega$ were extracted from the linear current range. The current and bridge output voltages variation with current were measured with a positive pressure difference applied on the backgate of the membrane. The pressure ranged from 0kPa to 20kPa with 5kPa increments for $0.5\times 0.5\text{mm}^2$ membranes and from 0kPa to 2kPa for $2\times 2\text{mm}^2$ ones with 0.5kPa increments. Both the current and output voltages variation with pressure displayed a linear relation to pressure for positive pressure differences. Finally the maximal sensitivity obtained for a n-type sensor was computed and it reached $2.096\text{ppm}/\text{Pa}/\text{mm}^2$ for an orthogonal $0.5\times 0.5\text{mm}^2$ membrane. Further improvements are discussed at the end of this chapter as future prospects which includes a discussion on the grass control in the DRIE process step and complementary measurements such as noise measurements, topography measurements for negative pressure differences and measurements in the climatic chamber.

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Chapter 7

Appendix

7.1 Biocloud project

7.1.1 Sample structure

The schematic representation with a top and cross view for a given sample I1 BIG P from the Biocloud project is given in Figure 7.1 and 7.3. The membrane is composed of a O-N-O stack with a 600nm thick silicon dioxide layer, a 300nm thick silicon nitride layer and a 200nm thick silicon dioxide top layer.

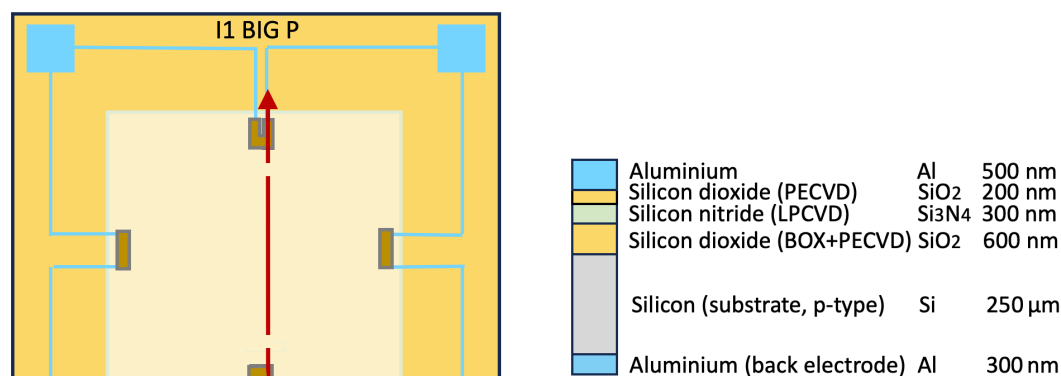


Figure 7.1: Schematic representation of the top view from a die "I1 Big P" with red arrow corresponding to the cross-section in Figure 7.3.

Figure 7.2: Schematic representation of the cross section of a Biocloud die with composition material and desired thickness for each layer.

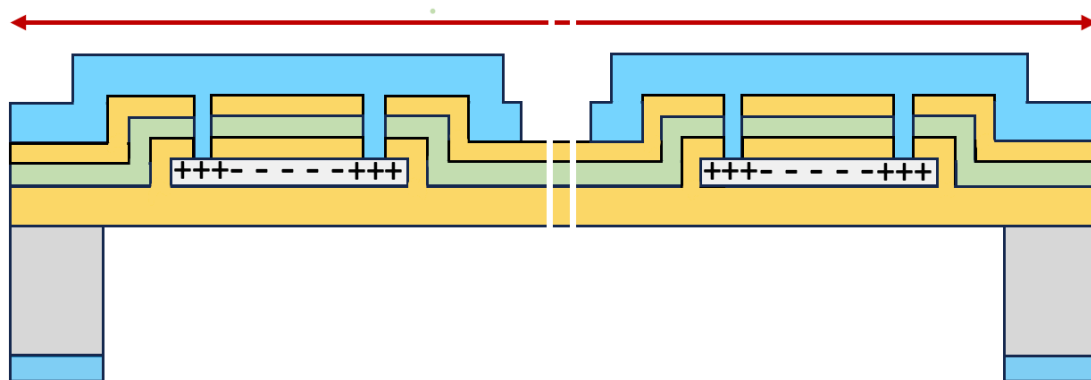


Figure 7.3: Schematic representation of the cross section of a die from the Biocloud project with composition material and desired thickness for each layer.

7.1.2 Central pattern design layout

The repeated pattern one can find on the central column of the design layout is shown in Figure 7.4 below. It is composed of four $520 \times 520 \mu\text{m}^2$ dies with $500 \mu\text{m}$ wide orthogonal membranes, two of which display a P-type configuration and the other two a N-type configuration, with and without islands. The main reason these dies were fully processed for this work is the difficulty firstly of handling the dies before and after the release stage of the membrane but also the low success rate for the wirebonding step of this type of die due to narrow gap of $10 \mu\text{m}$ between the edge of the die and the membrane which tends to break with the vibration of the wirebonding tip.

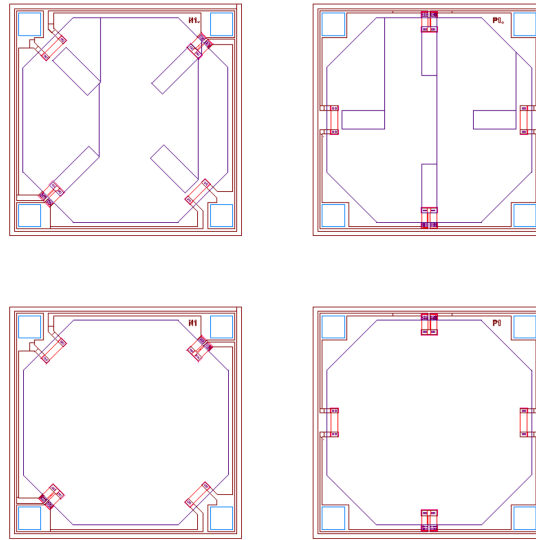


Figure 7.4: Central pattern design layout with 4 dies configuration : 2 N designs on the left and 2 P designs on the right, both with and without islands.

7.2 Additional results for silvaco simulations

This appendix aims to complement the results for Silvaco simulations presented in Section 4.3.1 with the visual diffusion for a n-doped silicon bar in Section 7.2.1 and a full simulation run for a p-doped silicon bar in Section 7.2.2.

7.2.1 Visual diffusion for a n-doped silicon bar

The visual doping diffusion for a n-doped silicon bar for each case study is shown in the figures below.

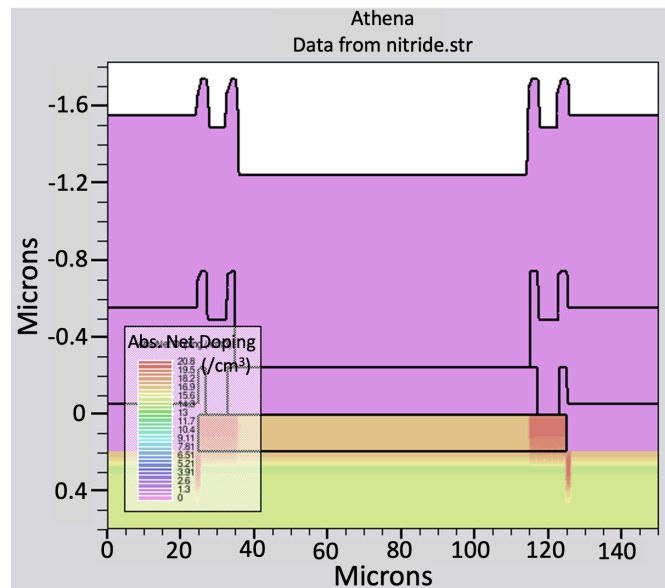


Figure 7.5: Diffusion plot for a n-doped silicon bar with one diffusion step at 850°C for 30 minutes.

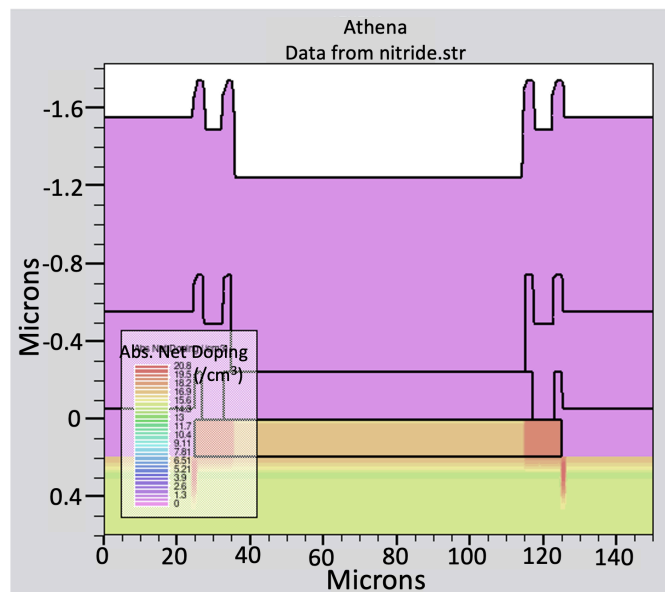


Figure 7.6: Diffusion plot for a n-doped silicon bar with one diffusion step at 950°C for 60 minutes.

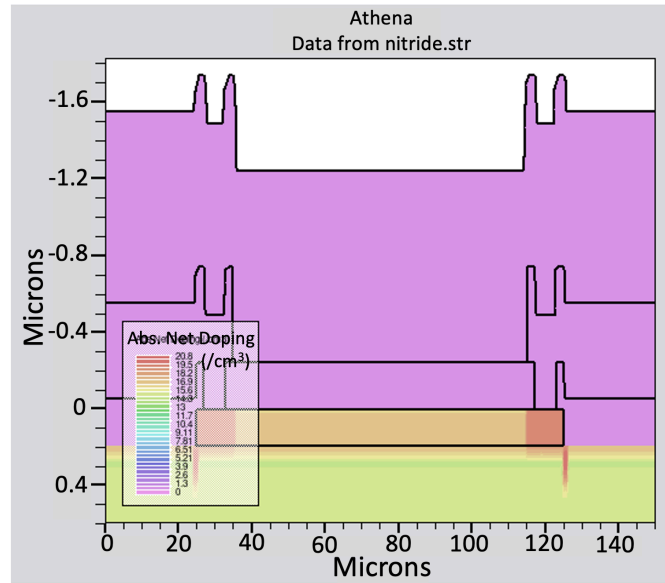


Figure 7.7: Diffusion plot for a n-doped silicon bar with one diffusion step at 850°C for 30 minutes followed by one diffusion step at 950°C for 60 minutes.

7.2.2 Simulations for a p-doped silicon bar

7.2.2.1 Silvaco absolute net doping simulated graphs for a p-doped silicon bar

The structure of the simulated stack is identical to the simulated n-doped silicon bar and is shown in Figure 4.9 where one can find the 4 numbered cutlines on which the absolute net doping was plotted to assess the doping levels of the silicon bar in each region of interest both vertically and horizontally. The same hypotheses regarding the simulation parameters were made for this stack. The results are shown for the p-doped silicon bar for each case study in Figures 7.8, 7.9 and 7.10. Based on the results obtained for both doping types, one can observe the dopants tend to diffuse slightly deeper with a 60 minutes diffusion step at 950°C but the orders of magnitude of the absolute net dopings are the same.

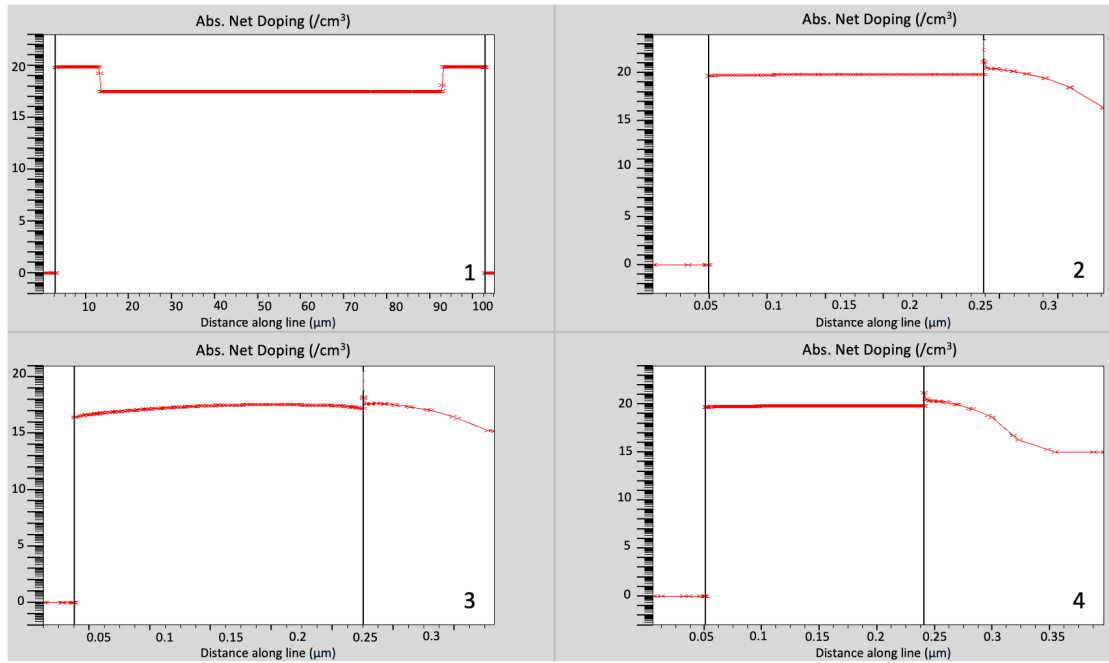


Figure 7.8: Silvaco absolute net doping simulated graphs for a p-doped silicon bar with one diffusion step at 850°C for 30 minutes. The numbers correspond to the cutlines in Figure 4.9 (right).

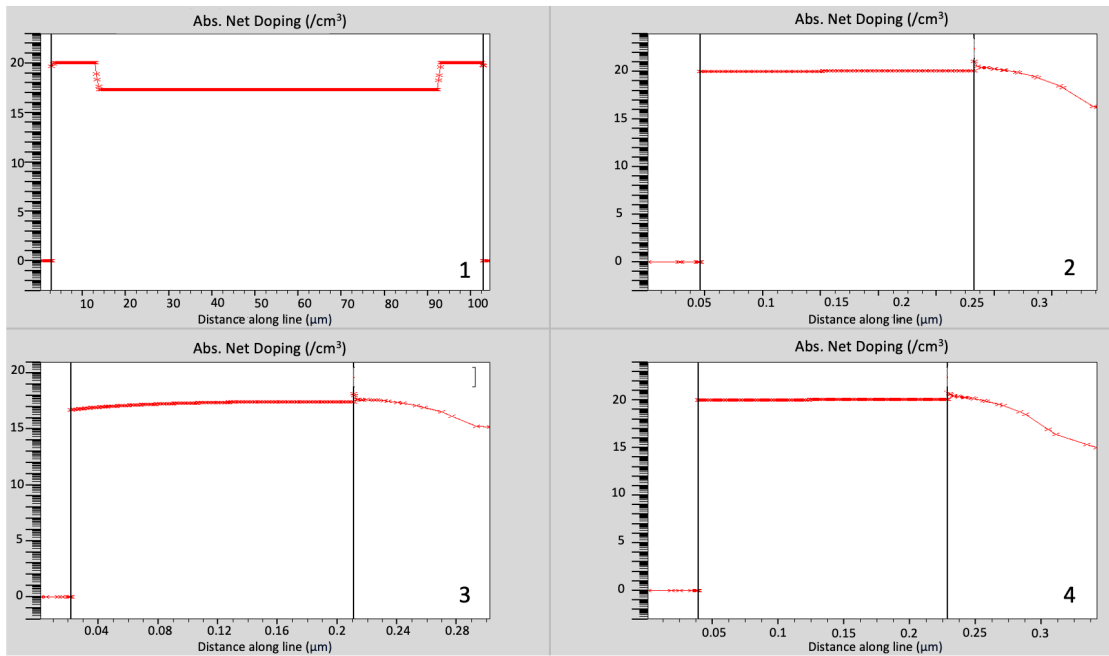


Figure 7.9: Silvaco absolute net doping simulated graphs for a p-doped silicon bar with one diffusion step at 950°C for 60 minutes. The numbers correspond to the cutlines in Figure 4.9 (right).

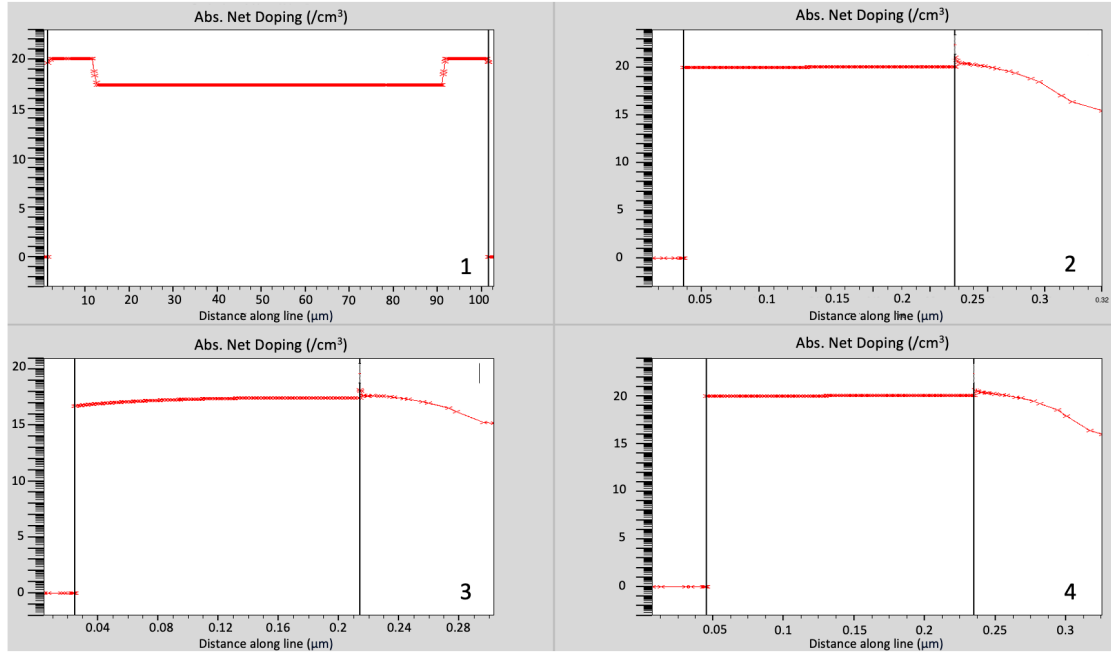


Figure 7.10: Silvaco absolute net doping simulated graphs for a p-doped silicon bar with one diffusion step at 850°C for 30 minutes followed by another one at 950°C for 60 minutes. The numbers correspond to the cutlines in Figure 4.9 (right).

7.2.2.2 I-V plots and resulting resistance for a p-doped silicon bar

By defining the aluminium layer as two electrodes, namely source and drain, the evolution of the drain current as a function of the gate voltage sweeping from 0V to 1V was plotted and the resulting simulated resistance in the actual 20μm width silicon bars could be obtained by first computing the resistivity of the simulated bar and recompute the resistance with a 20μm width using Equation 4.2. The obtained graphs are shown in Figure 7.11 together with the simulated resistance value.

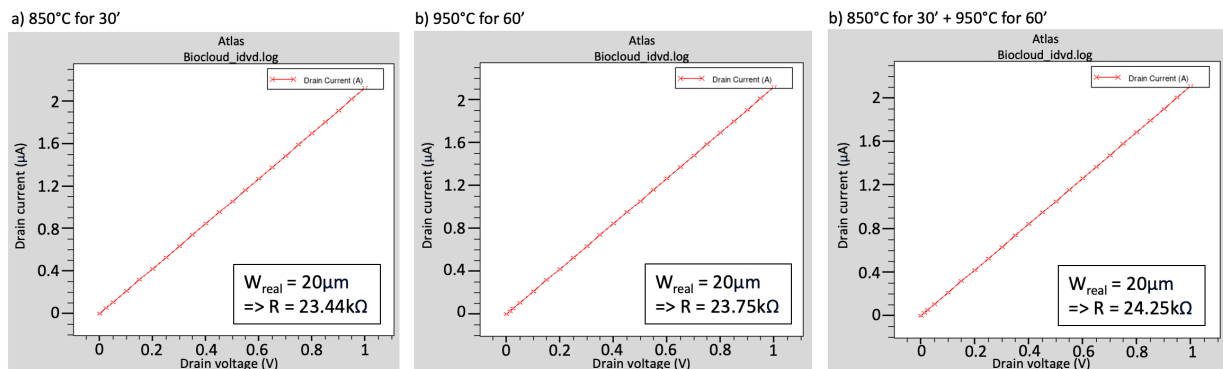


Figure 7.11: I-V plots for each case study and the resulting resistance.

7.2.2.3 Visual diffusion for a p-doped silicon bar

In addition to the previous graphs, the visual doping diffusion for each case study is shown in the figures below.

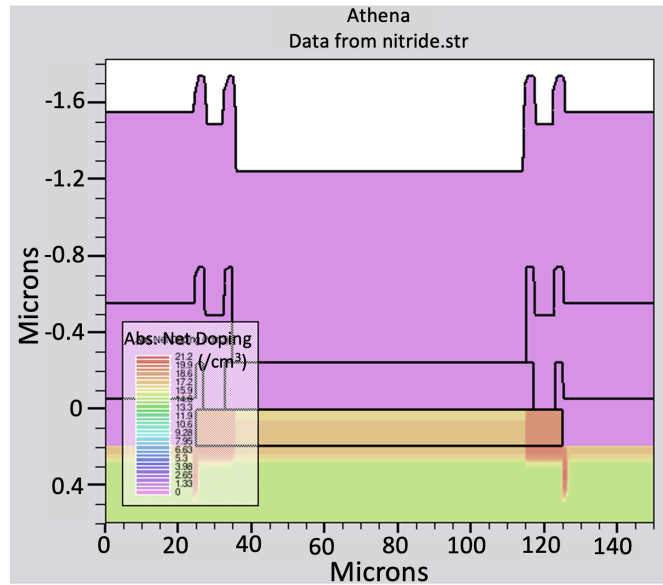


Figure 7.12: Diffusion plot for a p-doped silicon bar with one diffusion step at 850°C for 30 minutes.

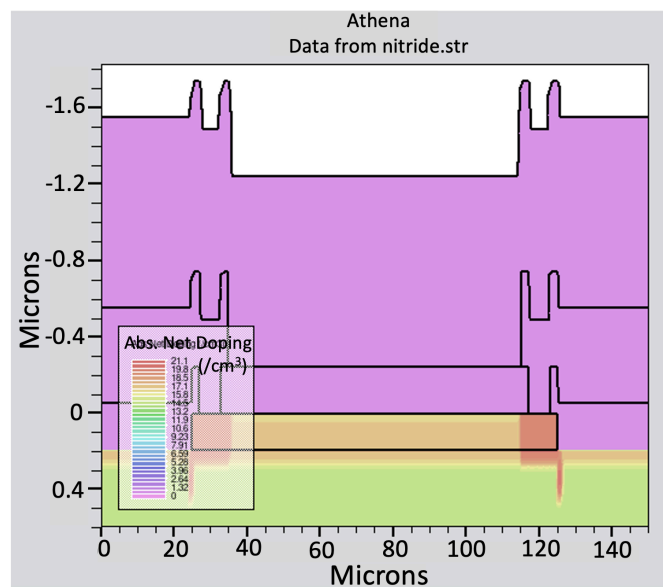


Figure 7.13: Diffusion plot for a p-doped silicon bar with one diffusion step at 950°C for 60 minutes.

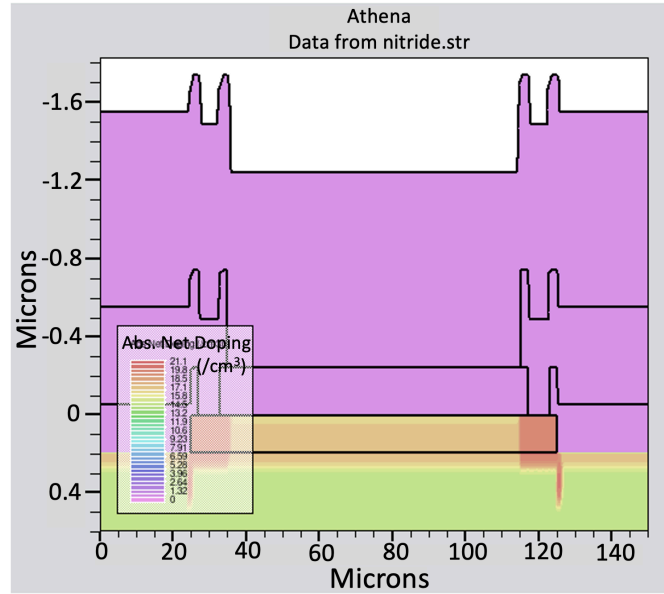


Figure 7.14: Diffusion plot for a p-doped silicon bar with one diffusion step at 850°C for 30 minutes followed by one diffusion step at 950°C for 60 minutes.

7.3 Sample cleaning techniques

7.3.1 Standard cleaning

A standard cleaning is a cleaning process performed to remove all organic contaminants, thin metal films such as native oxide and dust from a wafer and is used for pre-furnace process.[35] Note the standard cleaning procedure described hereafter is specific to the Winfab facility. It consists in a succession of chemical and DI water baths with fixed immersion time for each of them. The baths must first be emptied and refilled according to previous uses and the following cleaning sequence can take place :

- **Bath 1** : First the wafers stacked in a trail are placed in a bath with sulfuric acid (H_2SO_4) mixed with hydrogen peroxide (H_2O_2) with a 4:1 ratio[8], also called a piranha solution. The reaction being exothermic, one has to wait for the bath to settle to a 120°C temperature before placing the trail in the bath for 10'.
- **DI water bath** : The trail is then placed in the DI water bath for a 10' rinsing step under a continuous flow of not only DI water but also nitrogen bubbles activated once a succession of 5 emptying/refilling of the bath is done with a continuous flow of DI water on the trail lying in the bath. This process enables the wafers to be rinsed, thereby halting the chemical reaction, eliminating all traces of the piranha solution, and dislodging any particles that might be loosely adhered to the wafers.

- **Bath 2** : The trail is placed in another piranha bath with the same $H_2SO_4:H_2O_2$ ratio prepared before hand as well.
- **DI water bath** : The wafers are rinsed once again following the rinsing sequence described for the first DI water bath.
- **HF bath** : This bath is optional as it aims at removing an undesired oxide layer. The trail is firstly placed in HF for 10" and immediately put in a portative overflowing DI water bath for 5'.
- **DI water bath** : A final bath of DI water that is running 24/7 in the Winfab facility is taken for at least 10' and a flow of bubbles is activated once the trail is submerged.
- **Rinser dryer** : The trail is placed in a rinser dryer to be rinsed one last time with DI water before being spin dried by a nitrogen flow, while being in constant rotation.

7.3.2 Fuming nitric acid cleaning

Fuming nitric acide (HNO_3 95%) can be used to remove organic contaminants from a wafer and is usually used to instead of standard cleaning once a metallisation on the wafer has been performed as the metallic layer could be damaged by a piranha or a HF bath. Fuming nitric acid exhibits a high degree of selectivity towards silicon, silicon dioxide, and aluminum. This property makes it suitable for application after metallic contacts have been established in a process. As for the procedure to follow, the wafers are first placed on a trail and submerged in a beaker filled with nitric acid for 5' and then rinsed under a continuous flow of DI water in another beaker for 10'.[35]

7.4 Processing techniques

7.4.1 Physical Vapor Deposition

Physical vapor deposition is a category of techniques employed for depositing thin film materials. In this method, the material to be deposited is introduced into the equipment in its original form. Through physical processes like heat application or ion bombardment, the material is liberated from its source and deposited onto the wafer. Unlike chemical reactions, the foundation of this deposition technique is mechanical in nature, driven by physical principles.

7.4.1.1 Thermal evaporation VST

Thermal evaporation is a PVD technique that is performed in the VST equipment in the Winfab facility. When using e-beam thermal evaporation whose schematic representation is given in Figure 7.15, a current is first passed through a tungsten

filament which leads to joule heating and electron emission. High voltage is applied between the filament and the ground to accelerate these liberated electrons concentrated into a unified beam thanks to a strong magnetic field towards the crucible containing the material to be deposited. The energy of this beam of electrons is then transferred to the deposition material, in this work pellets of aluminium, causing its evaporation and deposition at the surface of the dies. The latter are fixed upside down on a wafer placed on a rotating platform and rotating on themselves simultaneously. Depending on the aperture of the crucible the walls of the chamber will be covered in aluminium as well, which is part of the process.[55]

E-beam evaporation has high deposition rates which vary with the material to be deposited, 12.5nm/min in this work, because it is capable of heating materials to much higher temperatures than it would be possible to achieve with crucible heater for example. Furthermore, films deposited by this technique can better maintain the purity of the source material by eliminating any undesirable components that might contaminate the vapors thanks to a water cooling of the crucible which tightly confines the electron beam heating to only the area occupied by the source material [55].

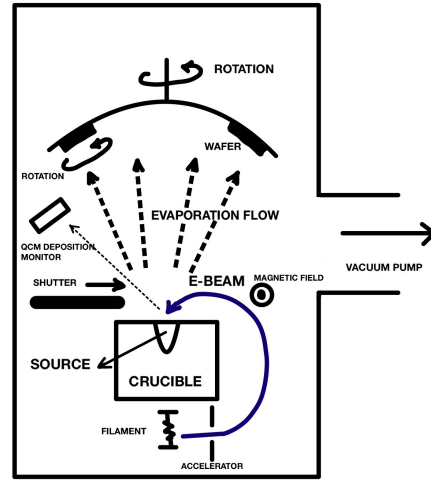


Figure 7.15: E-beam evaporation schematic representation.

7.4.2 Wet etching

Wet etching processes are based on the principle of transforming solid materials into liquid compounds through the use of chemical solutions. These processes exhibit a high level of selectivity, primarily due to the ability to finely tailor the chemical solutions to match the specific characteristics of each film being treated.

BHF bath Buffered HF can be used to etch silicon dioxide. It is composed of NH_4F -40% and HF-49% with ratio 7:1. NH_4F plays a critical role in neutralizing the solution. When the pH of the solution falls below 3, the resist layer used to protect some surface patterns can be etched with the conventional HF bath. However, by adjusting the solution's pH through tempering, its value is increased, ensuring that the resist remains intact and unaffected. The NH_4F therefore acts as a buffer to reduce the rate of etching and allows better control of the latter.[35]

H_3PO_4 bath It is a chemical wet etching used to etch pure Al and Al/Si-1% by using a resist mask to protect the patterns that must be kept onto the wafer. The bath contains H_3PO_4 -85% and IPA ($CH_3CH(OH)CH_3$) with the proportion

500:200ml. The density of the liquid has to be adjusted with the hydrometer to ensure a 1.45 density. As for the temperature it is set to 65°C for pure Al and 55°C for Al/Si-1% for a n etching rate of 300nm/min.[35]

7.4.3 Nitrogen degassing

Performing a nitrogen degassing in the Tempress furnace serves the purpose of removing any volatile contaminants or gases present on the wafer's surface. This process helps create a clean and controlled environment before proceeding with further steps, such as thin film deposition. The high temperature facilitates the release of these contaminants from the wafer's surface, ensuring that subsequent deposition processes occur on a clean substrate, which can improve both film quality and adherence. When performed after a standard cleaning, it ensures that any remaining volatile compounds are driven off by the high temperature and the flow of nitrogen. This additional step helps to further purify the wafer's surface

7.4.4 Grinding

Grinding is performed using the Grinder G&N MPS 2R 300S in the Winfab facility to thin the backside layer of a wafer. It is usually used to reduce the thickness of the silicon substrate of 3inch wafers and is done with grind wheels with rough and finer diamond grids under a continuous DI water flow.[35] A blue tape is often placed on the frontside of the wafer and cut to its shape to protect it during the grinding process. The grinding equipment works on the following principle: the wafers are placed individually on a 3inch circular platform and the air underneath is sucked to make sure that the wafers stay in place during the grinding process. Then the grinding wheel slowly goes down and by doing so, etches the backside of the wafers vertically. Once the grinding is finished a step called "sparking-out" occurs during which the wheels stay in place and rotate at the same level to smooth out the surface. However some grinding traces usually remain on the surface of the wafer which can be constraining depending on the rest of the process.

7.4.5 Dicing

Dicing a wafer consists in cut the wafer in order to separate each die according to predefined cutlines. The wafer must be spin coated before hand with a blue resist that protects the surface of the dies from dust and the backside is reinforced with adhesive blue tape which eventually helps keep all the dies together after the dicing process. The tempress 602 dicing equipment from the Winfab workshop can be used to dice silicon, glass and quartz for wafers up to 4inch and the individual die area must be at least 2x2mm². The depth of the cutlines can reach up to 1µm.[35]

7.4.6 Wirebonding

The ultrasonic wedge wire bonder is engineered to establish wire connections between contact pads of a manufactured die glued on a PCB. The bonding wires are either in gold (Au) or aluminium (Al) and have diameter of 20μ . The 4500 Digital Series Manual Wire Bonder in the Winfab workshop has some imperative requirements regarding the design of the pads as their minimum size must be $70 \times 70 \mu\text{m}^2$ with a minimum spacing between the dies of $50\mu\text{m}$. [35] The parameters such as the ultrasound frequency, the power, the bonding forces and bonding temperature must be adapted according to the die specifications.

7.5 In-process metrology devices

7.5.1 Ellipsometer

An ellipsometer is a commonly used optical thickness measurement method. The process involves directing a laser beam at a specific angle onto the wafer and scanning the wavelength of the light source. This light interacts with the various layers of materials in the wafer's stack, undergoing transmission, reflection, and diffraction. A sensor subsequently gauges the amplitude, phase, and polarity of the transmitted light. By knowing the optical constants of the film, the technique allows for the determination of film thickness as the software will estimate the diffraction pattern and attempt to match the measurement with the projected curve. [8]

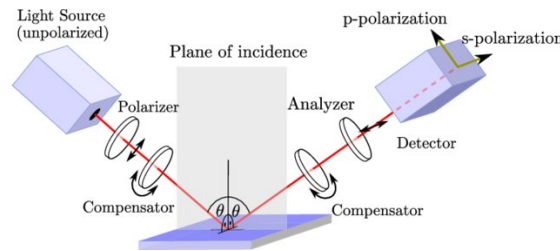


Figure 7.16: Ellipsometer schematic representation. [56]

In the case of extremely thin films, ellipsometry's accuracy diminishes due to the fact that the optical constants of films with thicknesses below 10 nm are not truly constant, despite the high precision. Conversely, for thicker films, the presence of multiple reflections and interference results in a periodic solution, necessitating supplementary information to determine the specific period in question. [8]

7.5.2 Profilometer

A profilometer is an instrumental tool used for characterizing materials, enabling the measurement of a wafer's profile and topography. The profilometer in the

Winfab facility is referred to as the Dektak which is a stylus profilometer. It uses a diamond tip that contacts the sample and takes the z-axis measures while moving in the x or y direction. To do so, it has to apply a constant force to keep in touch with the material and it uses the response of the tip to analyse the profile of the device. The obtained profile curves allow for example to compute the stresses induced by the deposition or the removal of a layer of material from the wafer's surface.

7.5.3 Scanning Electron Microscope

The SEM is a type of electron microscope that scans surfaces of microorganisms. It uses a beam of electrons moving at low energy to focus and scan specimens. It works on the principle of applying kinetic energy to produce signals on the interaction of the electrons. These electrons are secondary electrons, back-scattered electrons, and diffracted back-scattered electrons which are used to view crystalized elements and photons. The secondary and back-scattered electrons are used to produce an image. The secondary electrons are emitted from the specimen and play the primary role of detecting the morphology and topography of the specimen while the back-scattered electrons show contrast in the composition of the elements of the specimen.

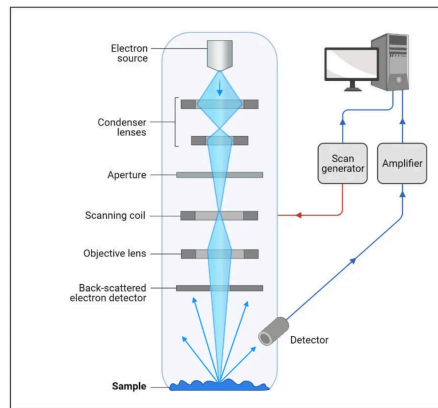


Figure 7.17: SEM schematic representation.[57]

In contrast to optical systems, the SEM's resolution is not constrained by diffraction limits, lens or mirror precision, or detector array resolution. Depending on the specific instrument, the resolution typically ranges from less than 1 nm to around 20 nm.[57]

