

École polytechnique de Louvain

Quantum bits coupling through titanium nitride superconducting nanostructures

**Towards phosphorous atoms and CMOS qubit
manipulation**

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Abstract

As quantum computing is expanding at an increasingly fast pace, the qubits hosted by the quantum processing chip are getting increasingly crowded. Yet, close proximity interactions between two qubits become rare as they are getting further apart in complex architectures, separated by many physical gates connections and many other qubits. This Master's thesis aimed at implementing titanium nitride superconducting nanostructures as a mean to couple and apply quantum gates on two distant qubits to be implemented in silicon, given the similarities between spin qubits and complementary metal-oxide-semiconductor transistors. Fabrication of titanium nitride by atomic layer deposition was prospected, and some key steps for designing quantum chips have been established. In particular, nanofabrication protocols for the realization of titanium nitride resonators and vias were put forward.

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AI usage disclaimer

This thesis has benefited from the use of various AI tools and technologies which have been instrumental in enhancing the quality and efficiency of the research and writing process. Specifically, the following AI tools have been employed:

- **ChatGPT:** Used for paraphrasing, generating summaries of PDFs, suggesting search keywords, and offering general assistance.
- **Monica Browser Extension:** Utilized for browsing and summarizing online content, and suggesting deepening research tracks.
- **DeepL Translator:** Used for translating text to ensure clarity and accuracy in multilingual content understanding.
- **Online AI Image Enhancers and Editors:** Various online tools were used to enhance and edit images included in this thesis. These tools helped in improving image clarity, resolution, and overall presentation quality.

The integration of these AI tools has been done in accordance with ethical guidelines and to ensure that the core research and analysis remain original and authentic. All interpretations, conclusions, and findings presented in this thesis are my own.

I acknowledge and take full responsibility for the content and any errors or omissions that may remain. The use of AI tools has been reserved for the purpose of improving the efficiency and clarity of my work, and not for generating original content or conducting research on my behalf. The sole exception being this very section, courtesy of ChatGPT.

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Chapter 1

Introduction

1.1 Quantum computing technologies

There are many types of quantum bits linked to various physical implementations, each with its own specific features and constraints. Of all these implementations, eight of the most important qubits to date and their subtypes are discussed hereafter. The two main subtypes of semiconductor qubits of interest for this thesis are further discussed in Section 1.1.1 and Section 1.1.2.

- **Superconducting qubits** : One of the most advanced type of qubits so far, superconducting qubits are already widespread across the industry. They often contain Josephson junctions, which are superconducting tunnel junctions formed from a thin layer of a non-superconducting material surrounded by two layers of superconducting material. Most superconducting qubits are fabricated onto silicon or sapphire substrates using complementary metal-oxide-semiconductor (CMOS) compatible techniques. [26]
They are subdivided into three types of fundamental qubits, which are : firstly, charge qubits, with quantum states given by the number of Cooper pairs on an island isolated by a Josephson junction (JJ) from a large superconducting reservoir; secondly, flux qubits, with quantum information and behaviour coming from the presence or absence of magnetic fluxons of circulating currents in a superconducting loop interrupted by a small Josephson junction in series with other components; [26] thirdly, transmon qubits, with their name coming from "transmission lines qubits", being a variant of the charge qubits placed into a superconducting resonator (*i.e.* a JJ with two superconducting islands and no reservoirs). [23]
- **Trapped ion qubits** : Particularly notable for their very long coherence time, trapped ion qubits have been studied for a long time. They are based upon isolated ions confined in radiofrequency traps, controlling the qubits states. Trapped-ion qubits can be categorized into four main types: hyperfine qubits, characterized by qubit states as hyperfine states of the ion with an energy splitting on the order of gigahertz; Zeeman qubits, where qubit states are magnetic sublevels split by an applied field; fine structure qubits, which involve qubit states residing in fine structure levels with separations typically in the tens of terahertz; and optical qubits, where the qubit states are distinguished by an optical transition. [4]
- **Semiconductor qubits** : Quantum dots qubits are a very common type of qubit that leverages semiconductor quantum dots (QDs), nanoscale regions where electrons are confined. These nanoscale regions are usually surrounded by electrostatic gates, controlling the interactions between dots and delimiting the electrons' confinement area. [15] The confinement area can also come from one or multiple donor atoms incorporated at precise locations; this technology of specific interest

for this thesis will be elaborated upon in greater detail in Section 1.1.1. Semiconductor quantum dots are made upon heterostructures of GaAs/AlGaAs or Si/SiGe as well as silicon metal-oxide-semiconductor structures; the latest being also of particular interest for this thesis and detailed in Section 1.1.2.

The quantum information from this type of qubits can either be in the form of : spin qubits, encoding quantum information in the intrinsic angular momentum, or spin of particles, either holes or electrons; or charge qubits, encoding quantum information in the electric charge of particles, their presence and absence being the $|0\rangle$ and $|1\rangle$ states.

- **Topological qubits** : Topological quantum computation uses non-Abelian ¹ quantum phases of matter. Qubit manipulations protects it from imperfections and from interactions with the environment. [43] The $|0\rangle$ and $|1\rangle$ states of the qubits come from interchange operations where there are two possible outcomes.
- **Diamond nitrogen-vacancy centre qubits** : Another type of implementation for spin qubits is the diamond nitrogen vacancy (NV) centres with excellent spin coherence and optical properties. They are made by a nitrogen atom substituting a carbon one and an adjacent vacancy in the diamond lattice. [33] As they are spin qubits, the quantum states come from the up and down states of an electron spin.
- **Nuclear magnetic resonance qubits** : Nuclear magnetic resonance (NMR) qubits were one of the first qubits type. NMR systems can be in liquid or solid-state. The quantum states come from atomic nuclei spin states. They are controlled by nuclear magnetic resonance spectroscopy and radio-frequency (RF) pulses. [47]
- **Photonic qubits** : As quantum properties are readily available for photons, it goes without saying that scientists tried implementing photonic qubits. Photons have multiple ways of encoding quantum information, some of the qubits coming from photons' properties are : polarization qubits, with information encoded in the polarization state of a photon; phase qubits, with information stored in the phase of a photon's wavefunction and are manipulated through phase shifters; path qubits, for which quantum information is the path traversed by the photon in a multi-branching circuit. [42] Photonic qubits are typically generated using sources such as lasers, resonators, quantum dots or nonlinear crystals. They can be manipulated using various optical elements like beam splitters, phase shifters, and polarizers.
- **Majorana qubits** : Sharing many similarities with topological qubits, Majorana qubits come from Majorana fermions, fermions that are their own antiparticle, and also obey non-Abelian statistics. They are made of one-dimensional semiconducting nanowires partially covered with a conventional superconductor, at the end of which the Majorana zero mode ² emerges. Majorana qubit states come

¹Non-Abelian quasiparticles are anyons, quasiparticles only existing in two dimensions, for which, after two particles are exchanged, their phase experiments a shift of $\theta = 2\pi\nu^{-1}$ (while for bosons and fermions it is 0 and π). This means that if the particles interchange twice, the system will not return to its previous state. Abelian quasiparticles are particles for which the interchanging order is unimportant, non-Abelian have thus the contrary condition. [38]

²Majorana zero mode is the zero energy excitation mode of Majorana quasiparticles emerging in the vortex core of topological superconductors. [44]

from even and odd parities of the two Majorana fermions of the wire (one at each end), forming a two-fold degenerate ground state. [27]

Ultimately, all these technologies converge towards a common objective : establishing a reliable and scalable approach for the development of quantum computers. This aims to enable the resolution of problems and the execution of simulations that were previously impossible within a reasonable timeframe. Table 1.1 compiles the lists of quantum computing potential use cases given in Ref. [32]. Those applications, along with possible others, will naturally discover utility across various sectors and span more and more over time.

Main topic	Use case	Description
Quantum chemistry	Molecular dynamics	Simulating the motion of atoms and molecules over time, which is important for understanding chemical reactions and protein folding.
	Electronic structure calculations	Determining the electronic structure of molecules and materials, which is important for understanding chemical bonding and predicting the properties of materials.
	Quantum Monte Carlo	A simulation method for quantum systems that can be used to calculate the properties of molecules and solids.
	Quantum chemistry in general	The simulation of the behaviour of molecules and chemical reactions at the quantum level, which would allow for more precise predictions of the properties of molecules, and the interactions between them.
Financial modeling	Portfolio optimization	Using quantum computing to optimize the performance of a portfolio of financial assets.
	Risk management	Using quantum computing to simulate and analyse different scenarios to better understand and manage financial risks.
	Option pricing	Using quantum computing to price financial derivatives, such as options, more accurately and quickly.
	Machine learning	Using quantum computing to train machine learning models on large financial datasets to make predictions and identify patterns.
	Cryptocurrency and blockchain	Using quantum computing to enhance the security of blockchain-based systems and to develop new forms of cryptocurrency.
	Fraud detection	Using quantum computing to analyse large amounts of financial data in real-time to detect fraudulent activity.
Black box problems	Global optimization	Many black box problems involve optimization, where the goal is to find the best solution out of numerous possibilities. Quantum computing can be used to search through large solution spaces more quickly than classical computers, making it well-suited for global optimization problems.

Main topic	Use case	Description
	Machine learning	Quantum computing can be used to train machine learning models on large datasets, even when the underlying data distribution is not known. This can be useful for applications such as image recognition and natural language processing, where the internal workings of the system are not fully understood.
	Cryptanalysis	Quantum computing can be used to break encryption schemes that are currently considered secure. Cryptanalysis is a black box problem as the internal workings of the encryption scheme are not known, but the encryption key is. Grover's algorithm and Shor's algorithm are two of the famous algorithms which are theoretically shown to be very useful in this domain. In fact, it has been predicted that the implementation of Shor's algorithm will completely disrupt the cybersecurity domain.
Machine learning	Speed-up of training	Quantum computing can be used to speed up the training of machine learning models by allowing them to process large amounts of data more quickly. This is particularly useful for training deep neural networks, which require a lot of computational resources.
	Quantum machine learning	Quantum machine learning is a field that combines quantum computing and machine learning; it uses quantum algorithms for tasks such as unsupervised learning, supervised learning, and reinforcement learning.
	Quantum kernel methods	Using quantum computing to define new types of kernel functions, which can be used in support vector machines and other kernel-based machine learning algorithms to improve their performance.

Table 1.1: Potential use cases of quantum computing. [32]

1.1.1 Quantum computing with phosphorus atoms

Overview

Phosphorus doping is an essential advancement in semiconductor technology, particularly in the realm of integrated circuits and quantum computing, playing a significant role in enhancing electronic and optoelectronic device performances. In integrated circuits, phosphorus doping into silicon substrates is employed to create n-type semiconductors, which is essential for the development of high-performance classical computing devices. Currently, new techniques are elaborated for allowing continuous scaling of integrated circuits while preserving or even reducing power budget and saving manufacturing expenses.

As the challenges associated with quantum error correction and scalability are dominant in the field of quantum computing, phosphorus doping emerges as a promising enabler for the development of practical and scalable quantum computing architectures.

Cost-effective dopant integration technologies

In Refs. [3, 53], an innovating and frugal way of introducing dopants into silicon substrates was introduced. Spin-on-dopant phosphorus integration takes place in three steps : first, patterning by lithography reveals the area to be doped; second, the dopant of interest is spin coated onto the substrate; third, a rapid thermal annealing diffuses the dopant in the substrate. In Ref. [53] the integration is made into silicon nanosheets instead of a silicon-on-insulator (SOI) wafer as in Ref. [3]. This technique is of particular interest as it is a simple, uniform and high-yield doping method with expenses diminished significantly. The simple process control involved in the three previously-mentioned steps allows fine-tuning; the annealing step in particular making way for different donor depth profiles.

Phosphorous donor qubits

The minimal gate density exhibited by isolated dopant atoms, coupled with their robust capacitive coupling and weak spin-orbit interaction, is the key for qubits with long spin relaxation times T_1 . [22, 24] Phosphorus atoms' spin of $\pm\frac{1}{2}$ implies that in such qubits, both the electron and the nucleus can serve as means of storing and processing quantum information. [28] The energy splitting between two states in the same qubit comes from the Zeeman effect following $E_Z = \gamma_e B_0$, with $\gamma_e = g\mu_B = -1.76 \times 10^{11}$ rad/s.T the electron gyromagnetic ratio, B_0 the static magnetic field, g the Landé g-factor and μ_B the Bohr magneton. [30] For two distinct, neighbouring qubits labelled L and R, the energy splitting corresponds to:

$$\Omega = \sqrt{J^2 + \Delta E^2}, \quad (1.1)$$

with Ω the inter-qubit energy splitting, J the electron wave function's magnitude and ΔE the absolute difference between the two qubits energies. Since

$$E = g\mu_B B_0 + \sum_{i=1}^N \langle I_z \rangle_i A_i, \quad (1.2)$$

with N the qubit's constituting number of donors, $\langle I_z \rangle = \pm\frac{1}{2}$ the expectation value of the nuclear spin operator and A the hyperfine coupling parameter ³:

$$\Delta E = |E_L - E_R| = \left| \sum_{i=1}^{N_L} \langle I_z \rangle_i A_i - \sum_{j=1}^{N_R} \langle I_z \rangle_j A_j \right|. \quad (1.3)$$

Equations 1.1 and 1.3 play a prominent role for two qubits exchange operations. Possible ΔE differences for interactions between a 3-phosphorus quantum dot qubit and a 2-phosphorus quantum dot qubit are displayed in Fig. 1.1. [28]

A significant distinction between standard quantum dot qubits and phosphorus donor qubits lies in the elimination of external micromagnets, and with it, the reduction of several fabrication steps. This originates in the utilization of nuclear spins as inherent magnets; precise engineering of nuclear spin leads to a great control over the magnetic field gradient, which is a key property for numerous applications. Differences with quantum dot-based qubits are illustrated in Fig. 1.2. Nuclear magnetic resonance allows

³The hyperfine coupling between an electron spin and a nuclear spin leads to small energy shifts in the atomic energy levels, known as hyperfine structure.

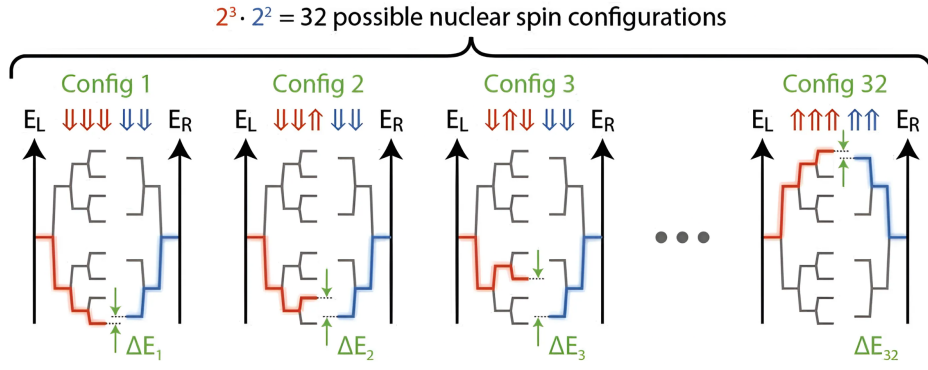


Figure 1.1: Nuclear spins configurations in a 3P-2P qubits coupling scenario. [28]

an accurate control over nuclear spins. [29] Asymmetry in the number of phosphorus atoms between qubits reduces spin relaxation and dephasing that originated from the magnetic field gradient's longitudinal part ($\nabla B_{\parallel}$). Nuclear spin engineering controls $\nabla B_{\parallel}$ and by adjusting ΔE judiciously, it increases two qubit gates fidelity. [30, 22, 29] Charge noise stands out as the principal limiting factor for qubit operation, but its impact can be reduced through the application of a high magnetic field gradient (above 800 MHz). In Ref. [24] it has been discussed that the spin relaxation rate is proportional to B^5 for magnetic fields above 3 T and below it follows a B^3 dependence for qubits constituted of multiple donors; while CMOS qubits are displaying a B law.

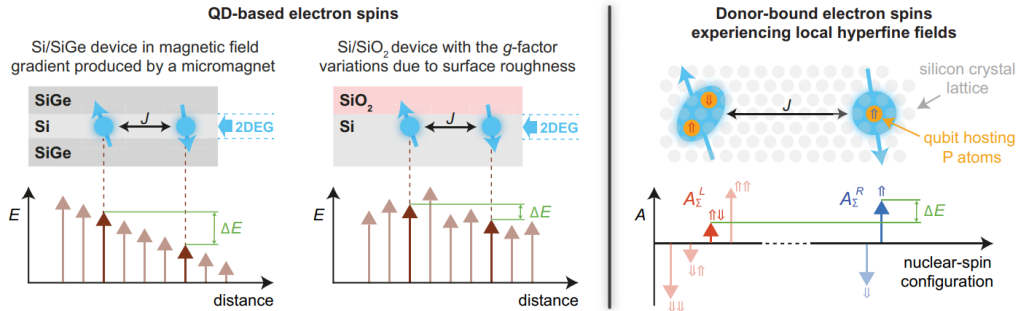


Figure 1.2: Illustration of the differences between quantum dot-based qubits and donor nuclear spin-engineered qubits. [29]

Tuning of phosphorus donor qubits can be achieved through two primary methods: adjusting the number of phosphorus atoms within each quantum dot and varying the inter-dot distance. Incrementation of phosphorus atoms' number per dot strengthens the energy of the frontmost ⁴ electron, which in its turn increases the transversal magnetic field gradient $\nabla B_{\perp}$ driving a higher hyperfine coupling A . *Per contra*, a larger hyperfine coupling upon one of the dots implies a larger $\nabla B_{\parallel}$ but this issue can be resolved by filling the quantum dot with more electrons for a shielding effect. [30] The hyperfine coupling value for each atom A_i is directly proportional to the number of donors per quantum dot, thereby allowing precise control over ΔE by judiciously selecting these numbers.

Additionally, the positioning of phosphorus atoms introduces further complexity to the modulation of A and ΔE . [29] In Ref. [22], it is stated that sensible tuning of atomic distances facilitates high-fidelity and independent spin readouts, but that

⁴Inside the dot of interest, the closest to the second quantum dot.

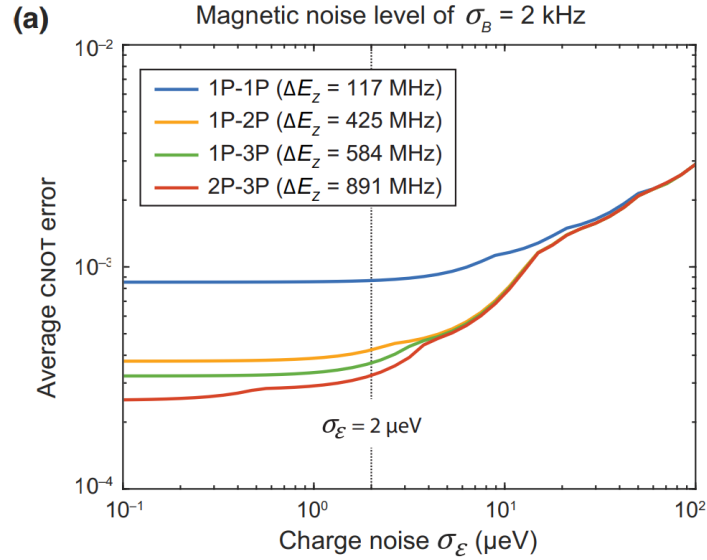


Figure 1.3: CNOT gate error rates with respect to charge noise for different quantum dots configurations. [29]

tuning is somehow intricate as phosphorus fifth electron's Bohr radius is rather small. In Ref. [24], experiments showed a more than three-fold difference in maximal spin relaxation times between single P-donor qubits and multi-donors ones, with $T_1 = 8$ s at $B_0 = 1.25$ T for single-donor and $T_1 = 30$ s at $B_0 = 1.5$ T for multi-donors qubits. Interpolation of those values for an increased distance between the donors in the same dot of 4 to 5 nm (from 1 nm initially), led to $T_1 \approx 45$ s for qubits with two phosphorus atoms and $T_1 \approx 207$ s for qubits with three phosphorus atoms, all at $B_0 = 1.5$ T. A careful configuration of nuclear spins could suppress hyperfine coupling by blocking the flip-flop of electrons⁵ and could increase electron spins relaxation times up to $T_1 \approx 223$ s in three phosphorus dots. Moreover, the electron spin relaxation time of $T_{1e} > 30$ s, the nucleus spin relaxation time is itself of $T_{1n} > 100$ s and their respective best spin dephasing times are of $T_{2e}^* \approx 0.27$ ms and $T_{2n}^* \approx 0.57$ ms from ^{28}Si suppressing background magnetic noise. [5]

Reference [28] affirms that a spin lifetime of 30 s with a coherence time of 0.6 s led to single qubit gate fidelity above 99.94%. This level of fidelity was also stated in Ref. [29] along with a fidelity F value of 99.8% for single shot readouts. The CNOT gate error rate compared to charge noise level and number of donors can be seen in Fig. 1.3. One of their method for increasing the fidelities came from setting the left qubit nuclear spins to the "up" state and the right one to the "down" state, which increased ΔE .

In Ref. [30], another way of making phosphorus dopant qubits was introduced. Electric dipole spin resonance flopping mode qubits originate in coupling electrons' spin with their charge degree of freedom coming from hyperfine interaction switch between $A \approx 117$ MHz in the donor atom and $A = 0$ MHz inside the quantum dot, but out of the donors' orbitals. The spin state is therefore controlled by the electron's movements. This particular type of qubit minimizes the coupling of charge noise with the device.

⁵Flip-flop interactions relate to situations where two nearby ions or electrons exchange their spins via magnetic dipole-dipole interaction.

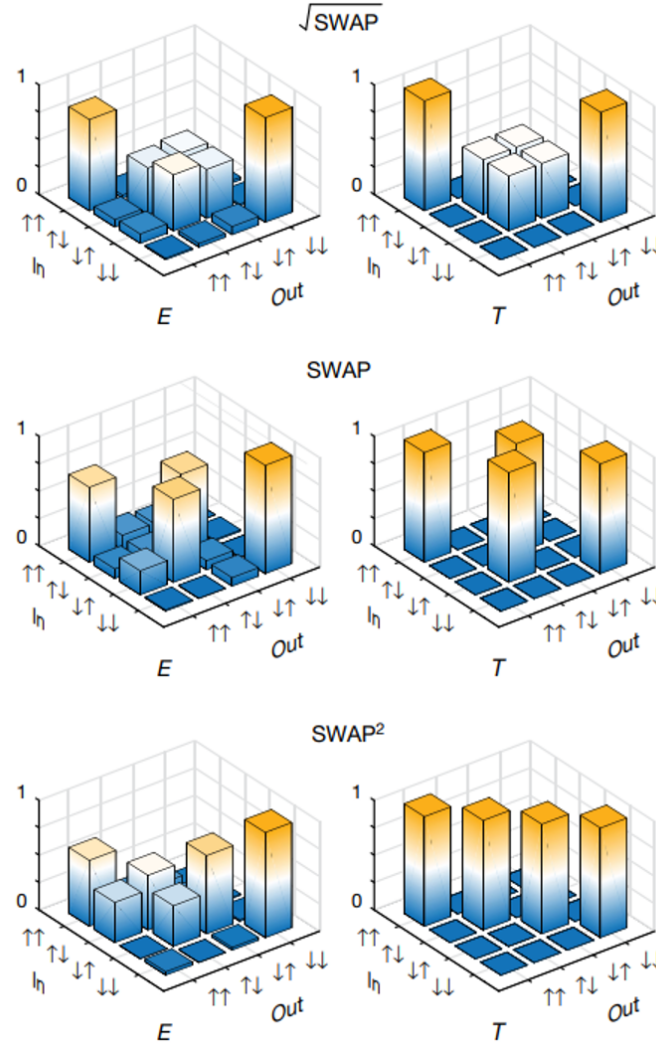


Figure 1.4: Results (E) of the truth tables of the $\sqrt{\text{SWAP}}$, SWAP and SWAP^2 gates compared with the corresponding ideal cases (T). [22]

Advanced manufacturing techniques

Atomic-precision advanced manufacturing is introduced in Ref. [5] as an advanced process for qubits fabrication with phosphorus donors. This process, illustrated in Fig. 1.6, is the one envisaged in this work; the different steps are detailed below. It still presents many challenges for future scaling, as the number of control features would need to be reduced, the whole-planar disposition is not the most optimal and the current ranges for gates interactions is very limited (10 to 40 nm). Other challenges for atomic-precision advanced manufacturing are the need for more precise, reliable and parallelized way of patterning the H-resist, having the ability of growing epitaxial and reaching a greater control over chemicals for increasing phosphorus doping yield. One method found to further improve P-doping yield is by using tip-assisted dissociation, as shown in Fig. 1.7, increasing the dopant integration yield to 100%.

The process of atomic-precision advanced manufacturing presented in Fig. 1.6 goes along the following steps:

1. Engraving of various alignment and guidance features in silicon, deep enough to be perfectly distinguishable after epitaxial Si deposition.

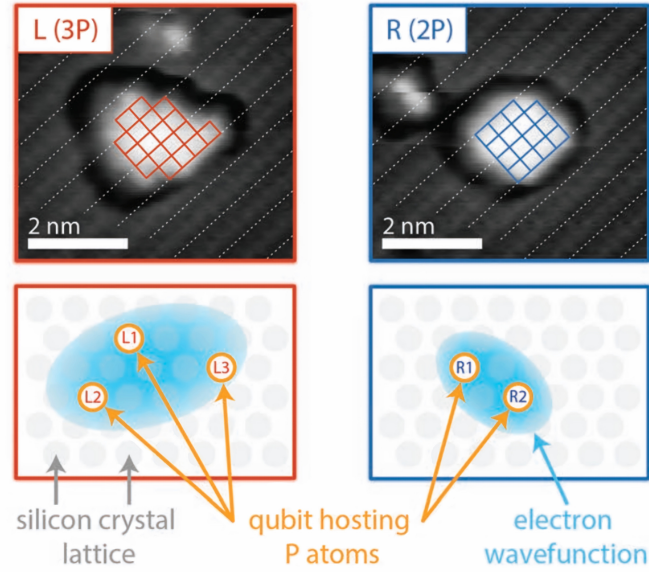


Figure 1.5: Illustration of exchange based spectroscopy with STM images of quantum dots above and phosphorus donors' location deduced from local magnetic field probing below. [28]

2. H-resist mono-atomic layer deposition.
3. H-resist patterning by applying a bias on the STM tip.
4. Phosphine gas exposure and annealing to incorporate phosphorus into the patterned areas.
5. Molecular beam epitaxy encapsulates phosphorus in ~ 20 nm Si.
6. Phosphorus contacting using pre-patterned marks.

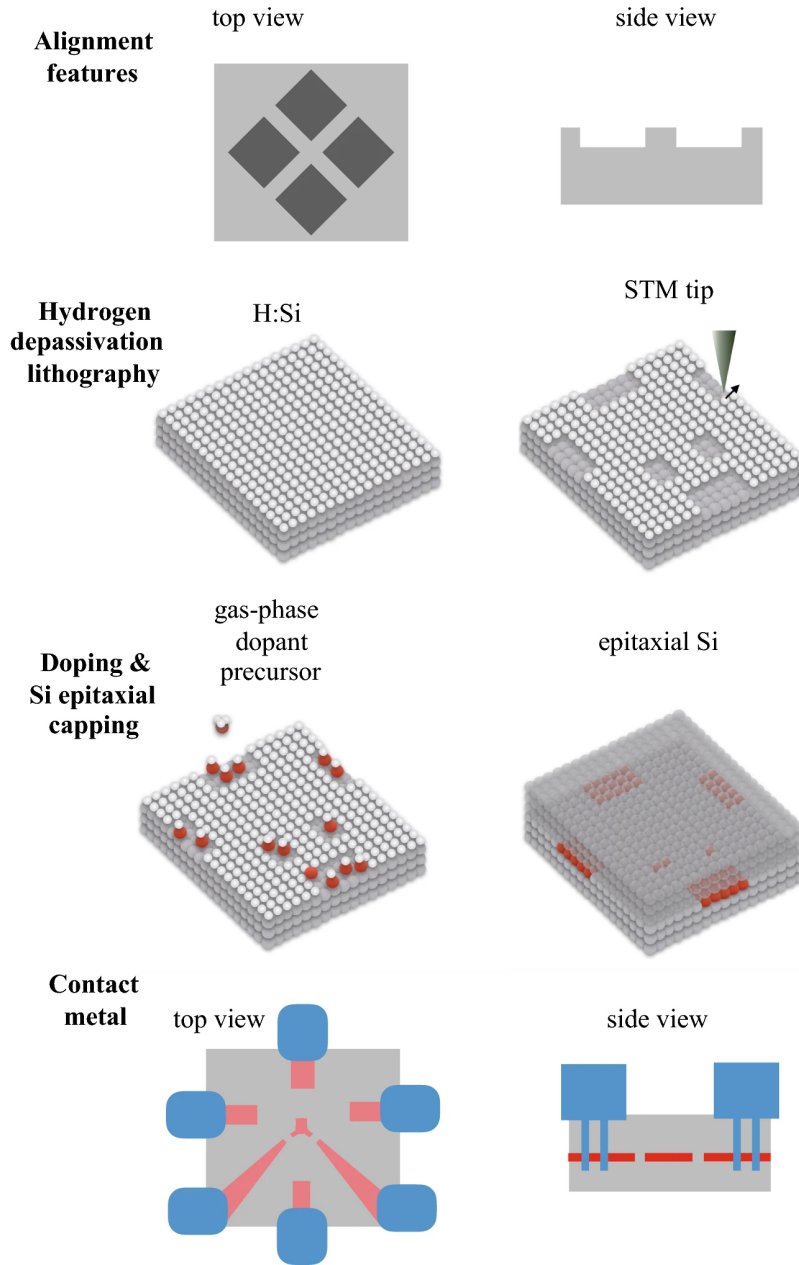


Figure 1.6: Atomic-precision advanced manufacturing process flow. [5]

Furthermore, in Ref. [10] it was demonstrated the ability to remove hydrogen from a monohydride silicon surface using extreme ultraviolet light with a resolution that could reach a few nanometres. This development paves the way for a parallelized, and thus much faster, lithographic step based on H-resist for the fabrication of quantum devices.

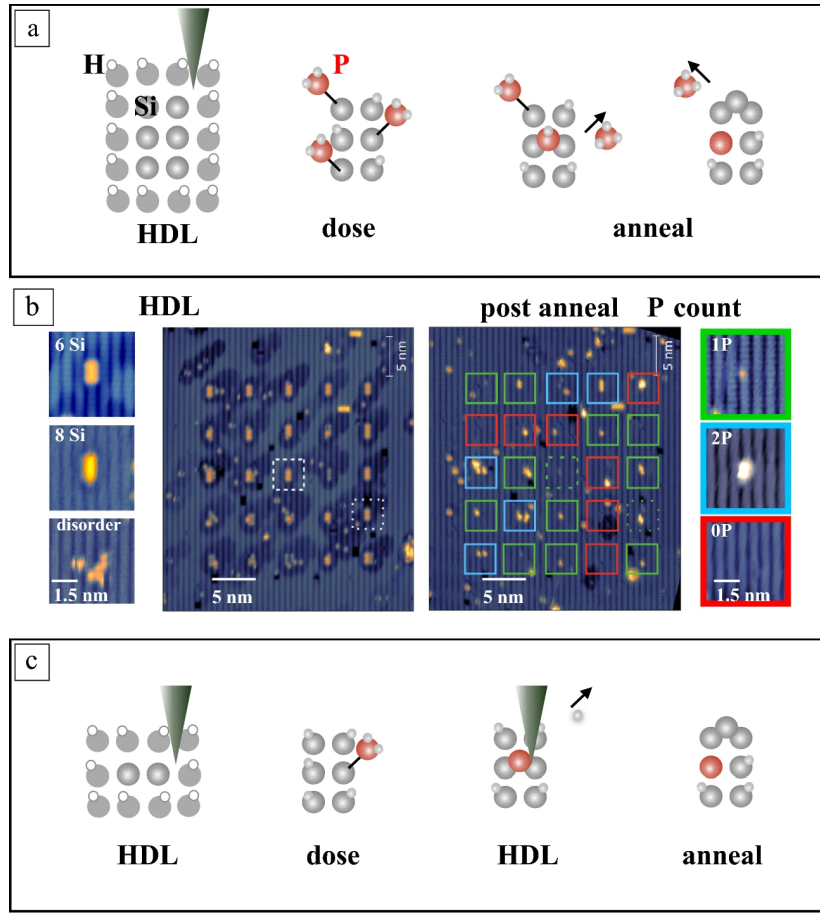


Figure 1.7: Illustration of atomic-precision advanced manufacturing for dopant qubits via a tip-assisted method: hydrogen depassivation lithography (HDL). [5]

1.1.2 Quantum computing with CMOS qubits

The use of equipment linked to CMOS chips fabrication facilitates the widespread adoption among researchers due to their familiarity and accessibility, enabling as well the exploration of cross-domain integration between quantum and classical computing within a single chip through already established methodologies. Most of the CMOS qubits are made with either GaAs/AlGaAs, Si/SiGe, or silicon-on-insulator wafers. [35] The existence of a spin-zero isotope for silicon, ^{28}Si , and its overall weak spin-orbit coupling is enabling isolation of spin states at cryogenic temperatures. [46]

Quantum dots and quantum gates implementations

Quantum dots aim at confining the qubits in a two-dimensional electron gas (2DEG) via electrostatic gates. The prototypical setup is displayed in Fig. 1.8 and some other examples are illustrated in Fig. ??.

Quantum gates, not to be mistaken with the contacting gates discussed above, can be realized in three main approaches. First, electrostatic interaction quantum gates employ the electrostatic interaction between quantum dots. They involve coherent oscillations influenced by electron position, allowing for two-qubit operations. With them various two-qubit operations like SWAP gate have already been achieved. Second, exchange interaction quantum gates employ the overlap of wave functions of electrons, and are particularly attractive for spin qubits. Single- and two-qubit gates are implemented

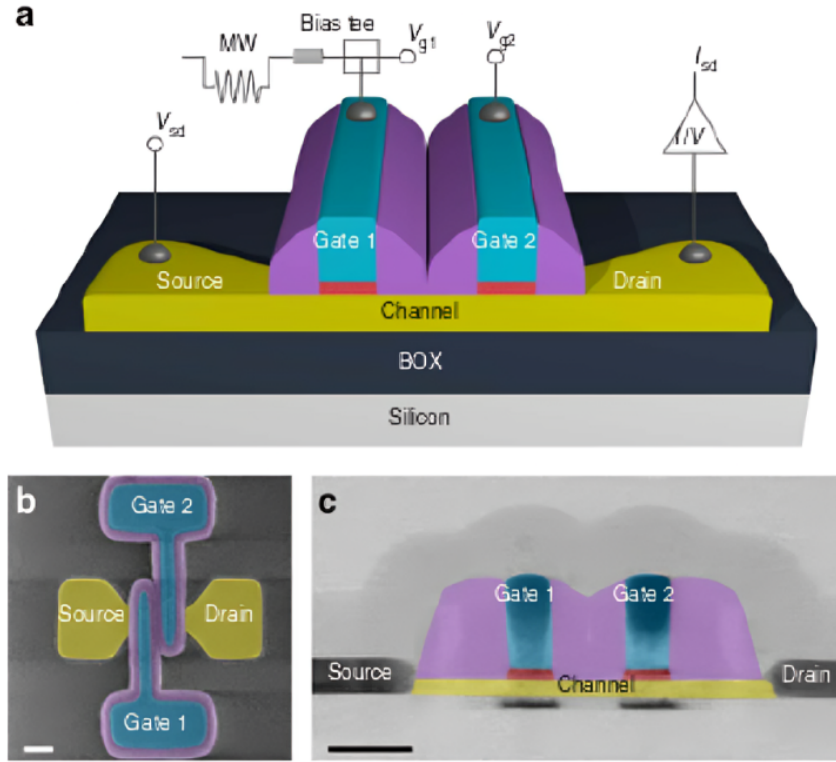


Figure 1.8: CMOS qubits. (a) Schematics of a silicon-on-insulator nanowire field-effect transistor with two gates (1 and 2). Using a bias tee, gate 1 is connected to a low-pass-filtered line, used to apply a static gate voltage V_{g1} , and to a 20 GHz-bandwidth line, used to apply the high-frequency modulation necessary for qubit operation. (b) Colourized top view of the device obtained by scanning electron microscopy just after the fabrication of gates and spacers. Scale bar is 75 nm. (c) Colourized transmission electron microscopy image of the device along a longitudinal cross-sectional plane, highlighting two QDs in series. Scale bar is 50 nm. [35]

using spin qubits with controlled interactions through pulse durations. This technique is useful in the case of reconfigurable and scalable quantum computation and has demonstrated gates like CNOT, CZ, and SWAP gates. Finally, quantum gates could involve an array of coupled quantum dots with some serving as charge injectors. Coupled QDs give rise to bonding and anti-bonding continuum states when they are aggregated in arrays and quantum operations take place between neighbouring arrays.

Cryogenic CMOS

Quantum computers need classical systems managing setup, gates and readout signals sent to and from the qubits. These controlling chips often reside outside the dilution refrigerators requiring numerous interconnects going in and out of it. In order to ease this issue, the team of Vandersypen [52] developed a CMOS cryogenic controller that can operate down to 3 K, underlining the possibility to reduce the operating temperature even lower. Being able to send control signals from the inside of the refrigerators and that with low power consumption and a high signal quality was a big step towards lowering interconnect complexity. It further implies that cryogenic CMOS technology reduces the thermal noise generated by the control circuit leading to higher fidelities

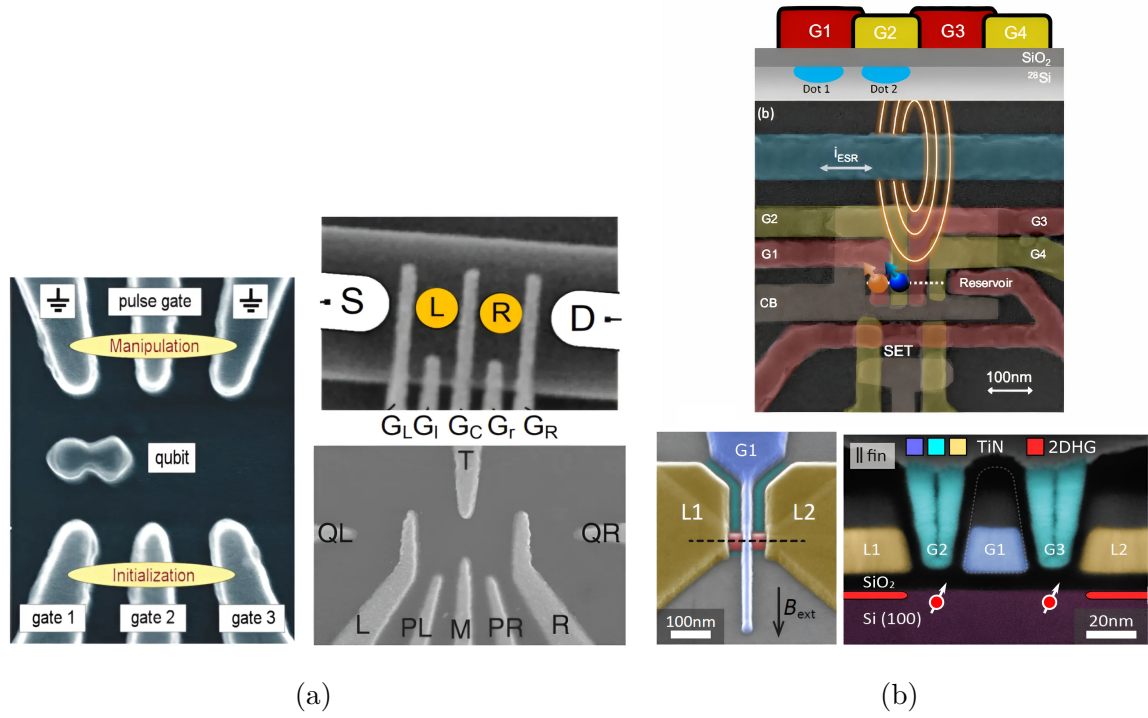


Figure 1.9: CMOS quantum dots with labelled gates. (a) Stadium-type quantum dots. (b) Top-gate defined quantum dots with colourized gates and qubits locations indicated. [19]

for the qubits. Having the possibility of locating CMOS control circuits at the same place as of a CMOS quantum processor introduces the opportunity of integrating both in a single package.

Qubit controls integration and scaling properties

As mentioned above, having CMOS control chips able to operate at cryogenic temperatures, from inside the dilution refrigerator, opens the way of integrating both classical chips and CMOS quantum processors together. Having all components (controls and qubits) in a single chip leads to a more compact device, much less constrained by latency. This latency is of the utmost importance, as the reduced time for communications between the in- and out-sides of the dilution refrigerator facilitates more operations onto the qubits, before they lose their quantum information by decoherence. A reduced interconnections density that causes much less power leakage is thus reducing the global consumed power and offers a better synchronization between the qubits and their respective control signals. However, having the control circuits closer to the qubits introduces as well a risk of coupling between them that may negatively impact signals quality and coherence times if not properly designed. The very mature CMOS manufacturing techniques imply that quantum chips will likely use CMOS qubits compatible with established large scale fabrication methods and equipment. Such quantum processors will be able to scale much faster and have a much easier to make quantum-classical co-integrated architecture. [19]

Partial swapping for universal gate

One of the latest advancements in quantum computing using CMOS compatible quantum processors comes from the team of Borselli [50], where the authors achieved a quantum analogue of the universal classical Fredkin gate with an array of six $^{28}\text{Si}/\text{SiGe}$ quantum dots. The array is shown in Fig. 1.10; the figure also shows possible extensions to two-dimensional arrays. Partial swap is a unitary superposition of swapping and not swapping spins j and k of an n -spin array, $U_{jk}(\theta) = \cos(\frac{\theta}{2})\text{I} + i \sin(\frac{\theta}{2})\text{SWAP}_{jk}$, with I the identity matrix and SWAP_{jk} the matrix associated with the SWAP operation on qubits j and k .

Partial swap allows operation of decoherence-free subsystems (DFS) as it avoids global dephasing caused by magnetic field fluctuations in quantum computers based on single-spin qubits. A fidelity of $96.3\% \pm 0.7\%$ for the application of CNOT gates and a fidelity of $99.3\% \pm 0.5\%$ for SWAP gates was measured. The current limiting principle for scalable fault tolerance is the hyperfine interaction between the qubits and ^{29}Si and ^{73}Ge atoms.

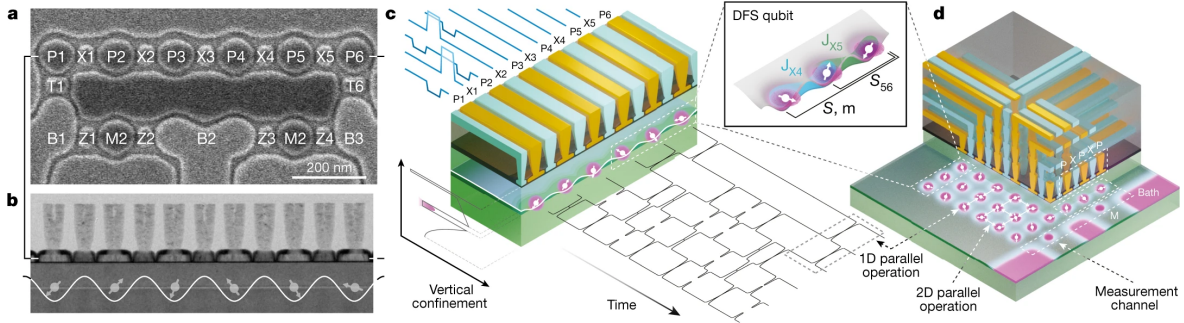


Figure 1.10: (a) Top-view scanning electron micrograph of the etched TiN single metal layer, defining the device's plunger (P), exchange (X), tunnel (T), bath (B), barrier (Z) and measure-dot (M) electrode gates. (b) Cross-sectional transmission electron micrograph of gate and TiN via electrodes. Electrons are vertically confined by the Si/SiGe heterostructure boundaries and laterally confined by the induced electrostatic potential from the device gates. $\text{Al}_2\text{O}_3/\text{HfO}_2$ dielectrics appear as a black boundary around the electrode gates. (c) Qubit states are manipulated using sequences of voltage pulses, that actuate nearest-neighbour exchange interactions. Entangling operations are performed on the two-qubit encoded subspace with sequences of partial swaps as shown to the right. (d) Schematic of a potential future device that enables scaling in the lateral dimension. [50]

1.1.3 Two-qubit operations

To enact rotational transformations on single qubits, the application of alternating currents at the resonance frequency of the qubit is imperative, typically achieved under the influence of a magnetic field inducing a Zeeman energy splitting. In the execution of controlled rotations within two-qubit gates it is essential for both qubits to be in close proximity. That close proximity is necessary *inter alia* to allow exchange interactions as well as to have the electrons' electrostatic potentials to overlap significantly for capacitive coupling. Subsequently, specific single-qubit operations are applied to each qubit based on the desired outcome, then capacitive coupling or exchange interaction is engaged via a voltage pulse gating the qubits. The duration of the said pulse applied to

one of the qubits' determines the magnitude of controlled rotation. Fig. 1.11 illustrates a sequence of single- and two-qubit operations implementing a CNOT gate. Such interactions commonly engage with the singlet-triplet states of qubits, as having both in the same dot logically increases their capacitive coupling. [48]

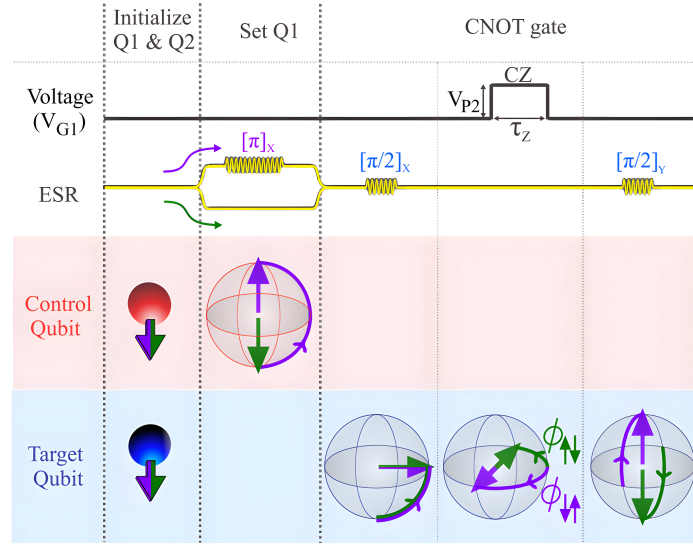


Figure 1.11: Pulsing protocol for CNOT operations. When the coupling is on, the qubits make in-plane rotations with a frequency determined by the exchange coupling and a direction that depend on the spin component of the other qubit. [48]

However, one might instead want to be able to apply gates on two distant qubits. This might be due to spatial constraints limiting the number of qubits in close proximity, as each qubit is often linked to multiple gates for read-outs, operations, *etc.* In such cases, other artefacts are required to induce some coupling between those qubits. A silicon quantum processor with robust long-distance qubit couplings was introduced by the team of Morello, based on the flip-flop qubit. [45] Two-qubit gates use the second-order electric dipole-dipole interaction, enabling selective coupling beyond the nearest-neighbour donors, nearly to one micron, while microwave resonators can extend the entanglement to macroscopic distances (up to 1 cm), as shown in Fig. 1.12. This methodology highlights the key role of quantum resonators for CMOS quantum computers.

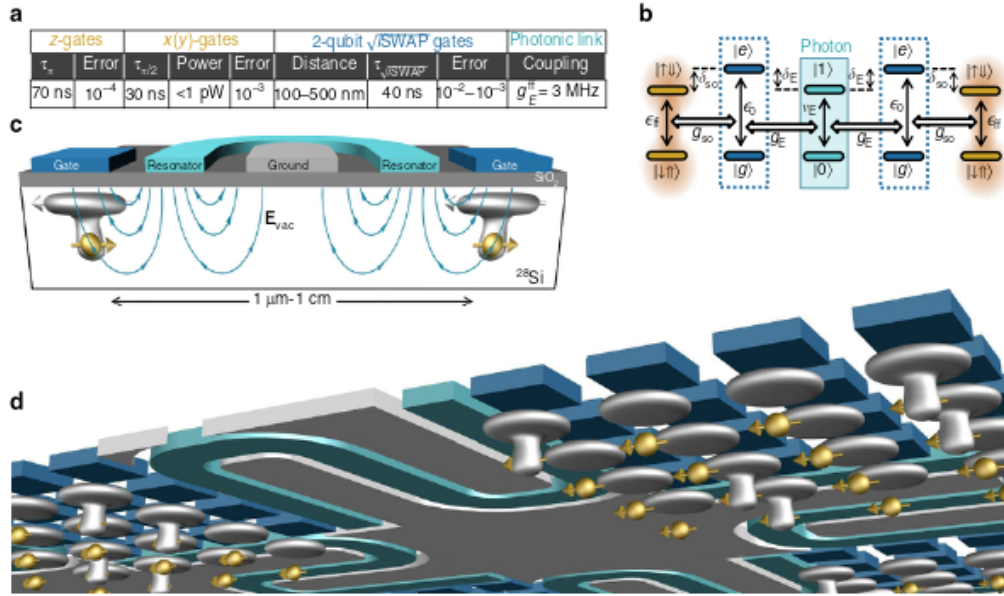


Figure 1.12: Silicon-based quantum processor. (a) Figures of merit for various gates assuming realistic noise sources. (b) Energy level diagram for distant flip-flop qubit coupling via a microwave resonator showing photon number states and off-resonant charge states. (c) Schematics for coupling qubits via a photonic link. Distant donors, placed close to the resonator centre line and biased to their ionization point, are subject to the vacuum electric field E_{vac} of a common microwave resonator. (d) Schematics of a large-scale quantum processor based on ^{31}P donors embedded in a quantum-grade Si layer, and manipulated through electric dipoles. Idle qubits have electrons at the SiO_2/Si interface, leaving the ^{31}P nucleus in the coherent ionized state. Electrons are displaced toward the donor for quantum operations. The panel illustrates a coupled QD architecture where an array of qubits is locally coupled via the electric dipole, and a cluster is further coupled to another array through interaction with a common microwave resonator. The drawing is not to scale, while control lines and readout devices are not shown. [45]

Chapter 2

Titanium nitride components for quantum computing

Titanium nitride or TiN is a ceramic material arranged in a face-centred cubic crystal structure resulting from a mixed bonding, dominated by an ionic bond between Ti^{3+} and N^{3-} as follows: $\text{Ti} \equiv \text{N}$, and a strong covalent bond. [9] Representations of its crystal structure and electronic localized function are displayed in Fig. 2.1. It has a hardness of ~ 2400 Hv, a coefficient of elasticity of 251 GPa, it melts at 2950°C and does not oxidise at temperatures below 800°C . [11, 25] Additionally, it is stable and inert; TiN does not react with most acids and is insoluble in alkalis. [1, 25] It also shows itself a bio-compatible material. [25] But the property that will interest us the most is its superconductive behaviour at temperatures below its critical temperature, which varies between $T_C = 3.0$ and 5.6 K depending on the thickness of the TiN layer. [41]

Titanium nitride properties depend on its composition, ranging from under-stoichiometric $\text{TiN}_{1.0-\chi}$ to stoichiometric $\text{TiN}_{1.0}$. Its nitrogen composition induces significant changes on its hardness, oxidation speed, colour and other properties. [31] Other possible stoichiometric stable compounds are Ti_6N_5 , Ti_4N_3 , Ti_3N_2 and Ti_2N at atmospheric pressure and TiN_2 at 60 GPa. Note that Ti_2N has a particularly high hardness located between 2651 and 2957 Hv. [56]

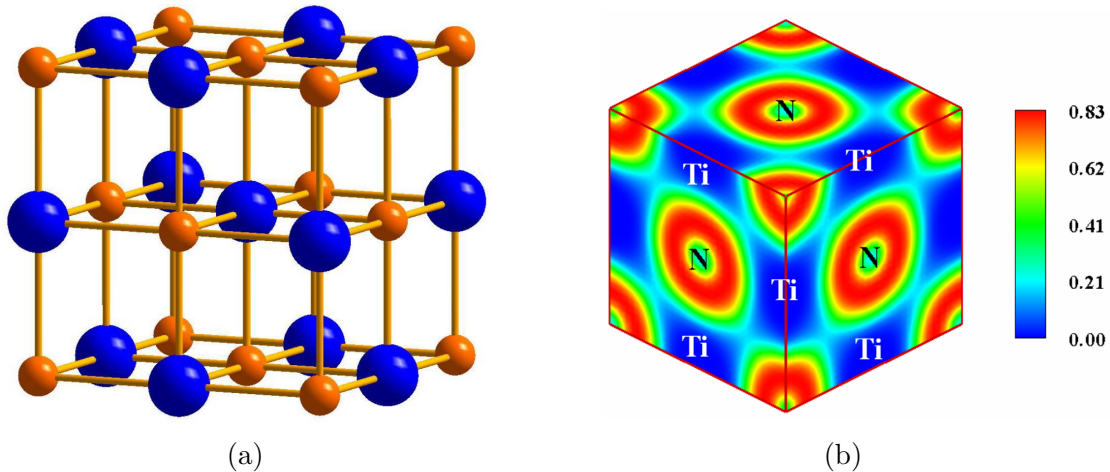


Figure 2.1: (a) The unit cell model of TiN. The yellow spheres represent N atoms, while the blue spheres represent Ti atoms. (b) The electronic localized function of TiN with the colour-scale representing the probability of the presence of an electron relative to the position occupied by a reference electron of the same spin. [9]

TiN is used in many fields, mostly as a coating material. Its main applications are in the manufacturing industry for its hardness and ability to extend the lifespan of

objects, as well as its lubricating properties. It is used to make or coat cutting tools (*e.g.* drill bits), punching and stamping tools, to lubricate and harden moulds and for sliding pieces. [25] In the medical field its bio-compatibility and resistance to oxidation allows it to be used in implants, dental devices, surgery tools and other instruments, and in bio-electronics for its resistance to corrosion by body fluids. In the aerospace sector, it extends the lifespan of different satellite components and is also part of some of their electronics. [25] In jewellery and aesthetics, it also coats some objects to obtain a gold-like colour at a cheaper price and to prolong their lifetime. [25] Finally, and as it will be discussed in the following section, titanium nitride has very interesting uses for the quantum computing sector and other nanoelectronics applications.

The deposition techniques used to coat titanium nitride are physical vapour deposition (PVD) and chemical vapour deposition (CVD). For nanofabrication purposes, an atomic layer deposition (ALD) technique is often used. In CVD the most common titanium precursors are tetrakis-(dimethylamido)titanium (TDMAT) and tetrakis-(diethylamido)titanium (TDEAT) with TiCl_4 also notable. The nitrogen comes from N_2 or NH_3 gases. The CVD process occurs at temperatures between 350 and 400 °C. [11] For ALD, the typical titanium precursor is TDMAT and the typical nitrogen source can, as for CVD, be either N_2 or NH_3 . The process can be thermal or plasma enhanced. The growth rates can reach 0.06 nm/cycle for a thermal ammonia based process with a resistivity of about 100 $\mu\Omega/\text{cm}$ or 0.08 nm/cycle with a resistivity of about 180 $\mu\Omega/\text{cm}$ for an optimized plasma enhanced NH_3 process. [37]

2.1 State of the art of TiN for quantum computing

Quantum computing is a rapidly expanding sector where new challenges appear all the time and with plenty of room for further research and optimization. Those challenges span many fields, from algorithms to materials science, going through new fabrication techniques. The need to find new materials which increase coherence time, suppress noise or fasten communication times is critical in order to scale up the systems and reach a sufficient number of logical qubits to run quantum algorithms. One of the most promising materials, especially for Josephson junctions qubits, but not limited to those, is titanium nitride. Indeed, its extreme resistance to many ageing effects, its superconductivity, its CMOS compatibility, *etc.* make it a very judicious choice for many applications.

Firstly, titanium nitride can be used for ultrafast lasers with pulses in the picosecond range. [54] In fact, quantum dots made from TiN exhibit great saturable absorber behaviour (*i.e.* with light absorption decreasing as its intensity increases). This property allows making ultrafast fibre lasers with pulses as short as 1.45 ps at a frequency of 1 GHz. [54] Figure 2.2 shows characteristics of such pulses. Ultrafast lasers can be very useful in the quantum computation domain in general, as timings are extremely critical to finish operations upon a qubit before it loses its quantum coherence. Therefore, faster lasers leading to greater communication speeds can make all the difference between the moment when the qubit still has all its information and the moment it loses it.

Secondly, TiN has already found many uses in Josephson junctions (JJs) and their related quantum bits. As a superconductor, its excellent stability makes it a perfect material. While aluminium JJs deteriorate a lot with time, titanium nitride ages quite

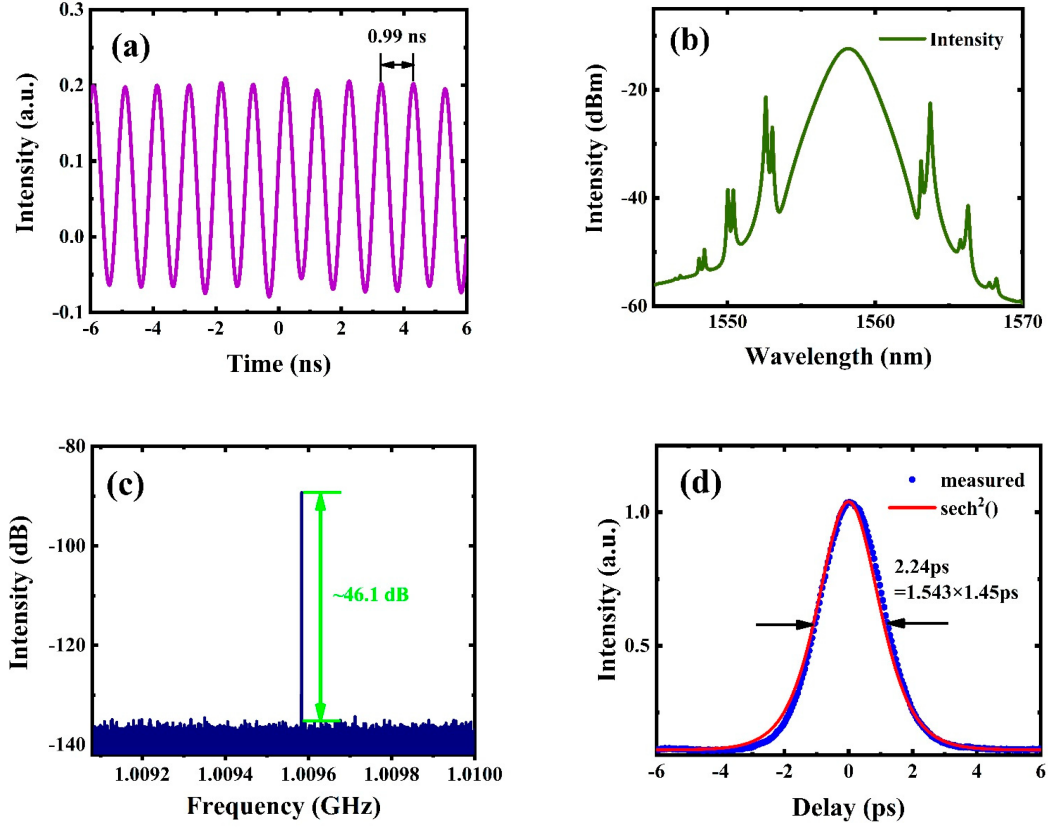


Figure 2.2: Characteristic diagrams of output pulses of TiN quantum dots saturable absorber fibre laser. (a) Pulse trains. (b) Spectrum. (c) RF spectrum. (d) Autocorrelation curve. [54]

well. Even if its thickness is as low as 3 nm it only has a $\sim 1\%$ decrease in its resonance frequency. [2] At $t_{\text{TiN}} = 3$ nm it still can behave as a superconductor with a critical temperature $T_C = 3$ K as shown in Fig. 2.3. The chemical stability and ability to form very clean interfaces with sapphire allowed the creation of JJs with reduced dielectric losses. With $t_{\text{TiN}} = 100$ nm deposited by magnetron sputtering onto *c*-plane sapphire and then etched by a wet etch technique using the SC1 solution¹ from the Radio Corporation of America standard cleaning, a qubit coherence time up to 300 μs was reached, and its associated quality factor is $Q \simeq 8 \times 10^6$. [14] The main limitation of this implementation is its interface dielectric loss around the JJ.

Figure 2.4a shows a nanobridge Josephson junction made with TiN on a silicon substrate, which was further used in Ref. [16] to make the nanometer-scale superconducting quantum interference device (nanoSQUID), highlighted in Fig. 2.4b. For that application, TiN was employed in particular for its large coherence length of ~ 105 nm at 4.2 K and its critical temperature of $T_C = 5$ K, which is perfectly suited for the nanobridge cooled down at 4.2 K. Given its Si compatibility, low microwave losses and its tunable optical properties, this TiN application was based on a Si substrate. Moreover, TiN easy patterning also played a role to allow simpler creation of Josephson junctions of various thicknesses with low kinetic inductances. [16] It is also noteworthy to know that TiN was previously used for TiN/AlN/TiN tunnel JJs, but their low

¹SC1 is used to remove organic contaminants from the surface of the wafers and involves a solution of ammonium hydroxide and hydrogen peroxide.

critical current densities and large subgap leakage currents were a big disadvantage. [34]

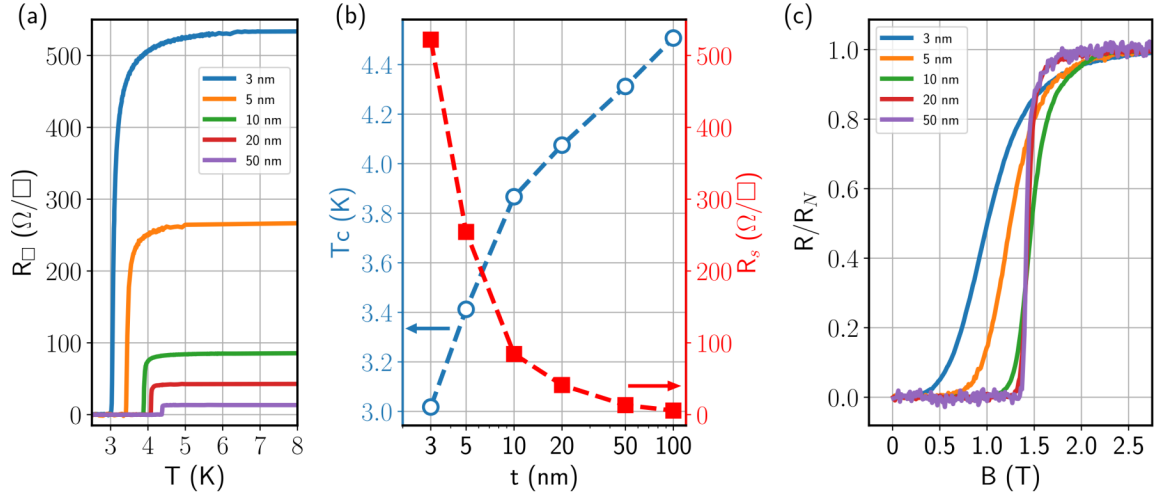


Figure 2.3: Superconducting transitions in TiN thin films. (a) Sheet resistance R_s (or $R_{\square}$) versus temperature T for TiN films of different thicknesses t . (b) T_C versus t , with blue open circles in left axis, and R_s versus t in red filled squares in right axis. (c) Normalized resistance versus perpendicular magnetic field B measured at $T = 2.0$ K for the same TiN film devices as presented in (a). Width of the superconducting to normal state transition increases with decreasing film thickness. [2]

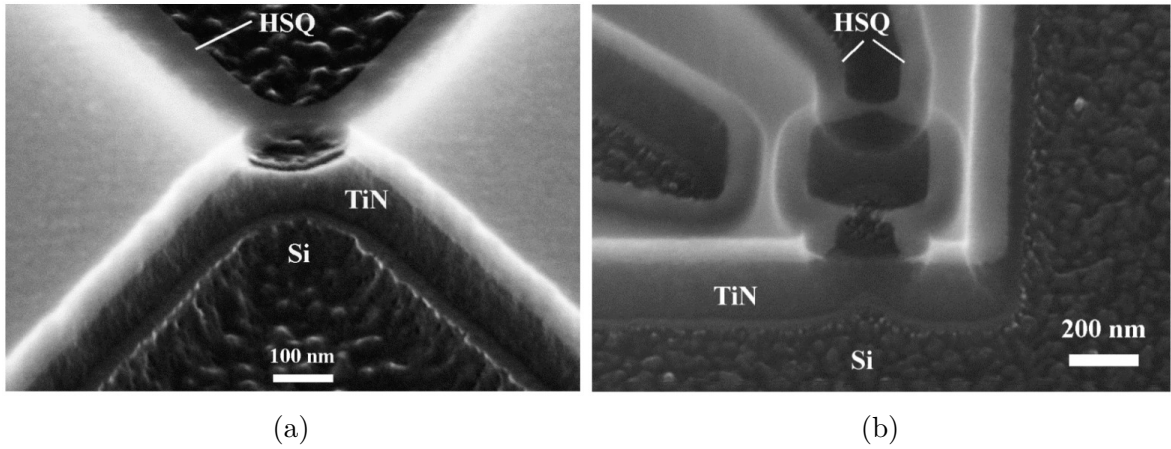


Figure 2.4: High-resolution SEM images of (a) a TiN nanobridge Josephson junction (JJ). (b) a TiN nanometer-scale superconducting quantum interference device (nanoSQUID). Both images were recorded at a 45° sample tilt angle. [16]

Thirdly, for transmon qubits, TiN was used in Ref. [8] to make interdigitated shunting capacitors, enabling enhanced relaxation and dephasing times. Indeed, their respective values are of $T_1 \approx T_2^* \approx 60 \mu\text{s}$, which were 6 times greater than what was reached using Al. Nevertheless, the main limitations of those TiN-based qubits are similar from those for Al and are its surface losses, partly due to residual radiations and partly from bulk dielectric losses. The device made in Ref. [8] and relaxation times in comparison with Al are shown in Fig. 2.5.

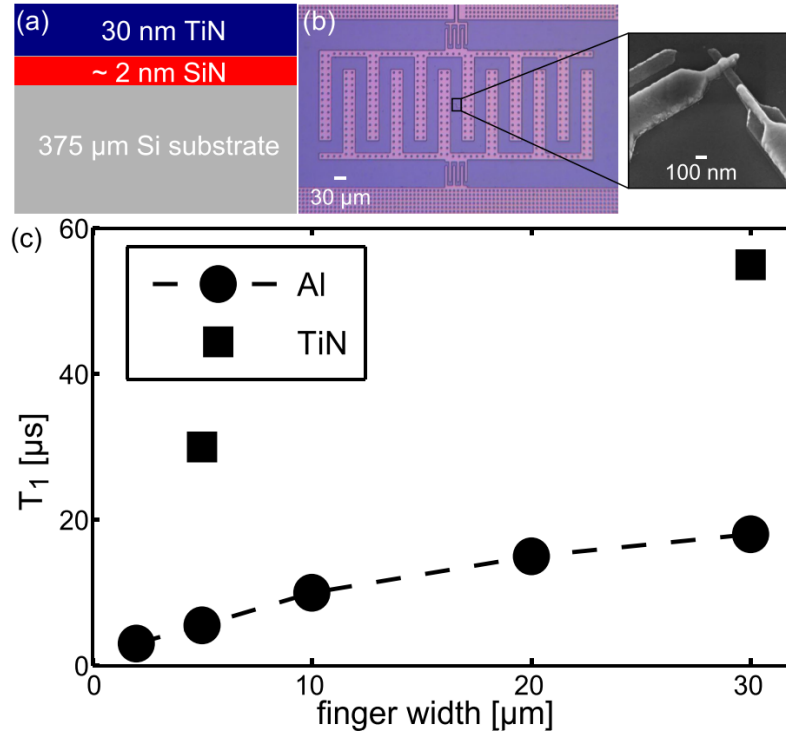


Figure 2.5: (a) A wafer cut showing that a thin seed layer of SiN was introduced on top of silicon. (b) Micrograph of the transmon, and zoom-in of the Josephson junction. (c) T_1 versus finger width dimension, keeping the finger width and separation constant for an interdigitated capacitor of total capacitance $C = 100$ to 150 fF. Coherence times of qubits using aluminium (circles) and TiN (squares), which showed a dramatic improvement. [8]

Fourthly, TiN has found a purpose as a diffusion barrier. In Ref. [17] almost stoichiometric titanium nitride (because it had a little excess nitrogen) was deposited between superconducting indium and aluminium to prevent diffusion between one another in the making of superconducting interconnects compatible with superconducting qubit technology. In addition to that, its critical temperature of $T_{C,TiN} = 5.6$ K in this case did not affect the overall transition temperature needed to have a fully superconducting interconnect as $T_{C,TiN} > T_{C,In} > T_{C,Al} = 1.1$ K.²

Fifthly, as a resonator and more specifically microwave resonator, TiN already found many uses due to its very low dielectric losses, with metal-air interface evaluated as 10 times less lossy than Al in Ref. [36]. For that purpose, TiN CMOS compatibility, as studied in Ref. [2], allows such resonators to be used in many quantum circuits. In Ref. [18] a TiN/sapphire superconducting coplanar waveguide resonator was made using highly crystalline, epitaxial TiN, as shown in Fig. 2.6. The authors reached a critical temperature of $T_C = 3.8$ K, tested different wet- and dry-etching techniques and had their best results with dry-etching giving a quality factor $Q = 3.3 \times 10^6$ in the single photon regime. The tests have also proven TiN highly practical for future applications in high coherence superconducting quantum circuits.

²Note that $T_{C,In} = 3.4$ K.

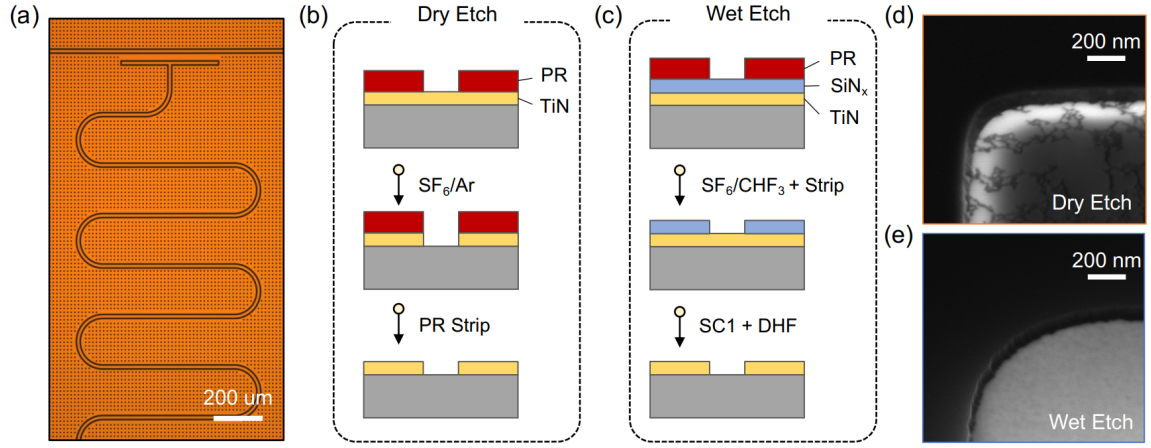


Figure 2.6: (a) The optical image of a resonator. Process flows of (b) dry- and (c) wet-etch techniques using patterned photoresists (PR). (d,e) SEM images of the edge profiles of the fabricated devices. The dry-etch technique yields sharper edges, while there are signs of substrate surface damages or contamination. The wet-etch technique (with diluted aqueous hydrofluoric acid [DHF]) yields clean substrate surfaces, while the edges are slightly curvy. [18]

2.2 TiN superconducting resonators

One out of many challenges of quantum computing is the need for quantum bits to be able to communicate their states, interact and couple over long distances. One solution is to use superconducting resonators coupled to both qubits; such resonators make use of particularly high impedances compared to standard microwave waveguides to increase coupling between the dots and the resonator. [51]

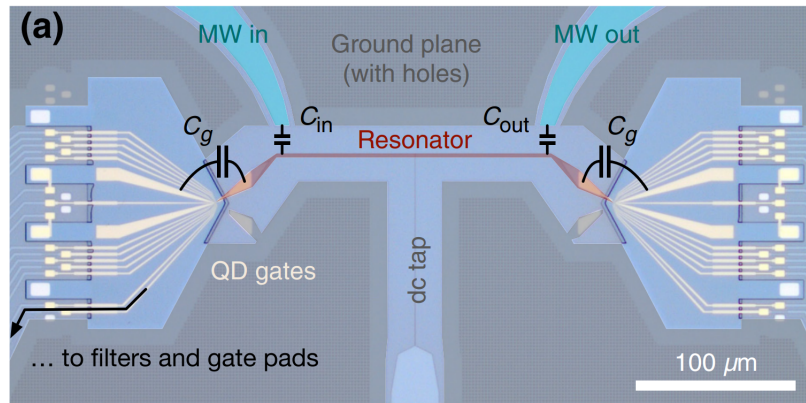


Figure 2.7: (a) Optical image with false-colour shading showing a superconducting high impedance nanowire resonator. The resonator is probed in transmission through the “in” and “out” ports, with coupling capacitances C_{in} and C_{out} . At each end, an extra capacitance $C_g \ll \{C_{in}, C_{out}\}$ causes the microwave energy to escape from the resonator, primarily through the gate fanout lines. [21]

In Ref. [21], a NbTiN high-impedance, high-kinetic inductance, superconducting resonator, in the form of a straight line, is used for coupling two double quantum dots. The resonator is connected to a DC bias at its centre (Fig. 2.7).

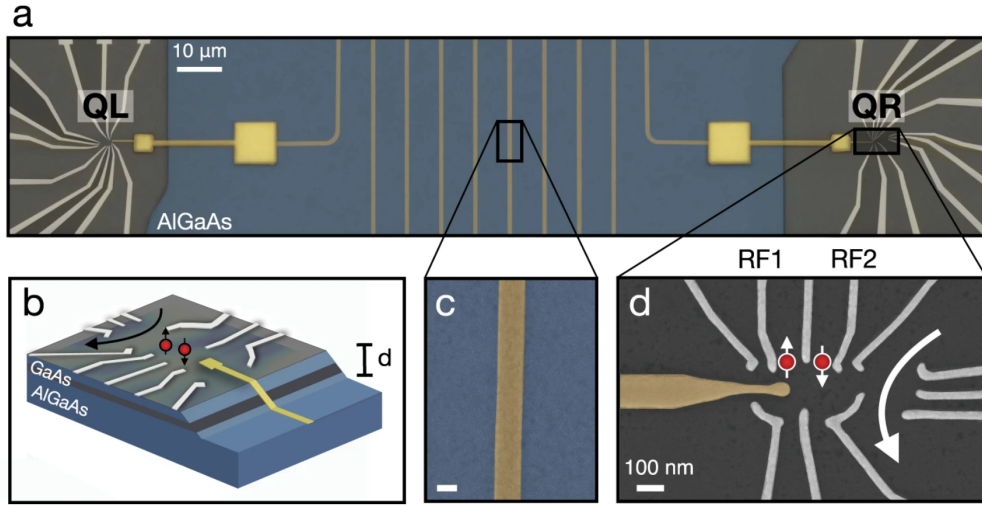


Figure 2.8: (a) False-coloured scanning electron microscope (SEM) image of two double quantum dots (DQDs) that are placed at each end of a superconducting resonator made from thin film NbN. The resonator is meandering across the sample. (b) Illustration of the resonator climbing the edge of the etched region with a height of $d \sim 90$ nm. (c) SEM image of a part of the resonator. The scale is 100 nm. (d) SEM image showing the right DQD. [6]

In Ref. [6], a high-impedance, high-kinetic inductance superconductor resonator is used for coupling two double quantum dots. It is a meandering thin NbN wire which ends with a low pass filter on each side, themselves ending with a small waveguide coupled capacitively to the dots' electric field (Fig. 2.8).

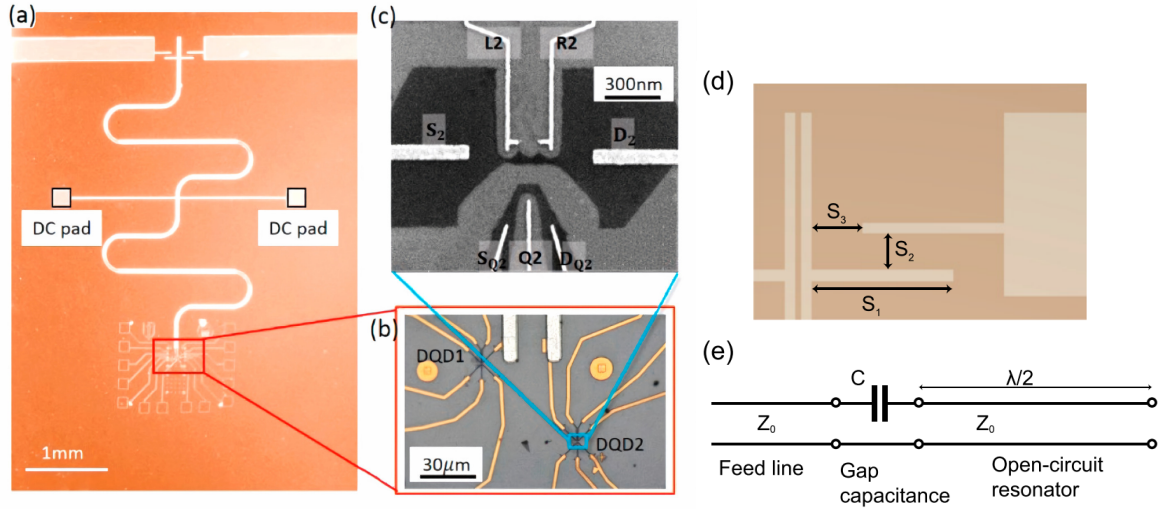


Figure 2.9: (a) Schematics and micrograph of the hybrid device. The half-wavelength reflection-line resonator is connected to the two DQDs at one end of its two strip lines, while the other end is used for microwave input and output. (b) The two DQDs are separated about $60 \mu\text{m}$ and are each coupled to one strip line respectively through their source leads. (c) Microscopic view of a double quantum dot with its contacts labelled. [13] (d) Specification of the finger capacitors. (e) Equivalent circuit model of the coupled microstrip reflection line resonator with a gap. [57]

In Ref. [13], a resonator introduced in Ref. [57] is used for double quantum dots distant coupling. It consists of a pair of coupled microstrip lines forming a half-

wavelength open-circuit resonator. The resonator has no ground plane and was further coupled to quantum dots, via symmetric differential excitation, which is immune to common-mode noise and has the potential for large coupling strength (Fig. 2.9).

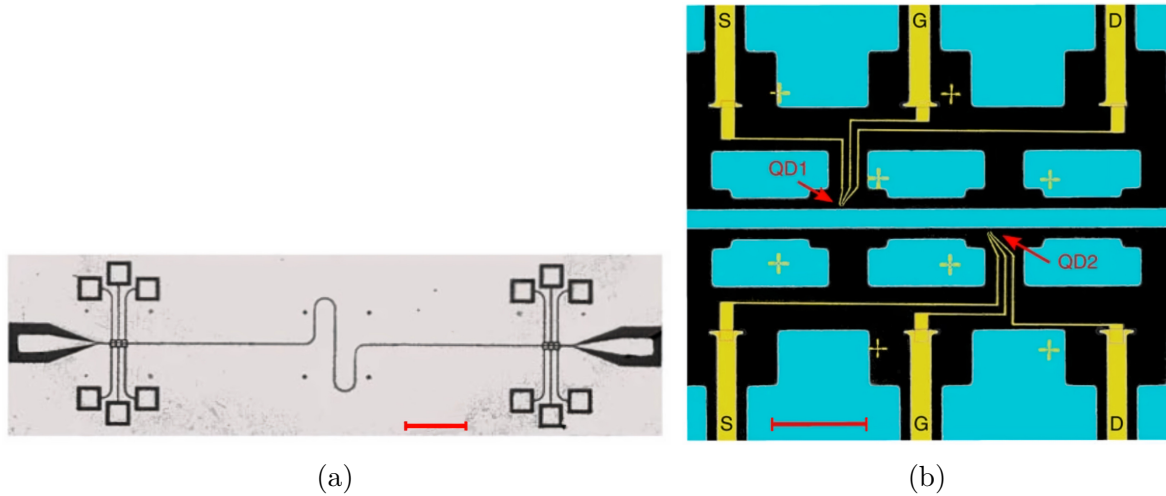


Figure 2.10: (a) Optical micrograph of an Al microwave resonator in coplanar waveguide geometry. Four sets of three DC lines allow contacting up to four quantum dots inside the cavity. The red bar is 1 mm. (b) False-colours optical micrograph showing the two quantum dots structures inside the microwave cavity. Aluminium elements of the resonator are represented in blue (transmission line and ground plane). The red bar is 50 μm . [12]

In Ref. [12], a resonator (Fig. 2.10), is used to allow distant interactions between multiple quantum dots.

Considering the technologies involved and possible implementation in UCLouvain technological ecosystem, the following procedure is designed to test prototypical geometries of the resonator and, if conclusive, to be further implemented in the final device:

1. Wafer marking for delimiting dies, electron beam deposition step and vias definition.
2. Titanium nitride thin film deposition by means of atomic layer deposition.
3. Titanium nitride dry etching.
4. Wafer dicing, including dies of 0.5 cm by 1 cm and 0.5 cm by 1 cm for scanning tunnelling microscopy setup.
5. Design electrodes by electron beam lithography.
6. Electron-beam resist development.
7. Metal deposition for lift-off process.
8. Electron-beam resist removal.

2.3 TiN via holes

In addition to the resonators allowing horizontal (*i.e.* intrachip), long distance qubit-to-qubit interactions, vertical connections are to be developed for further scaling up the number of qubits in a single quantum computer by using multiple interconnected and stacked chips. This implies the need for via holes (vias) as a mean to vertically connect multiple chips together. Chips stacking brings opportunities of increasing the qubits number while improving the quantum circuit architecture, crucial in the current quantum computer setups inside dilution refrigerators. In this respect, metallization processed also need to be redesigned for using superconducting materials. [55] Furthermore, vias can be used for controlling parasitic microwave modes frequencies which, once again, increases coherence times.

A via is a small aperture drilled or etched through a substrate, such as a printed circuit board (PCB) or a semiconductor wafer (Fig. 2.11). Vias, coated with some conducting material, serve as electrical connectors between different layers or regions within the substrate. Typically of cylindrical shapes, via holes are fabricated during the manufacturing process by drilling or etching through the substrate material. They come in different types, including through-hole, blind, and buried vias, each serving specific connection needs within electronic circuits.

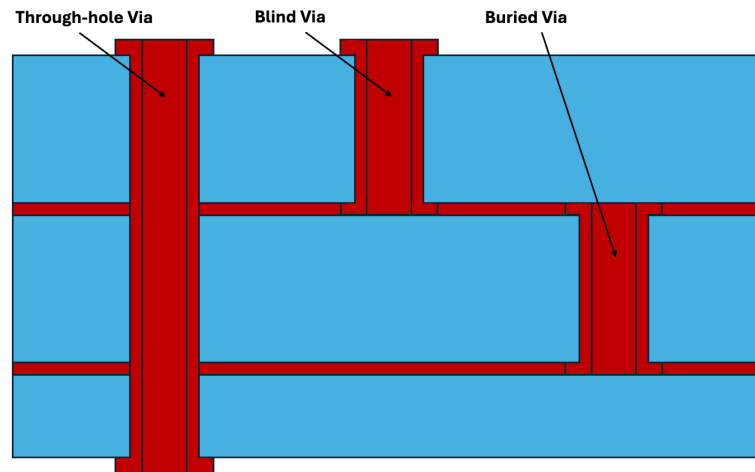


Figure 2.11: Illustration of the different via types.

In Ref. [55], the authors introduced a chip stacking concept based on a qubit chip, a superconducting multi-chip module, and an interposer chip. It is aimed at facilitating vertical signal delivery to a 2D array of qubits while maintaining qubit coherence. For that purpose, vias, particularly through-silicon vias, play a crucial role in connecting these chips. The interposer chip contains through-silicon vias lined with superconducting TiN for facilitating low-resistance electrical paths between the qubit chip and superconducting multi-chip module without resistive loss. The integration of high aspect ratio superconducting through-silicon vias with superconducting qubits is highlighted, enabling compact vias of $10\ \mu\text{m} \times 20\ \mu\text{m}$ through a $200\ \mu\text{m}$ thick chip. As the pitch is 1 via per $100\ \mu\text{m}$, it allows for up to 10,000 through-silicon via interconnects on a $10\ \text{mm} \times 10\ \text{mm}$ chip, ensuring consistent ground connection. The compatibility of the process with high-performance qubits was demonstrated by achieving $T_1 \approx 20\ \mu\text{s}$ for qubits separately fabricated on a qubit chip bonded to the interposer, as well as for qubits fabricated directly on the interposer chip surface.

Reference [20] details the fabrication and characterization of qubit-compatible microwave resonators on silicon wafers with through-silicon vias stitching the front and back ground planes. The through-silicon vias structure involves a main electrode layer, a hollow via with metallized walls, a metal membrane covering the via, and metallization on the back side of the wafer. Fabrication begins with sputtering a titanium nitride and tantalum bilayer onto high-resistivity silicon, followed by patterning and deposition processes to create the vias and membranes. In this article, the aspect ratio is around eight, with a nominal diameter of $60\text{ }\mu\text{m}$ and substrate thickness of $525\text{ }\mu\text{m}$. The study demonstrates improved resonator performance despite the added complexity of through-silicon vias integration. This suggests that state-of-the-art qubit coherence times could be achieved using similar processes for transmon-type qubits. Stitching ground planes with through-silicon vias is crucial for controlling parasitic microwave modes within the silicon chip, enabling the fabrication of larger quantum processor chips. The critical currents of the through-silicon vias leave room for improvement, potentially due to issues such as roughness of via walls or imperfect conformality of the plasma-enhanced ALD process.

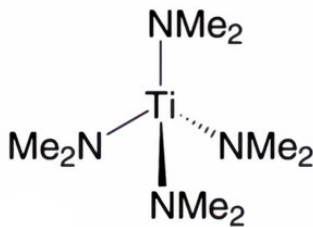
Chapter 3

Fabrication processes

3.1 Atomic layer deposition of titanium nitride

The experiment discussed here used a composition of $\text{TiN}_{1.0}$ deposited via atomic layer deposition (ALD). If further down this document the nitrogen composition is not specified, one can always assume that it is $\text{TiN}_{1.0}$.

The deposition process aimed at depositing a layer of 30 nm of TiN onto a bulk 3 inch silicon wafer.¹ The deposition occurred in a *Cambridge NanoTech Fiji F200* tool, following a recipe given by the manufacturer. The precursors were tetrakis(dimethylamido)titanium (TDMAT), represented in Fig. 3.1a, and a N_2/Ar plasma. An additional injection of H_2 is possible, yet not used in this process. As shown in Fig. 3.1b, the system uses a load lock and a turbo pump/throttle valve.



(a)



(b)

Figure 3.1: (a) Tetrakis(dimethylamido)titanium chemical structure. [7]. (b) Image of the *Cambridge NanoTech Fiji F200* system.

The deposition went through the following steps (see Appendix B): first, after introducing the sample in the chamber, the throttle valve was opened and Ar flows were set to standby at 20 and 40 sccm, as carrier gas for the precursor and through the plasma tube, respectively. Both reactor zones, the trap and the chuck were then heated at 250 °C and the system waited for the temperatures to stabilize. Then the instrument pumped away residual H_2O and O_2 that could have come from sample introduction for an hour. Afterwards, the N_2 pneumatic valve opened and the N_2/Ar plasma entered the chamber. The flows of the Ar (carrier gas), Ar (plasma) and N_2 (plasma) were set to 60 sccm, 200 sccm and 50 sccm, respectively. After a small waiting

¹Note that high resistivity Si samples ($> 5000 \text{ Ohm.cm}$) will be used for definition and patterning of the TiN components of the quantum circuits.

period of 15 seconds to stabilize the reactor, a first pulse of TDMAT precursor at 75 °C was sent for 0.2 seconds, then the instrument waited again for 6 seconds to purge the precursor. Then the N₂/Ar plasma (300 W) entered the chamber for 20 seconds, then it was stopped, and there was a 5 seconds delay. These deposition steps (starting from the TDMAT pulse) grow a layer of 0.5 Å/cycle nominal thickness and were thus repeated 600 times to reach the desired final thickness of 30 nm. After deposition, the flows were set back to standby levels, the N₂ valve was shut off, and the throttle valve was re-opened.

The thickness of the TiN layer was then checked using an ellipsometer. Those measurements yielded first a thickness of $t_{\text{TiN}} = 32.4$ nm. The layer is thus 8.03% thicker than expected. This should not impact negatively further experimentation, as this increased thickness should ease the observation of superconducting behaviour in TiN.

The next TiN depositions by ALD also targeted the performance of the dry etching protocol required to pattern the quantum resonators. In brief, three TiN depositions were made with the following nominal thicknesses: $t_{\text{TiN}} = 30$ nm at 250°C, $t_{\text{TiN}} = 60$ nm at 250°C and $t_{\text{TiN}} = 60$ nm at 450°C. Ellipsometry measurements were conducted using *Sentech's SE850* ellipsometer, as illustrated in Fig. 3.3. Typical measured curves, also displayed in Fig. 3.3, are then fitted to a three layer model containing the measured sample parameters; in this case adapting the TiN thickness so that the theoretical curves are as close as possible to the measured ones. Ellipsometer measurements were taken for each process, giving, respectively, 32.4 nm, 76.1 nm and 38.9 nm.²

The third TiN deposition result was also observed under a scanning electron microscope (SEM), yielding an average value of 69 nm, as shown in Fig. 3.4. Depositions lasted for 600 cycles for the first one, 1110 and 555 cycles for the subsequent two, having taken into account the overshoot of the first deposition. The third result indicates that the growth rate doubles at 450°C reaching 1.2 ± 0.1 Å/cycle.

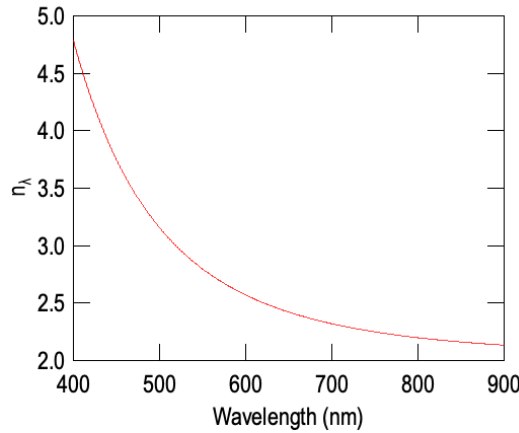


Figure 3.2: Refractive index dispersion behaviour for TiN according to simplified Cauchy formula: $N_0 = 2.027$ and $N_2 = 7046.6 \times 10^7$.

²A simplified form of Cauchy's equation is $n_\lambda = N_0 + N_2/\lambda(\text{nm})^4$, where n_λ is the refractive index, λ is the wavelength, with N_0 and N_2 coefficients. Considering $n_\lambda = 2.4665$ at 632.8 nm (see Fig. 3.2) a thickness of 38.9 nm was estimated for the deposition performed at 450 °C (fits to the data are not shown). This value is smaller than the expected 60 nm thickness, revealing that ellipsometry alone is not sufficient to determine precisely the thickness of the sample based on Cauchy formalism.

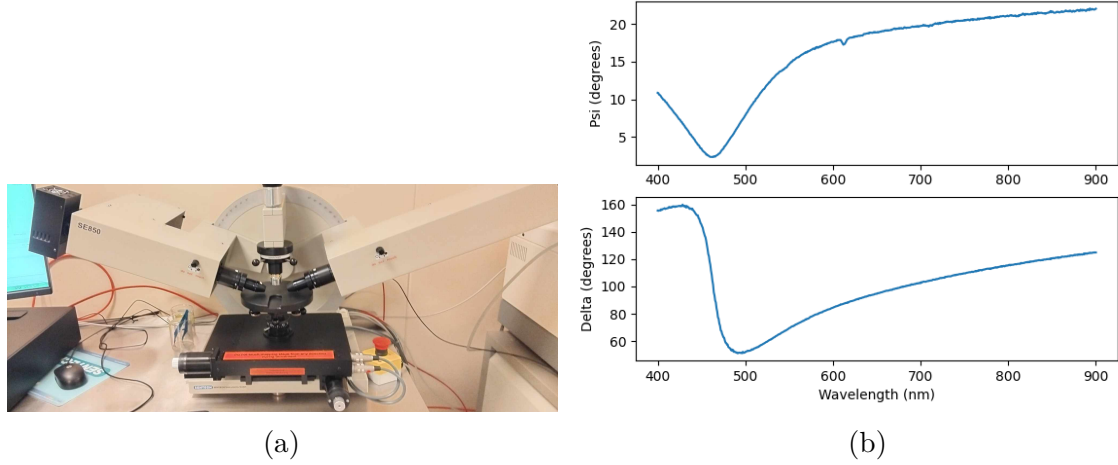


Figure 3.3: (a) Picture of the *Sentech SE850* ellipsometer used for layers' thickness measurements. (b) Ellipsometry curves for TiN deposited at 450°C with 555 deposition cycles. The measurement was made at an angle of 70° in a spectral range from 400 nm to 900 nm.

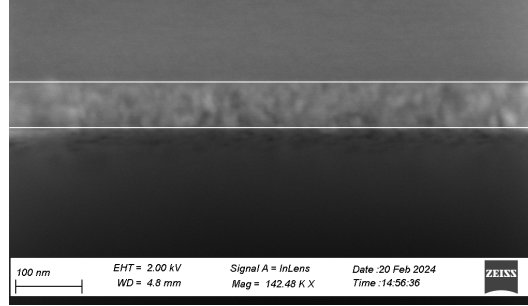


Figure 3.4: Scanning electron microscope cross-section image of the TiN deposition at 450°C.

3.1.1 Characterization

The sheet resistance R_s of the samples at room temperature are 228 Ohm/square ($t_{TiN} = 30$ nm at 250°C), 109 Ohm/square ($t_{TiN} = 60$ nm at 250°C), and 1020 Ohm/square ($t_{TiN} = 60$ nm at 450°C). The resistivities of the three samples were measured a second time after an annealing step to assess the effect it could have on the samples' structure. The annealing was conducted in a *Mila-5000* from *ULVAC* at a temperature of 600°C for 15 minutes with a 30 seconds heating period to reach 600°C, and constant H_2 and N_2 gases flow. After annealing the measured sheet resistance read as: $t = 30$ nm TiN deposited at 250°C - $R_s = 351 \pm 274 \Omega/\text{sq}$, $t = 60$ nm TiN deposited at 250°C - $R_s = 362 \pm 93 \Omega/\text{sq}$, $t = 60$ nm TiN deposited at 450°C - $R_s = 780 \pm 268 \Omega/\text{sq}$.

Superconducting behaviour of TiN thin films was tested to assess if the ALD protocol reached its objectives: depositing a superconducting layer, with a precise critical temperature T_C , to be patterned into the device's electrical connecting pads and superconducting resonator.

For the first experiment, the diced specimen was 2 mm x 4 mm and contacted with

Al strips, 0.5 mm wide, 300 nm-thick, and separated by 1 mm.³ The specimen was bonded to a dual-in line sample holder, using gold wires and silver paste and then placed in a *Montana Instruments* cryostat (Fig. 3.5).

For the second experiment, the diced sample (5 mm x 6 mm) was fixed first to a copper plate using thermally conducting epoxy and bonded to a custom printed circuit board using gold wires and silver paste, in a van der Pauw geometry. Then, the printed circuit board was inked to the horizontal socket of the cryostat using low thermally conducting manganin wires (Fig. 3.6).

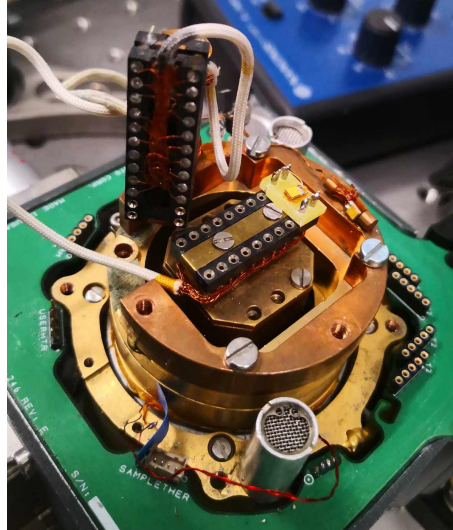


Figure 3.5: Picture of the cryostat head for the first test. The sample is connected to the horizontal socket in the same way as the thermometer (yellow).

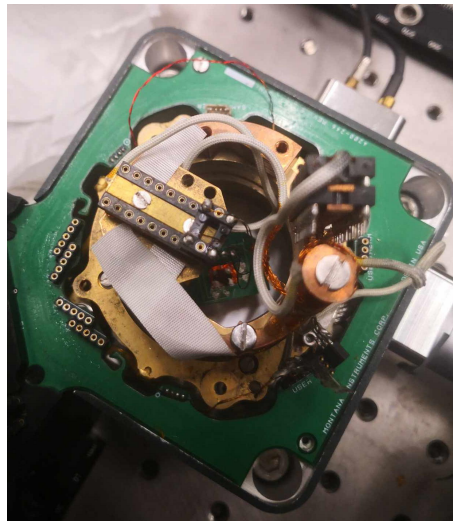


Figure 3.6: Picture of the cryostat head for the second test. Some pieces were removed compared to the first test. The sample is visible at the bottom; the connection to the horizontal socket through manganin wires can be seen.

The resulting resistance-temperature curves from the tests of both TiN layers deposited at 250°C are displayed in Fig. 3.7. The temperature range was from 300 K

³The experimental conditions for physical vapour deposition: base pressure 1.8×10^{-7} mbar and deposition rate 2 Å/s.

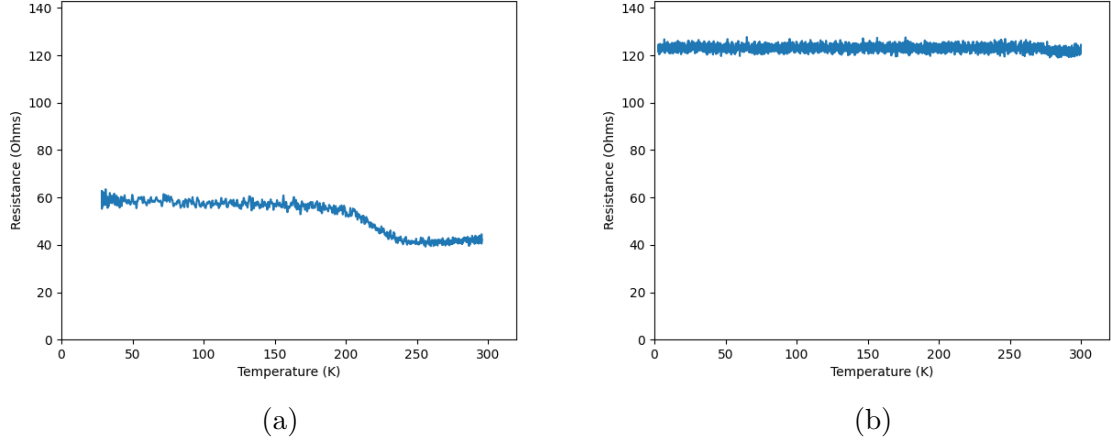


Figure 3.7: Superconductivity test results for (left) $t_{TiN} = 30$ nm and (right) $t_{TiN} = 60$ nm at 250°C .

down to only 28 K due to issues with the cryostat in the first experiment (Fig. 3.7left). The second experiment (Fig. 3.7right) spanned a temperature range of 300 K down to 2.6 K. These two measurements pointed towards the modification of the TiN deposition recipe as the absence of superconducting transition could originate from a suboptimal crystal structure.

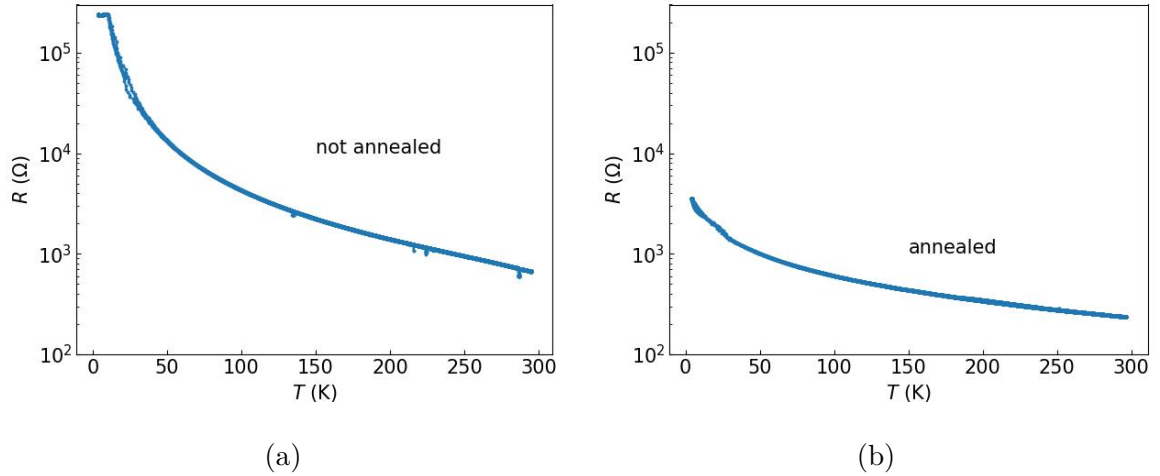


Figure 3.8: Superconductivity test results for pristine (left) $t_{TiN} = 60$ nm and annealed (right) $t_{TiN} = 60$ nm samples, deposited at 450°C . The as-deposited sample was too resistive at low temperature for the chosen sensing parameters ($10\ \mu\text{A}$ current source).

The resulting resistance-temperature curves for pristine and annealed TiN layers deposited at 450°C are displayed in Fig. 3.8. Unfortunately, both materials, as-deposited and thermal-treated, do not behave as superconductors at low temperature.

The main hypotheses for explaining this behaviour are that either the TiN has an improper crystal orientation or it is its stoichiometry that is improper for superconductivity. The possibility that superconductivity is indeed achievable in the samples at temperatures below the lowest reached during the experiments is unlikely, considering the observed data.

An improper TiN crystal orientation could arise from the orientation of the Si

wafer itself which would not allow the TiN structure to grow properly. An improper stoichiometry also directly impacts TiN's orientation and its critical temperature [49], as shown in Fig. 3.9. Stoichiometry issues could originate from changes in N_2 flow as shown in Fig. 3.9, too long purge times for high temperature depositions which increases the precursor's thermal decomposition, as advised on the ALD system's manufacturer TiN recipe, or any other minor change in the deposition process influencing Ti:N ratio and thus the final material's properties.

Thus, deposition parameters adjustments as N_2 flow, temperatures, plasma power, other TiN precursor like $TiCl_4$, *etc.*, could be investigated for reaching a superconducting state and could be complemented by other substrates as (111)-Si and SiN. The film's thickness increase from 100 to 300 nm is another straightforward next test, as the critical temperature increases with the film thickness as demonstrated in Ref. [41].

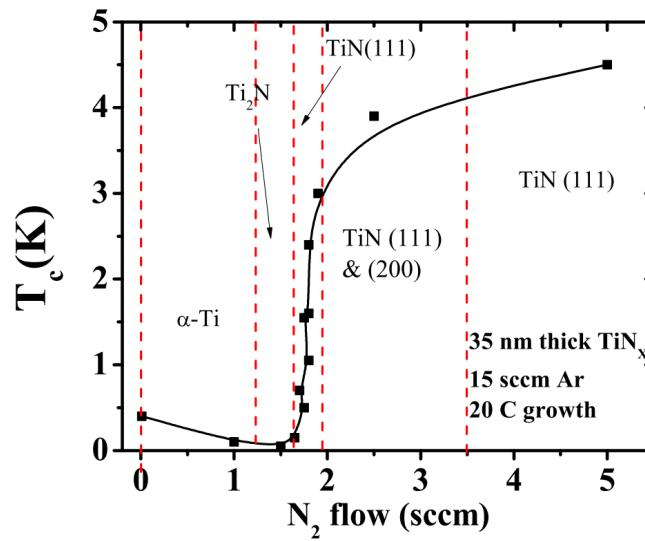


Figure 3.9: Superconducting transition temperature T_c of TiN films grown with different nitrogen flows [49].

3.2 TiN reactive ion etching

Preliminary titanium nitride etching tests were conducted onto both 250°C and 450°C deposited TiN layers, in order to characterize their etch speed and fine tune the etching recipe. The used TiN etching method is a dry SF_6 reactive ion etching in an *Oxford Plasmalab 100* tool [40].

All tests were conducted at a chamber pressure of 10 mTorr with 5 mTorr of helium back pressure, SF_6 flow rate was constant at 100 sccm for various periods. The parameters under investigation include the radio frequency (RF) power and the duration of SF_6 plasma injection.

Tables 3.1 and 3.2 give the resulting TiN thickness for each tested set of parameters, respectively for the 76.1 nm TiN layer deposited at 250°C and the 64.9 nm TiN layer deposited at 450°C.

Test	RF power (W)	Etch period (s)	Resulting thickness (nm)
1	250	60	/
2	250	60	/
3	100	60	/
4	50	30	~ 24.89
5	50	15	~ 38.96

Table 3.1: Reactive ion etching test results for the 76.1 nm TiN layer deposited at 250°C. The inductively coupled plasma (ICP) power, which was set at 1000 W for the very first test and then turned off for all the subsequent ones.

Test	RF power (W)	Etch duration (s)	Resulting thickness (nm)
1	100	90	/
2	100	30	~ 30.89
3	50	30	~ 42.73
4	50	22	~ 52.17
5	50	15	~ 55.10

Table 3.2: Reactive ion etching test results for the 64.9 nm TiN layer deposited at 450°C.

3.3 Bosch process for vias

In view of creating large scale quantum computers, chips' stacking and vertical inter-connections will be needed in order to optimize the available space in the coolest parts of the refrigeration system. For that later purpose, tests for etching vias were made by deep reactive ion etching, often called Bosch process ⁴, in an *Oxford Plasmalab 100* tool.

The used mask to pattern a top Al protective layer ⁵ and defining the emplacements and dimensions of via holes is shown in Fig. 3.10. It contains 2 rows of 2×4 rectangles made by multiple juxtaposed octagonal holes with 8 distinct hole diameters, ranging from $37.5 \mu\text{m}$ to $80 \mu\text{m}$ with one hole per $100 \times 100 \mu\text{m}$ square.

Figure 3.11 shows the patterned Al protective layer of thickness 100 nm. The Bosch process occurred at a temperature of -10°C under a pressure of 15 mTorr with a helium back pressure of 2 mTorr (see Appendix C). It involved the repeated application of the following steps for multiple cycles: first, SF_6 etchant injection at 100 sccm for 10 seconds with ICP and RF power, respectively, set to 1500 W and 30 W; second, C_4F_8 passivation layer deposition at 150 sccm for 6 seconds with ICP and RF power, respectively, set to 2000 W and 10 W. The tests lasted for subsequently 50 then 100 cycles, for allowing an in-line assessment of the etching process.

For characterization of the process, cross-section images of $40 \mu\text{m}$ wide holes were taken in a scanning electron microscope and are displayed in Fig. 3.12. Figure 3.12 shows that $159.1 \mu\text{m}$ of silicon was etched in 150 cycles which indicates that approximately 380 cycles would be required to go through a $380 \mu\text{m}$ thick silicon wafer.

⁴The Bosch process is a microfabrication technique used to create deep, high aspect ratio features. It involves alternating cycles of etching and passivation for precise control over feature depth and sidewall profile.

⁵The mask used was "RY1".

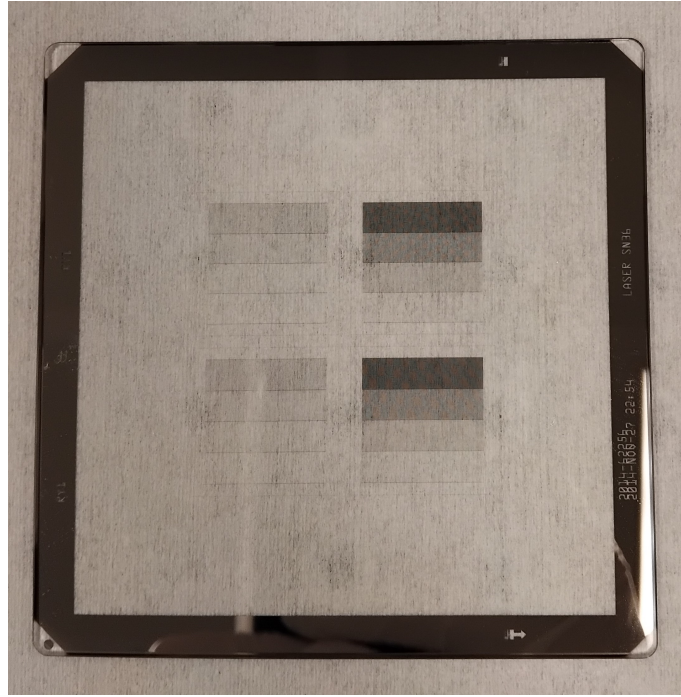


Figure 3.10: The mask used for the definition of the vias.

A complete process for vias integration was carried out. This process was done along the following steps.

First, the wafer, a highly resistive wafer of 50.8 mm diameter and 280 μm thick, was cleaned following standard cleaning procedure: 10 minutes immersion in a Piranha solution bath (a mixture of H_2SO_4 and H_2O_2 at 100°C) then 10 minutes of rinsing repeated a second time and then a 30 seconds immersion in a 2% HF solution followed by again 5 minutes of rinsing.

Secondly, a 300 nm layer of aluminium was deposited using electron beam sputtering in a *TDF 462* by Vacuum Systems Technology. This layer served as a protective layer for silicon as aluminium's etch rate with SF_6 is known to be drastically lower than silicon's SF_6 etch rate. This aluminium layer was then patterned by coating on it a negative photoresist exposed under a mask shown in Fig. 3.10 and then wet etched by soaking it in H_3PO_4 at 30°C for 5 minutes with manual shaking. Before the resist coating the wafer, too small to be handled by the *Suss Gamma80*, was fixed on a standard 3 in wafer using Miller two faces adhesive.

Thirdly, the Bosch process, as detailed in Section 3.3 and following the recipe of Appendix C, took place for 400 cycles. The sample was rotated 90 degrees every 100 cycles. After the fourth set of 100 cycles holes having perforated the backside were clearly visible for the 70 μm diameter ones as well as some of the 50 μm diameter ones. Larger diameter holes are not mechanically stable when patterned as a dense array shown in Fig. 3.11. The SEM pictures of the front- and back-side of 70 μm holes are shown in Fig. 3.13. As visible in Fig. 3.13a the aluminium mask withstood some damage distributed all over it and has been under-etch around the holes.

Fourthly, the aluminium mask was removed by soaking the samples in H_3PO_4 at

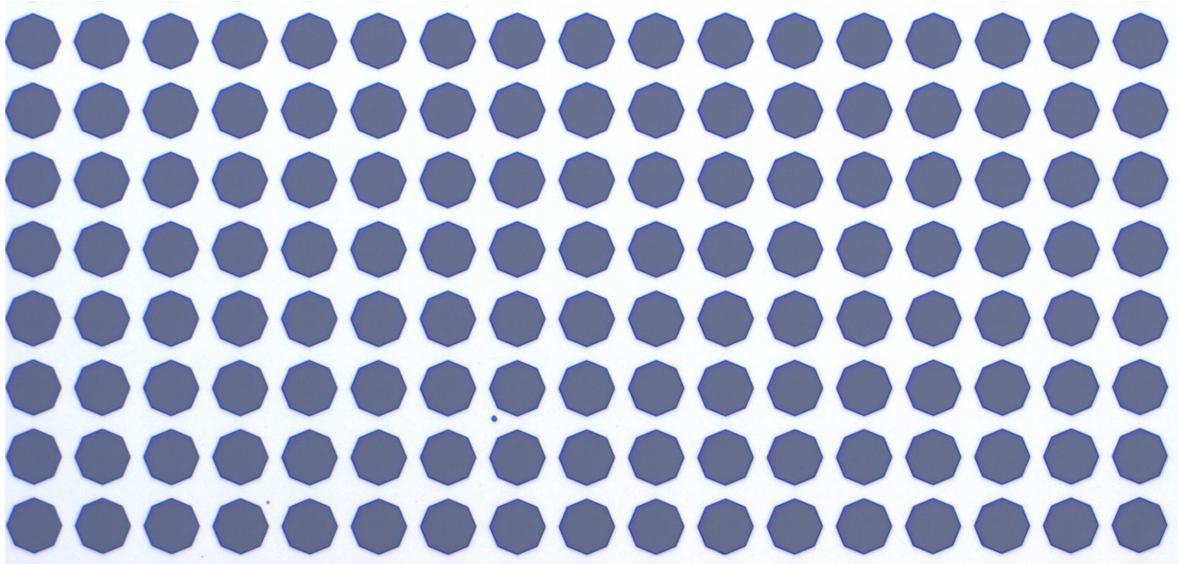


Figure 3.11: Patterned aluminium protective layer in view of the Bosch process containing holes with a diameter of $80\text{ }\mu\text{m}$.

30°C for 5 minutes with manual mechanical agitation. Then the samples were put for 10 minutes in a plasma barrel with a power starting at 100 W and incremented by another 100 W every 2 minutes.

Fifthly, titanium nitride has been deposited following the previous recipe at 450°C with the sample slightly elevated so that TiN is deposited on the back side simultaneously as on the front side and through the holes.

The resistance between the front and back sides of an area of $4\text{ mm} \times 4\text{ mm}$ is cca 4 k Ω . Based on the morphology analysis, as highlighted in the Fig.3.14a, it would be better to proceed with a double deposition, one on each side. This two-sides TiN deposition would likely result in more uniform structures and better electrical behaviour.

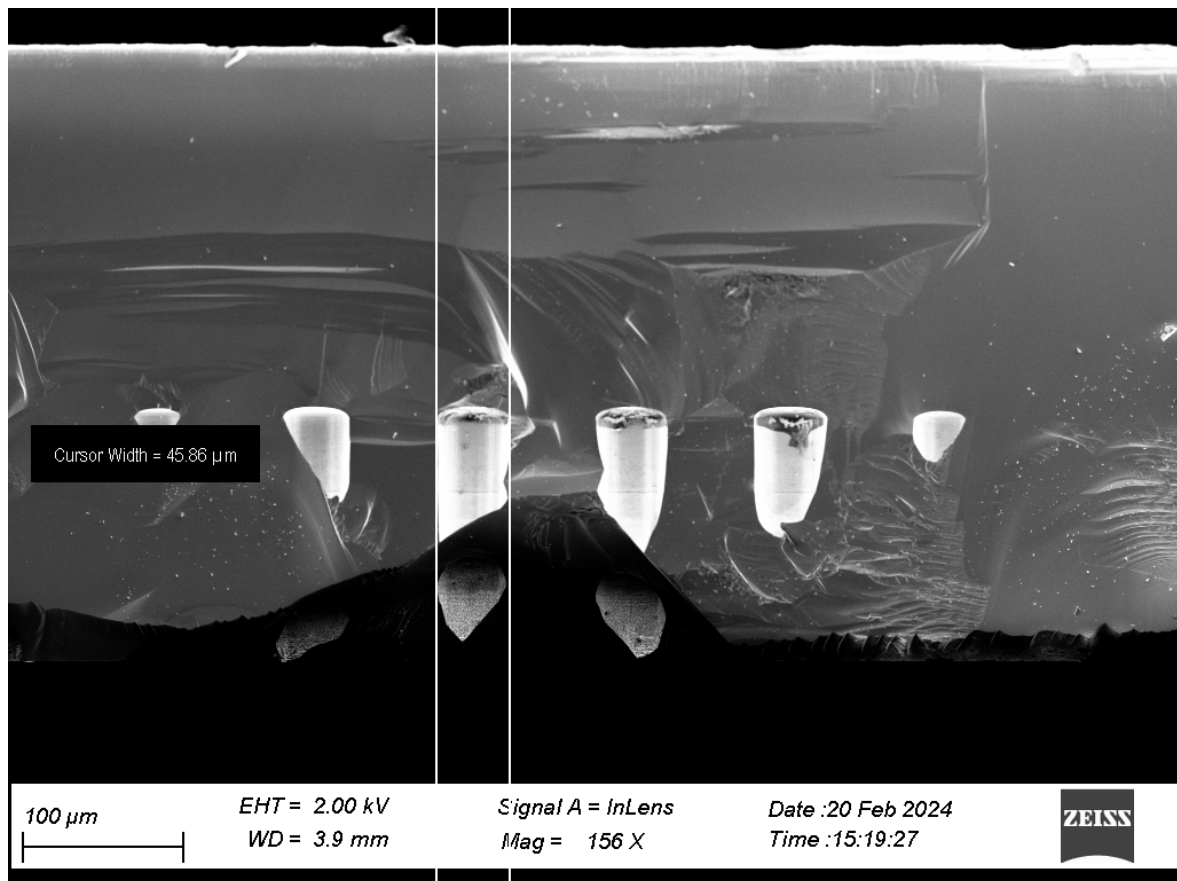


Figure 3.12: Annotated SEM image of a 40 μm wide hole after 150 Bosch process cycles.

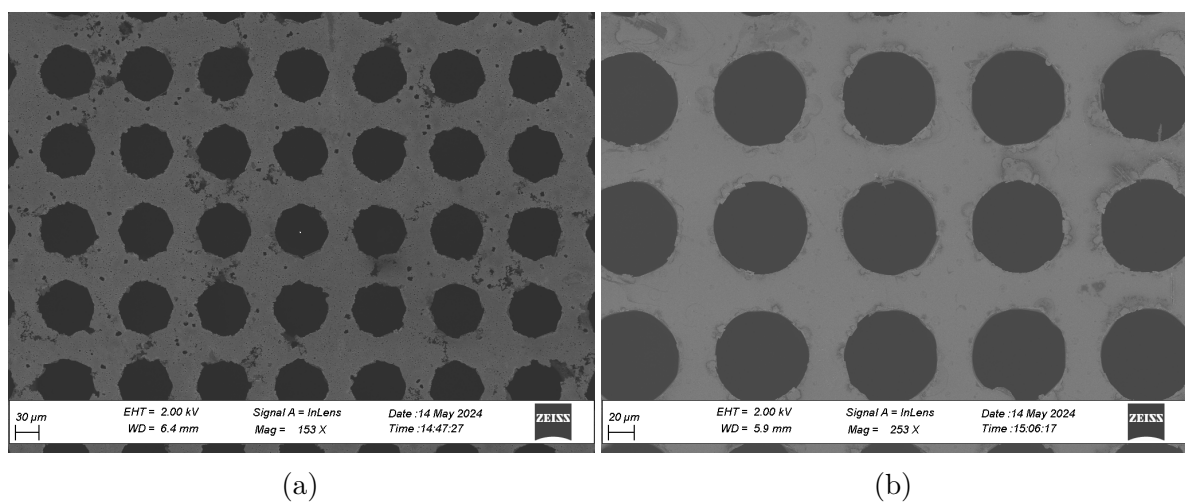


Figure 3.13: SEM pictures of 70 μm diameter holes (a) frontside with aluminium mask and (b) backside with bare silicon.

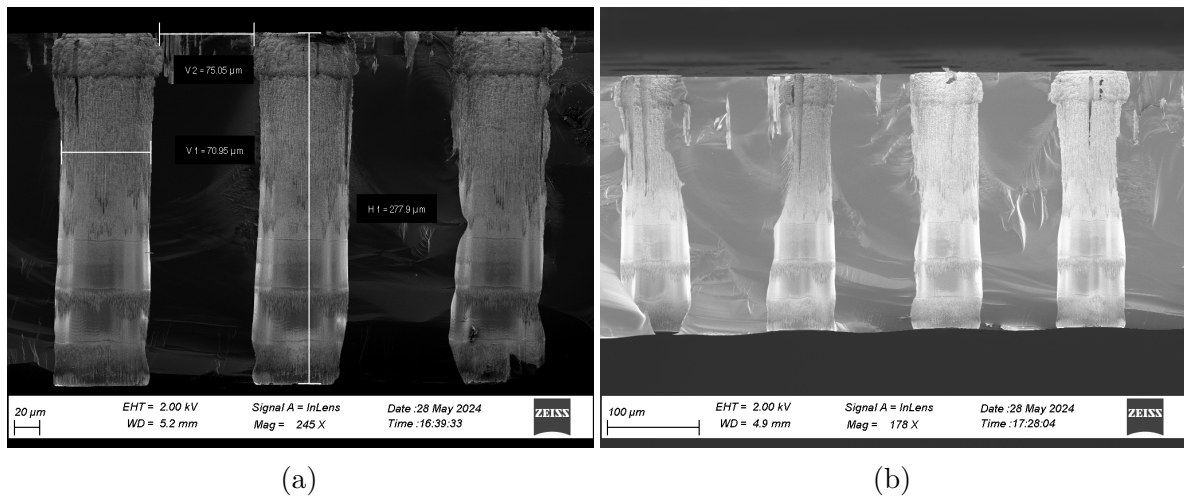


Figure 3.14: SEM pictures of 70 μm diameter holes filled with TiN. The front (deposition) side is at the top.

3.4 TiN resonator fabrication and characterization

Due to the minuscule dimensions of the circuit's features, it is imperative to ensure accurate calibration of the electron beam patterning and to carefully select the resist material.

Thus, experimental tests were conducted in a *Pioneer Two* electron beam patterning tool to determine the ideal dose for the *ma-N 2400* resists series by *micro resist technology* for the 60 nm thick TiN layer deposited at 250°C (10 kV accelerating voltage) and 450°C (20 kV accelerating voltage). The doses spanned from 10 to 160 $\mu\text{C}/\text{cm}^2$ with a step of 10 $\mu\text{C}/\text{cm}^2$ and a beam size of 6 nm (10 kV accelerating voltage) or 8 nm (20 kV accelerating voltage, up to 100 $\mu\text{C}/\text{cm}^2$). The electron-beam resist thickness is 300 nm and the spin coat parameters were 3000 rpm, 600 rpm/s, for 1 min. The electron-beam resist was developed for 30 seconds with the *ma-D 525* developer by the same manufacturer.

The result for 60 $\mu\text{C}/\text{cm}^2$ area dose, spot size 8 nm, 20 kV beam accelerating voltage, can be seen in Fig. 3.15. An area dose of $\sim 30 \mu\text{C}/\text{cm}^2$ should be optimal for the thinnest features (those with dimensions below 500 nm), while one of 50 $\mu\text{C}/\text{cm}^2$ could be used for the larger ones.

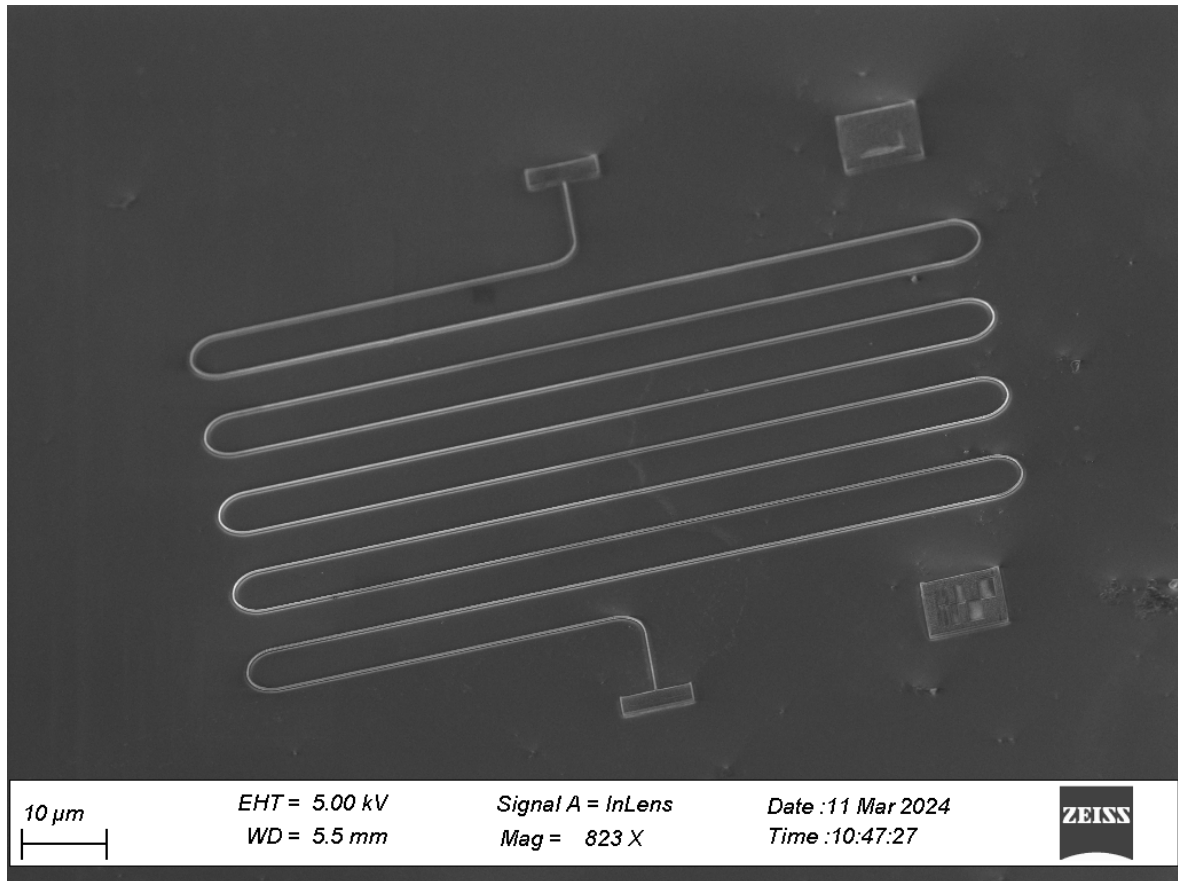


Figure 3.15: Annotated SEM image of a patterned nanoresonator at 60 $\mu\text{C}/\text{cm}^2$ with nominal width 150 nm and length 964 microns. The spot size was 8 nm for the 20 kV beam accelerating voltage. The etching parameters were 65 s for RF power of 100 W (ICP power turned off). The development of the electron-beam resist was carried out with acetone for 20 s at room temperature (no sonication). The specimen was washed with methanol, then blown dry with nitrogen.

Chapter 4

Conclusion

The work centred on TiN thin layers which are a key material in many quantum chips, including CMOS qubits and P-based qubits, rivalling thus the traditional Al for the gates and essential circuitry. This material is also the key buffer layer for Si substrates to grow state-of-the-art nitride Josephson junctions, for example NbN/AlN/NbN. Several implementations have been discussed in this work and the main target was the growth of superconducting TiN layers by ALD. Unfortunately, we were not able to reproduce the results of Ref. [41].

The planned work can be seen in the diagram below (Fig. 4.1), and the steps that have been accomplished are summarized as follows.

Titanium nitride structure: aimed at depositing superconducting TiN by atomic layer deposition. Three different depositions were tested with unsuccessful results, leading to yet another variation of the deposition process to be made.

Superconducting resonator: targeted e-beam lithography and the reactive ion etching and first tests were promising. Multiple resonators layouts have been designed (see Appendix D) and are now to be made, tested and then compared.

Vias: aimed at sustaining future superconducting cross-chips interconnects. After validating the Bosch process on a 280 μm thick wafer, vias were coated in TiN through ALD. This deposition covered less than half of it from the backside and more than half of it from the front. A resistance measurement suggested that the current indeed directs itself through the vias as the wafer's resistivity is above 10 k Ω . As the coverage with a single deposition on an elevated wafer does not cover the vias entirely, due the ALD being plasma enhanced instead of thermal, future depositions aimed at covering vias uniformly will have to be repeated twice: one deposition with the frontside exposed and a second deposition with the backside exposed.

Phosphorus donor quantum bits: involved preparatory layouts for a phosphorus wire realization and subsequent contacting tests as well as a first phosphorus dopant double quantum dot design as included in Appendix D.

Although some fabrication steps were very difficult to achieve and are tightly interconnected, inducing thus delays for the careful analysis of the entire process to engineer and test quantum bits, we can conclude that the work progressed steadily towards the ambitious objectives set in the beginning.

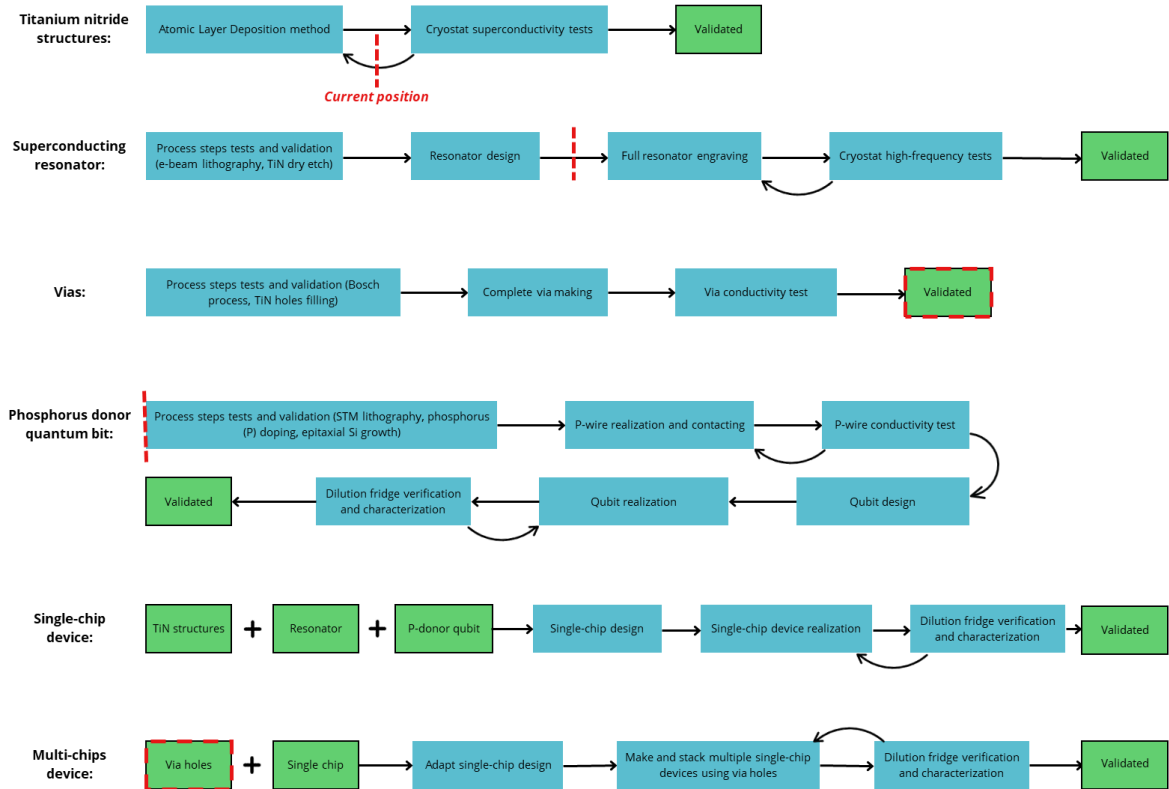


Figure 4.1: Several tasks are running in parallel with different stages of validation, attained or to be attained next.

Appendices

Appendix A

Qubits: Basics

This appendix explores basic notions related to quantum bits and more broadly to quantum computing.

Bloch sphere: The Bloch sphere is a common way for representing the state of a single qubit. As illustrated in Fig. A.1 the quantum state can be represented by two angles: θ and φ , and thus a point on a sphere's surface. The angles determine the proportion of its states' superposition, *i.e.* the qubit's probability of being in state $|0\rangle$ or $|1\rangle$ along the z axis, $|+\rangle$ or $|-\rangle$ along the x axis, and $|+i\rangle$ or $|-i\rangle$ along the y axis. However, the Bloch sphere has no simple generalization for multiple qubits entangled states. [39]

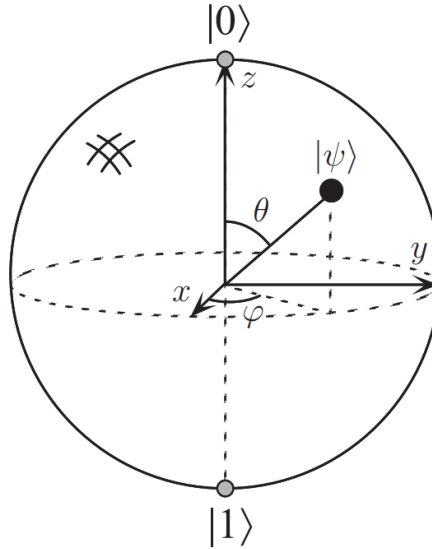


Figure A.1: Bloch sphere representation of a qubit; its state $|\psi\rangle$ is characterized by angles θ and φ . [39]

Relaxation time T_1 : T_1 , also known as the qubit relaxation time or longitudinal relaxation time, characterises the speed at which the higher-energy state $|1\rangle$ tends to relax down to the lower-energy state $|0\rangle$. [39]

Dephasing time T_2 : T_2 , also known as the qubit dephasing time or transversal relaxation time, characterises the speed at which the initial and final states of the qubit become uncorrelated upon interacting with the environment. This perturbation can be understood as phase damping and results in a loss of information between the $|+\rangle$, $|-\rangle$, $|+i\rangle$ and $|-i\rangle$ states, upon changes of the φ angle. [39]

Quantum decoherence: The loss of quantum coherence, called quantum decoherence refers to any noise process in quantum processing resulting in the loss of

information for the quantum system. It is due to unwanted interactions with the outside world and can be qualified with, but is not limited to, T_1 and T_2 time constants. [39]

Quantum computation: Quantum computation refers to the use of quantum mechanical systems in information processing tasks. Quantum algorithms, algorithms designed to be executed on quantum computers, are applied through a quantum circuit, a defined sequence of quantum gates, initialization and measurements, that most often ends up with a final reading of the quantum state for some qubits of interest. [39]

Qubit gates: Analogously to classical gates, the qubit gates are logic gates performing manipulations of the information *i.e.* they are operations on one or multiple qubits. Qubits gates can be for example CNOT, CZ, Pauli (X, Y, or Z), Hadamard gates, *etc.* and are often represented in circuit or matrix forms, as illustrated in Fig. A.2. [39]

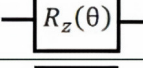
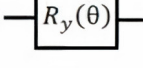
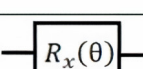
Gate	Symbol	Matrix
Pauli-X (NOT)		$\begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$
Pauli-Y		$\begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix}$
Pauli-Z (Phase flip)		$\begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}$
S		$\begin{pmatrix} 1 & 0 \\ 0 & i \end{pmatrix}$
T		$\begin{pmatrix} 1 & 0 \\ 0 & e^{i\pi/4} \end{pmatrix}$
Hadamard		$\frac{1}{\sqrt{2}} \begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix}$
Rotation Z		$\begin{pmatrix} e^{-i\theta/2} & 0 \\ 0 & e^{i\theta/2} \end{pmatrix}$
Rotation Y		$\begin{pmatrix} \cos(\frac{\theta}{2}) & -\sin(\frac{\theta}{2}) \\ \sin(\frac{\theta}{2}) & \cos(\frac{\theta}{2}) \end{pmatrix}$
Rotation X		$\begin{pmatrix} \cos(\frac{\theta}{2}) & -i\sin(\frac{\theta}{2}) \\ i\sin(\frac{\theta}{2}) & \cos(\frac{\theta}{2}) \end{pmatrix}$
CNOT		$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix}$
Swap		$\begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{pmatrix}$

Figure A.2: List of qubit gates with their quantum circuit symbols and matrix representations.

CNOT gate: The typical controlled NOT gate, CNOT, is a two qubits gate which inverts the second qubit only if the first is $|1\rangle$. Its circuit symbol and matrix representation are given in Fig. A.2.

Gate fidelity: The average fidelity of a quantum gate, also applicable on quantum channels, is a distance measure that can take positive values up to 1, characterizing thus the quantum gate's quality.

Appendix B

Atomic layer deposition protocol

This appendix contains the full instruction set to reproduce the 30 nm TiN deposition at 250°C on a *Cambridge NanoTech Fiji F200*.

	Instruction	#	Value	Units
0	flow	0	20	sccm
1	flow	1	40	sccm
2	heater	17	150	deg C
3	heater	16	150	deg C
4	heater	13	250	deg C
5	heater	14	250	deg C
6	heater	12	250	deg C
7	heater	20	75	
8	stabilize	17		sec
9	stabilize	12		sec
10	stabilize	20		
11	stabilize	13		
12	wait		1800	sec
13	APC		16	
14	MFCvalve	2	1	
15	flow	0	60	sccm
16	flow	1	200	sccm
17	flow	2	50	sccm
18	wait		15	sec
19	pulse	3	0.2	sec
20	wait		6	sec
21	plasma		300	Watts
22	wait		20	sec
23	plasma		0	Watts
24	wait		5	sec
25	goto	19	600	cycles
26	flow	0	20	sccm
27	flow	1	40	sccm
28	flow	2	0	sccm
29	MFCvalve	2	0	
30	APC		100	
31	heater	15	0	deg C
32	heater	20	0	deg C

Table B.1: ALD instructions for 32.4 nm-thick TiN deposition in *Cambridge NanoTech Fiji F200 atomic layer deposition system*.

Appendix C

Bosch process protocol

This appendix contains the instruction set used for the vias Bosch process on an *Oxford Plasmalab 100*.

1. move and wait
2. wait
3. initial etch
4. Repeat 100
5. (si-drie) deposition
6. (si-drie) etch
7. Loop
8. He stop
9. move table down

Element	Value	Units
Step time	10	s
Log interval	1	s
Helium backing pressure	10	Torr
Chamber pressure	10	Torr
SF ₆ flow	1	sccm
C ₄ F ₈ flow	140	sccm
RF forward power	30	W
ICP	1000	W

Table C.1: Bosch process "(si-drie) deposition" step instructions.

Element	Value	Units
Step time	14	s
Log interval	1	s
Helium backing pressure	10	Torr
Chamber pressure	10	Torr
SF ₆ flow	120	sccm
C ₄ F ₈ flow	1	sccm
RF forward power	30	W
ICP	1000	W

Table C.2: Bosch process "(si-drie) etch" step instructions.

Appendix D

Layouts

A mask for testing different fabrication schemes has been designed as represented in Fig. D.1. As a general remark, the blue colour represents various metallic marks while dark colour represent patterns in the TiN layer. Without entering the details of each chip, we note that a series of devices feature microwave cavities. The microwave resonator characteristics (coplanar waveguide geometry) are given together with the salient features of the design as follows.

QE1L: Resonator 10 microns width with separation of 2 microns, length 7300 microns, coplanar three gates with and without vias

QE1R: Resonator 10 microns width with separation of 2 microns, length 7300 microns, coplanar three gates with and without vias and ground with holes for flux trapping

QE2L: Resonator 10 microns width with separation of 2 microns, length 6650 microns, coplanar four gates with and without vias

QE2R: Resonator 10 microns width with separation of 2 microns, length 6650 microns, coplanar four gates with and without vias and ground with holes for flux trapping

QE3L: Resonator 7 microns width with separation of 4 microns, length 7600 microns

QE3R: Resonator 7 microns width with separation of 4 microns, length 7600 microns and ground with holes for flux trapping

QE4L: Resonator 10 microns width with separation of 4 microns, length 6800 microns

QE4R: Resonator 10 microns width with separation of 4 microns, length 6800 microns and ground with holes for flux trapping

The chip labelled QE2L is further detailed in Fig. D.2.

Besides these test platforms, a series of chips were designed to enable a comparative study for controlled phosphorus delta-doping from a GaP decomposition solid source or a valved cracker for phosphorus (for producing P_2) as an alternative to the toxic phosphine gas for donor patterning onto H:Si(001) templates engineered by STM.

QE5: STM lithography with metallized and etched marks

QE6: P-donors and P-wire test chip with etched marks

The chip labelled QE6 is further detailed in Fig. D.3.

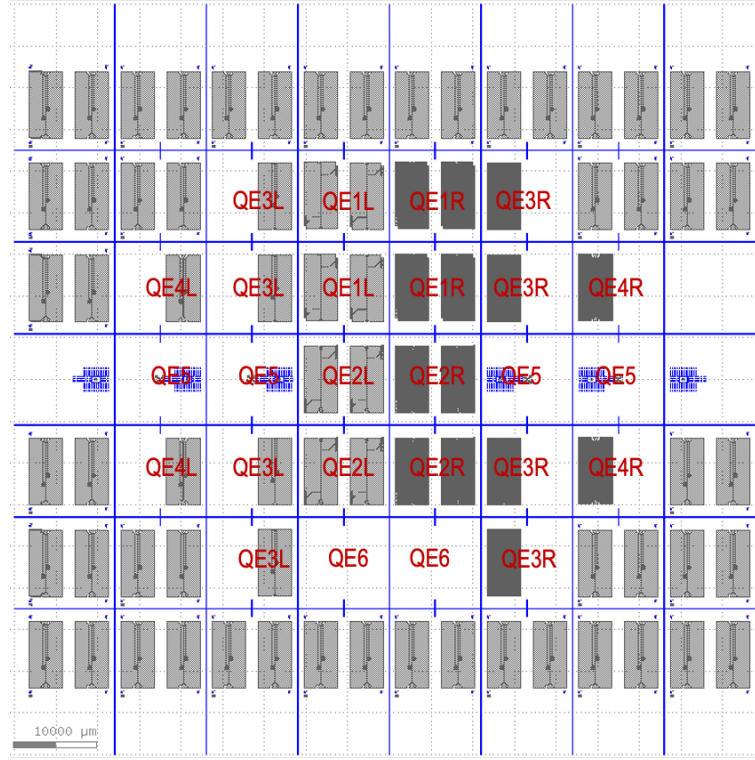


Figure D.1: Picture of the designed mask with a variety of chips to test several fabrication procedures for semiconductor qubits.

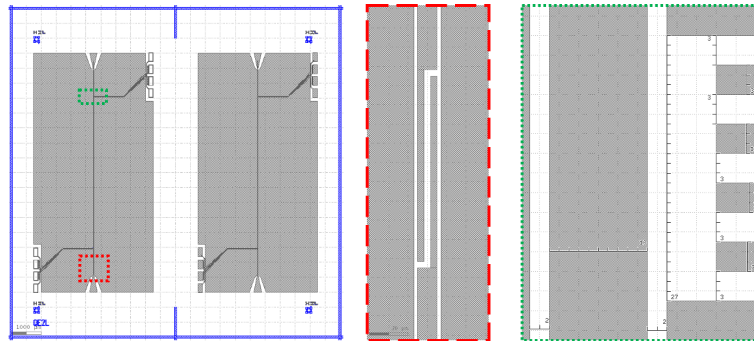


Figure D.2: Picture of a chip, labelled QE2L, to test the interaction between distant quantum dots mediated by microwave photons.

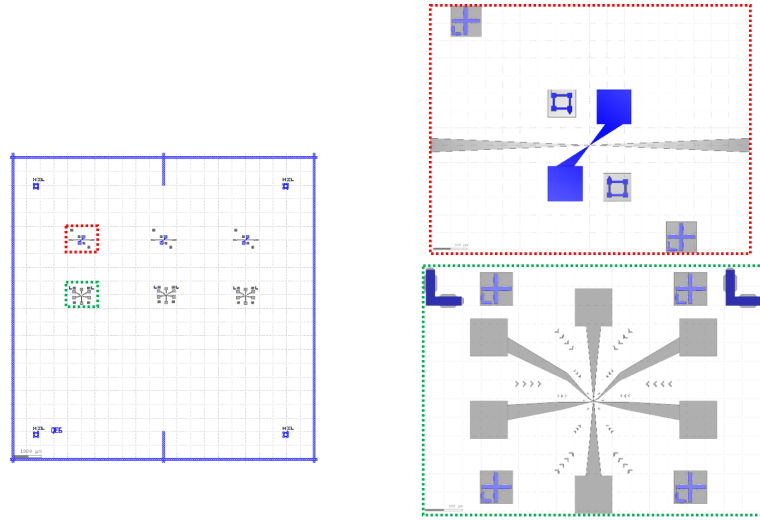


Figure D.3: Picture of a chip, labelled QE6, to test fabrication steps related to phosphorous doping by STM lithography.

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