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The investigation of aluminum oxide (Al_2O_3) as gate dielectric in ultra thin body and buried oxide (UTBB) fully depleted (FD) Silicon-on-Insulator (SOI) transistor

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Chapitre 1

Introduction

1.1 The purpose and objective of this works

Nowadays, the semiconductor industry requires high performance (speed), low power consumption and high density of transistors on a wafer. This is reached by reducing the dimensions of the metal-oxide-semiconductor field-effect transistor (MOSFET). The rapid shrinking of the transistor feature size includes not only the channel length, but also the gate dielectric thickness. When the current gate dielectric (SiO_2) is reduced to 1.3 nm [1], a number of critical problems appear, such as gate leakage current, band gap change, reliability, boron penetration and so on. To solve these problems, high-k dielectric materials have been considered to replace SiO_2 for sub-0.1-μm CMOS technology. To be potential replacements for SiO_2 such as dielectric materials HfO_2 and Al_2O_3, many material properties of them must be considered. The dielectric constant k should be high enough for good insulation. The dielectric is sandwiched between gate and silicon channel. Therefore, it should have the same thermodynamic stability as silicon. In addition, it should be compatible with gate materials. The energy gap of the dielectric should be large enough to avoid the gate leakage current (such as the gate tunneling current). Importantly, the interface between the dielectric and silicon should have a good electrical quality (specifically, low fixed charge Q_f and interface charge density D_{it}). Moreover, the dielectric should not damage electric properties of the silicon channel (such as electron mobility, threshold voltage V_{th}) and so on). The dielectric process should be compatible with CMOS technology. Due to the principle of sustainable development we should avoid to use rare metal oxides when selecting the high-k dielectric materials. According to these requirements, Al_2O_3 attracts our attention. In this thesis, we fabricate MOS capacitor stacks by using Al_2O_3-based materials as gate dielectrics. We analyze the advantages and disadvantages of these stacks by C-V measurements and Silvaco-Atlas simulation. For comparison, we prepare several kinds of the reference stacks, with different high-k dielectrics and different thick. Hereafter, all the discussed MOSFETs refer to ultra-thin body and thin buried oxide (UTBB) SOI transistors.

1.2 Thesis outline

This thesis is organized into 6 chapters. After the introduction chapter, a state of the art on high-k materials will be detailed in **chapter 2**. The main objective of **chapter 2** is to compare the properties of different high-k dielectrics, indicate challenges encountered by researches, and find the theoretical solution in downscaling MOSFET. Therefore, **chapter 2** is fundamental for good understanding of gate dielectrics.

Chapter 3 will present the fabrication process of the MOS capacitor stacks. We will focus on the main fabrication technology : atomic layer deposition (ALD). In this work, we fabricate many kinds of the MOS capacitor stacks with different thickness. These stacks combine Al_2O_3 with the other dielectrics, such as SiO_2 and HfO_2 for comparing the Al_2O_3 gate oxide behaves.

The goal of **chapter 4** is to characterize the fixed charge Q_f and interface charge density D_{it} on the MOS capacitor stacks. The most efficient way to obtain the Q_f and D_{it} is the conventional C-V measurement. To precisely extract the Q_f and D_{it} without the parasitic effect, we build the equivalent circuits for the complex structure of the MOS capacitor stacks.

In **chapter 5**, we will investigate the physics mechanism of the MOS capacitor stacks and the behaviors of the negative charges in Al_2O_3 by a simulation tool (Silvaco Atlas). We will compare the simulation results with the measurement data. We will also analyze the possibility for replacing SiO_2 by Al_2O_3 in 65-nm-node technology.

In **chapter 6**, we will summarize the main scientific results of this work. We also will indicate challenges and discuss the future work.

Chapitre 2

Properties of gate dielectric materials

This chapter is a review of material properties of gate gate dielectric. According to the requirements for scaling down, these properties should be considered with the comparison between SiO_2 and expected gate dielectric Al_2O_3. It is divided into seven sections : Section 2.1 reviews the relative permittivity and equivalent oxide thickness. Section 2.2 investigates the effect of thermodynamic stability between dielectric and silicon. Section 2.3 shows the importance of gate materials compatibility with gate dielectric. Section 2.4 describes that the energy gap of the dielectric should be large enough to avoid gate leakage current. Section 2.5 presents that interface between the dielectric and silicon should have a good electric quality (low fixed charge and interface charge density). Section 2.6 discusses how the gate dielectric effects electronic quality of silicon channel. Section 2.7 describes fabrication process of gate dielectric which is compatible with silicon.

2.1 Choice of high-k value

The drive current of MOSFET is given if both source and substrate are grounded as

$$I_D = \frac{W}{L}\mu C_{inv}(V_G - V_T - n\frac{V_D}{2})V_D \tag{1}$$

$$C_{inv} = \frac{\epsilon_0 k}{t} \tag{2}$$

Where the C_{inv} is the inversion capacitance per unit area, k is the relative permittivity, n is the body factor and t is the thickness of gate dielectric. The rest of the parameters can be found in the related references [2]. Initially, I_D increases linearly with V_D and then reaches the saturation value I_{Dsat}. When $V_{Dsat} = V_G$ - V_T in saturation and n is equal to 1 by assuming the maximum depth of the depletion region does not vary from source to drain, equation (1) supress to :

$$I_{Dsat} = \frac{W}{L}\mu C_{inv}\frac{(V_G - V_T)^2}{2} \tag{3}$$

From equation (3), we can see that I_{Dsat} increases with C_{inv}. If C_{inv} is assumed to be fixed and SiO_2 is replaced by a high-k dielectric, one obtains :

$$\frac{t_{eq}}{k_{eq}} = \frac{t_{Highk}}{k_{Highk}} \tag{4}$$

Here t_{eq} is the equivalent oxide thickness (EOT), k_{eq} is the dielectric constant of SiO_2 (= 3.9), and t_{Highk} is the physical thickness of high-k dielectric. k_{Highk} is the dielectric constant of high-k dielectric. For example, 1.5-nm-thick SiO_2 is replaced by Al_2O_3 with a $k = 9$, the thickness of Al_2O_3 is calculated to be 3.5 nm. Therefore, 3.5-nm-thick Al_2O_3 yields the same equivalent capacitance as 1.5-nm-thick SiO_2. But, the gate leakage current and the power consumption are smaller in Al_2O_3 than in SiO_2 as shown in Fig.2.1 [2]. This is the reason why high-k dielectrics, for example Al_2O_3, are considered to replace SiO_2.

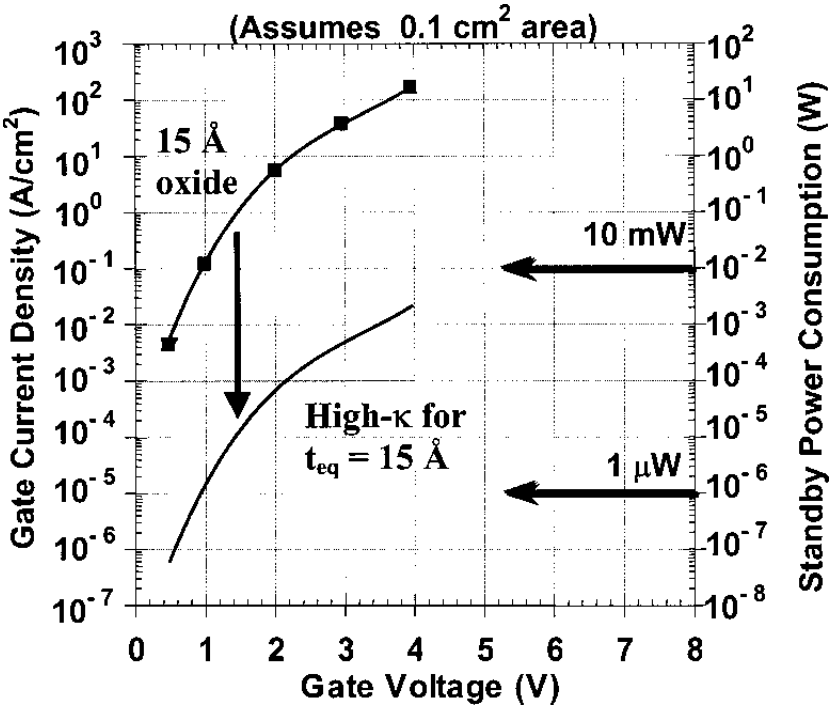


FIGURE 2.1: Gate leakage current density and power consumption for a chip, which has a 1.5-nm-thick SiO_2 gate dielectric compared to high-k dielectric Al_2O_3 by exhibiting the same equivalent oxide thickness

2.2 Thermodynamic stability

Many dielectric materials have a higher dielectric constant ($k > 3.9$). However, when contact with silicon, they are not thermodynamically stable and react with Si to form an undesirable interfacial layer. This fact limits the most of high-k dielectric applications.

$$MO_2 + Si = M + SiO_2 \tag{5}$$

$$MO_2 + 2Si = MSi + SiO_2 \tag{6}$$

MSi (a silicide formed by equation 5) is metallic which will short out the field effect. To avoid the silicide reaction, a thin layer of SiO_2 is normally introduced in serials with the high-k dielectrics, which increases the EOT and degrades the performance of new oxide. In conventional CMOS process, for activing dopants, annealing is carried out at high temperatures (900°C to 1000°C). The gate dielectrics should retain

insulating property without degrading.

The high-k dielectric materials with wide band gap are thermodynamically stable since their silicide reactions are formed at high temperatures. From a view of this point, a lot of binary oxides in columns II, III and IV in periodic table are restricted to few. The feasible materials are Al_2O_3, ZrO_2, HfO_2, Y_2O_3, La_2O_3 and the lanthanides Pr_2O_3, Gd_2O_3 and Lu_2O_3 [4][5]. The properties of ZrO_2 and HfO_2 are similar since Zr and Hf come from same column IV in Periodic table. ZrO_2 is stable with respect to silicide formation under 900°C. This degree of robustness approaches the standard of CMOS process flow. HfO_2 is more perfect in stability. Y_2O_3 remains stable after annealing at 950°C. Although the dielectric constant of La_2O_3 is slightly higher than HfO_2, it is hygroscopic. The other lanthanides are potential candidates comparable to La_2O_3 [6]-[10]. For example, Pr_2O_3 with a k value of 30 can be heated at 1050°C for 20 min in N_2 and the standard gas. However, it can react with air, leading to an interfacial layer SiO_x which degrade electrical performance. Al_2O_3 is hard to react with silicon and its k value is acceptable. A useful method for assessing the metal oxide (MO_x) stability in contact with silicon is to use ternary phase diagrams [3]. If the existence of a tie line between MO_x and Si, they are thermodynamic stable. Fig.2.2 shows isothermal sections of Ta-Si-O and Al-Si-O systems at 1 bar. The tie line is to found between Ta_2O_5 and Si [10]-[11], which means their contact are not in equilibrium. For the Al-Si-O system, Al_2O_3 is connected with Si by a tie line, indicating that their contact is in equilibrium. Therefore, Al_2O_3 is quite stable.

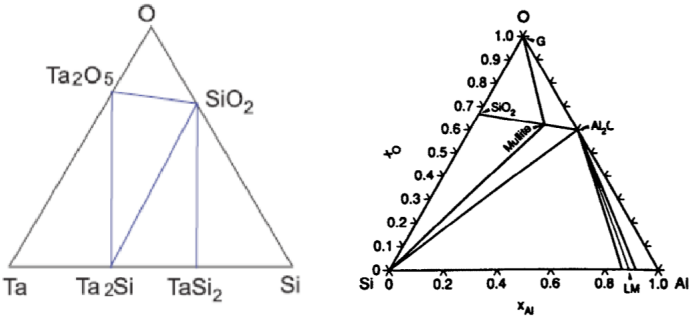


FIGURE 2.2: Comparison of ternary phase diagrams of unstable Ta-Si-O and stable Al-Si-O systems[3]

2.3 Gate material compatibility

Then we consider about high-k dielectric compatibility with gate material in the standard CMOS technology.

The desirable gate material is to use poly silicon since the threshold voltage (V_{th}) is easy to control by tuning dopant for nFET transistor or pMOS transistor.

Unfortunately, dopant penetration is often observed in many high-k dielectrics. For example, both boron and phosphorous dopant diffusion has been observed in Al_2O_3 gate dielectric, which cause undesired shifts of the flatband voltage (V_{FB}) and V_{th} values. To solve this problem, 4 approaches are found for choosing the compatible gate materials with high-k dielectrics : (i) To use single midgap metal (such as TiN), whose Fermi level locates at the midgap of the Si substrate (see Fig.2.3a). In this case, the V_{th} is symetrical for both nMOS and pMOS transistors. The band gap of silicon is 1.1 eV and thus the V_{th} is 0.5V for both nMOS and pMOS transistors. However, the value of 0.5V is too large for sub$-0.1-\mu m$ CMOS technology. (ii) To use two separate metals : one with a high work function (Pt and Au) is for pMOS transistor and the other one with a low work function (Al) for nMOS transistor (see Fig.2.3b). Although the V_{th} is about 0.2 V for nMOS and pMOS transistors, Pt and Au are expansive, as well as Al can be easily to be oxidized to form Al_2O_3. (iii) To use conducting metal oxides, such as IrO_2 and RuO_2. Zhong et al reported that RuO_2 is stable up to 800°C, has a resistivity of 65 $\mu\Omega-$cm, and a work function of 5.1 eV [13]-[14]. (vi) To use poly-$Si_{1-x}Ge_x$ [15]-[16] gates for achieving higher boron activation levels for both pMOS and nMOS transistors. Although the poly Si dopant penetration phenomenon exists in Al_2O_3, this issue could be overcome by using compatible gate materials.

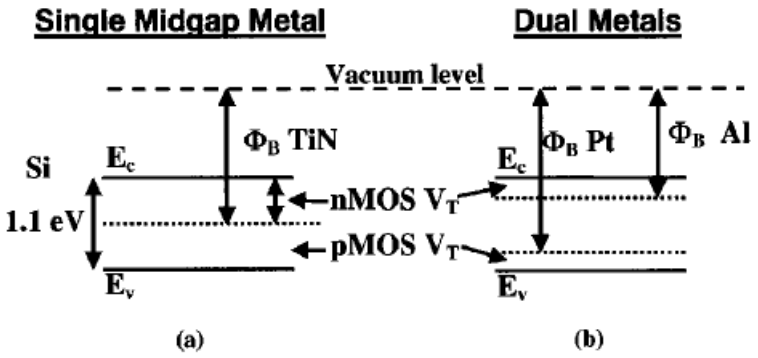


FIGURE 2.3: Energy diagrams of threshold voltages for nMOS and pMOS devices using (a) midgap metal gates and (b) dual metal gates

2.4 Band gap and offset

From the point of view to choose the k value of the dielectric, the higher the better is. However, we find that the k values are inversely proportional to band gaps from table 1. A large band gap leads to a good insulation, thereby low leakage current. The better k value is in the range of 10 to 30 after considering the trade-off between the energy band and the k value. Moreover, band offset is an important parameter to be considered for choosing the dielectric. It can be seen in Fig.2.4 that the conduction band offset $\Delta E_c = q[X - (\Phi_M - \Phi_B)]$ is the barrier for electrons traveling from the gate to the silicon substrate. The tunneling current increases exponentially with decreasing the barrier height (ϕ_B) and the dielectric thickness.

The band offsets for some high-k dielectrics are also listed in Table 1. The literature indicates that band offset has to be over 1eV to avoid large tunneling current. From Table I we can see that Al_2O_3 has the largest band offset besides SiO_2 and its band gap is very close to that of SiO_2 among the dielectrics listed in Table 1.

Materials	k	Gap(eV)	$\Delta E_c(eV)$
Si	–	1.1	–
Si_3N_4	7	5.1	2
Al_2O_3	9	8.7	2.8
Ta_2O_5	26	4.5	1-1.5
TiO_2	80	3.5	1.2
ZrO_2	25	7.8	1.4
HfO_2	25	5.7	1.5
Y_2O_3	15	5.6	2.3
La_2O_3	30	4.3	2.3

TABLE 2.1: Summary of the relative permittivity and energy gap for high-k dielectric materials

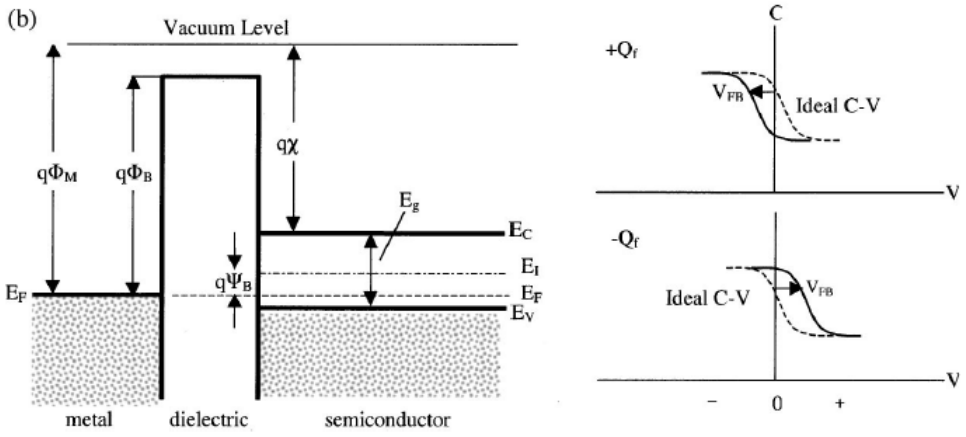


FIGURE 2.4: Energy band structure of MOS capacitor (left), C-V curves shift for different gate oxides due to different fixed oxide charge (right) [17]-[18]

2.5 Interface quality

The interface quality mainly depends on fixed charge (Q_f) and interface charge density (D_{it}) at the dielectric/Si interface. In SiO_2, the typical D_{it} value is around $2 \times 10^{10} cm^{-2}$ and the Q_f is below $10^{11} cm^{-2}$. While most of high-k materials show D_{it} around $10^{11} - 10^{12} cm^{-2}$ and Q_f about $10^{12} cm^{-2}$. To replace SiO_2 with other high-k dielectrics, the main goal is to achieve a good interface quality. However, a lot of reports indicate that it is hard to obtain much better interface quality. It is crucial to understand the origin of Q_f and D_{it} in any of high-k dielectric. Recently,

two methods are developed for achieving a high quality interface of SiO_2-silicon. One is to use an amorphous SiO_2, and the other is to epitaxially grow crystalline SiO_2 on the silicon. Amorphous and crystalline SiO_2 with less grain boundaries grown epitaxially lead to a decreased leakage current. Amorphous SiO_2 deposited by atomic layer deposition, shows a D_{it} of $10^{11}cm^{-2}$. On the contrary to SiO_2, the fixed charge is negative in Al_2O_3, resulting in a positive V_{FB} (see Fig.2.4). This negative fixed charge in Al_2O_3 has same sign as the charge in inversion layer(p type), which prevent channel electrons tunneling the oxide layer to the gate. Even if one interfacial layer SiO_2 is added between Al_2O_3 and SiO_2,the total fixed charge will still be negative. This is a great advantage of Al_2O_3.

2.6 Electronic quality of silicon channel

2.6.1 Mobility

To achieve fast speed, high density, and low power consumption, the transistor feature size has been scaled down the nanometer range. The source−drain current is mainly determined by carrier mobility. So the main point is to find out the limitation for carrier mobility ($(\mu_n(y))$ and impactor factors to it. The carrier mobility depends on vertical electric field in the channel, which varies from source to drain. This electric field ($\epsilon_x(y)$) is average electric filed of the vertical field at the boundary between the inversion layer and depletion region, and the electric field of the vertical field at the silicon-oxide interface.

$$\mu_n(y) = \frac{\mu_{no}}{1 + \Theta\epsilon_x(y)} \tag{7}$$

$$\epsilon_x(y) = \frac{\epsilon_{so}(y) + \epsilon_{si}(y)}{2} \tag{8}$$

It is worth that the distribution and sign of the charges inside gate oxides will affect the electric field, which is the origin of mobility degradation.

Takagi[32] has developed one model for mobility that only depends on effective gate field and the silicon orientation, [100], [110] or [111]. Different field has different effect on mobility. At low fields, the Coulombic scattering(C) dominant it by trapped charges, channel and gate electrode interface. At moderate field and high field, mobility is limited by phonon scattering(PH) and surface roughness(SR), respectively. The mobility of devices with SiO_2 gate oxide is close to universal limit[19] which is above the mobility of other high k dielectric. This is an interesting point to understand the reasons and to correct it. The reasons are probably from two aspects. The first aspect is scattering by interface states and trapped charges. As shown in some references, the amount of trapped charges are much more than that in SiO_2 oxide. The second reason is the remote scattering by low lying polar phonon modes[20]. Although SiO_2 has a best behavior of electron mobility, in all potential high-k materials Al_2O3 has a similar performance with SiO_2 when effective electric field achieves around 0.1 MV/cm. This kind of good quality for Al_2O3 is beneficial for scaling down.

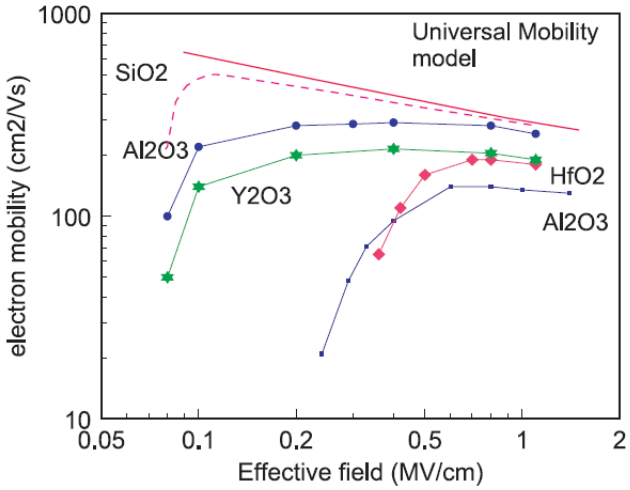


FIGURE 2.5: Carrier mobility of n-type Si, for various gate oxides [19]

2.6.2 V_{th} stability

The other important property is the threshold voltage stability. The threshold voltage(V_{th}) can be expressed below with respect to V_{FB}.

$$V_{th} = V_{FB} + 2\Phi_F + \frac{qN_a x}{C_{ox}} \tag{9}$$

$$V_{FB} = \Phi_{ms} - \frac{Q_{ox}}{C_{ox}} \tag{10}$$

The flatband voltage(V_{FB}) is the sum of 1)differences in work functions of the semiconductor and the gate electrode Φ_{MS}, 2)the presence of charges in the oxide Q_{ox}. V_{FB} can be derived from the capacitance-voltage curve of a gate - gate oxide - Si capacitor. If the fixed oxide is negative, the V_{FB} will shift to the right. Otherwise, it will shift to the left(see Fig.2.4). Compared with SiO_2 high k dielectrics have a large interface defect density, causing a large V_{th}. If SiO_2 is replaced by Al_2O_3, the V_{th} is increased due to negative Q_{ox}. In order to keep the V_{th} unchanged, as seen in equation (9) and (10), we may decrease the dopant concentration (N_a).

2.6.3 Charge trapping

From the previous discussion, we have already known that the defect and interface charge density ($10^{11} - 10^{12} cm^{-2}$) of high-$k$ oxides are larger than SiO_2 ($2 \times 10^{10} cm^{-2}$). The flatband voltage and threshold are influenced by the amount of trapped charges. Normally, we use heat annealing to reduce the trapped charges in the fabrication. The annealing is carried out in mixed gas (N_2/H_2), or other containing nitrogen gases such as ammonia. It would be helpful to have a clear understanding for the origin of the trapped charges.
In fact, the trapped charges origin from intrinsic defects in the oxide and interface traps. The nature of the intrinsic defects in ionic oxides is different from those in SiO_2. They are oxygen vacancies, oxygen interstitials, or oxygen deficiency defects. Fig.2.6 shows $I_d - V_g$ curve for a nMOS transistor with the HfO_2 gate oxide. The hysteresis appears when the gate voltage sweeps up and down. This indicates that

the charge trapping is active and released. Specifically, the holes are trapped when the gate voltage sweeps positively, while the charges are released when the gate voltage sweeps negatively. Moreover, the identical curves for up and down show that no new defects are created. After annealing, the flatband voltage shift can be reduced to 7 mV. It is to note that the larger the flatband voltage shift, the more the trapping charges are.

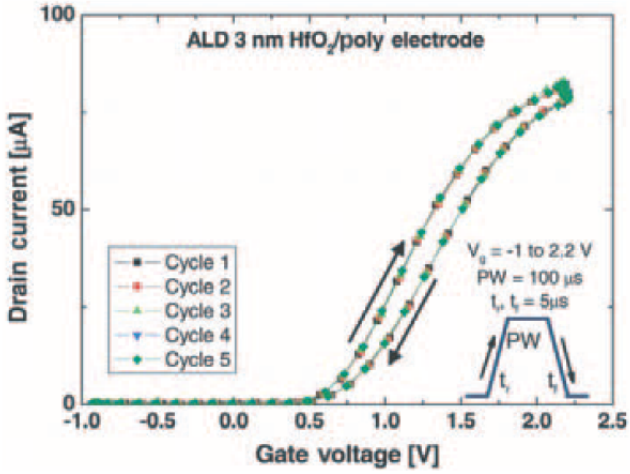


FIGURE 2.6: Electron trapping in HfO_2 gate oxide layer. The hysteresis between the up and down ramps shows the presence of sizable trapping. The identical curves for up and down show that no new defects are created[25]

Ratan.Kotipalli et al reported [33] that for the ALD Al_2O_3 with a thickness of 15 nm, the interface charge trap density (D_{it}) is about $10^{11}cm^{-2}$. This is acceptable compared to the value of SiO_2. Importantly, the D_{it} can be further reduced by introducing a thin layer of thermal SiO_2 between Al_2O_3 and silicon. This means that a field passivation can reduce the D_{it} in the MOS capacitor stack of $Al_2O_3/SiO_2/Si$.

2.7 Process compatibility

Beside the impact factors mentioned above, process compatibility, complexity, and cost should be considered for the SiO_2 replacement by high-k dielectrics. Physical vapor deposition (PVD), chemical vapor deposition (CVD), and atomic layer deposition (ALD) are common techniques in the dielectric deposition. It is possible to obtain different dielectric quality and properties form different technologies. Although PVD (such as magnetron sputtering), widely used in the semiconductor industry, can provide high deposition rates and preserve film stoichiometry, it generates extensive surface damage from high energy sputtered atoms, thereby creates interface traps. For CVD method, we should pay attention to reaction kinetics which controls the interface quality. In order to avoid unwanted impurities in the film and control interface quality to the same level as the SiO_2/silicon interface, a graded composition for dielectric materials is required. Therefore the process is complex.

ALD is very useful for ultra-thin dielectric growth since it allows for controlling the thickness and uniformity of the deposited films with atomic-level precision while avoiding physical damage of energized atoms to the surface. It also decreases the undesirable impurities such as Cl, H elements. Based on water and oxygen, ALD techniques are classified into thermal atomic layer deposition (TE-ALD) and plasma enhanced atomic layer deposition (PE-ALD). ALD has been recently used for Al_2O_3[27], HfO_2[31] and ZrO_2 deposition [28]-[30]. This layer-by-layer method is potential for growing crystalline (such as ZrO_2) in real manufacturing environment in the future. To compare the property and quality of high-k dielectrics (D_{it} and Q_f), we will choose ALD for growing different MOS capacitor stacks in this work.

2.8 Summary

This chapter has reviewed the various properties of new high-k dielectric materials for replacing SiO_2. The new oxide must satisfy following conditions as a gate oxide : (i) it has a significantly higher dielectric constant than amorphous SiO_2 (3.9) ; (ii) it is stable in contact with Si (capable of withstanding at 900°C annealing) ; (iii) it is compatible with gate materials (poly Si) without dopant penetration ; (iv) it has a bandgap high enough (4-5 eV) to provide sufficiently low gate leakage ; (v) it has a low interface charge density (D_{it}) and fixed charge (Q_f) ; (vi) it does not degrade the electrical properties of the Si channel (threshold voltage, mobility and so on) ; (vii) its process is compatible with CMOS technology. Among all the high-k materials discussed above, Al_2O_3 is a good candidate due to many favorable properties, including acceptable dielectric constant (9), thermodynamic stability on silicon under high temperatures, high band gap (8.8 eV). Compared with other high-k materials composed with rare metals, it is common and easy to get. The most important advantage is the negative fixed charges, preventing electrons tunneling. Moreover, it is amorphous and has less interface defects.

Chapitre 3

The fabrication of MOS capacitor stack

In the previous chapter, we have known the challenges faced by SiO_2, reviewed the properties of the potential high-k dielectrics, and discussed the possibility for replacing SiO_2 by Al_2O_3. This chapter describes the fabrication of the MOS capacitor stacks based on Al_2O_3. ALD is the main experiment tool used in the Al_2O_3 deposition. Section 3.1 presents the working principle of the ALD. In order to investigate the electrical quality of the Al_2O_3/Si interface, different MOS capacitor stacks are designed in Section 3.2. The fabrication process of the MOS capacitor stacks is provided in Section 3.3. Section 3.4 evaluates the thickness of the MOS capacitor stacks by spectroscopic ellipsometry.

3.1 The principle of fabrication devices

3.1.1 A principle of Atomic layer deposition (ALD)

The ALD is a variant of chemical vapor deposition (CVD) which is irreversible and saturating gas-solid reactions of at least two compounds, which are repeated in a cyclic manner. The ALD grows thin films atomic layer by layer so that it can well control the film thickness to sub nanometer. The ALD is cataloged into thermal ALD with water precursor (TE-ALD) and plasma ALD with oxygen plasma (PE-ALD). We use TE-ALD as an example to explain the working principle with the formation of Al2O3. Steps (1-6) below illustrates the TE-ALD reaction steps of Al2O3 as seen in Fig.3.1 and Fig.3.2 :

1. To introduce gas precursor TMA (Tri-methyl aluminum $Al(CH_3)_3$) ;
2. Methyl groups (CH_3) in TMA reacts with the hydroxyl groups (OH^-) on the surface of the substrate. This reaction forms one layer of Al atoms and liberates the by-product methane (CH_4). it is self-limiting ;
3. To remove the unreacted TEM and the by-product CH_4 by flowing inert gas (such as argon) over the surface
4. To introduce and adsorb precursor water (H_2O) to the surface
5. To remove the unreacted H_2O and CH_4 by flowing inert gas over the surface. One atom layer of Al_2O_3 is formed

6. To repeat the cycle described above, uniform thin layer of Al_2O_3 will be formed.

The working principle of the PE-ALD is the same as that of the TE-ALD except for replacing H_2O by oxygen radicals (see Fig.3.3).

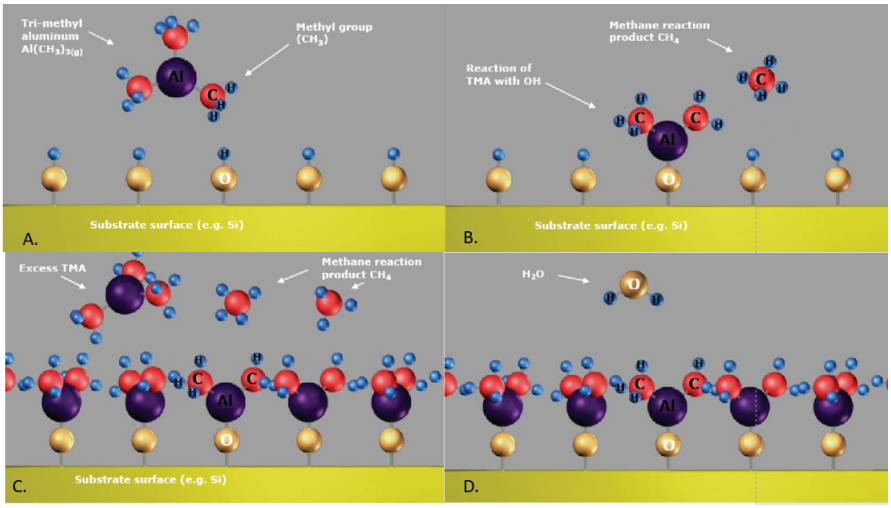


FIGURE 3.1: ALD deposition steps for Al_2O_3

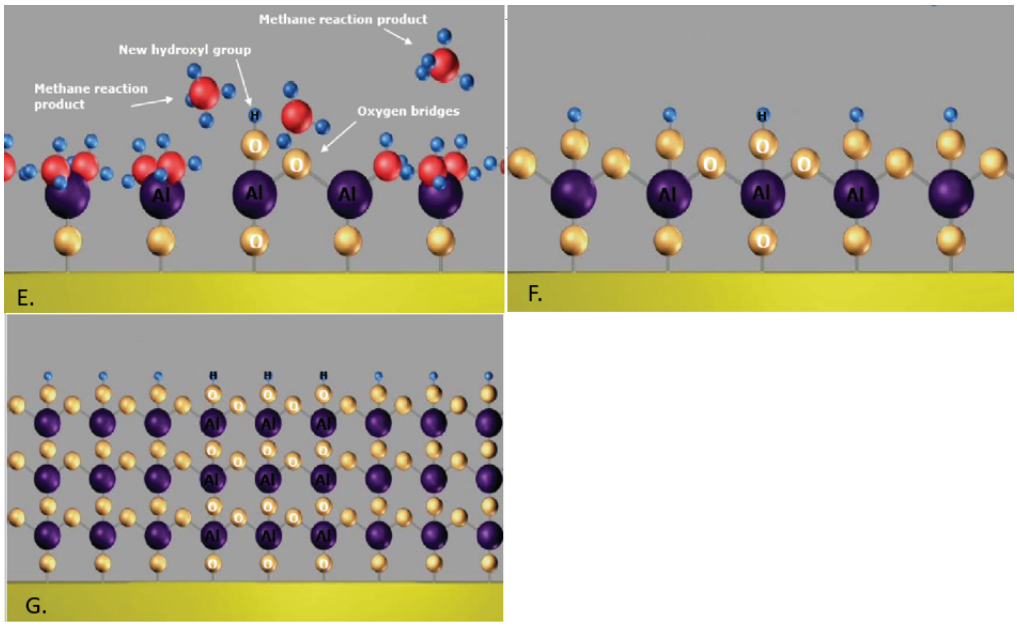


FIGURE 3.2: ALD deposition steps for Al_2O_3 [33]

3.1.2 A principle of ellipsometry

Ellipsometry (See Fig.4) is a non-destructive and non-contact technique by which the samples can be characterized without prepare. This sensitive measurement technique provides thin film thickness with angstrom resolution. Through an analysis of the state of polarization of the light which is reflected from the sample, the technique allows the accurate characterization of different properties including roughness, the

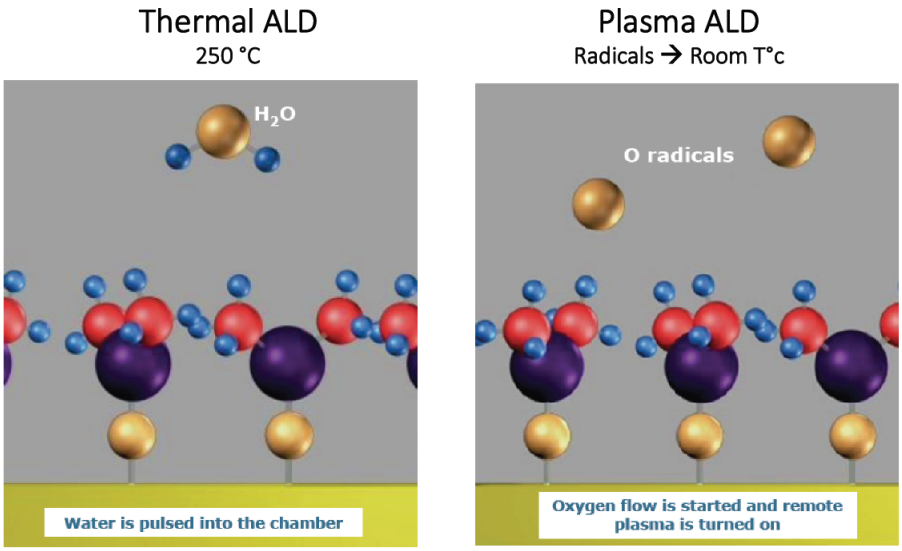


FIGURE 3.3: Thermal ALD and plasma ALD deposition steps for Al_2O_3[33]

layer thickness, optical constants, crystallinity, anisotropy and uniformity. Thickness determinations ranging from a few angstroms to tens of microns are possible for single layers or complex multilayer stacks. The general measurement includes four steps as seen in Fig.3.4.

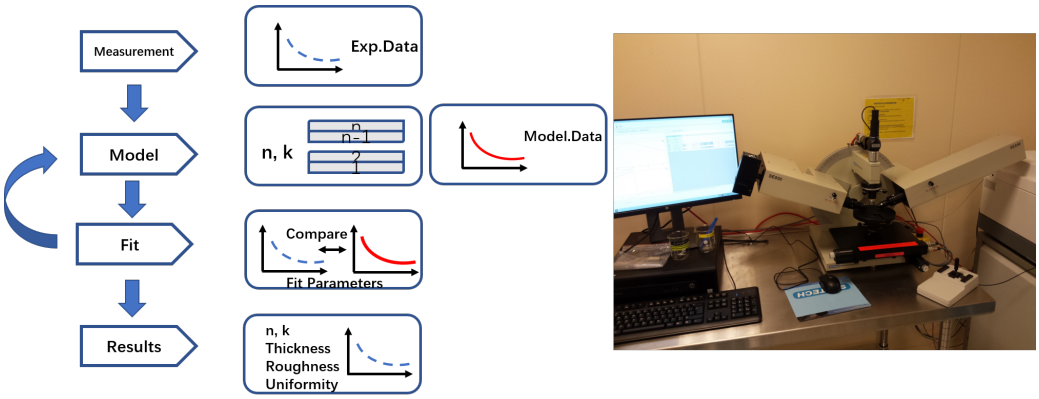


FIGURE 3.4: the characterization steps of ellipsometry[33]

3.2 Fabrication process design and experiments

3.2.1 Design of MOS capacitor stacks

Firstly, it is important to define the equivalent oxide thickness (EOT) for the MOS capacitor stack. When the MOS capacitor stack includes two dielectrics in series, the total capacitance of two dielectrics is :

$$\frac{1}{c_{tol}} = \frac{1}{c_1} + \frac{1}{c_2} \tag{3.1}$$

Here c_1 and c_2 are the capacitance of the two layers. If the MOS capacitor only includes one layer of high-k dielectric, the EOT is :

$$t_{eq} = \frac{k_{ox}}{k_{High-k}} t_{High-k} \tag{3.2}$$

If the MOS capacitor stack is composed of two dielectrics : top layer is high-k dielectric and the bottom layer is SiO_2. To combine equation (3.1) and (3.2), the EOT is given by

$$t_{eq} = t_{SiO_2} + \frac{k_{ox}}{k_{High-k}} t_{High-k} \tag{3.3}$$

Rewirte (3.3) as :

$$t_{High-k} = \frac{t_{eq} - t_{SiO_2}}{3.9} k_{High-k} \tag{3.4}$$

In this work, we design different MOS capacitor stacks based on Al_2O_3 dielectric. Table I summarizes all the parameters, including dielectric type, dielectrics thickness, and deposition method. For comparison, we also prepare two reference capacitors with HfO_2 and SiO_2.
Group 1 is a reference capacitor with 3-nm SiO_2 dielectric. In general, HfO_2 is also considered as a potential replacement for SiO_2 since its high-k value (25). However, Hf is a rare element so we chose abundant Al_2O_3 in this work. For comparison, we also prepare a MOS capacitor with a single layer of HfO_2 as reference sample (group 2). To obtain an equivalent capacitance density of the 3-nm-thick SiO_2, the physical thickness of HfO_2 is calculated to be 19 nm according to equation 2. Although group 3 and 4 have the same thickness of 7-nm Al_2O_3, their growth methods are different : the plasma ALD (PE-ALD) and thermal ALD (TE-ALD). These two groups is used to compare the quality of Al_2O_3 deposited by two kinds of ALD, including fixed oxide charges, interface trap density (D_{it}), gate leakage and so on. As mentioned in chapter 1, the typical D_{it} value in the interface of SiO_2/Si is $2 \times 10^{10} cm^{-2}$, while the best value for the interface of Al_2O_3/Si is about $10^{11} cm^{-2}$. To reduce the D_{it} value, a thin layer of SiO_2 is added between Al_2O_3 and the Si substrate. For this end, we design the Al_2O_3/SiO_2 stacks. The SiO_2 quality is very important for the stacks. To investigate the influence of SiO_2 quality on the D_{it}, the thin SiO_2 layers are grown by Koyo system (group 7-8) and deposited by PE-ALD (group 9-10). As well known, SiO_2 with a thickness of about 1-nm can naturally be grown on the Si substrate in air. So we design group 5-6 to check if the native SiO_2 can improve the D_{it} value. All the MOS capacitor stacks are listed in Fig.3.7 and the samples for the rate of ALD calibration are listed in Fig.3.8.

3.2.2 Experimental details

Experiment and measurement set up

Fiji F200 ALD system (Fig.3.5) is employed in our experiments. $Al_2(CH_3)_6$ (TMA), $[(CH_3)_2N]_4Hf$ (TDMA-Hf), and $SiH(N(CH_3)_2)_3$ (TDMAS) are used as precursors for Al_2O_3, HfO_2, and SiO_2, respectively. Koyo system is used to thermal oxide Si to form thin SiO_2. All the dielectric thicknesses are measured by using fixed-angle (70°) spectroscopic ellipsometry (300-900 nm).

The electrical properties of the MOS capacitor stacks are measured by MDC 802C Mercury Probe (Fig.3.6) and Agilent HP 4284A Precision LCR Meter (20 Hz to

1 MHz). It is important to note that the Mercury Probe eliminates the metalization step for the fabrication of the MOS capacitors. It employs a mercury dot with a diameter of 760 μm as the metal electrode. In our work, the p-type Si substrate is used as the bottom electrode and the mercury dot acts as top electrode for the MOS capacitor stacks.

FIGURE 3.5: Fiji F200 Atomic Layer Deposition Machine

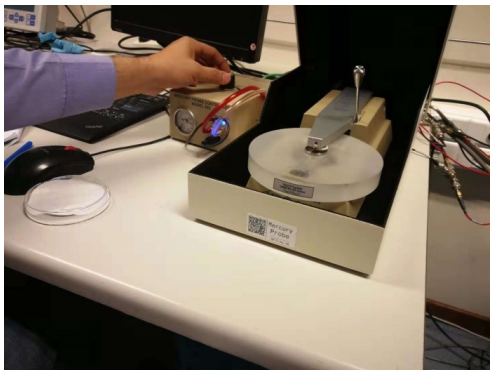


FIGURE 3.6: MDC 802C Mercury Probe

ALD recipes

The recipe of PE-ALD Al_2O_3 at 250°C the pulse duration for TMA and oxygen plasma (300 watts) are respectively set at 0.06 s and 20 s for each cycle. The deposition rate is 1.09 Å/cycle. To remove the unreacted TMA and the product CH_4, 200-sccm argon flows for 5 s.
The recipe of TE-ALD Al_2O_3 at 250°C : the pulse duration for TMA and H_2O are respectively set at 0.06 s and 0.06 s for each cycle. The deposition rate is 1 Å/cycle. To remove the unreacted TMA and the product CH_4, 200-sccm argon flows for 10 s.
The recipe of PE-ALD HfO_2 at 200°C : the pulse duration for TDMA-Hf and

oxygen plasma (300 watts) are respectively set at 0.25 and 20 s for each cycle. The deposition rate is 1.1 Å/cycle. To remove the unreacted TDMA-Hf and the product $(CH_3)_2NH$, 200-sccm argon flows for 5 s.
The recipe of PE-ALD SiO_2 at $200°C$: the pulse duration for TDMA-Si and oxygen plasma (300 watts) are respectively set at 0.25 and 20 s for each cycle. The deposition rate is 0.55 Å/cycle. To remove the unreacted TDMA-Si and the produce $HN(CH_3)_2$, 200-sccm argon is flow over 5s.

Fabrication process

3-inch Si substrates (100, p-type, 10 $\Omega \times cm$) are cleaned in the standard clean solution (H_2SO_4/H_2O_2 5 :1) (10 min), de-ionized (DI) water rinse (10 min), 20s etch in HF (2%) to produce $Si-H$ surfaces and then immediately put into the ALD machine or Koyo system for growing high-k dielectrics or thermal SiO_2. After cleaning :
For group 1 in table I, the Si substrate is put into Koyo system for the thermal SiO_2 growth at $800°C$ for 30 minutes.
For group 2-4, the Si substrates are put into the ALD machine. According to the different recipes, the high-k dielectrics (Al_2O_3 and HfO_2) are deposited on the Si substrates. The number of the cycles is calculated by the designed thickness and deposition rates. For example, 7-nm TE-ALD Al_2O_3 needs 70 cycles since its deposition rate is 1 Å/cycle.
For group 5-6, to grow native oxide, we put Si substrates in air for 2 weeks after standard clean. The Si substrates are put into the ALD machine for growing TE-ALD and PE-ALD Al_2O_3.
For group 7-8, the Si substrates are put into Koyo system for the thermal SiO_2 at $800°C$, then immediately transferred to the ALD machine for growing Al_2O_3.
For group 9-10, the Si substrates are put into the ALD machine for PE-SiO_2 and then for PE-Al_2O_3 or TE-Al_2O_3 without breaking the vacuum.
To well control the dielectric thickness, we grow the thick dielectric layers for the ALD machine calibration. Table II lists the ALD deposition rates for Al_2O_3, HfO_2 and SiO_2. The values listed in the table I represent the mean of 16 measurement points over a 3-inch wafer.

Thickness distribution

In order to get a relatively precise thickness distribution, several important points should be noticed. When characterizing the thickness of wafers with ultra thin layers, using deep ultraviolet (DUV) light ranging from 240 nm to 930 nm rather than ultraviolet (UV) light is more precise for the measurement of ultra thin film. Besides, the choice of the number of points and the location of these points should represent the variation of wafer thickness and the quality of fabrication. 16 points distributed in 4 ×4 on the main region of 3-inch wafer are measured by ellipsometry (See Fig.3.9). With these points the contour plot can be made to evaluate the distribution of thickness on the wafer. Drawing contour lines of thickness involves map points of equal value. Map data are provided as discrete points with known X and Y coordinates as location. Z value represents the thickness of each point. Since contouring provides a method for converting spot information into continuous surfaces repre-

Sample N°	Dielectric stack	Calculated thickness	Approximated thickness
1	Thermal SiO2 (Koyo)	3 nm	3 nm
2	PE-ALD HfO2	19.2nm	19 nm
3	PE-ALD Al2O3	6.9nm	7 nm
4	TE-ALD Al2O3	6.9 nm	7 nm
5	Native SiO2 + PE-ALD Al2O3	1 + 4.6 nm	1 + 5 nm
6	Native SiO2 + TE-ALD Al2O3	1 + 4.6 nm	1 + 5 nm
7	Thermal SiO2 + PE-ALD Al2O3	2 + 2.3 nm	2 + 3 nm
8	Thermal SiO2 + TE-ALD Al2O3	2 + 2.3 nm	2 + 3 nm
9	ALD SiO2 + PE-ALD Al2O3	2 + 2.3 nm	2 + 3 nm
10	ALD SiO2 + TE-ALD Al2O3	2 + 2.3 nm	2 + 3 nm

FIGURE 3.7: Samples with different composition

Sample N°	Dielectric stack	Thickness	Deposit rate of ALD
1	TE-ALD Al_2O_3	30 nm	1.0 Å / cycle
2	PE-ALD HfO_2	37 nm	1.1 Å / cycle
3	PE-ALD Al_2O_3	32.7 nm	1.09 Å / cycle
4	PE-ALD SiO_2	26.55	0.55 Å / cycle

FIGURE 3.8: Calibration for the deposition rate of ALD using three materials

sented with contour lines, the relatively precise distribution of thickness is produced by more data. Using the scattered data interpolation can approximate the thickness of unknown region without characterization. A good quality of wafer has a Gaussian distribution of thickness. In the other word, a random distributed thickness with smaller surface variation results in good thickness uniformity and less defects such as cracks. In Fig.**??** to Fig.3.17 (right), the Gaussian process is applied to 16 measured data. The function of Gaussian process is below :

$$y = y_0 + Ae^{-\frac{(x-\mu)^2}{2\sigma^2}} \tag{3.5}$$

where μ is the mean of thickness and σ is the standard deviation. Both parameters describe the average thickness and surface variation respectively. All of the samples have been analyzed by Gaussian model and the data are collected in Fig.3.18.

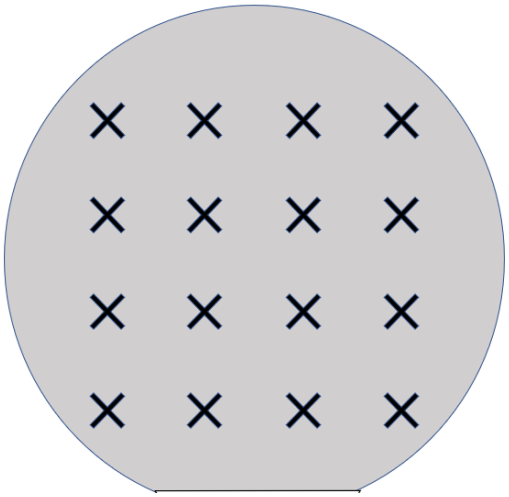


FIGURE 3.9: 4 × 4 points measured by ellipsometry on the wafer

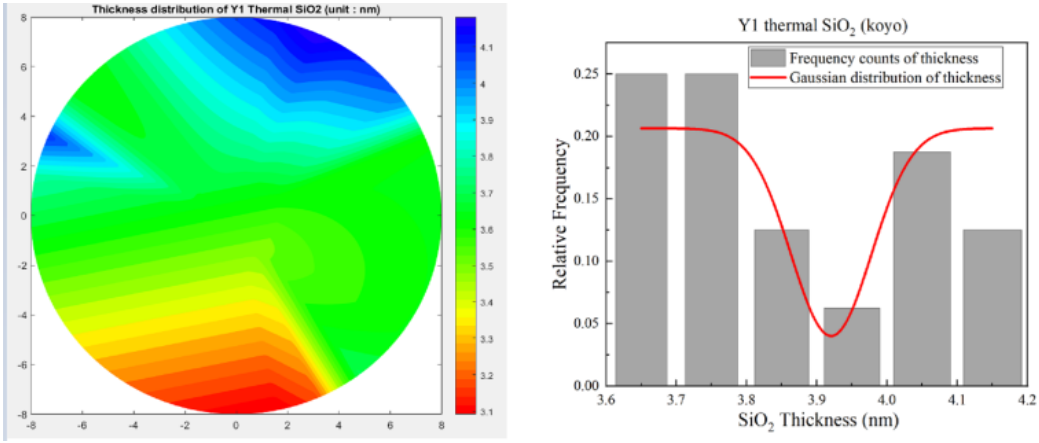


FIGURE 3.10: The thickness distribution of thermal SiO_2 (koyo) (left) and the Gaussian distribution (right)

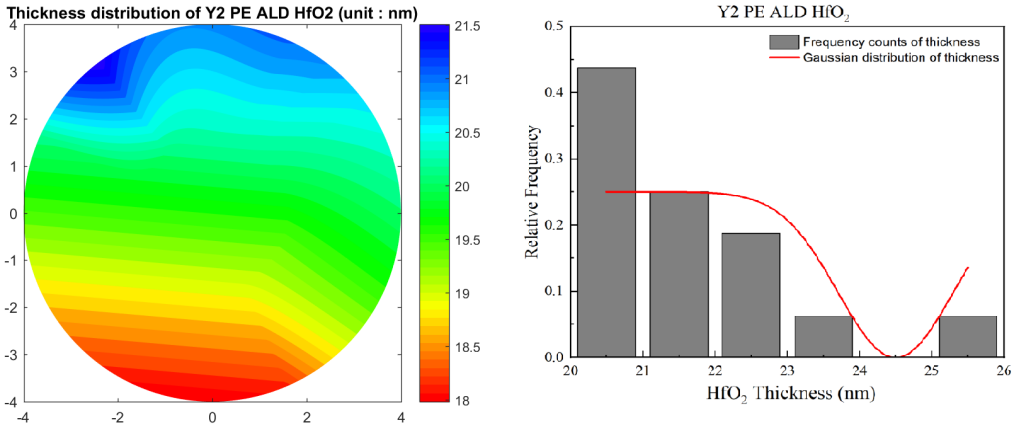


FIGURE 3.11: The thickness distribution of PE ALD HfO_2 (left) and the Gaussian distribution

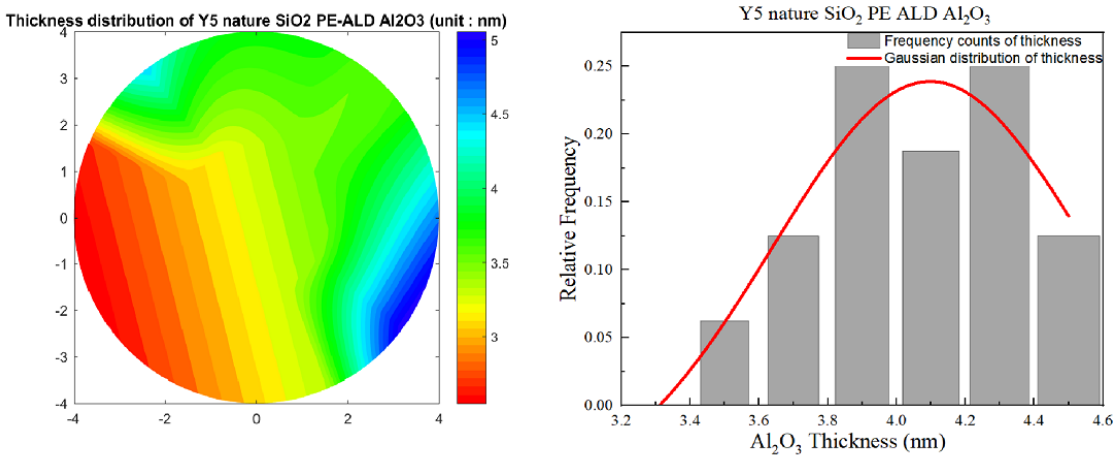


FIGURE 3.12: The thickness distribution of nature SiO_2 PE-ALD Al_2O_3 stack (left) and the Gaussian distribution (right)

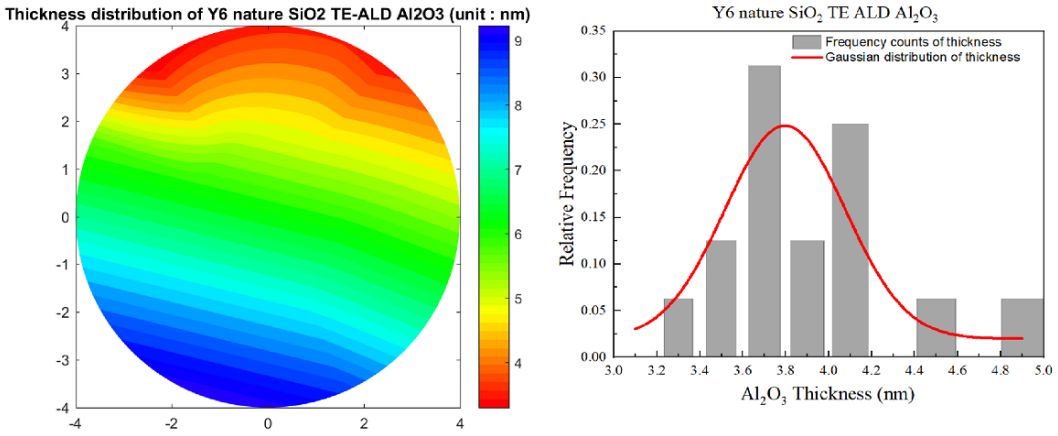


FIGURE 3.13: The thickness distribution of nature SiO_2 TE-ALD Al_2O_3 stack (left) and the Gaussian distribution (right)

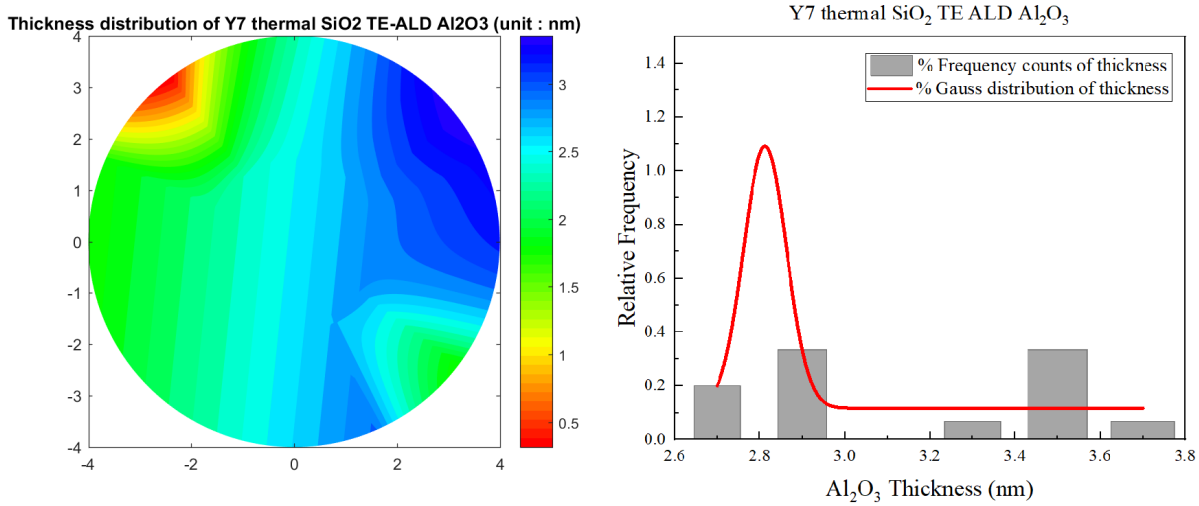


FIGURE 3.14: The thickness distribution of thermal SiO_2 TE-ALD Al_2O_3 stack (left) and the Gaussian distribution (right)

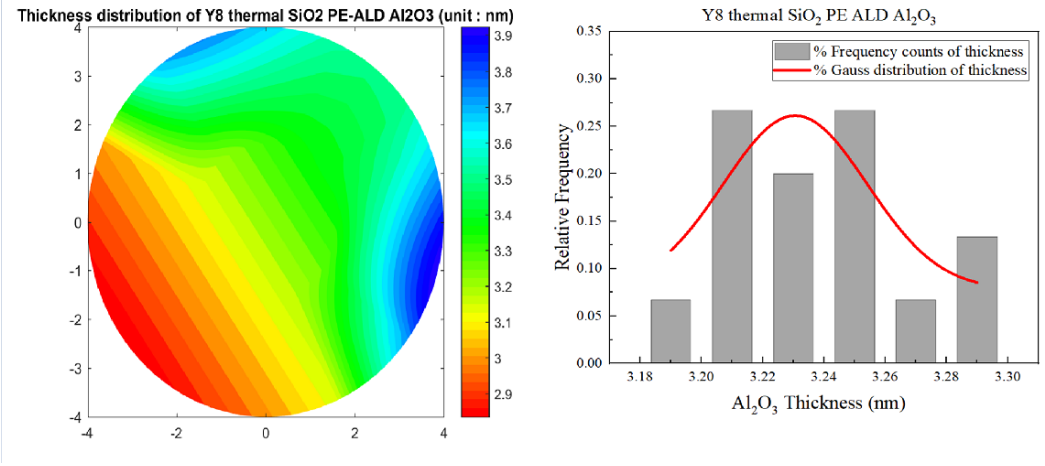


FIGURE 3.15: The thickness distribution of thermal SiO_2 PE-ALD Al_2O_3 stack (left) and the Gaussian distribution (right)

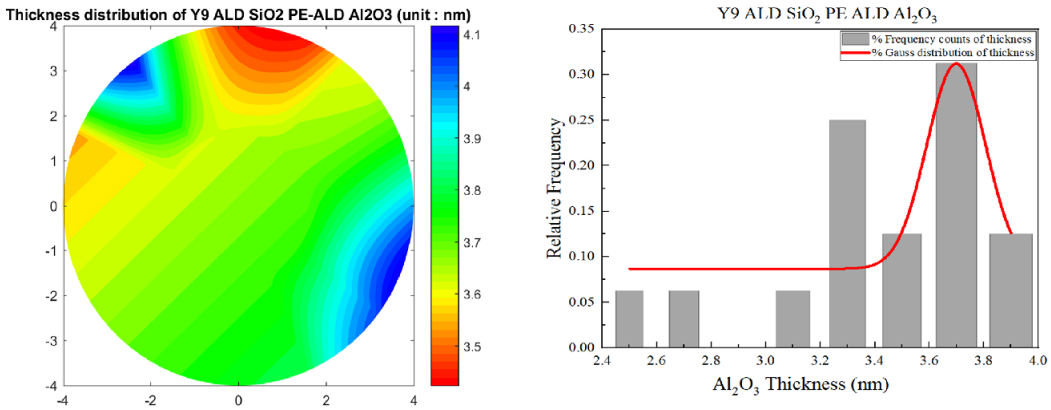


FIGURE 3.16: The thickness distribution of ALD SiO_2 PE-ALD Al_2O_3 stack (left) and the Gaussian distribution (right)

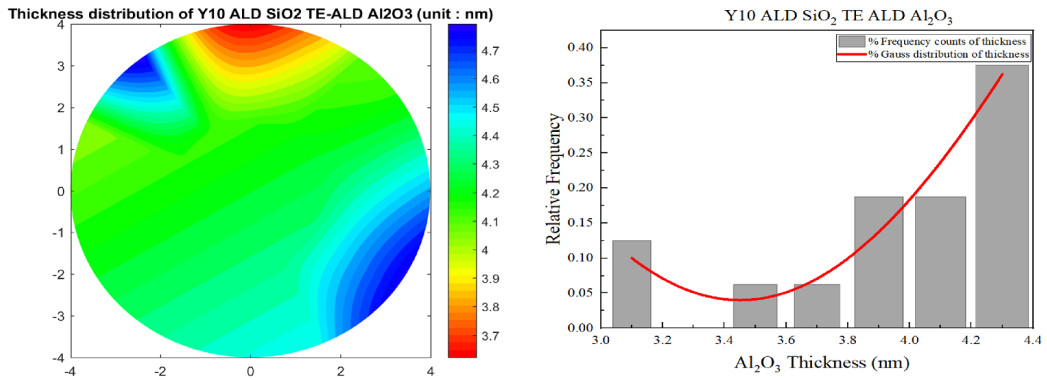


FIGURE 3.17: The thickness distribution of ALD SiO_2 TE-ALD Al_2O_3 stack (left) and the Gaussian distribution (right)

Sample N°	Dielectric stack	Mean μ	Standard deviation σ	Expected thickness
1	Thermal SiO2 (Koyo)	3.9 nm	0.057	3 nm
2	PE-ALD HfO2	24.5 nm	0.798	19 nm
3	PE-ALD Al2O3 (annealing mistakes)	-	-	7 nm
4	TE-ALD Al2O3 (annealing mistakes)	-	-	7 nm
5	Native SiO2 + PE-ALD Al2O3	1.63 + 4.097 nm	0.457	1 + 5 nm
6	Native SiO2 + TE-ALD Al2O3	1.63 + 3.797 nm	0.280	1 + 5 nm
7	Thermal SiO2 + PE-ALD Al2O3	2 .5+ 2.812 nm	0.101	2 + 3 nm
8	Thermal SiO2 + TE-ALD Al2O3	2 .5+ 3.231 nm	0.047	2 + 3 nm
9	ALD SiO2 + PE-ALD Al2O3	2 .5+ 3.70 nm	0.215	2 + 3 nm
10	ALD SiO2 + TE-ALD Al2O3	2 .5+ 3.45 nm	2.570	2 + 3 nm

FIGURE 3.18: The parameters of Gaussian process and expected thickness

Chapitre 4

Measurement and characterization

Capacitance-voltage (C-V) and current-voltage (I-V) measurements are two fundamental characterization techniques for detecting the gate dielectric quality of MOS devices, such as interface charges and doping concentration profile . Inaccurate characterizations of capacitance and conductance will lead to errors in the analysis of electrical quality. The ideal C-V measurement will present the same C-V curves with different measurement frequencies. When the capacitance in accumulation region appears strongly depends on the measurement frequencies, the measured C-V characteristics cannot be directly analyzed. MOS capacitance value in accumulation region is important for some electrical parameters, such as dielectric constant and flat voltage. Thus, accurate extraction of accumulation capacitance is inevitable. Typical three-element model and four-element model can be used for capacitance correction. However, the frequency dispersion still exists for ultra thin insulator MOS capacitors due to the stack of two dielectric layers (Al_2O_3 and SiO_2). To extract the intrinsic gate capacitance and conductance from the measured non-idea MOS C-V and G-V date, a six-element reconstruction model is used here to eliminate the effects of series resistance and oxide leakage and correct for the measured capacitance and conductance.
This chapter is the core of this thesis. It is divided into four sections : Section 4.1 reviews C-V characteristics of MOS capacitor. Section 4.2 describes the measurement setup and conditions of C-V and I-V characterization. In section 4.3 we use two kinds of models to analyze the measured capacitance and conductance. Section 4.4 presents the results of the electrical qualities for different samples.

4.1 C-V characteristics of MOS capacitor

4.1.1 Accumulation region

For a p-type MOS capacitor, the accumulation region of the C-V curve is observed when negative voltages are applied to the gate and the silicon substrate is grounded. The MOS capacitor behaves like a parallel-plate capacitor : two electrodes are the gate and the silicon substrate with back contact, oxide as insulator between electrodes. In our work, the gate is mercury probe and the silicon substrate with back contact respectively,and the insulator between both electrodes is the oxide Al_2O_3 or the related stacks. Hereafter, we call insulator them as oxide. The negative polarity causes majority carriers (holes) to be attracted toward the gate. If the oxide

is perfect without leakage current, these holes accumulate at the substrate-to-oxide interface to form accumulation layer.
No matter what types of small ac signal is applied to MOS capacitor, the capacitance measured in the strong accumulation region (where the voltage is negative enough) is essentially constant and the C-V curve slope is flat in Fig.4.1. Besides, the capacitance in accumulation will not change with frequencies. The oxide thickness can be extracted from the oxide capacitance (C_{ox}) in the accumulation region, specifically,$C = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$. Here E_{ox} is oxide dielectric constant. However, the series resistance or other reasons will cause the frequency dispersion when high frequency ac signal is applied. In these cases, the measured capacitances differ from the true oxide capacitance.

4.1.2 Depletion region

When the gate voltage increases from negative value to positive value, holes near the silicon surface are repelled by the gate. A carrier-depleted region forms and a negative charge appears beneath the gate oxide, creating an insulator. As a result, there are two capacitances in series : the oxide capacitance and the depletion capacitance. As the gate voltage becomes more positive, the depletion zone penertrates deeply into the silicon. The increased depletion depth x_d leads to the decrease in total measured capacitance as seen in Fig.4.1. It is noting that the depletion depth is the depth in which holes are repelled. When the depletion region reaches the maximum depth when the gate-voltage increases do not deplete the silicon substrate, the measured capacitance reaches the minimum capacitance. After solving the Poisson's equation, the depletion depth can be expressed as a function of the surface potential [35] :

$$x_d = \sqrt{\frac{2\epsilon_{si}\phi_s}{qN_a}} \tag{4.1}$$

The total measured capacitance can be written as a function of gate voltage[35] :

$$C = \frac{C_{ox}}{\sqrt{1 + \frac{2{C_{ox}}^2 V_G}{qN_a\epsilon_{si}}}} \tag{4.2}$$

The doping concentration can be calculated from equation (4.2).

4.1.3 Inversion region

For a p-type MOS capacitor, the positive gate voltage generates electron-hole pairs and attracts electrons (minority carriers) toward the gate. Since the gate oxide is insulator, these minority carriers accumulate at the substrate-to-oxide interface. The accumulated minority-carrier layer is called the inversion layer. In this case, the measured capacitance is the oxide capacitance in series with the depletion capacitance in the maximum depletion depth. The capacitance that is measured by LCR meter is the oxide capacitance in series with maximum depletion capacitance, referred to as the minimum capacitance. With a low-frequency ac signal (quasi-static curve in Fig.4.1) in inversion region, when the gate voltage is further increased, the measured capacitance is again equal to C_{ox}. If the measurement repeats with

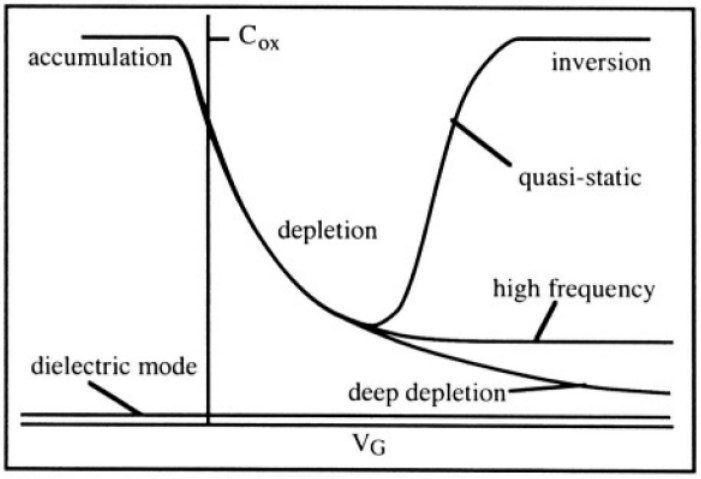


FIGURE 4.1: C-V curves of a MOS capacitor on a P-type substrate[35]

a higher frequency signal (1 MHz typically), thermal generation cannot create minority carriers fast enough to support a variation of charge in the inversion layer. In this case, the capacitance of the MOS capacitor keeps the minimum value, as same as in the maximum depletion depth. It is to say if the delay time between each point of gate voltage is too short to generate minority carriers. Therefore, no inversion layer forms when gate voltage swept fast. But charge neutrality must be satisfied by ionized donors alone, the depletion layer depth becomes larger than in thermal equilibrium, and the capacitance decreases below its thermal equilibrium saturation value. This non-equilibrium condition is called deep depletion. If a very high-frequency ac signal is used, even majority carriers have no time to react with gate voltage variation. In this case, the whole sample behaves as a dielectric (dielectric mode of operation in Fig.4.1).
Therefore, the portions of the C-V curve in accumulation and depletion are identical (except dielectric mode) in the different frequency measurements while the inversion part of the C-V curve is different.

4.2 Measurement setup and conditions of C-V

4.2.1 Measurement setup

The capacitance-voltage measurements are carried out by means of a HP484A LCR meter and a mercury probe station as a temporary contact either to the sample bottom or to the top as seen in Fig.4.2. The use of mercury probe avoids the deposition of metal electrodes on the wafer, which simplifies the process of the MOS capacitors. The diameter of the mercury probe is 907 μm and the contact area is sufficiently well defined for profile measurement. The mercury probe station allows lateral capacitance profiles by continuously dragging the wafer on the probe station. The mercury contact does not damage the wafer nor leave mercury on the surface. The wafer surface should be treated before the Hg contacts the surface for reproducible measurements.
HP 4284A LCR meter can be used for evaluating LCR components, materials, and semiconductor devices over a wide range of frequencies (1kHz to 1MHz). The two

modes series connection Cs-Rs and parallel connection $C_p - G_p$ were used to measure the C-V curves.

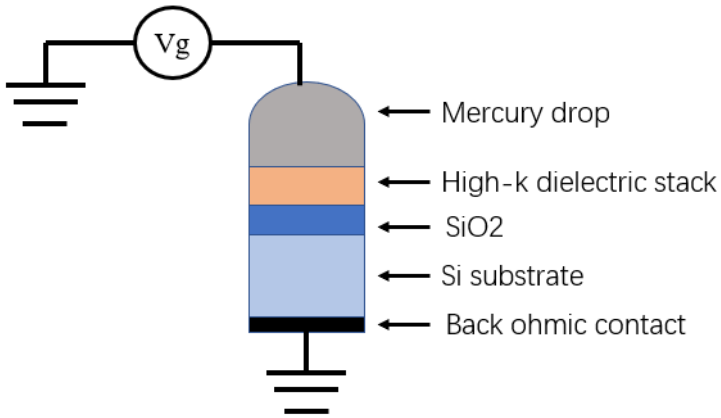


FIGURE 4.2: Schematic representation of the mercury probe measuring MOS stack capacitor : mercury drop as electrode, the dielectric stack (high-k dielectric and SiO_2) and Si substrate.

4.2.2 Measurement conditions

C-V measurements were performed for all the samples. The total capacitance C_m was measured as a function of the gate voltage V_G in the parallel C_p-G_p model with a HP 4284A LCR meter. The bias was swept from negative to positive values with a step of 20 mV. The ac signal level was set at 30 mV for frequencies from 1 kHz up to 1 MHz. In order to obtain the precise and reasonable measurement results, the following factors are important. (i) the measurements should be performed under equilibrium conditions ; (ii) the series resistance should be compensated ; and (iii) the parasitic capacitance should be considered.

— Measuring under equilibrium conditions
The equilibrium conditions are referred to that after the MOS capacitor is fully charged, one starts to record the data from C-V measurement. To reach the equilibrium conditions, sufficient hold time and delay time are required. Hold time is defined as the wait time before starting the C-V sweep at the first bias voltage, while delay time is the time before starting the capacitance measurement at each C-V sweep step. Besides, an initial voltage can be used to charge the MOS capacitor for reaching the equilibrium conditions. When the voltage is swept up and down, a hysteresis characteristics appears in C-V curves, namely the C-V curves is different when the voltage is swept from positive to negative and from negative to positive directions. Sufficient hold time and delay time are helpful to minimize the hysteresis. One method to find the sufficient hold time and delay time is to generate a pair of C-V curves from two directions with the change of hold time and delay time : one C-V curve from inversion to accumulation and another C-V curve from accumulation to inversion until the two curves look the same for both sweep directions. When the C-V measurement starts from accumulation to inversion or opposite direction, the effects of hold time and delay time are relatively subtle

compared with inversion region. In the inversion region, if the sweep is too fast (the delay time is small) the MOS capacitor has no time to generate minority carriers to form the inversion layer. From negative to positive gate voltage, in the non-equilibrium state the MOS capacitor becomes deep depleted. The measured capacitance value is below the equilibrium minimum value. In Fig.4.3 the dotted line shows the deep depletion. From positive to negative voltage, if non-equilibrium occurs the capacitance in the inversion region is higher than the equilibrium value in Fig.4.3. Performing a C-V curve from inversion to accumulation is faster and controllable than opposite direction from accumulation to inversion.
If it is necessary, a short light can be applied to help the samples to generate minority carriers before sweep starts. The measurement should be performed in the darkness since the silicon is sensitive to light.

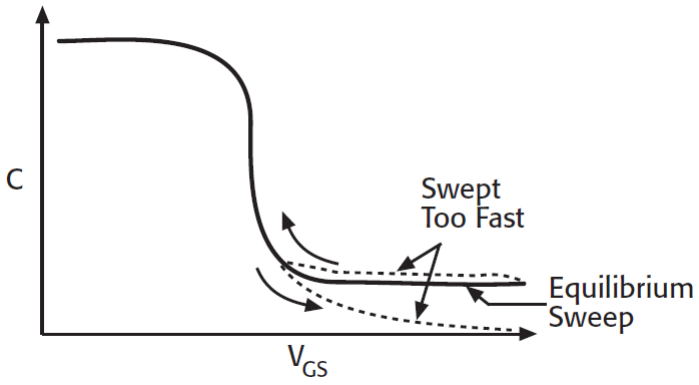


FIGURE 4.3: Effect of non-equilibrium state on C-V curves from two directions in p-type substrate[36]

— Compensating the series resistance
The maximum capacitances in accumulation region are not constant for different measurement frequencies. a surprising variation appears and the capacitances are not constant. It is found that the capacitance in accumulation region increases consistently with decreasing frequency. This phenomenon is due to the series resistances coming from substrate or dielectric leakage. The extraction of series resistance does not be considered in a simple two-element (series or parallel) model in the HF-CV analyzer. However, depending on the structure of MOS capacitor the different reconstruction models are required to calculate and remove the series resistances such as three-element (C-G-rs) model in Fig.4.4.

— considering parasitic capacitance
In our work, the mercury probe station and LCR meter are used to measure the C-V curves of the MOS capacitor. The parasitic capacitance from the interconnect cables of both instruments may be added into the measurement results. This may induce the frequency dispersion of the capacitance. To evaluate the influence of both instruments, we use a dissipation factor (D) to investigate the accuracy of the measurement. The formula $0.1 \times \sqrt{1+D^2}$ and $D = \frac{G_m}{2\pi f C_m}$ can be used to approximate the instrument error (%). If the instrument error is less than 0.5% for all the frequencies, this indicates that the frequency dispersion of capacitance is not due to instrument error. In our

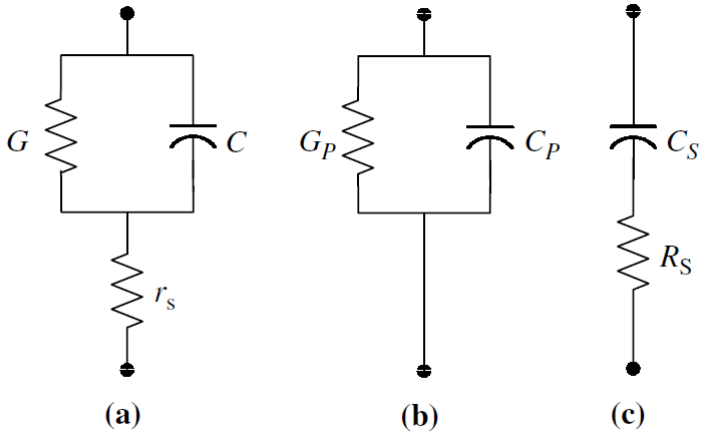


FIGURE 4.4: (a)Actual circuit of MOS capacitor stack, (b) parallel equivalent circuit, and (c) series equivalent circuit

case, the maximum error % equaling 0.204 % is less than 0.5 %. Therefore, the frequency dispersion of measured capacitance is not due to instrument error.

4.3 C-V and I-V characterization

4.3.1 I-V characterization

Using B1500 with mercury probe station can get I-V curves at three different points on MOS capacitor with thermal SiO_2 TE-ALD Al_2O_3 shows that the leakage current of this sample is less than 4.5 $\times 10^{-11}$ A as seen in Fig.4.5. This illustrates this kind of MOS capacitor is not leaky, which satisfies our expectation and make sense to continue C-V measurement.

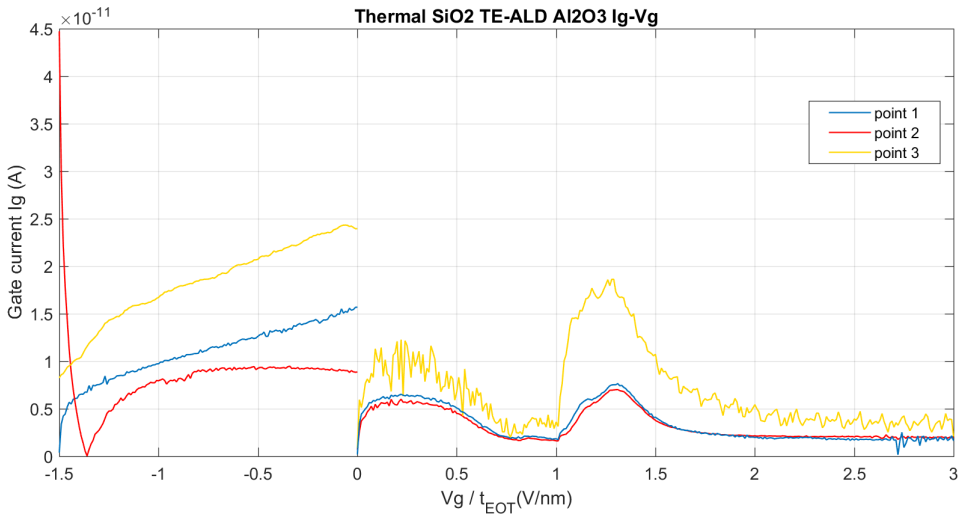


FIGURE 4.5: I-V measurement of MOS capacitor with thermal SiO_2 TE-ALD Al_2O_3 at three different points

4.3.2 Flatband Voltage

The flatband voltage (V_{FB}) is determined by the metal-semiconductor work function difference ϕ_{MS} and the various oxide charges through the relation [37]

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{Q_{it}(\phi_s)}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x}{t_{ox}} \rho_m(x) dx - \frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x}{t_{ox}} \rho_{ot}(x) dx \quad (4.3)$$

where $\rho(x)$ = oxide charge per unit volume. The fixed charge Q_f is considered to be at the interface of oxide. Q_{it} is represented as $Q_{it}(\phi_s)$ as the occupancy of the interface trapped charge depends on the surface potential. Mobile and oxide charges maybe distribute through the oxide. However, equation (4.3) for determining V_{FB} does not always have solution due to various unknowns. Another way to determine V_{FB} is to plot $(1/C_{HF})^2$ or $(1/C_{HF}/C_{ox})^2$ versus V_G as shown in Fig.4.8. After differentiating this curve, V_{FB} is obtained to be 1V at the maximum slope of the left flank of the differentiated curve as seen in Fig.4.6 and Fig.4.7.

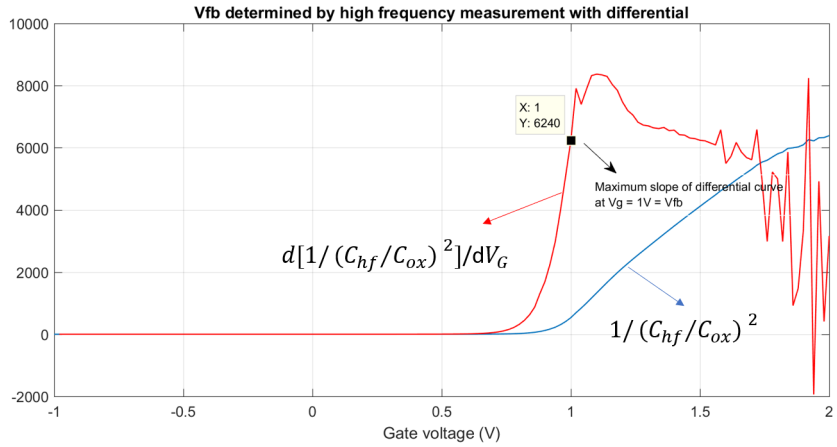


FIGURE 4.6: The flatband voltage determined by the differential

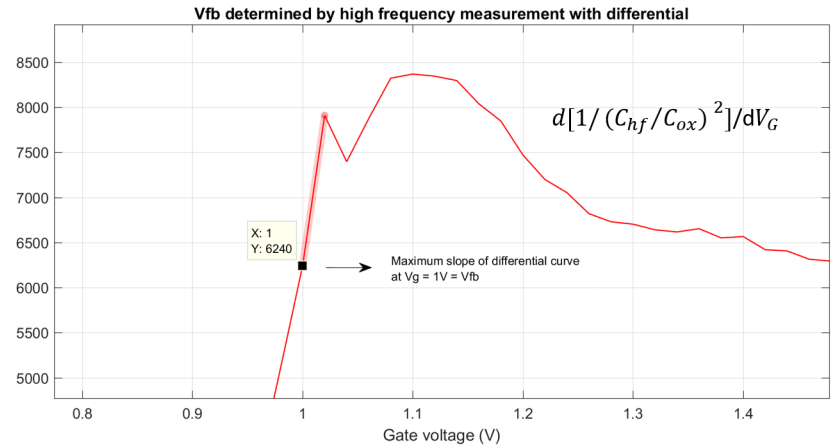


FIGURE 4.7: Zoom in : The flatband voltage determined by the differential

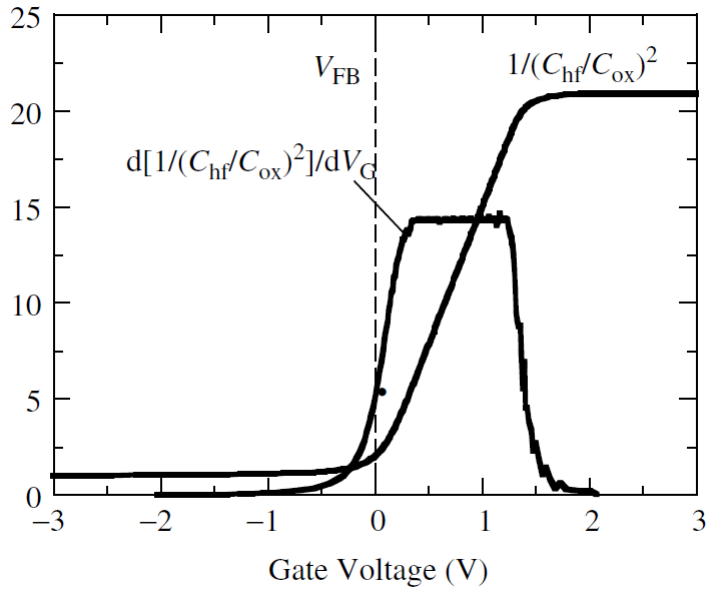


FIGURE 4.8: Deterimine V_{FB} from the high frequency C-V measurement with differential[37]

4.3.3 Fixed Charge

Q_f is related to the flatband voltage by equation [35]

$$Q_f = \frac{(\phi_{MS} - V_{FB})C_{ox}}{q} \tag{4.4}$$

where ϕ_{MS} is the metal-semiconductor work function difference between mercury and silicon and q is the amount of charge approximately [35] 1.6×10^{-19} C.

$$\phi_{MS} = \phi_M - \phi_S \tag{4.5}$$

From equation (4.5), we can calculate the ϕ_{MS} = -0.435 V. From equation (4.4), we can obtain the negative oxide charge Q_f = -4.04 $\times10^{10} cm^{-2}$ based on the positive flatband voltage V_{FB} = + 1 V and the oxide capacitance C_{ox} = 4.5 $\times10^{-9} F/cm^2$ calculated from experiments .

4.3.4 Interface trapped charge

Interface trapped charge, known as interface traps or states, are attributed to dangling bonds at the semiconductor/insulator interface. To determine the density of interface traps (D_{it}), the most sensitive method is the conductance method, in which the equivalent parallel conductance G_p of MOS capacitor is measured as a function of voltage under different frequencies. It is worth noting that the capacitance method is difficult and complicated since the measured capacitance includes several capacitances : oxide capacitance, depletion layer capacitance, and interface state capacitance.
The conductance method is fundamental to understand interface traps. In depletion region, as minority carrier density is very low, the interface trap occupancy changes mainly by capture and emission of majority carriers (holes in p-type and electrons in

n-type) produced by variation of gate voltage. The interface trap levels are detected by the loss resulting from changes in their occupancy. A small ac voltage applied to the gate of MOS capacitor moves the band edges toward or away from the Fermi level. Majority carriers are captured or emitted, changing occupancy of interface trap levels in a small energy gap centered around the Fermi level. An energy loss, observed at all frequencies except the very lowest frequency or very high frequency, is caused by the capture and emission of majority carriers. This energy loss is measured as an equivalent parallel conductance G_p. An approximation expression giving the interface trap density in terms of the measured maximum conductance is [37]

$$D_{it} \approx \frac{2.5}{qA}(\frac{G_p}{w})_{max} \tag{4.6}$$

where $w = 2\pi f$, $q = 1.6 \times 10{-}19$ and $A = 0.005\ cm^2$. According to the peak of G_c/w as a function of V_g, we can calculate the D_{it} equal $7.76 \times 10^{10}\ cm^{-2}eV^{-1}$ which is less than $10^{11}\ cm^{-2}eV^{-1}$.

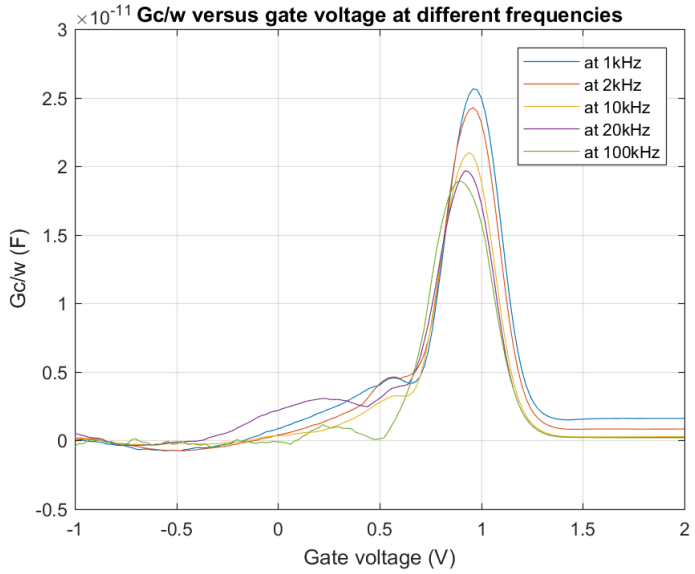


FIGURE 4.9: G_c/w versus voltage gate to investigate the interface trap density

4.3.5 Reconstruction models of extract electrical parameters

Dissipation factor D

LCR meter has various modes for C-V measurement. In the thesis, parallel and series connection measurements will be used as shown in Fig.4.10. The admittance Y_p of the parallel circuit and the impedance Z_s of the series circuit are

$$Y_p = G_p + jwC_p \tag{4.7}$$
$$Z_s = R_s + 1/jwC_s \tag{4.8}$$

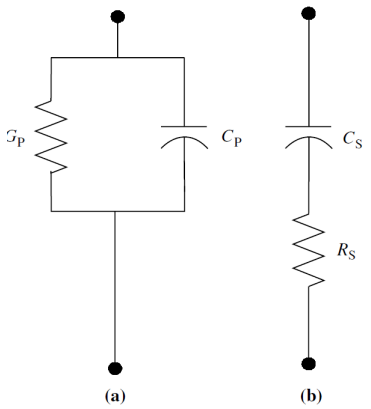


FIGURE 4.10: (a) Parallel and (b) series connection modes

where $w = 2\pi f$. Here two circuits can be converted to each other. Equating these two expression as $Y_p = 1/Z_p$ gives

$$C_p = \frac{1}{1 + {D_s}^2} C_s \tag{4.9}$$

$$G_p = \frac{{D_s}^2}{1 + {D_s}^2} \frac{1}{R_s} \tag{4.10}$$

with the dissipation factor D_s :

$$D_s = wC_sR_s \tag{4.11}$$

The same method is used to calculate :

$$C_s = 1 + {D_p}^2 C_p \tag{4.12}$$

$$G_p = \frac{{D_p}^2}{1 + {D_p}^2} \frac{1}{G_p} \tag{4.13}$$

with the dissipation factor D_p

$$D_p = \frac{G_p}{wC_p} \tag{4.14}$$

For an ideal capacitor, there is no conductance or resistance $G_p = 0$ and $R_s = 0$, resulting in $C_s = C_p$. However, the material of capacitor is not perfect and has some degree of leakage so $G_p \neq 0$ and $R_s \neq 0$. The instrument approximate error for C-V measurement is given by $\%error = 0.1 \times \sqrt{1 + D^2}$ mentioned in prvious subsection. It is important to evaluate the influence of the connections from the instrument on frequency dispersion before the data analysis with reconstruction models.

Three-element circuit model

The normal model to analyze the series resistance is three-element circuit model in Fig.4.4(a). The admittance Y for (a) is

$$Y(a) = \frac{1}{Z(a)} = \frac{1}{r_s + 1/(G + jwC)} = \frac{G + jwC}{1 + r_s(G + jwC)} \tag{4.15}$$

$$= \frac{(G + jwC)(1 + r_sG - jwC)}{(1 + r_sG + jwr_sC)(1 + r_sG - jwr_sC)} \tag{4.16}$$

where Z is the impedance. $Y(a)$ can be written as

$$Y(a) = \frac{G + r_s G^2 + r_s (wC)^2}{(1 + r_s G)^2 + (w r_s C)^2} + \frac{jwC}{(1 + r_s G)^2 + (w r_s C)^2} \tag{4.17}$$

The admittance for Fig.4.4(b) is simply written as

$$Y(b) = G_p + jwC_p \tag{4.18}$$

Since (b) mode is the equivalent circuit of (a), the real and imaginary parts of (4.17) and (4.18) can be equated as

$$C_p = \frac{C}{(1 + r_s G)^2 + (w r_s C)^2} \tag{4.19}$$

$$G_p = \frac{G + r_s G^2 + r_s (wC)^2}{(1 + r_s G)^2 + (w r_s C)^2} \tag{4.20}$$

For (c) circuit in Fig.4.4, it is better to consider the impedances of both circuits. The impedance of (a) is

$$Z(a) = r_s + \frac{1}{G + jwC} = \frac{r_s (G^2 + (wC)^2) + G}{G^2 + (wC)^2} - \frac{jwC}{G^2 + (wC)^2} \tag{4.21}$$

and the impedance of (c) is

$$Z(c) = R_s + \frac{1}{jwC_s} = R_s - \frac{jwC_s}{(wC_s)^2} \tag{4.22}$$

Equating real and imaginary parts of (4.21) and (4.22) gives

$$C_s = C(1 + (G/wC)^2 \tag{4.23}$$

$$R_s = \frac{r_s (G^2 + (wC)^2) + G}{G^2 + (wC)^2} = r_s + \frac{G}{G^2 + (wC)^2} \tag{4.24}$$

To determine C from series connected measurements at two different frequencies, equation (4.23) can be written as

$$C = \frac{{w_2}^2 C_{s2} - {w_1}^2 C_{s1}}{{w_2}^2 - {w_1}^2} \tag{4.25}$$

where C_{s2} and C_{s1} are the measured capacitances in $C_s - R_s$ at frequencies w_1 and w_2 respectively (as seen in Fig.4.11 C-V measurement using $C_s - R_s$ mode at four frequencies). To get r_s, C in equation (4.24) should be calculated firstly by substituting measured C_s at two different frequencies in equation (4.25) and then solving equation (4.23) with acquired C gives G. As there are two frequencies in equation (4.25), rotation in frequencies was substituted to w_1, keeping w_2 equal 1MHz at which the capacitance disperses a lot. As seen in Fig.4.12, r_s equals 90 Ω and 115 Ω depending on the choice of frequency for calculations. The same iteration is applied when w_1=100kHz, where r_s equals 380 Ω. However, the substrate of sample has a range of resistivity from 10 Ω ·cm to 20 Ω ·cm, which convert to 58.97 Ω and 117.93 Ω respectively. Therefore, the two r_s of former case (90 Ω and 115 Ω) are considered to remove the effect of series resistance. However, in Fig.4.13b the remove of series resistance failed after applying three-element model on C-V curves in Fig.4.13a. The capacitance in strong accumulation at 100 kHz and 1KHz increased slightly. Therefore, the three-element mode does not work properly for this MOS capacitor due to multi-layer oxides. We need more complex model to analyze the different layer instead of using one C or G including two dielectric layers.

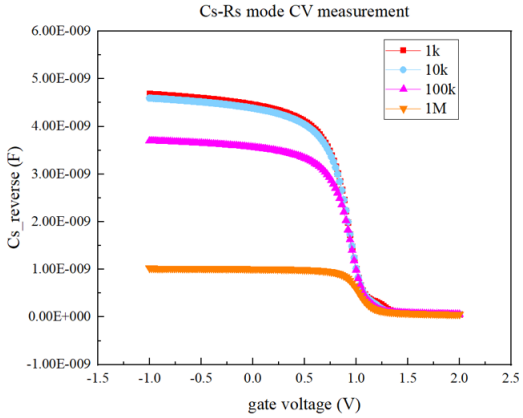


FIGURE 4.11: Cs-Rs in series-connection mode for Y7 thermal SiO_2 TE-ALD Al_2O_3

Six-element circuit model

Three-element circuit model used in our calculation failed to fully remove the effect of series resistance. This indicates that the three-element circuit model is not proper for analyzing the MOS capacitor stack with multiple dielectric layers. In order to accurately analyze our MOS capacitor stack, the six-element circuit model is used [38] as seen in Fig.4.14. To explain how to correct the measured capacitance with the model, we use the MOS capacitor with thermal SiO_2 and TE-ALD Al_2O_3 as an example. C_{ox} is the oxide capacitance of Al_2O_3 layer. The SiO_2 layer is modelled by R_t and C_t elements connected in parallel. R_t and C_t elements are converted to R_e and C_e in a series equivalent circuit written in equation (4.26) and (4.27) :

$$C_e = \frac{{G_t}^2 + w^2{C_t}^2}{w^2 C_t} \tag{4.26}$$

$$R_e = \frac{G_t}{{G_t}^2 + w^2{C_t}^2} \tag{4.27}$$

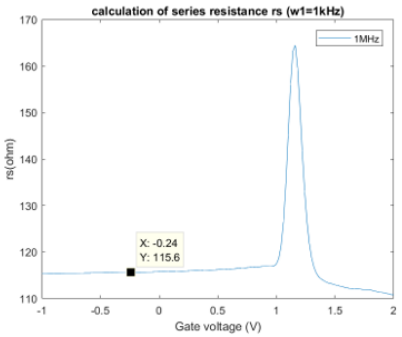
where $G_t = \frac{1}{R_t}$. In strong accumulation, interface traps occupancy does not change due to the presence of large amount of majority carriers. Therefore, the effect of interface trap will not be observed in the accumulation portion of C-V curve. In addition, the equivalent circuit model can be shown in Fig.4.15 where capacitance C_{ma} and conductance G_{ma} in parallel. In this case, the measured capacitance C_{ma} actually includes the effect of dielectric SiO_2 which are related to C_e and ${R_s}'$, where ${R_s}'$is given by

$${R_s}' = R_s + R_e \tag{4.28}$$

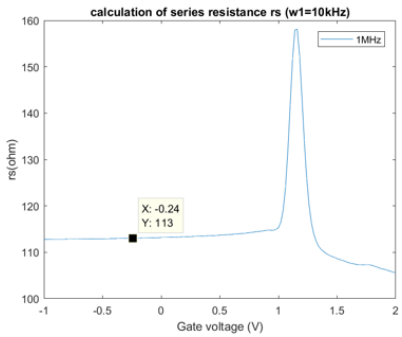
In strong accumulation from Fig.4.16, the measured impedance Z_{ma} and the total circuit impedance Z_A can be expressed as

$$Z_{ma} = \frac{1}{G_{ma} + jwC_{ma}} \tag{4.29}$$

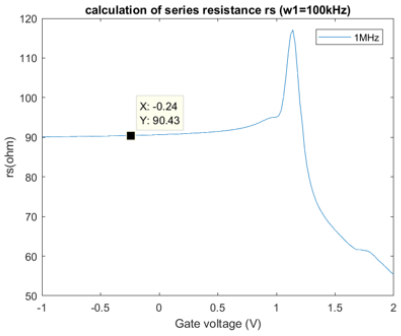
$$Z_A = R_s' - j\frac{C_e + C_{ox}}{wC_{ox}C_e} \tag{4.30}$$



(a) Series resistance when w_1 = 1kHz versus gate voltage



(b) Series resistance when w_1 = 10kHz versus gate voltage



(c) Series resistance when w_1 = 100kHz versus gate voltage

FIGURE 4.12: Series resistance vs gate voltage with different-frequency calculation

Comparing the real and imaginary parts of equation (4.29) and (4.30), it is obtained

$$R'_s = \frac{G_{ma}}{G_{ma}^2 + w^2 C_{ma}^2} \tag{4.31}$$

$$C_e = \frac{-C_{ox}(G_{ma}^2 + w^2 C_{ma}^2)}{w^2(C_{ma}^2 - C_{ma}G_{ma}) + G_{ma}^2} \tag{4.32}$$

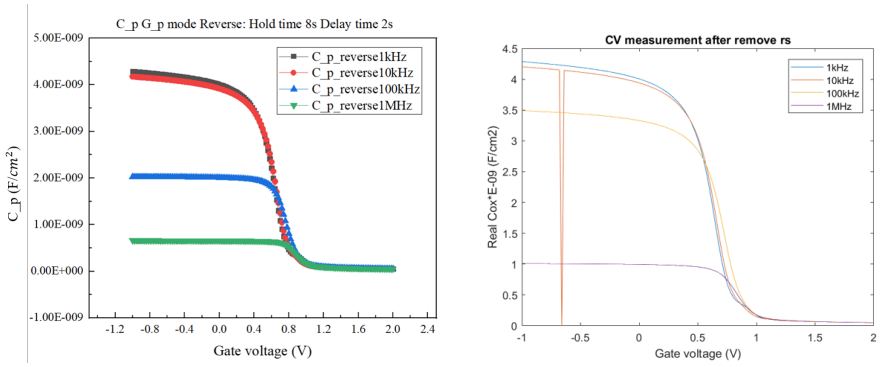
From equation (4.29) and (4.30), R'_s and C_e can be obtained from the measured capacitance C_{ma} and conductance G_{ma} in strong accumulation. In Fig.4.17, the series of the oxide capacitance and $C_d - Y_{it}$ in parallel is equivalent to impedance Z_c and the series of C_e and R'_s is equivalent to Z_s. The measured total impedance Z_m of the parallel RC circuit is the sum of the series of Z_c and Z_s , the relationship given by expression

$$Z_c = \frac{1}{G_c + jwC_c} = Z_m - Z_s \tag{4.33}$$

After comparing the real and imaginary parts in equation (4.33) and mathematical process, the corrected capacitance C_c and conductance G_c related to the real oxide capacitance can be expressed as

$$C_c = \frac{(w^2 C_m C_e - G_m^2 - w^2 C_m^2)(G_m^2 + w^2 C_m^2)C_E}{(w^2 C_e^2)[G_m(1 - R'_s G_m) - w^2 R'_s C_m^2]^2 + (G_m^2 + w^2 C_m^2 - w^2 C_m C_e)^2} \tag{4.34}$$

$$G_c = \frac{[G_m(1 - R'_s G_m) - w^2 R'_s C_m^2](G_m^2 + w^2 C_m^2)(w^2 C_e^2)}{(w^2 C_e^2)[G_m(1 - R'_s G_m) - w^2 R'_s C_m^2]^2 + (G_m^2 + w^2 C_m^2 - w^2 C_m C_e)^2} \tag{4.35}$$



(a) The measured C_p versus gate voltage characterized from C_p-G_p parallel-connection mode

(b) The real oxide capacitance C_{ox} versus gate voltage after removing the effect of series resistance

FIGURE 4.13: C-V measurements before and after removing series resistance

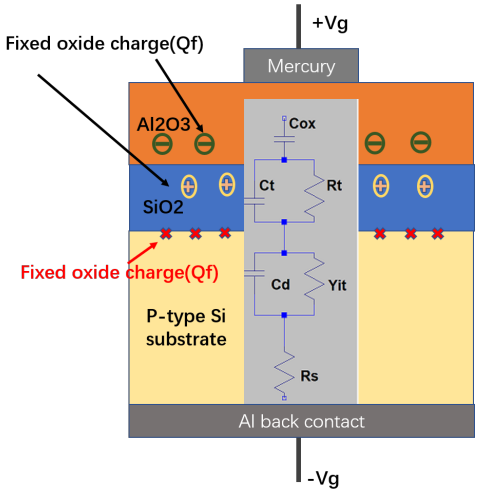


FIGURE 4.14: Six-element circuit model on MOS capacitor stack

The expressions in equations (4.34) and (4.35) represent the reconstruction formula of correction capacitance and conductance that are removed the effect of series resistance and dielectric SiO_2. In equation (4.32) and (4.34), the oxide capacitance C_{ox} is the only unknown parameter. An initial estimation was used to obtain the value of t_{ox}. In Fig.4.19, from the strong accumulation at smaller frequency 1kHz t_{ox} was extracted from this curve which yields the most realistic value for oxide thickness of Al_2O_3. This value can then be used to calculate $C_{ox}(F/cm^2)$ $(= \frac{\epsilon_0 \epsilon_{Al_2O_3}}{t_{Al_2O_3}})$ $= 4.5 \times 10^{-9} F/cm^2$. This estimated value is then used in equation (4.34). When the variation of curves at different frequencies becomes less in the whole range of measured gate voltage, the estimated C_{ox} is correct. In this approximation the oxide thickness Al_2O_3 is 2.2 nm and $\epsilon_{Al_2O_3}$ is 11. The 2.2 nm Al_2O_3 is approximately consistent with the TE-ALD Al_2O_3 in the fabrication. Fig.4.20 shows the corrected C_c-V characteristics without frequency dispersion after the elimination of the series R_s.

Since in the model the C_e and R_e is equivalent to C_t and R_t in parallel as seen in

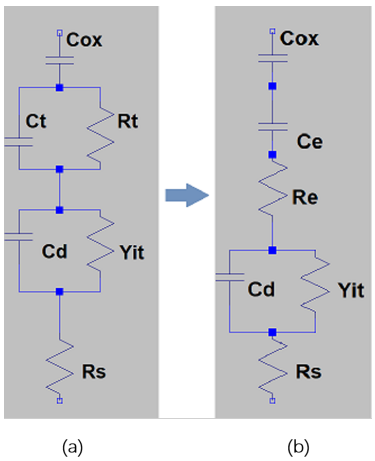


FIGURE 4.15: (a)Proposed model, taking into account the presence of two dielectric layers. (b)The parallel C_tR_t network could be represented by a series C_eR_e network, where C_e and R_e are represented by equation (4.26) and (4.27) respectively.

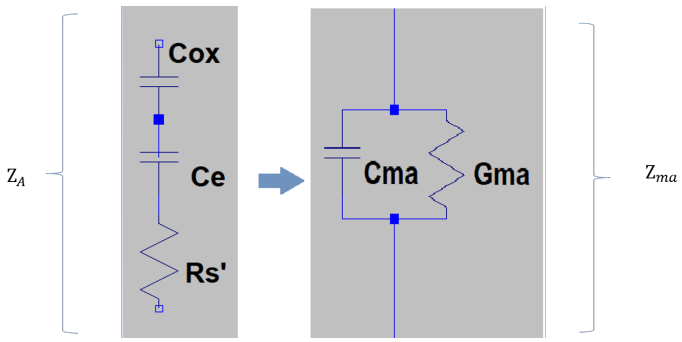


FIGURE 4.16: (a)Measured impedance in strong accumulation region, Z_{ma} includes the effect of oxide capacitance C_{ox} of Al_2O_3, the dielectric SiO_2 and series resistance C_e and $R_s{}'$. (b)The equivalent circuit of (a).

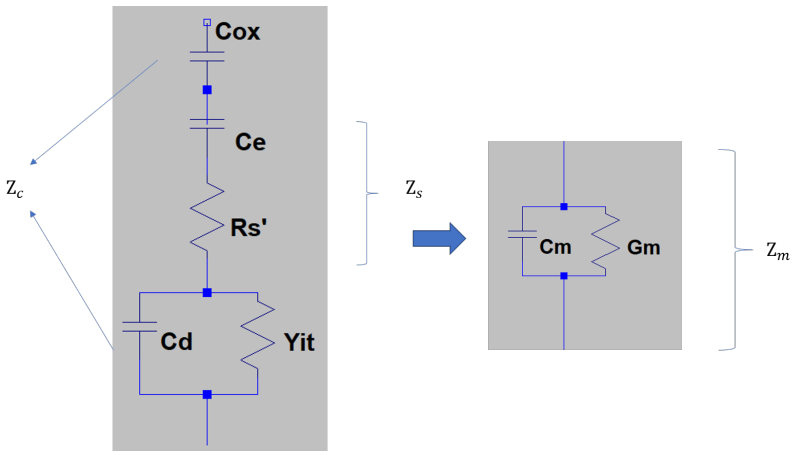


FIGURE 4.17: Measured impedance including the effect of oxide capacitance C_{ox}, the effect of dielectric SiO_2, the series resistance, the depletion capacitance C_d and the admittance of interface trap Y_{it}.

Fig.4.15. We write the equivalent impedance of C_t and R_t in parallel as Z_t :

$$Z_t = \frac{R_t}{jwC_tR_t + 1} = \frac{1}{(wC_tR_t)^2 + 1} - j\frac{jwC_tR_t^2}{(wC_tR_t)^2 + 1} \tag{4.36}$$

The impedence of C_e and R_e in series is written as Z_e :

$$Z_e = R_e - j\frac{1}{wC_e} \tag{4.37}$$

Equating the real and imaginary part of equation (4.36) and (4.37), we obtain :

$$R_e = \frac{1}{(wC_tR_t)^2 + 1} \tag{4.38}$$

R_s can be subtracted by equation (4.28) and (4.31). However, we have to solve C_t and G_t first. Standard forms [39] were build for C_t and G_t/w frequency dependence in written below :

$$C_t = \frac{a}{[1 + (\frac{w}{b})^2]^k} \tag{4.39}$$

$$\frac{G_t}{w} = \frac{c}{w}\ln(1 + dw^2) \tag{4.40}$$

where a, b, c, d and k are fitting parameters which allow C_e calculated by C_t and G_t using equation (4.26), (4.39) and (4.40) to match C_e calculated by equation (4.32). By solving kinds of equations, the fitting parameters a, b, c, d and k are presented below :

$$a = 1.24 \times 10^{-7}(F) \tag{4.41}$$

$$b = 2 \times 10^{5}(s^{-1}) \tag{4.42}$$

$$c = 4.0214 \times 10^{-7}(Fs^{-1}) \tag{4.43}$$

$$d = 2.9290 \times 10^{-10}(s^2) \tag{4.44}$$

$$k = 0.8 \tag{4.45}$$

After substituting the fitting parameters into equation (4.39), (4.40) to get C_e by equation (4.26), we can plot two C_e curves as a function of frequency by two different calculations in Fig.4.21. We can see the fitting parameters are proper to $C_t - G_t$ due to the approximation of two curves. In order to calculate the series resistance R_s, it is necessary to know C_t and G_t as seen in Fig.4.18. Besides, G_t/w curve can be obtained as seen in Fig.4.18. The curve G_t/w shows the presence of the trap density at the Al_2O_3-SiO_2 interface around the peak value equaling 5.527 $\times 10^{-12}$ F. Using equation (4.6) we can obtain the D_{it} equaling 1.716 $\times 10^{10} cm^{-2}eV^{-1}$. The thickness of SiO_2 equals 2.7 nm by using C_t at low frequency 1kHz. The thickness of SiO_2 calculated is approximately equal to the thickness of thermal SiO_2 in fabrication. In Fig.4.17, Z_c can be written as :

$$Z_c = \frac{1}{jwC_{ox}} + \frac{1}{Y_{it} + jwC_d} = \frac{1}{jwC_{ox}} + Z_d \tag{4.46}$$

where Z_d is the equivalent impedance of C_d and Y_{it} in parallel. Z_c can be calculated by C_c and G_c using equation (4.33). Therefore, we can obtain Z_d :

$$Z_d = \frac{G_c - jwC_c}{G_c^2 + w^2C_c^2} + j\frac{1}{wC_{ox}} \tag{4.47}$$

After comparing real and imaginary part, the equations become below :

$$\frac{Y_{it}}{Y_{it}^2 + w^2 C_d^2} = \frac{wG_c C_{ox}}{(G_c^2 + w^2 C_c^2) wC_{ox}} \tag{4.48}$$

$$\frac{wC_d}{Y_{it}^2 + w^2 C_d^2} = \frac{w^2 C_c C_{ox} - G_c^2 - w^2 C_c^2}{(G_c^2 + w^2 C_c^2) wC_{ox}} \tag{4.49}$$

Solving equation (4.48) and (4.49), we could have Y_{it}/w and C_d as a function of gate voltage as seen in Fig.4.22 and Fig.4.23.

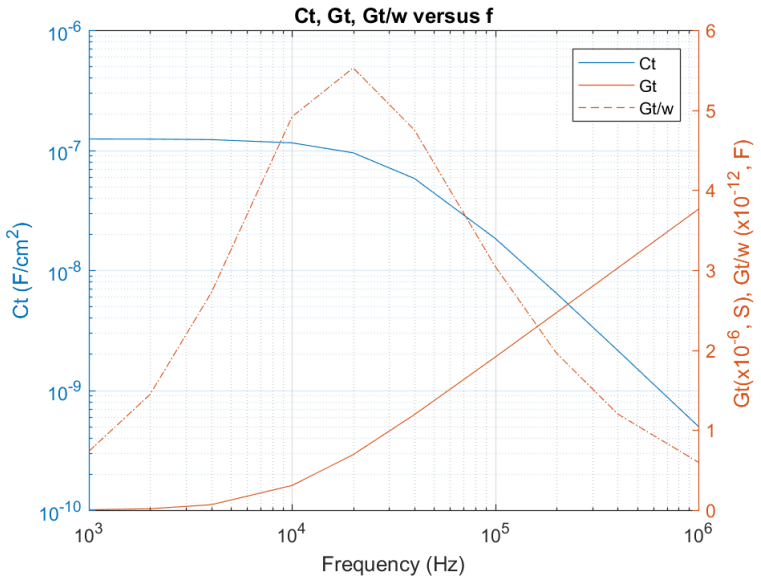


FIGURE 4.18: Plot of C_t, G_t and G_t/w as a function of frequency

This is the whole analysis for MOS capacitor stack using six-element circuit model. The same steps can be applied to other MOS capacitors. As the MOS capacitor with thermal SiO_2 and PE-ALD Al_2O_3 is used to compare the sample we have analyze in details, we list its important graphs here :

According to our calculation, the different parameters of the MOS capacitor with thermal SiO_2 and TE-ALD Al_2O_3 and the MOS capacitor with thermal SiO_2 and PE-ALD Al_2O_3 are compared in Fig.4.27. Due to the presence of Al_2O_3 the fixed oxide charge are negatives and the flatband voltages are both positive. Compared with the interface traps density in two samples, the MOS capacitor with thermal SiO_2 and PE-ALD Al_2O_3 has less D_{it} than MOS capacitor with thermal SiO_2 and TE-ALD Al_2O_3. Both of their D_{it} are less than 10^{11} $cm^{-2}eV^{-1}$, which expects our requirement for a good MOS capacitor.

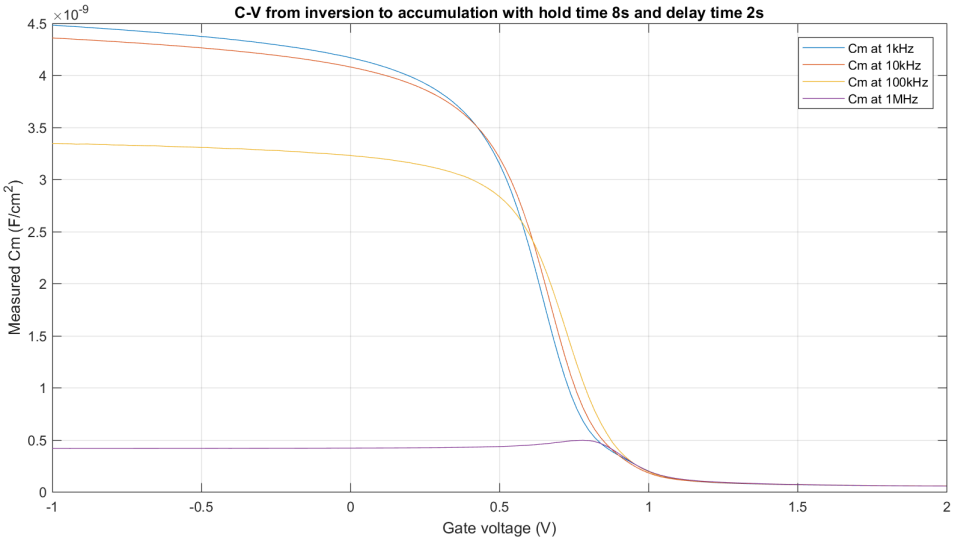


FIGURE 4.19: The measured C-V curves were obtained by $C_p - G_P$ mode from inversion to accumulation with 8s hold time and 2s delay time between each voltage step to set equilibrium state. This is high frequency C-V curve which has a wide frequency range from 1kHz to 1MHz.

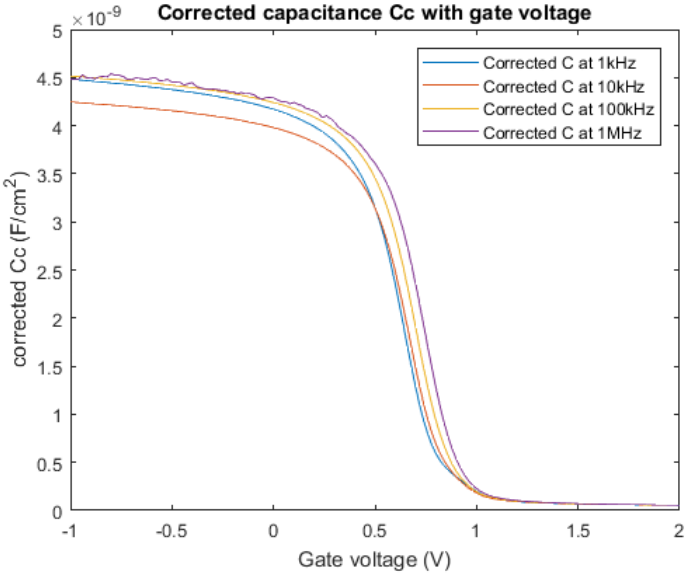


FIGURE 4.20: Plot of corrected capacitance C_c with gate voltage at four frequencies from 1kHz to 1MHz. No frequency dispersion occurs in strong accumulation region.

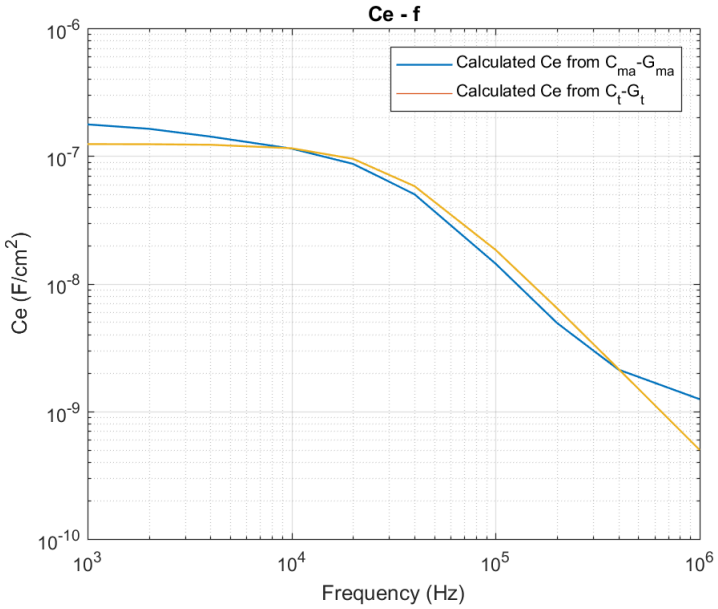


FIGURE 4.21: Ce calculated by measured C_{ma} and G_{ma} in strong accumulation at different frequencies , Ce calculated by fitting C_t and G_t

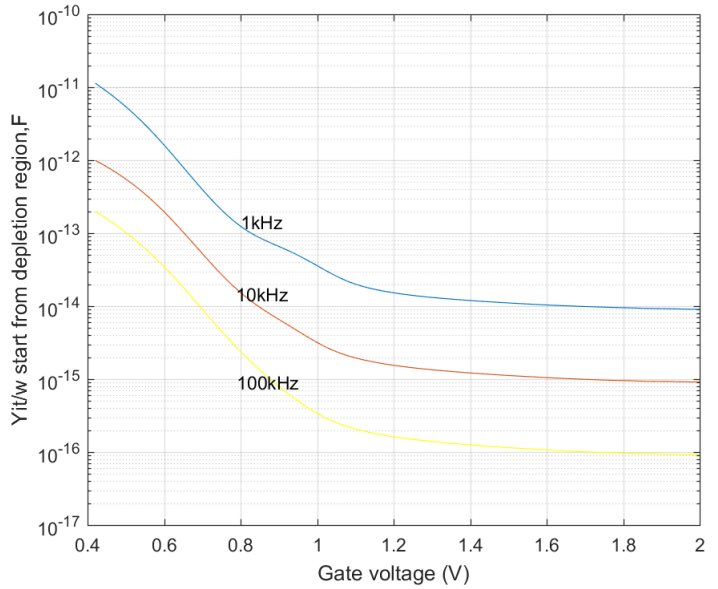


FIGURE 4.22: Y_{it}/w versus gate voltage V_g from depletion region at different frequencies

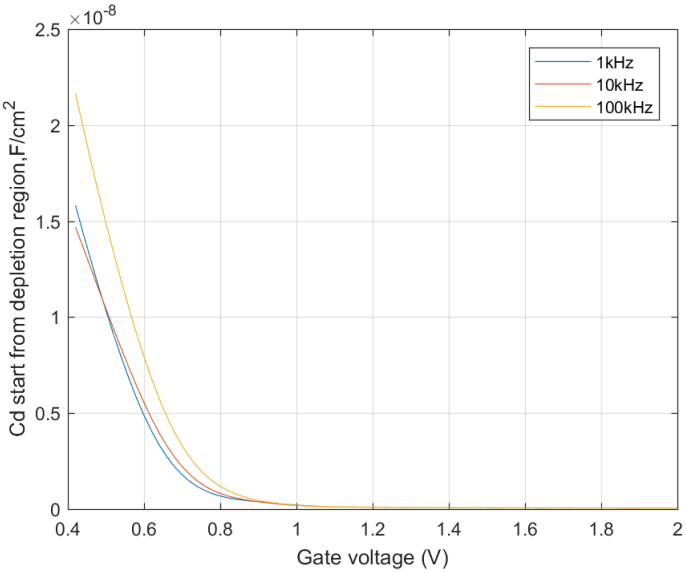


FIGURE 4.23: C_d versus voltage gate V_g from depletion region at different frequencies

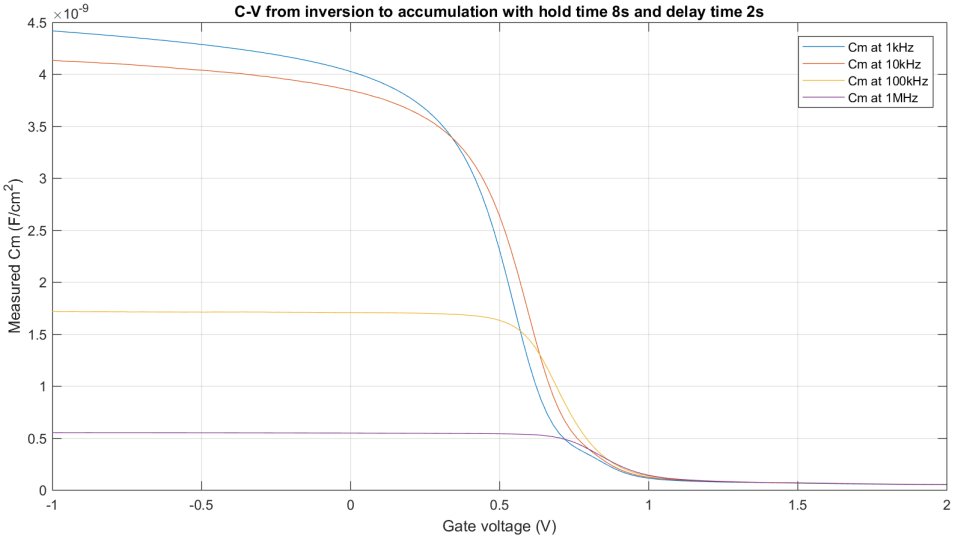


FIGURE 4.24: The measured C-V curves were obtained by $C_p - G_P$ mode from inversion to accumulation with 8s hold time and 2s delay time between each voltage step to set equilibrium state. This is high frequency C-V curve which has a wide frequency range from 1kHz to 1MHz.

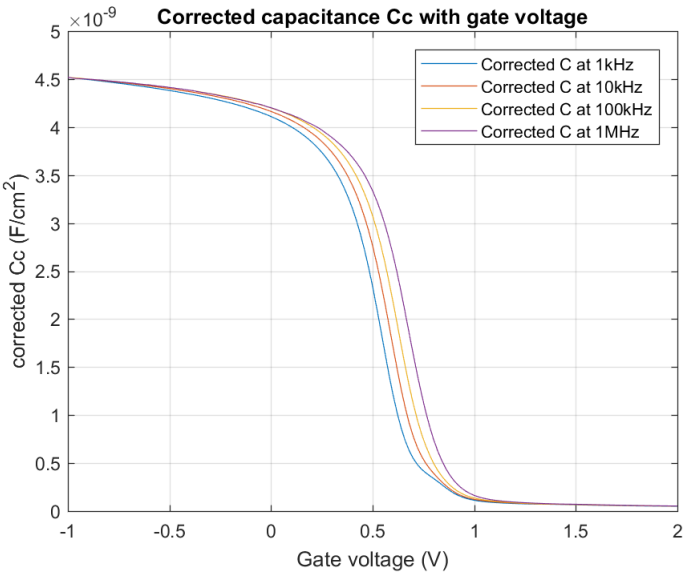


FIGURE 4.25: Plot of corrected capacitance C_c with gate voltage at four frequencies from 1kHz to 1MHz. No frequency dispersion occurs in strong accumulation region.

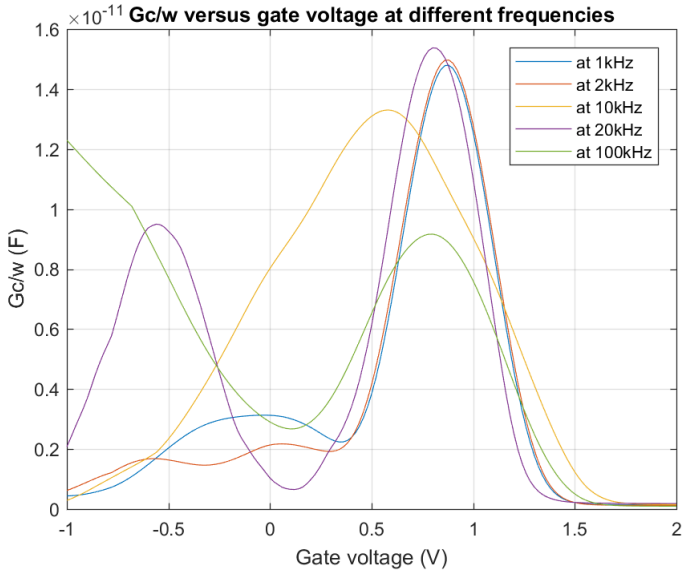


FIGURE 4.26: G_c/w versus voltage gate to investigate the interface trap density

Dielectric layer	C_{ox} (F/cm^2)	V_{FB} (V)	Q_f (cm^{-2})	D_{it} ($cm^{-2}eV^{-1}$)
Thermal SiO_2 + TE-ALD Al_2O_3	4.50×10^{-9}	+ 1 V	- 4.04×10^{10}	7.76×10^{10}
Thermal SiO_2 + PE-ALD Al_2O_3	4.50×10^{-9}	+ 0.96 V	- 3.92×10^{10}	3.6275×10^{10}

FIGURE 4.27: The electrical parameters comparison between two MOS capacitors

Chapitre 5

Simulation

In this chapter, We will investigate the physics mechanism of the MOS capacitor stacks and the behaviors of the negative charges in Al_2O_3 by a simulation tool (Silvaco Atlas). We will compare the simulation results with the measurement data. We will also analyze the possibility for replacing SiO_2 by Al_2O_3 in 65-nm-node technology.
It is divided into three sections. Section 5.1 will present the basic codes with the brief description of their physical models. Section 5.2 will show that the simulation results and the comparison between the simulations and the experiments. Section 5.3 will summarize the problems of inconsistency in simulations and measurements.

5.1 Physical models and codes of simulations

5.1.1 Basic definitions in simulation

Since our MOS capacitor has two ultra layers : Al_2O_3 and SiO_2 , 3 nm and 2 nm respectively. In order to fully simulate the C-V characterization, the number of nodes defined by meshes should be at least 10 points in 1 nm. Besides, it is precise to use more dense meshes at the interface of two materials as seen in Fig.5.1. The region definition is defined as seen in Fig.5.2.
Electrode is defined by mercury with workfunction 4.49 eV. Back contact is 300

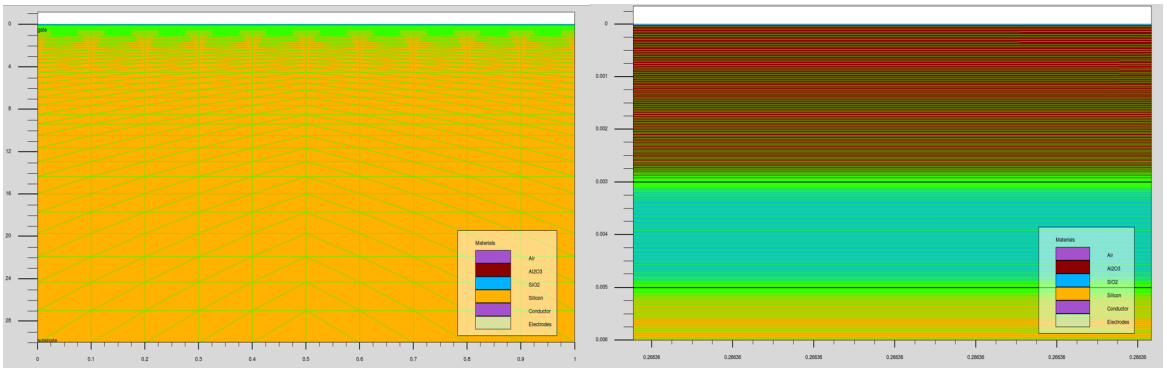


FIGURE 5.1: The mesh definition of MOS capacitor stack

μm thick Al. Based on our analysis in previous chapter, we are interested in fixed oxide charge (Q_f) and interface trap density (D_{it}) when doing C-V characterization.

For the MODEL statement related to these physical models, as the traps also are recombination centers the Shockley-Read-Hall (SRH) Recombination model should be used [40]. Lombardi CVT Model is to define the mobility which could override any other mobility models. We have no requirements for specific mobility model thus we can use it. The other basic details of codes can be seen in Appendix.

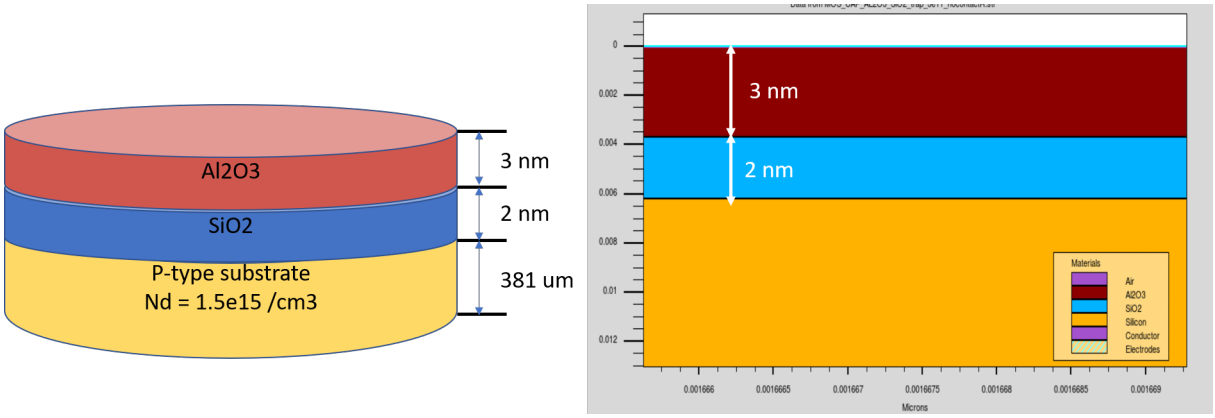


FIGURE 5.2: The MOS capacitor stack with thermal SiO_2 and ALD Al_2O_3 (left) and the same structure with additional electrodes Hg and Al in Atlas (right) (P-type substrate $N_d = 1.5 \times 10^{15}\ cm^{-3}$)

5.1.2 Fixed oxide charge

Q_f can be implemented by two methods : DOPING statement and INTERFACE statement as seen in Fig.5.3. After testing, the first method can be plot on the structure as seen below in Fig.5.4. However, for the second method it can not probe the concentration of Q_f in the profile plot. Therefore, we choose DOPING statement.

```
#first method of fixed oxide carges
doping region = 2  ox.charge conc=$"Qf"

# second method of fixed oxide charges
interface charge = 4e10 y.min=$"t_gox"    y.max=$"t_gox"+$"t_sio2"
```

FIGURE 5.3: Two methods to define the fixed oxide charges in dielectric

5.1.3 Interface trap density

In our MOS capacitor, the interface traps are introduced by dangling bonds at interfaces. Trap centers, whose associated energy lies in the forbidden gap of silicon, exchange charges with the conduction and valence bands through the emission and capture of electrons and holes. There are two kinds of traps : donor-like trap and acceptor-like trap. Donor-like traps usually lie near the valence band. Likewise, acceptor-like traps usually lie near the conduction band.
We have two statements to define interface traps : INTERFACE statement and INTTRAP statement. For the first method, adjusting the density of interface charge by

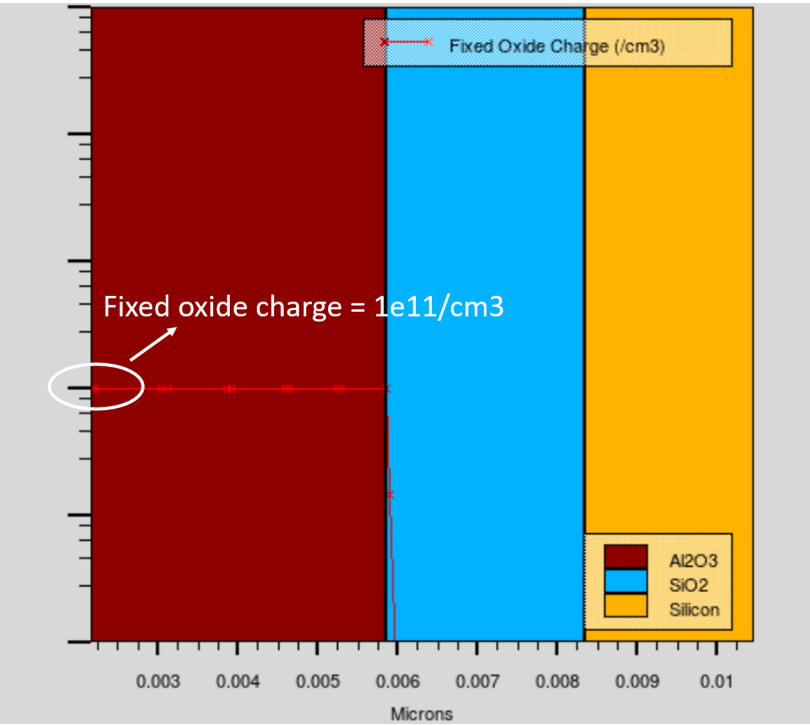


FIGURE 5.4: Fixed oxide charge defined by DOPING statement in dielectric Al_2O_3

'qf' and specifing the location of interface traps are allowed without any other requirements as seen in Fig.5.5.
In second method, we should think about the electrical properties of interface traps.

```
# Interfacial charge Si / top oxide layer
interface qf = 7.38e10 y.min=$"t_gox"+$"t_sio2" y.max=$"t_gox"+$"t_sio2"
```

FIGURE 5.5: INTERFACE statement simulates the interface traps at SiO_2/silicon interface

In p-type silicon, we define the interface trap as the donor-like trap which has the similar density defined by 'density' as we calculated before. The donor-like trap is close to middle of forbidden band of silicon. The energy level is E_c-0.6 eV. Here, 'degen' is the degeneracy factor which shows the ratio of empty states and states with electrons in simplification. According to the relative example of silicon/SiO_2 interface, the 'degen' is set to 4. Their rate of response to changes in the energy of the Quasi-Fermi level in the semiconductor depends linearly on the values of the carrier capture cross-sections, SIGN and SIGP in definition of interface traps. If we use Heiman model[41] to help the simulation, they are further to relate to distance d into insulator as

$$SIGN(d) = SIGNe^{-K_e d} \tag{5.1}$$

$$SIGP(d) = SIGPe^{-K_h d} \tag{5.2}$$

where

$$k_e^2 = \frac{2m_e * (E_c - E_{tA})}{\hbar^2} \tag{5.3}$$

and

$$k_h^2 = \frac{2m_h * (E_{tD} - E_v)}{\hbar^2} \tag{5.4}$$

are the evanescent wavevectors of the semiconductor electron and hole states as they tunnel into the insulator. In Atlas, the implementation of traps at a semiconductor-insulator interface assumes that the traps are located exactly at the interface. The trap density distribution into the insulator is uniform and it can be specified at the interfaces by 'depth'. 'hpoints' is the number of equally spaced internal points describing the internal trap distribution for each interface node. For each interface node, the trap distribution is calculated at each of the HPOINTS points. All the implementation can be seen in Fig.5.6. Here we should consider the delay time

```
inttrap e.level=0.6 donor density=7.0e10 s.x degen=4 sign=1.0e-13 \
        sigp=1.0e-14 heiman depth=$"t_gox"+$"t_sio2"   hpoints=10
```

FIGURE 5.6: Interface trap definition in Atlas

for gate voltage ramp using Heiman model. Bias ramps are carried out with the ramptime set to 2 seconds by using the TIMESPAN parameter in Solve statements as seen in Fig.5.7. SOLVE statement defines the small signal simulations with ramp gate voltage at different frequencies to acquire C-V characterization.

```
#************************************************
#Section1: Mesh Specifications
#************************************************

mesh space.mult = 1


## X mesh
 x.mesh loc = 0                          spacing=0.1
 x.mesh loc = 1                          spacing=0.1

 ##Y mesh
 ##the thickness for Al2O3 and 4 mesh points in the field oxide
y.mesh loc = 0.0                        spacing= 0.0001

 ##the thickness for dielectric layer sio2 and 4 mesh points in the sio2
y.mesh loc = $"t_gox"-0.0004                    spacing= 0.00005
y.mesh loc = $"t_gox"    spacing= 0.00001
y.mesh loc=$"t_gox"+0.0004     spacing= 0.00005

#1nm mesh on the interface of SiO2 and Si substrate
y.mesh loc=$"t_gox"+$"t_sio2" -0.0004          spacing=0.00005
y.mesh loc=$"t_gox"+$"t_sio2"           spacing=0.00001
y.mesh loc=$"t_gox"+$"t_sio2" +0.0004       spacing=0.00005
y.mesh loc = $"t_sub"                   spacing = $"t_sub"/10
```

FIGURE 5.7: Bias ramp at 1kHz with ramp time (delay time) 2s

5.2 Comparison between experiments and simulations

In Silvaco Atlas, we could not simulate the fabrication process and distinguish both the MOS capacitors with thermal SiO_2 but different in TE-ALD Al_2O_3 and PE-ALD Al_2O_3. So here we will focus on the influence of Q_f and D_{it} on C-V curves. Using $Q_f = 4 \times 10^{10}\ cm^{-2}$ and $D_{it} = 7 \times 10^{10}\ cm^{-2}eV^{-1}$ in simulation, we got the C-V curves at 9 frequencies as seen in Fig.5.8. The unit here for capacitance between

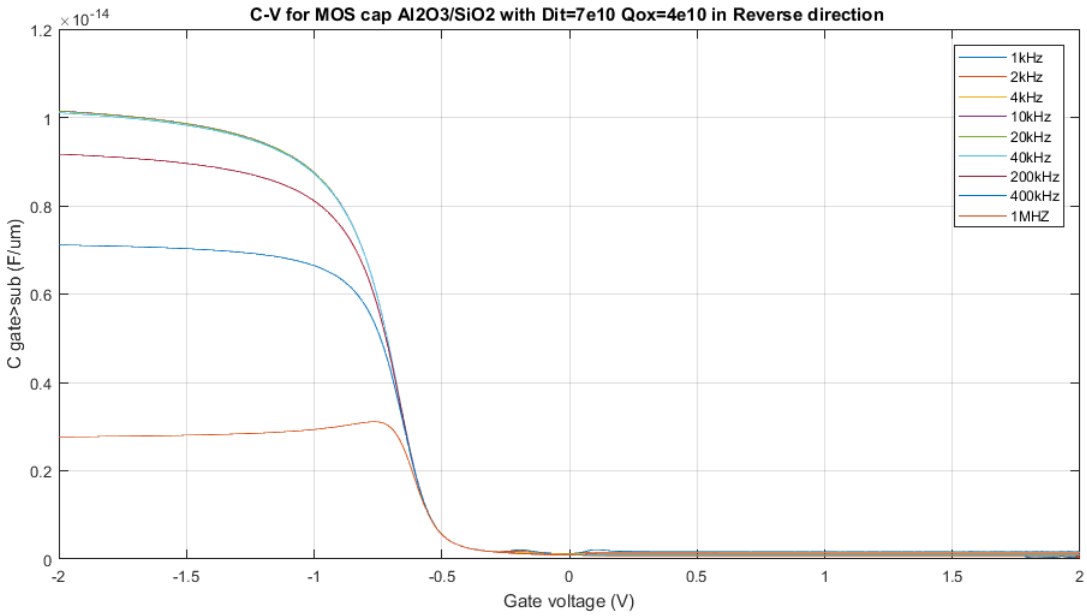


FIGURE 5.8: C-V curves of MOS capacitor stack with $Q_f = 4 \times 10^{10}\ cm^{-2}$ and $D_{it} = 7 \times 10^{10}\ cm^{-2}eV^{-1}$ from frequency 1 kHz to 1 MHz from inversion to accumulation with delay time 2s

the gate and the substrate is in 2D $\frac{F}{\mu m}$. Generally,

$$C[\frac{F}{cm^2}] = \frac{\epsilon_0 \epsilon_r}{d} A \tag{5.5}$$

where A is replaced by L of MOS capacitor ($L = 1\ \mu m$ in simulation). According to unit calculation, value with unit $\frac{F}{\mu m} \times 10^4$ is the value with unit $\frac{F}{cm^2}$. In Fig.5.8, we observed the frequency dispersion at high frequencies : 200kHz, 400kHz and 1MHz. In the week inversion region, there are some variations as seen in Fig.**??** which are introduced by interface traps. In order to look D_{it} more clearly, we plot G and $\frac{G}{w}$ as a function of gate voltage seen in Fig.5.10 and Fig.5.11. In Fig.5.10, we can see that at V_g=-0.17 eV, there is a small peak showing the effect of interface traps in the depletion region, seen obviously in relative low frequencies (1kHz, 2kHz and 3kHz). In Fig.5.11, the peak is also shown at V_g = -0.17 V. According to the equation (4.6), the D_{it} is around 6.63 $\times 10^{10}\ cm^{-2}eV^{-1}$ that aprroximately equal to the defined value 7 $\times 10^{10}\ cm^{-2}eV^{-1}$. This can show the equation is proper for calculation of D_{it} from G/w-V_g curves.

When decreasing the D_{it} from 7 $\times 10^{10}\ cm^{-2}eV^{-1}$ to 3 $\times 10^{10}\ cm^{-2}eV^{-1}$, the C-V curves show less frequency dispersion appears in accumulation region. However, in the inversion region some peaks appeared for some unknown reasons seen in Fig.5.12 and Fig.5.13. Besides, In Fig.5.13, the G/w-V curves are depends on frequency in the accumulation region, which is not consistent with the measurements. Due to the unknown peaks, we can not distinguish which peak can be used for D_{it} calculation.

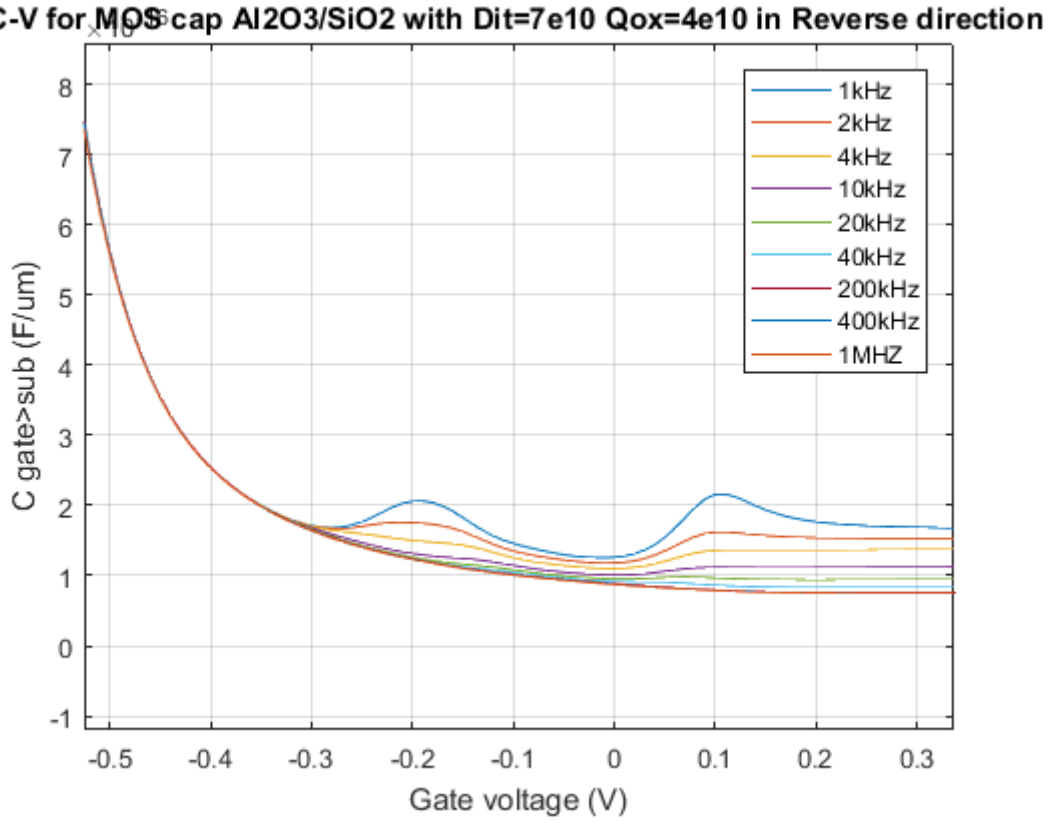


FIGURE 5.9: Zoom out of Fig.5.8 in the depletion-inversion region

5.3 Analysis of simulation problem

No shift of V_{FB}

Compared with measurements, C-V simulations does not show the shift of V_{FB} depends on the sign and amount of Q_f. However, using probe tools we can see the fixed oxide charge existed in the dielectric Al_2O_3 seen Fig.5.4. I even gave SiO_2 a positive Q_f to see whether the curves had a shift. But no change at all. Besides, the work function difference can effect the V_{FB} but not a lot. Due to the difference of work functions in references, I changed this parameter but we still had no shift.

G/w in the inversion region

Compared with measurements, G/w-V curves of MOS capacitor stack with Q_f = 4 $\times 10^{10}$ cm^{-2} and D_{it} = 3 $\times 10^{10}$ $cm^{-2}eV^{-1}$ in simulations show some strange peaks inversion region. But the case in MOS capacitor stack with Q_f = 4 $\times 10^{10}$ cm^{-2} and D_{it} = 7 $\times 10^{10}$ $cm^{-2}eV^{-1}$ has no such variation. The only difference in both codes is the value of D_{it}. Besides, the frequency dispersion did not exist in C-V but in G/w-V it appeared. How to deal with this needs more investigation.

The simulation of MOS transistors with MOS capacitor stacks

Since the time is not enough to fabricate MOS transistors with this dielectric stack to test the electrical properties, the simulation could help us to test its possibi-

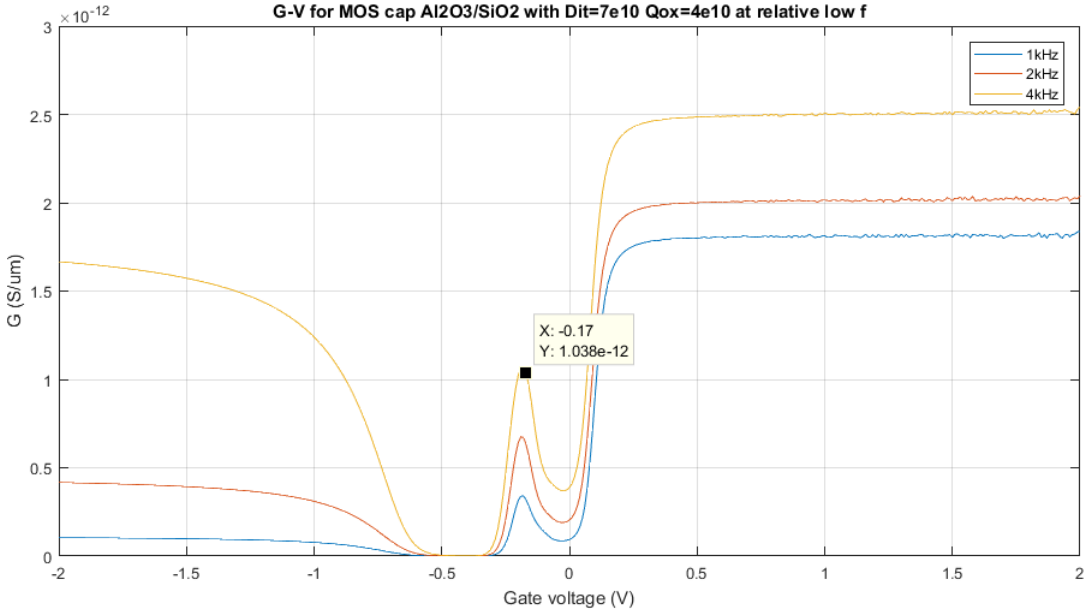


FIGURE 5.10: G ($S/\mu m$) versus gate voltage at relatively low frequencies for MOS capacitor stack with $Q_f = 4 \times 10^{10}\ cm^{-2}$ and $D_{it} = 7 \times 10^{10}\ cm^{-2}eV^{-1}$

lity as a potential replacement of SiO_2 and another rare high-k dielectric in advance. This will be very meaningful to investigate this kind of dielectric stack.
In summary, the simulation results did not match the measurements very well due to unsuitable definition or misunderstanding of physical concepts. We should deep into it to find the solutions of these problems.

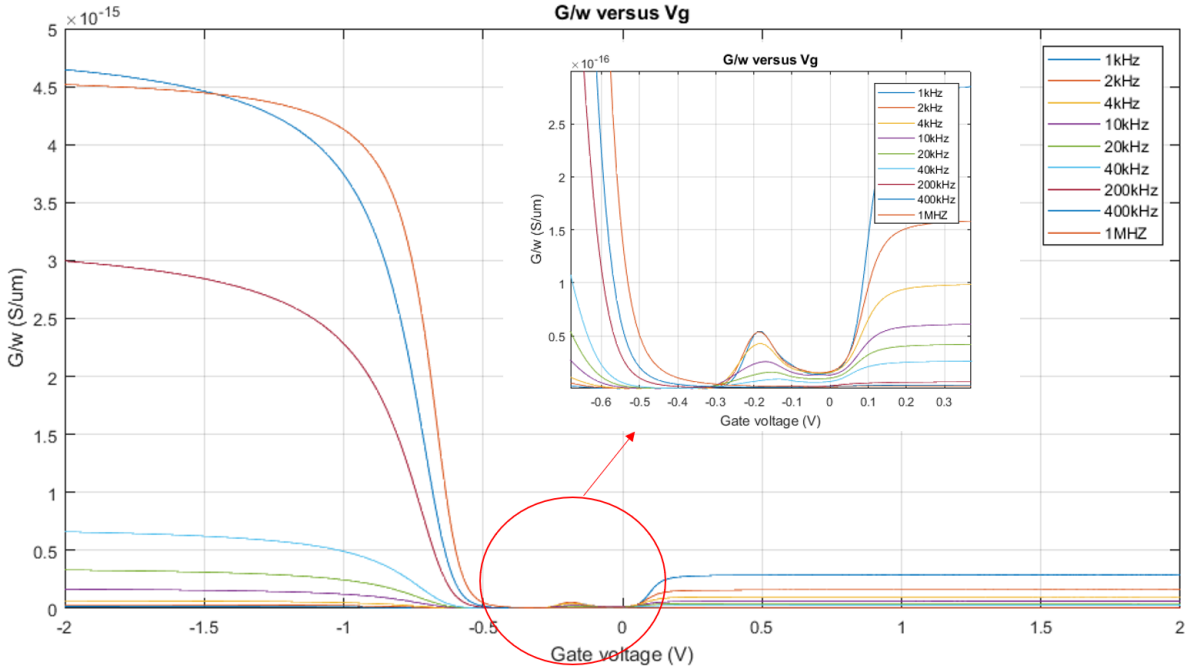


FIGURE 5.11: G/w versus gate voltage at different frequencies for MOS capacitor stack with $Q_f = 4 \times 10^{10}\ cm^{-2}$ and $D_{it} = 7 \times 10^{10}\ cm^{-2}eV^{-1}$

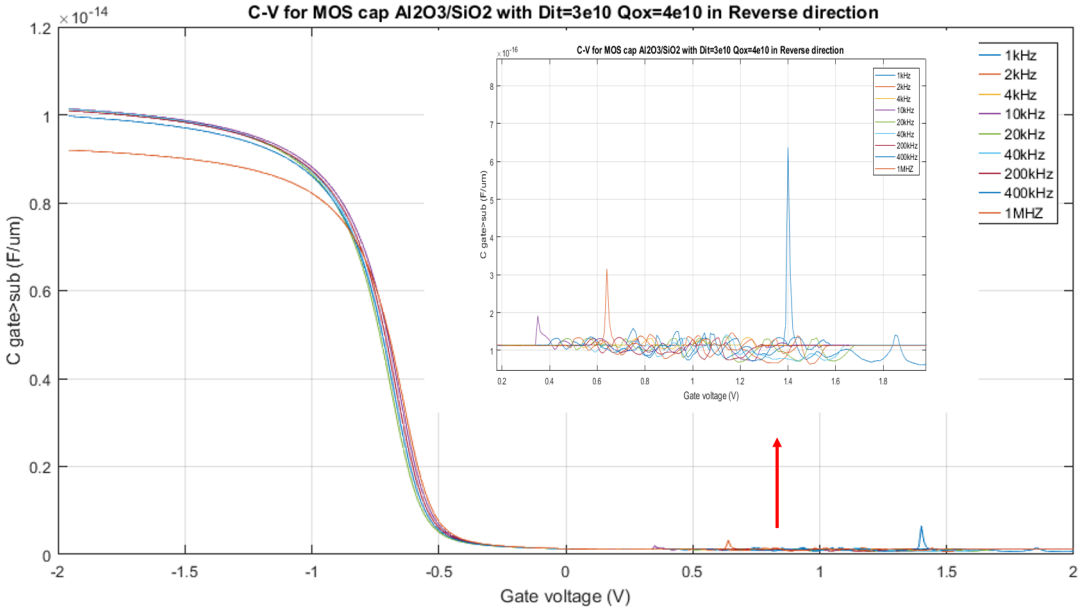


FIGURE 5.12: C-V curves of MOS capacitor stack with $Q_f = 4 \times 10^{10}\ cm^{-2}$ and $D_{it} = 3 \times 10^{10}\ cm^{-2}eV^{-1}$ from frequency 1 kHz to 1 MHz from inversion to accumulation with delay time 2s

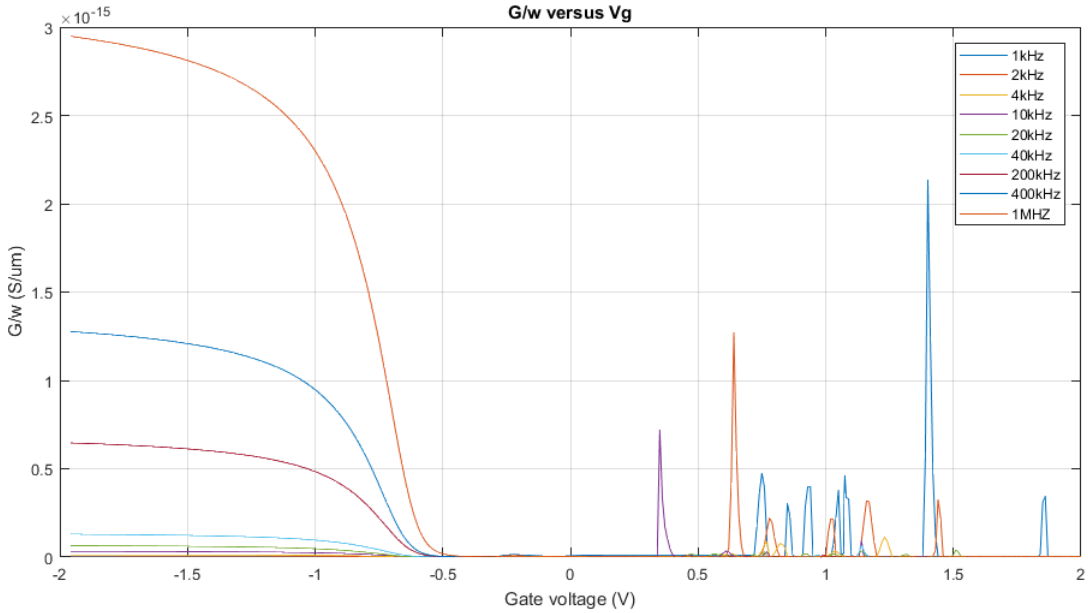


FIGURE 5.13: G/w versus gate voltage at different frequencies for MOS capacitor stack with $Q_f = 4 \times 10^{10}\ cm^{-2}$ and $D_{it} = 3 \times 10^{10}\ cm^{-2}eV^{-1}$

Chapitre 6

Conclusion

With the rapid shrinking of the transistor feature size, high-k dielectrics are considered to replace SiO_2 for sub-0.1-μm CMOS technology. Among high-k materials, Al_2O_3 is a potential candidate due to the advantages of higher dielectric constant, larger energy gap and band offset, good thermal stability, CMOS process compatibility, and less influence for electrical mobility in silicon channel. Specifically Al_2O_3 has negative fixed charges, preventing oxide leakage or electrons tunneling. However, the poly silicon dopant penetration phenomenon exists in Al_2O_3 and the negative fixed charges increase the threshold voltage of the transistor. In addition, it is reported that the defect and interface charge density of high-k dielectrics are larger than SiO_2.These issues could be overcome by introducing an ultra thin layer of thermal SiO_2 between Al_2O_3 and silicon.

In this work, we prepared various MOS capacitors for investigating the electrical performance of the Al_2O_3/SiO_2 (3/2 nm) stack, such as interface charge density and fixed charges. The C-V characteristics of the Al_2O_3/SiO_2 stack present the frequency dispersion effect, namely the oxide capacitances in accumulation region strongly depend on measurement frequencies. This makes the electrical parameter extraction from the measured C-V curves impossible. The six-element circuit model was used to eliminate series resistance in the measured C-V curves. After the correction, the oxide capacitances were free from any measured frequencies and the related electrical parameters ware extracted. It is found in Fig.4.27 that the Al_2O_3/SiO_2 stack has the good parameters ($Q_f = 4.0 \times 10^{10} cm^{-2}$ and D_{it} around $10^{10} cm^{-2} eV^{-1}$) compared to the stacks made of HfO_2/SiO_2, pure Al_2O_3 and HfO_2. The C-V characteristics of the $Al_2O_3/\ SiO_2$ stack was also simulated by using Silvaco Atlas simulator and the inconsistent results needs to be analyzed.

The Q_f and D_{it} values in the Al_2O_3/SiO_2 stack are acceptable compared to that in SiO_2 ($D_{it} = 2 \times 10^{10}\ cm^{-2}$ and$Q_f = 10^{12}\ cm^{-2} eV^{-1}$). To further reduce these values and improve the interface quality of the Al_2O_3/SiO_2 stack, we need to further investigate their physical origin by the other characteristic tools, for example, by using high-resolution transmission electron microscopy. The poly silicon dopant penetration and threshold voltage shift could be solved by using the other gate materials and by decreasing the channel doping concentration, respectively. Therefore, the Al_2O_3/SiO_2 stack could be used as gate dielectric for 60-nm-node MOSFET.

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Appendix

The codes for simulation :

```
go atlas simflags="-p 6"

#My constants
set Nd_rho_10=1.5e15

#device parametres

#substrate
set typeSi = "p.type"
set Nd =$"Nd_rho_10"

set filename = "2080_MOS_CAP_AL2O3_SiO2_inttrap_3e10_trap_Qox4e10N_newmesh"
assign name=myfile c.value="$filename"

set t_gox = 0.0030
set t_sio2 = 0.0020
set t_sub = 30

#Negative fixed oxide charges for Al2O3
set Qox_1 = -4e10

set mWF = 4.49
set T = 298.15
#************************************************
#Section1: Mesh Specifications
#************************************************

mesh space.mult = 1


## X mesh
 x.mesh loc = 0                          spacing=0.1
 x.mesh loc = 1                          spacing=0.1

 ##Y mesh
 ##the thickness for Al2O3 and 4 mesh points in the field oxide
y.mesh loc = 0.0                        spacing= 0.0001

 ##the thickness for dielectric layer sio2 and 4 mesh points in the sio2
y.mesh loc = $"t_gox"-0.0004                    spacing= 0.00005
y.mesh loc = $"t_gox"    spacing= 0.00001
y.mesh loc=$"t_gox"+0.0004      spacing= 0.00005

#1nm mesh on the interface of SiO2 and Si substrate
y.mesh loc=$"t_gox"+$"t_sio2" -0.0004          spacing=0.00005
y.mesh loc=$"t_gox"+$"t_sio2"           spacing=0.00001
y.mesh loc=$"t_gox"+$"t_sio2" +0.0004        spacing=0.00005
y.mesh loc = $"t_sub"                   spacing = $"t_sub"/10
```

```
#*************************************************
#Section1: Mesh Specifications
#*************************************************

mesh space.mult = 1


## X mesh
 x.mesh loc = 0                          spacing=0.1
 x.mesh loc = 1                          spacing=0.1

 ##Y mesh
 ##the thickness for Al2O3 and 4 mesh points in the field oxide
y.mesh loc = 0.0                        spacing= 0.0001

 ##the thickness for dielectric layer sio2 and 4 mesh points in the sio2
y.mesh loc = $"t_gox"-0.0004                  spacing= 0.00005
y.mesh loc = $"t_gox"   spacing= 0.00001
y.mesh loc=$"t_gox"+0.0004     spacing= 0.00005

#1nm mesh on the interface of SiO2 and Si substrate
y.mesh loc=$"t_gox"+$"t_sio2" -0.0004         spacing=0.00005
y.mesh loc=$"t_gox"+$"t_sio2"          spacing=0.00001
y.mesh loc=$"t_gox"+$"t_sio2" +0.0004       spacing=0.00005
y.mesh loc = $"t_sub"                   spacing = $"t_sub"/10
```

```
#*************************************************************************
#Section2: Structure Specification (REGIONS, ELECTRODES, & DOPING LEVELS
#*************************************************************************
# Regions definition
#*************************************************************************

# --- Bulk Silicon ----------------------

region number=1 material=air      x.min=0         x.max=1       y.min=-20             y.max=$"t_sub"

#---Gate Oxide ---------------------

region number=2 material=al2o3    x.min=0         x.max=1       y.min=0               y.max=$"t_gox"
region number=3 material=SiO2     x.min=0         x.max=1       y.min=$"t_gox"        y.max=$"t_gox"+$"t_sio2"
region number=4 material=silicon  x.min=0         x.max=1       y.min=$"t_gox"+$"t_sio2"              y.max=$"t_sub"

#*******************************************************
# define electrodes
#*******************************************************

electrode name=gate number=1 top
#electrode name=substrate number=2 substrate
electrode name=substrate number=2 x.min=0 x.max=1 y.min=30 y.max=30.3

contact name=gate  workfun=$"mWF"
contact   name=substrate neutral



#*******************************************************
# define the doping
#*******************************************************
# doping region
doping region=4 uniform conc=$"Nd"      $"typeSi"
#doping the negative fixed oxide charge in al2o3
doping region = 2  ox.charge conc=$"Qox_1"

# Interfacial charge Si / top oxide layer
#interface qf=$"Qoxf_top" y.min=0              y.max=$"t_gox"
 #interface qf = 1e11  x.min=0 x.max=1  y.min=$"t_gox"+$"t_sio2" y.max=$"t_gox"+$"t_sio2"


# Thermal contacts
thermcontact number=1  y.min=-20  y.max=$"t_sub"  ext.temp=$"T"


#*******************************************************
# Interfacial charge Si / BOX
#*******************************************************
#Heiman model interface trap definition
inttrap e.level=0.6 donor density=3.0e10 s.x degen=4 sign=1.0e-13 \
        sigp=1.0e-14 heiman depth=$"t_gox"+$"t_sio2"   hpoints=10
```

```
#****************************************************
# Section3: Material Model specifications
# Simulation method
#****************************************************
models cvt srh print

output band.param charge val.band con.band h.mobility e.mobility ox.charge qfn qfp qss taurn taurp traps e.velocity\
ex.velocity ey.velocity h.velocity hx.velocity  hy.velocity recomb flowlines photogen opt.intens devdeg U.TRANTRAP

method gummel block Newton carriers=2

probe name=bulk_rho_probe x=175 y=400 RESISTIVITY

solve initial
solve previous

save outf="${myfile}.str" master
tonyplot "${myfile}.str"


load infile="${myfile}.str" master
log outf="${myfile}1F.log"
solve vgate=-2 vstep=0.01 vfinal=2 name=gate ac freq=1e3 direct TIMESPAN = 2
save outf="${myfile}".str

load infile="${myfile}.str" master
log outf="${myfile}1R.log"
solve vgate=2 vstep=-0.01 vfinal=-2 name=gate ac freq=1e3 direct TIMESPAN = 2
save outf="${myfile}".str

load infile="${myfile}.str" master
log outf="${myfile}2.log"
solve vgate=2 vstep=-0.01 vfinal=-2 name=gate ac freq=2e3 direct TIMESPAN = 2
save outf="${myfile}".str

load infile="${myfile}.str" master
log outf="${myfile}4.log"
solve vgate=2 vstep=-0.01 vfinal=-2 name=gate ac freq=4e3 direct TIMESPAN = 2
save outf="${myfile}".str

load infile="${myfile}.str" master
log outf="${myfile}10.log"
solve vgate=2 vstep=-0.01 vfinal=-2 name=gate ac freq=1e4 direct TIMESPAN = 2
save outf="${myfile}".str

load infile="${myfile}.str" master
log outf="${myfile}20.log"
solve vgate=2 vstep=-0.01 vfinal=-2 name=gate ac freq=2e4 direct TIMESPAN = 2
save outf="${myfile}".str



load infile="${myfile}.str" master
log outf="${myfile}40.log"
solve vgate=2 vstep=-0.01 vfinal=-2 name=gate ac freq=4e4 direct TIMESPAN = 2
save outf="${myfile}".str

load infile="${myfile}.str" master
log outf="${myfile}200.log"
solve vgate=2 vstep=-0.01 vfinal=-2 name=gate ac freq=2e5 direct TIMESPAN = 2
save outf="${myfile}.str".str

load infile="${myfile}.str" master
log outf="${myfile}400.log"
solve vgate=2 vstep=-0.01 vfinal=-2 name=gate ac freq=4e5 direct TIMESPAN = 2
save outf="${myfile}.str".str

load infile="${myfile}.str" master
log outf="${myfile}1m.log"
solve vgate=2 vstep=-0.01 vfinal=-2 name=gate ac freq=1e6 direct TIMESPAN = 2
save outf="${myfile}.str".str


tonyplot -overlay "${myfile}1F.log" "${myfile}1R.log"
tonyplot -overlay "${myfile}1R.log" "${myfile}2.log" "${myfile}4.log"  "${myfile}10.log" "${myfile}20.log"\
 "${myfile}40.log" "${myfile}200.log" "${myfile}400.log" "${myfile}1m.log"


tonyplot "${myfile}.str"
quit
```

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