

MPPT based on synchronous demodulation

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Nomenclature

BCR Battery charge controller

BDR Battery discharge controller

BOL Beginning of life

CCM Continuous conduction mode

DET Direct energy transfer

DSB-SC Double side-band - suppressed carrier

DSSS Direct-sequence spread spectrum

EMC Electromagnetic compatibility

EMI Electromagnetic interference

EOL End of life

ESA European Spatial Agency

FDM Frequency-division multiplexing

GEO Geostationary orbit

GM Gain margin

ISS International Space Station

LEO Low Earth orbit

LFSR Linear-feedback shift register

LPF Low-pass filter

MLS Maximum-length sequence

MM Modulus margin

MPP Maximum power point

MPPT Maximum power point tracking

P&O Perturb and observe

PID Proportional-integral-derivative

PLL Phase-locked loop

PM Phase margin

PRBS Pseudo-random binary sequence

PSD Power spectral density

PWM Pulse width modulation

RMS Root mean square

S2R Switching shunt regulator

S3R Sequential switching shunt regulator

S4R Sequential switching shunt series regulator

SA Solar array

SNR Signal to noise ratio

VCO Voltage-controlled oscillator

Chapter 1

Introduction

1.1 Context

Nowadays, the three main sources of energy used to power the satellites are the solar, the nuclear and the (electro)chemical energies.

In cheap and low-power applications (several watts), simple batteries are already able to power the whole system during a couple of days. However, this solution is not sufficient any more for bigger satellites whose equipment requires hundreds of watts up to a few kilowatts, and which are sent in space for several weeks. In such applications, fuel cells appear to be a more interesting alternative. But this technology relies on a given quantity of fuel stored in the satellite, limiting the time duration of the mission without refuel.

For longer missions, the vast majority of satellites therefore harvest part of the almost unlimited power irradiated by the sun. This light energy is collected by means of solar arrays and is then converted into electricity using the photovoltaic effect. Most of the time, this technology is coupled to a set of batteries that power the satellite during eclipse periods. But this solution is not suited for all types of missions, and especially out of the solar system where the sunlight cannot be caught.

In such cases, the only viable solution is the nuclear energy using radioisotopes or reactors. These nuclear sources generate their power in the form of heat, which is then transformed into electrical energy by means of thermoelectric converters. However, the cost of these nuclear equipments, inflated by the security measures that have to be taken, exceed by far that of a power system based on solar arrays.

This is the reason why solar energy is currently dominating in space applications, and explains why lots of research are still conducted all around the world in order to improve the performance of these systems or to reduce their costs. However, all of this light power reaching the solar arrays has to be adequately extracted to avoid undesired losses (due for instance to inappropriate controllers). Therefore, this power extraction relies more and more on maximum power point trackers (MPPT), with the objective to use the solar arrays as efficiently as possible.

1.2 Motivation

In particular, this work aims at testing the performances of a MPPT based on the principle of synchronous demodulation, which has been extensively used in telecommunication strategies. As in several other MPPTs, the idea is to introduce a small perturbation in the system at a precise frequency and to see how it reacts. The difference here lies in the fact that a single current sensor placed on the bus side would allow several converters to work simultaneously with the same current measurement, thereby eliminating the cost of additional sensors and conditioning circuits.

1.3 Thesis outline

This thesis will first introduce the three fundamental concepts used throughout this paper, namely the solar arrays, the dc-dc converters and the associated MPPTs as well as the synchronous demodulation. It will continue with a state-of-the-art on solar array regulation in satellites, both in terms of power conditioning and bus regulation. Subsequently, the principle of maximum power point tracking based on synchronous demodulation will be detailed and simulated in order to analyse the performances that can be achieved; the potential problems will be identified and some solutions will be proposed to improve its robustness. A way to address one of these issues has been implemented in the following chapter, and its performances are compared to that of synchronous demodulation. Finally, the thesis will end up with a conclusion summing up the important results coming out of this work.

Chapter 2

Technical background

2.1 Solar arrays

In space, one of the most important source of energy is the light that the sun irradiates. In order to harvest this free energy source, the satellites are equipped with solar arrays that transform this energy into electricity to power the on-board equipments. Since solar array's concepts will be ubiquitous in this paper, this section aims at introducing their main characteristics to those who are unfamiliar with this technology.

2.1.1 Structure of a solar array

Solar string

As represented in figure 2.1, a solar string results from the series connection of several solar cells. The string voltage is defined by the number of cells connected in series, while its current does not exceed that of a single cell.

A bypass diode is also added in parallel with each cell to provide a path for the current in case of a cell failure, which avoids to loose the entire string.

Solar array

Basically, a solar array (SA) is the just a combination of several identical strings connected in parallel to sum up their currents; the number of those strings will depend on the power requirements of the loads.

An additional blocking diode is also added at the end of each string to prevent them from drawing current from the others. In some satellites, the connectors separating the SAs from the loads can be quite long; in this situation, strings with a higher voltage are used to minimize the Joule losses.

2.1.2 Electrical equivalent circuit

The aim of this section is not to make a deep analysis on how solar cells work, but to present their main characteristics in order to develop a simplified model that can be easily used in the following chapters.

Basically, a solar cell can be seen as a current source placed in parallel with a diode as represented in figure 2.2. More advanced models also include a series and a parallel resistor at the output as well as a capacitor in parallel, or even several diodes in parallel with the current source; but these parasitic elements will be neglected in this paper for the sake of simplicity.

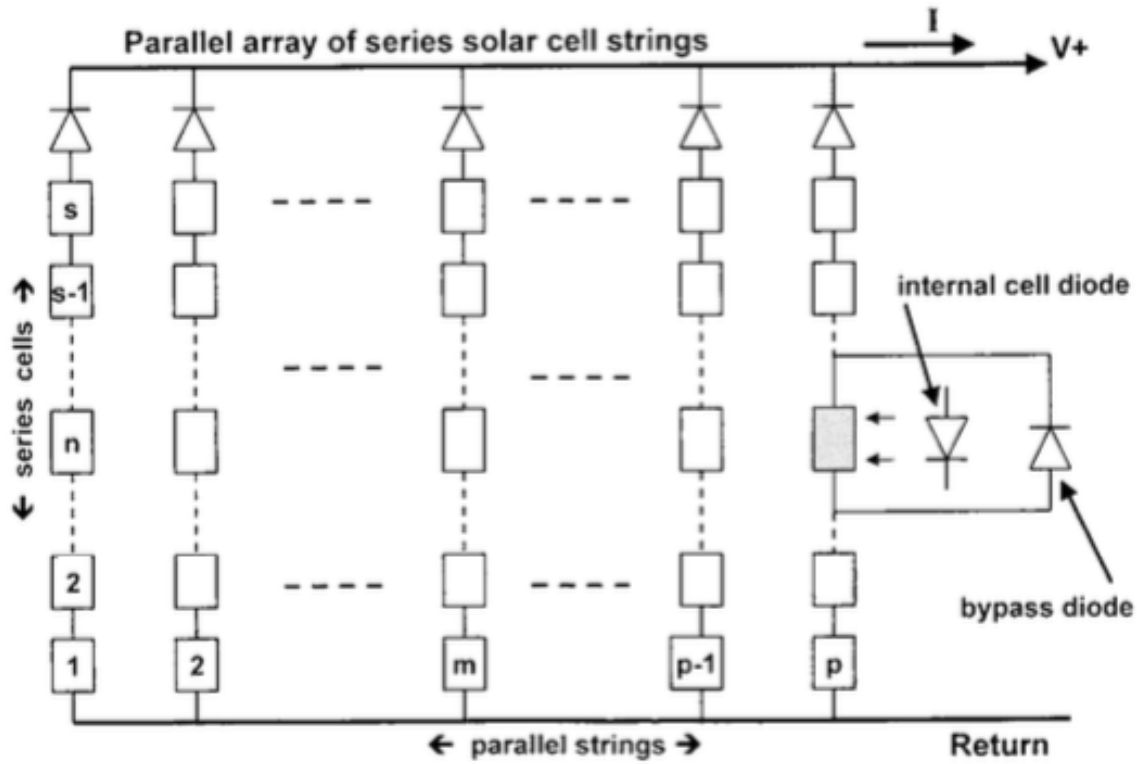


Figure 2.1: Typical structure of a solar array. With the courtesy of [14].

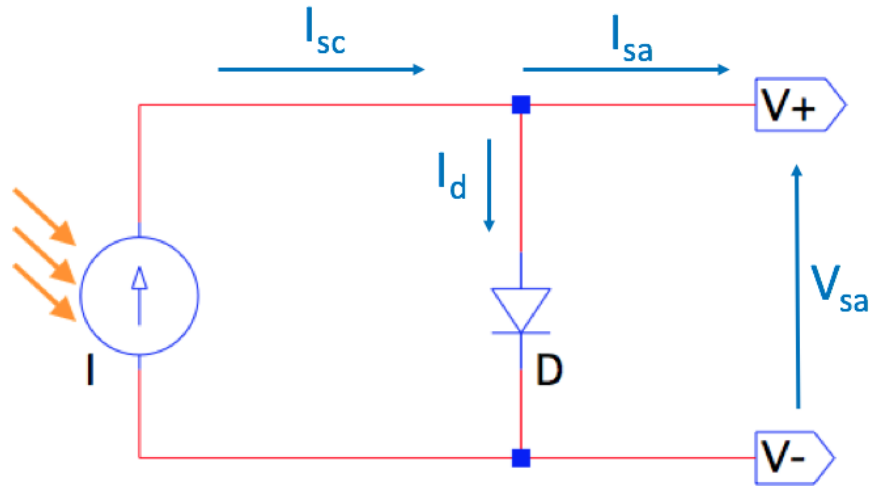


Figure 2.2: Simplified electrical circuit of a solar cell.

The current source models the photo-generated current resulting from the conversion¹ of the light energy into electrical energy. Next to that, a diode is added in parallel to model the amount of current being diverted from the load due to different recombination effects.

The equations linking this diverted current I_d and the voltage V_d across the diode terminals are the

¹This conversion process is based on the photovoltaic effect.

following:

$$I_d = I_o \left(e^{V_d/V_t} - 1 \right) \quad (2.1)$$

$$V_t = \frac{kT}{q} N_i \quad (2.2)$$

where:

- I_o is the diode saturation current (in $[A]$)
- k is the Boltzmann's constant ($= 1.3806 \cdot 10^{-23} [J/K]$)
- T is the cell's temperature (in $[K]$)
- q is the electron charge ($= 1.6022 \cdot 10^{-19} [C]$)
- N_i is the diode ideality factor (number close to 1 in practice, here we consider that $N_i = 1$)

If several cells are connected in series, the same model can be used but the voltage V_t has to be multiplied by the number of cells; the voltage measured across the string is then multiplied by the same number. On the contrary, a parallel connection maintains the same voltage but sums up their currents.

In the end, under a voltage V_{sa} , a solar array delivers a current I_{sa} given by:

$$I_{sa} = I_{sc} - I_o \left(e^{V_{sa}/V_t} - 1 \right) \quad (2.3)$$

where I_{sc} represents the photo-generated current (which corresponds to the short-circuit current in this simplified model).

2.1.3 I-V and P-V characteristics

A solar cell (and by extension a solar array) is often represented by its "I-V" and "P-V" characteristics. These curves, represented in figure 2.3, describe its possible operating points under given conditions (irradiance and temperature).

From the upper graph of figure 2.3, we can state that a solar array can be assimilated to a current source ($I_{sa} \approx I_{sc}$) if its voltage is sufficiently smaller than V_{MPP} . However, if the voltage continues to increase, the current starts to drop significantly until zero (in open-circuit conditions).

As it can be seen from the lower graph, the electrical power produced by the solar array also strongly depends on its operating voltage, which is defined by the circuit connected to its terminals. Several so-called "maximum power point tracking" (MPPT) algorithms have therefore been developed to force the solar array to work at V_{MPP} , and then to produce as much power as possible.

The last point worth mentioning here is that the slope (dP/dV) of the "P-V" curve is :

- negative before the MPP,
- zero at the MPP,
- and positive after the MPP.

This simple observation is one of the key aspects used by the MPPT algorithm evaluated in this report.

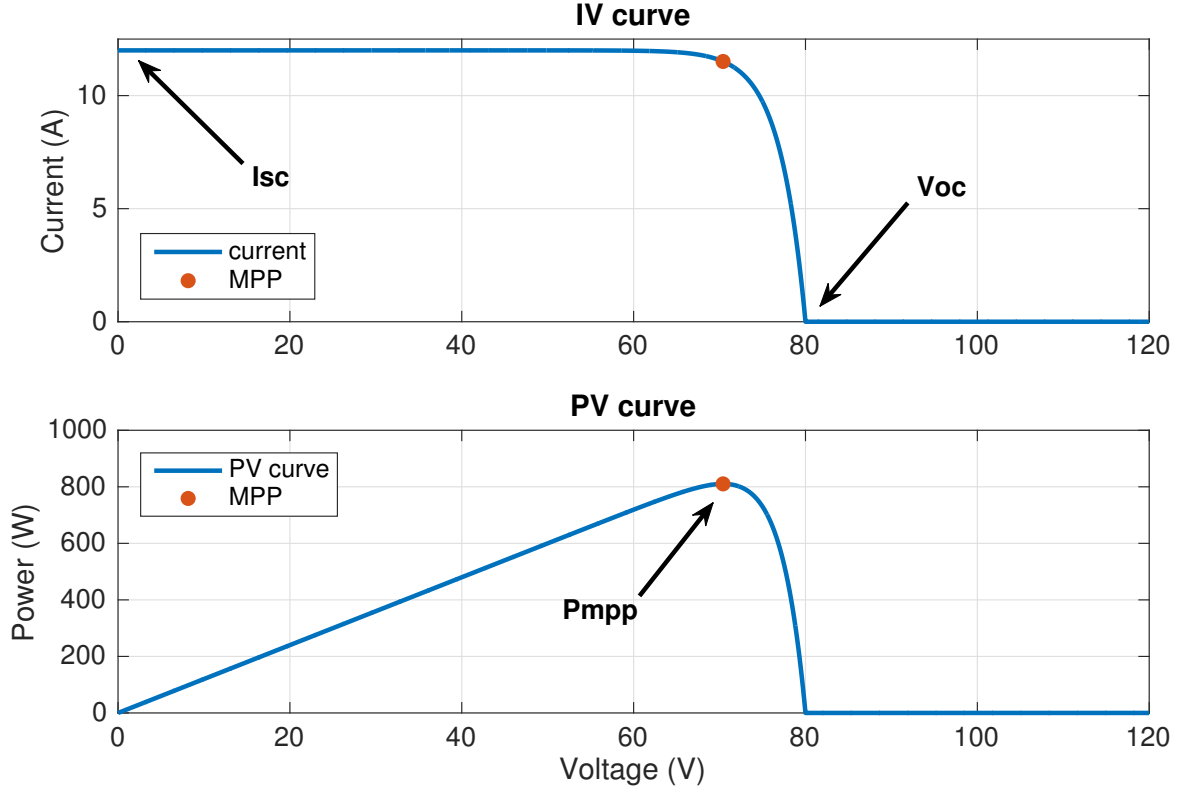


Figure 2.3: I-V and P-V characteristics of the solar array considered in this paper (at 25°C).
 I_{sc} = short-circuit current, V_{oc} = open-circuit voltage, MPP = maximum power point.

2.1.4 Effect of the temperature

As stated before, the characteristic curves presented in the previous section vary with the environmental conditions. An important factor is the temperature of the P-N junction, which typically varies from -100 to 100°C .

The temperature dependence of the solar array can be taken into account as follows :

- the short-circuit current I_{sc} is modified: $I_{sc}(T_1) = I_{sc,298} (1 + \alpha_{I_{sc}}(T_1 - 298))$, where $\alpha_{I_{sc}} > 0$
- the open-circuit voltage V_{oc} is modified: $V_{oc}(T_1) = V_{oc,298} (1 + \beta_{V_{oc}}(T_1 - 298))$, where $\beta_{V_{oc}} < 0$
- the thermodynamic voltage V_t varies according to the equation 2.2.

The impact of these temperature deviations are depicted in figure 2.4.

2.1.5 Effect of the illumination

The solar flux irradiating the solar array obviously modifies the electrical power that it can produce. In the practical range of operation, the light intensity does not affect the photo-conversion efficiency η . The relation between the photo-generated current I_{ph} and the light power P_{light} caught by the array can be approximated as [2]

$$I_{ph} = K(T)\eta(T)P_{light} \quad (2.4)$$

with K being a temperature-dependent factor. For a given temperature, we can then assume that the photo-generated current is proportional to the incoming light power.

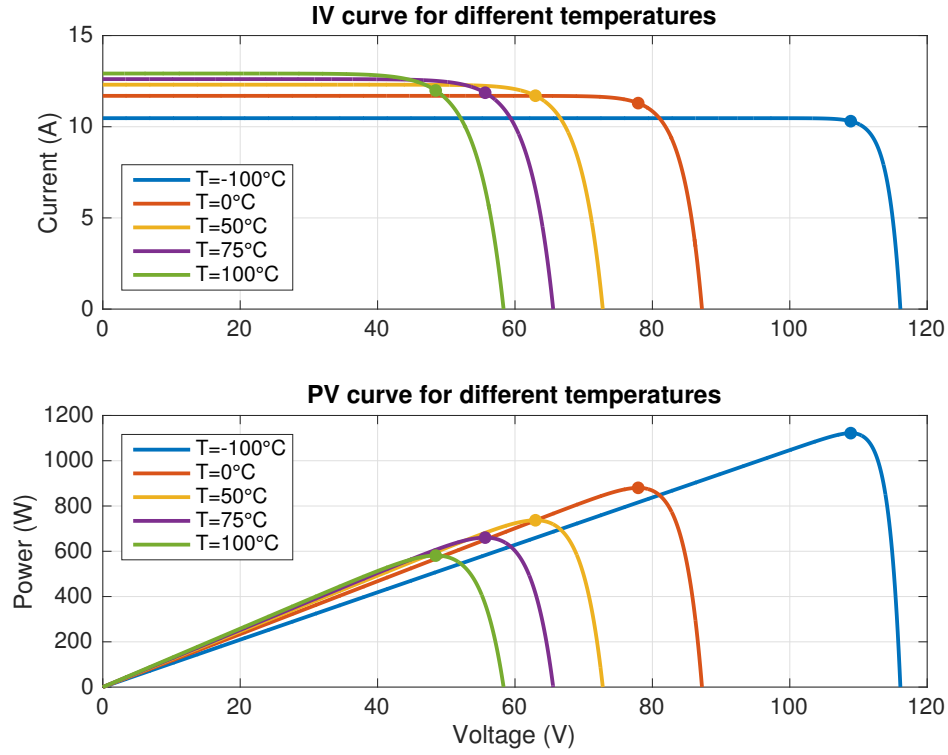


Figure 2.4: Evolution of I-V and P-V characteristics with temperature.

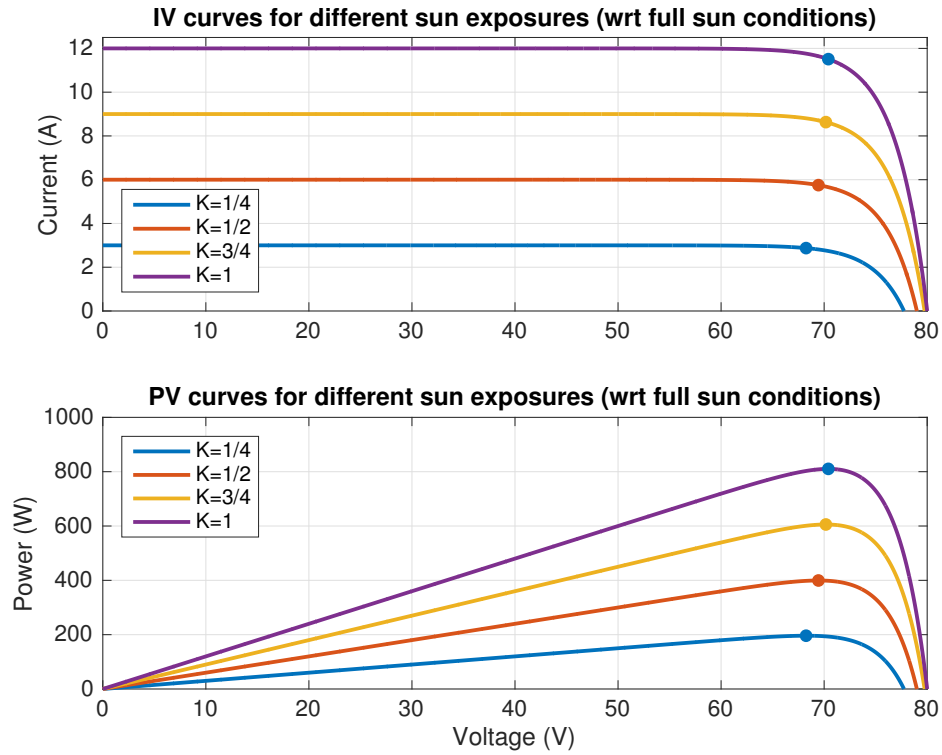


Figure 2.5: Evolution of I-V and P-V characteristics with the incoming light power.

The figure 2.5 depicts how the illumination affects the I-V and P-V characteristics of an array. As suggested in this figure, the open-circuit voltage also slightly varies in practice.

2.2 DC-DC converters and maximum power point tracking

If the solar arrays presented above were directly connected to the batteries, the latter would impose the operating voltage to the arrays. Unfortunately, this voltage is not necessarily equal to V_{MPP} , meaning that the solar arrays could work under their full potential.

To prevent this waste of energy, a common solution is to place a switched-mode dc-dc converter between the array and the bus. This controllable electronic circuit allows to adapt the voltage to the user needs.

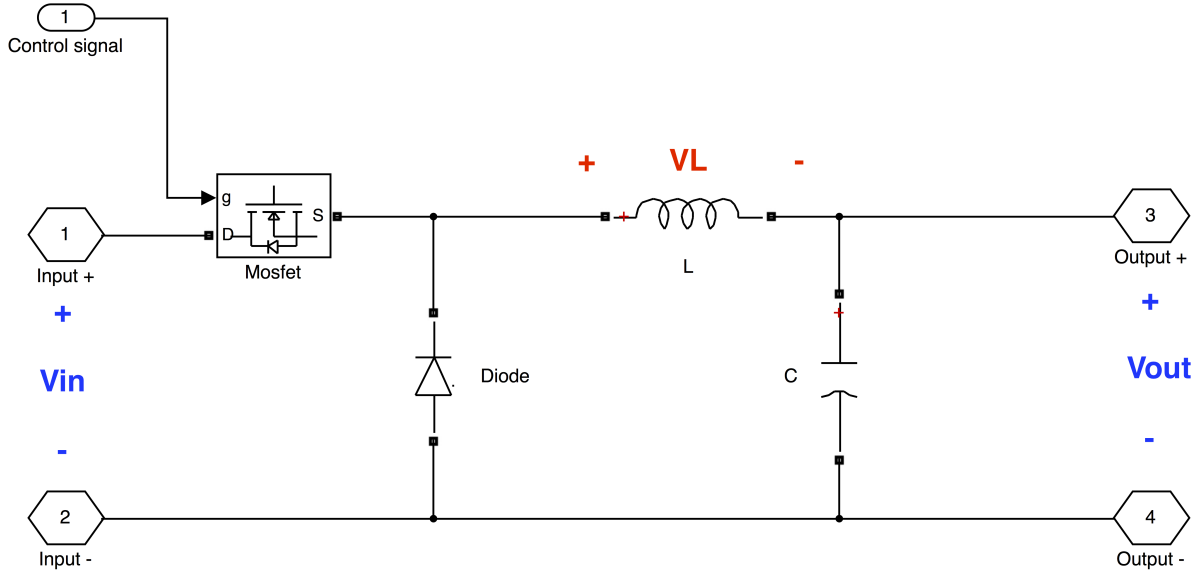


Figure 2.6: Schematic of a buck converter with its output LC filter.

The converter topology that will be used in our model is the well-known *buck* (or *step-down*) converter. This circuit, depicted in figure 2.6, first converts the input voltage in an AC pulsed signal using a switching device (like a MOSFET) and a diode, and then converts this signal back into a DC voltage by means of an LC filter.

The control signal, usually generated by pulse width modulation (PWM), is either *HIGH* or *LOW* and determines the state ("ON" during θT and "OFF" during $(1 - \theta)T$ seconds, with θ the duty cycle) of the switching device:

- during ON state, the switch conducts and the diode is blocked $\rightarrow V_L = V_{in} - V_{out}$
- during OFF state, the switch is open and the diode conducts the current $\rightarrow V_L = -V_{out}$

In steady state the inductor does not accumulate any energy, meaning that the mean voltage over a switching period T is equal to zero:

$$0 = \bar{V}_L = \frac{1}{T} \left(\int_{t_0}^{t_0+\theta T} (V_{in} - V_{out}) dt + \int_{t_0+\theta T}^{t_0+T} (-V_{out}) dt \right) \quad (2.5)$$

$$= (V_{in} - V_{out})\theta - V_{out}(1 - \theta) \quad (2.6)$$

$$= V_{in}\theta - V_{out} \quad (2.7)$$

Therefore, in a step-down converter operating in continuous conduction mode² (CCM), the input and output voltages are related to each other by

$$V_{in} = \frac{V_{out}}{\theta} \quad (2.8)$$

In our case the output voltage is fixed by the batteries; the input voltage can then be controlled through the duty cycle θ of the converter. The control of this converter is performed by a maximum power point tracker (MPPT) whose role is to continuously adapt the duty cycle (through the *control signal*) to keep V_{in} as close as possible to V_{MPP} .

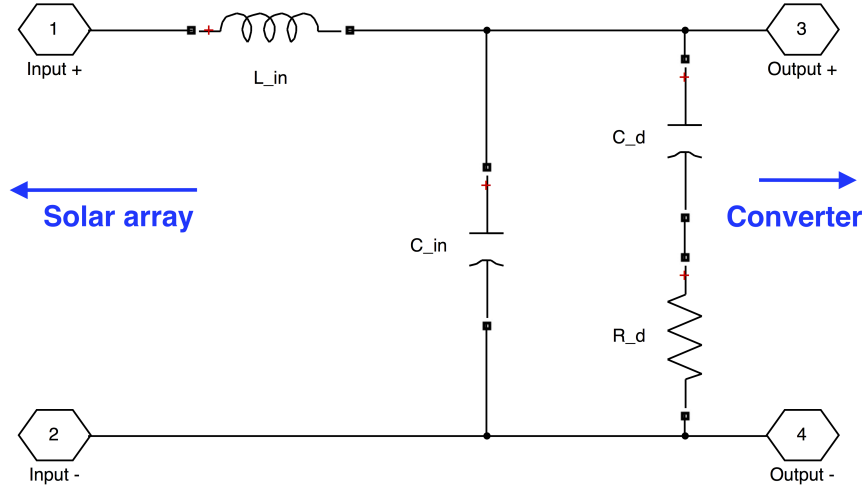


Figure 2.7: Parallel-damped LC filter usually placed between the solar array (on the left) and the converter (on the right).

In practice, an input filter (as represented in figure 2.7) is added between the solar array and the converter to avoid pulling a pulsed current out of the solar array, because such a situation would drastically reduce the power produced.

However, this low-pass filter has an inherent drawback: it adds some inertia to the system and then limits the bandwidth of the control system. When it is possible, its cut-off frequency should therefore be chosen in such a way that it does not interfere with the MPP tracker.

For land applications, lots of MPP tracking algorithms have been developed. Among them, we can cite the well-known *Perturb and Observe* (often referred to as P&O) or the *Incremental Conductance* algorithms.

The principle of the P&O algorithm is very simple. It increases or decreases the duty cycle θ_{i-1} by a small step $\Delta\theta$ to modify the operating point of the array. The resulting power P_i is then measured, and

- if the power has increased compared to the last measurement ($P_i > P_{i-1}$), it continues in the same direction (i.e. increasing or decreasing θ_{i-1});
- if the power has decreased compared to the last measurement ($P_i < P_{i-1}$), it goes back in the opposite direction.

²The current in the inductor is always positive during the whole switching period.

Its main drawback is that it never knows when the MPP has been reached. Therefore, it continuously jumps from one operating point to another around the MPP and this induces a voltage ripple which reduces the efficiency. To reduce this ripple, the duty cycle step can be chosen smaller, but this solution adds inertia to the system since more cycles will be needed to cover the same voltage range.

Unlike the P&O, the Incremental conductance algorithm has the advantage to know when the solar array operates at its MPP, thereby eliminating or at least reducing the ripple. However the additional computation complexity of this solution compared to the efficiency improvement sometimes does not worth it. This method is based on the slope of the P-V curve ($dP/dV = I + V[dI/dV]$):

- if the slope is negative ($dP/dV < 0 \Rightarrow dI/dV < -I/V$): the solar array operates on the left side of the MPP;
- if the slope is positive ($dP/dV > 0 \Rightarrow dI/dV > -I/V$): the solar array operates on the other side;
- if the slope is zero ($dP/dV = 0 \Rightarrow dI/dV = -I/V$): the solar array produces as much power as it can.

However, most of these MPPT are usually implemented onto microprocessors, which is generally avoided in space-borne systems. It may happen in some cases that the MPPT relies on the main satellite's computer to operate, but it is usually a costly solution because it increases the development efforts and the risks. For that reason, the majority of MPPT algorithms implemented in space are based on analog control loops and must therefore preferably stay quite easy to implement.

2.3 Synchronous demodulation and correlation

Since the MPPTs that will be implemented in chapters 4 and 5 will be based on the principles of synchronous demodulation and autocorrelation, these two concepts will be briefly introduced in this section.

2.3.1 Synchronous demodulation

The principle of synchronous detection is based on the orthogonality property of sinusoidal signals. If a sine signal is multiplied by another sine and then integrated over a long period of time (much longer than the sine periods), the resulting signal $y(t)$ will be close to zero if their frequencies are different, and close to 1/2 if they are the same (a phase-shift would reduce that value):

$$y(t) = \frac{1}{T} \int_t^{t+T} A_1 \sin(\omega_1 \tau + \phi) A_2 \sin(\omega_2 \tau) d\tau \quad (2.9)$$

$$= \frac{1}{T} \int_t^{t+T} \frac{A_1 A_2}{2} (\cos((\omega_1 - \omega_2)\tau + \phi) - \cos((\omega_1 + \omega_2)\tau)) d\tau \quad (2.10)$$

Depending on the frequency matching:

$$\text{if } f_1 = f_2 \Rightarrow y(t) \approx \frac{A_1 A_2}{2} \cos(\phi) \quad (2.11)$$

$$\text{if } f_1 \neq f_2 \Rightarrow y(t) \approx 0 \quad (2.12)$$

Now, if we have a modulated signal

$$x(t) = A_1 \sin(\omega_1 t) + \sum_{k=0}^{\infty} A_{x,k} \sin(\omega_k t) \quad (2.13)$$

whose amplitude A_1 is the information that we want to extract, and containing other parasitic signals; a receiver equipped with

- an ideal³ oscillator, to produce a signal $A_c \sin(\omega_1 t)$ called *carrier*;
- a mixer, to multiply the incoming signal with the carrier;
- an ideal⁴ low-pass filter, to integrate the signal from the multiplier;

would therefore be able to extract the useful information, with a potential offset due to the parasitic signal (if it contains a component at a frequency ω_1):

$$y(t) = \frac{A_c}{2}(A_1 + A_{x,1}) \quad (2.14)$$

2.3.2 Cross-correlation

The cross-correlation is a well-known technique used to measure the similarity of two signals s_1 and s_2 . The idea is to compute "how similar to s_1 " every delayed version of s_2 is. The correlation is then a function of the delay. If the two signals are real, their cross-correlation can be expressed as:

$$y(\tau) = (s_1 \star s_2)(\tau) = \int_{-\infty}^{\infty} s_1(t) s_2(t + \tau) dt \quad (2.15)$$

The synchronous demodulation presented above can then be seen as a particular case of cross-correlation using sinusoidal signals. With an ideal oscillator ($\phi = \tau = 0$), the maximum correlation would be obtained, resulting in an output signal of $y(0) = (s_1 \star s_2)(0)$.

The material required to perform a cross-correlation is then the same as for synchronous demodulation. The only difference is that the oscillator does not necessarily produce a sinusoidal signal.

³Without phase-shift.

⁴Completely suppresses non-DC components.

Chapter 3

Solar array regulation in satellites: state of the art

The electrical power systems embedded in satellites are responsible for the on-board power management, control and distribution. Nowadays, lots of different architectures are present on the market but the global picture generally stays the same (see figure 3.1). What differs is the way to implement the basic functions, namely the solar array (SA) conditioning, the bus regulation and the power distribution.

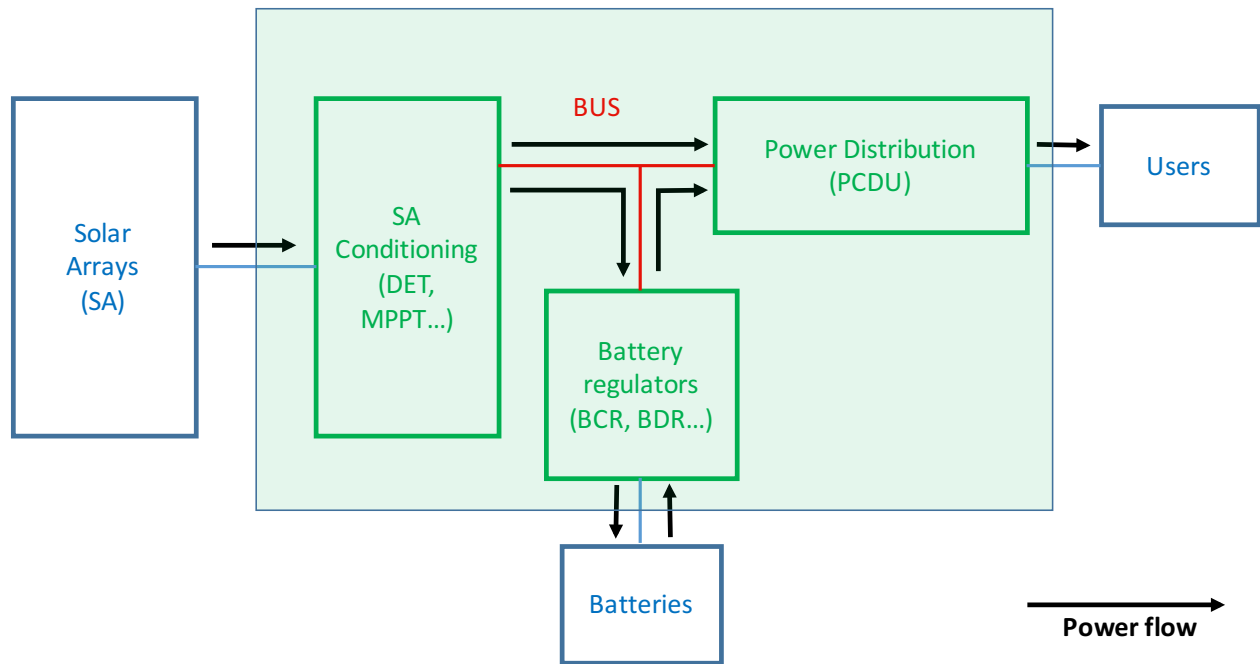


Figure 3.1: General structure of the electrical power system.

This chapter will be divided in two sections, the first section will be devoted to the SA power conditioning techniques (DET and MPPT) while the second will be focused on the most famous bus regulation schemes. Since the power distribution is of lower interest in this analysis, the topic will not be discussed.

3.1 Solar array conditioning

Among the existing topologies, two categories have to be distinguished:

- *direct energy transfer* (DET) systems, where the bus is connected directly to the SA;
- *non-direct energy transfer* systems where the bus voltage is decoupled from the SA by means of dc-dc converters (or more generally by active components). Usually, these converters are controlled by *maximum power point tracking* (MPPT) algorithms.

3.1.1 DET systems

The main advantage of DET systems is their simplicity: it saves weight, costs and power losses. This solution is for instance well-suited in missions where the I-V characteristics do not vary significantly during the mission, and whose period of sun exposure is long enough to recharge the batteries at a lower rate than if the SA was operating at MPP.

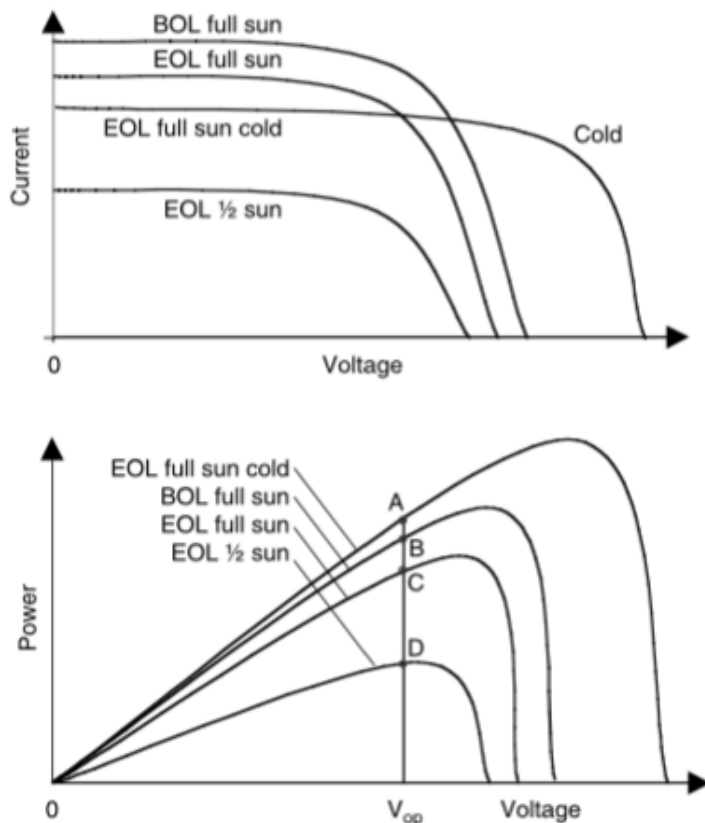


Figure 3.2: Evolution of the solar array I-V and P-V curves with sun exposure, temperature and ageing effects.
With the courtesy of [14].

Since the SA operates at the bus voltage, it does not produce as much power as it can; we usually say that the extracted power is in average 10% lower than the MPP. For that reason, the SA has to be oversized compared to a MPPT solution.

Moreover, because of the continuous degradation of the array, the I-V and P-V curves evolve with time as represented in figure 3.2. In DET systems, the operating point has to be chosen according to the end-of-life (EOL) characteristic and in non-optimal sun exposure conditions, thereby wasting a significant portion of the available power at the beginning-of-life (BOL). In such situations, the MPP tracker would adapt the operating point to the conditions and stay close to the peak power point (when necessary).

The inherent coupling between the array and the bus also reduces the flexibility regarding the components selection. Indeed, for a given technology, the number of cells per string has to be chosen in accordance with the selected bus voltage.

The DET topologies can be classified in two categories:

- shunt regulation: the excess of SA power is suppressed by shunting several sections of an array;
- series regulation¹: the power is transferred to the bus through a power regulator.

¹To be correct, series regulators should be placed in the non-DET systems; but the following section will focus on MPPT systems.

Shunt regulators

The most basic topology is known as the *linear shunt regulator* and was a common choice for small low-power satellites (see figure 3.3). The principle is simple: all the power that the loads do not use is diverted from the bus to be dissipated through transistors (and sometimes also resistors); the transistor's control signal determines the amount of current to draw from the bus.

Its main drawback lies in the excessive heat generation that makes the task of thermal designers more difficult. For that reason, this topology has been replaced in most applications by switching regulators.

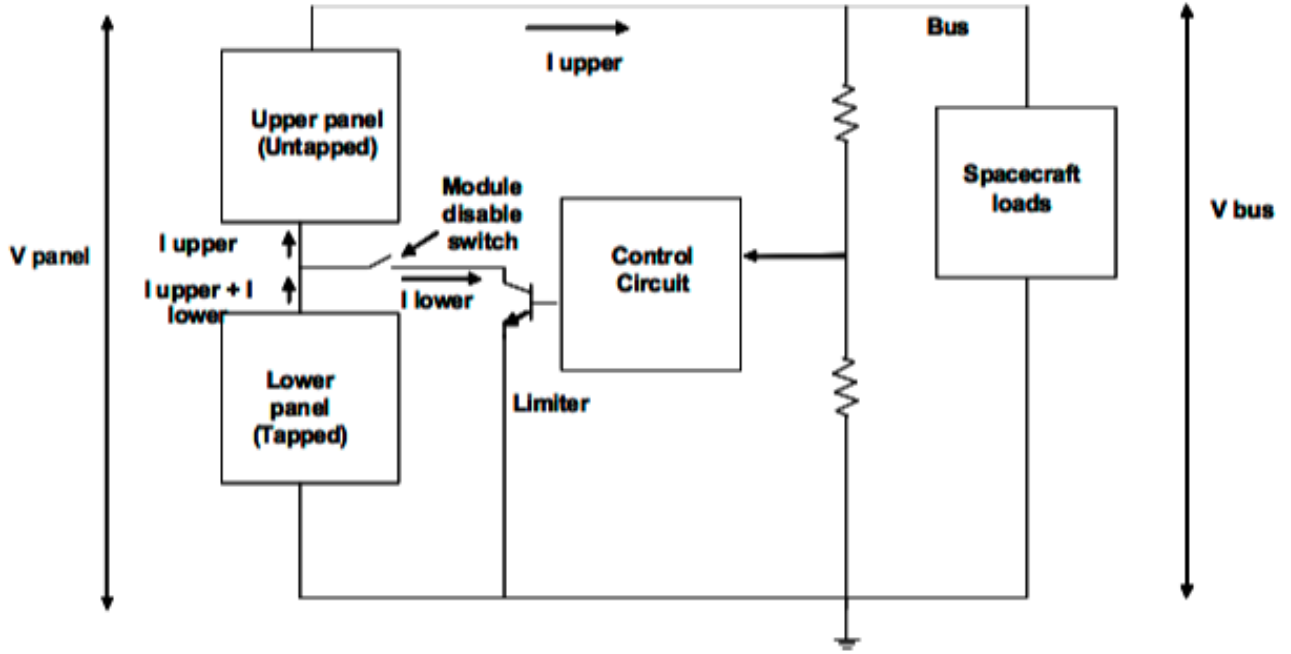


Figure 3.3: Architecture of a linear shunt regulator.

With the courtesy of [13].

A well-known switching shunt regulation scheme is the S3R architecture, which is mainly used in high power systems² and in regulated bus topology (see section 3.2.3). The idea of a *switching shunt regulator* is to divide the SA into discrete sections that are switched on and off depending on the power requested by the loads (see figure 3.4). Each switching device is associated to a comparator having two predetermined hysteresis thresholds. These thresholds are slightly different for each switch such that a single voltage is sufficient to control all the comparators. This voltage therefore defines the amount of current delivered by the SA, and is itself determined by an error amplifier comparing the bus voltage with a predetermined value (e.g. fixed by means of a zener diode).

To avoid shunting the whole bus, an additional diode is placed between each switch and the bus. For safety reasons, a second diode is also added in series with the first to protect the bus in case of a diode failure; but this additional safety margin comes at the cost of a reduced efficiency.

The particularity of this type of shunt regulator is that one of the switches is controlled in a PWM fashion (all the others are either on or off). The advantage is that the power sent on the bus can be controlled with precision without dividing the array into lots of small sections being either on or off. This approach also benefits from a reduced power dissipation compared to linear regulators, but at the cost of extra EMI generation due to the switching harmonics.

²E.g. this solution has been widely used in European geosynchronous satellites.

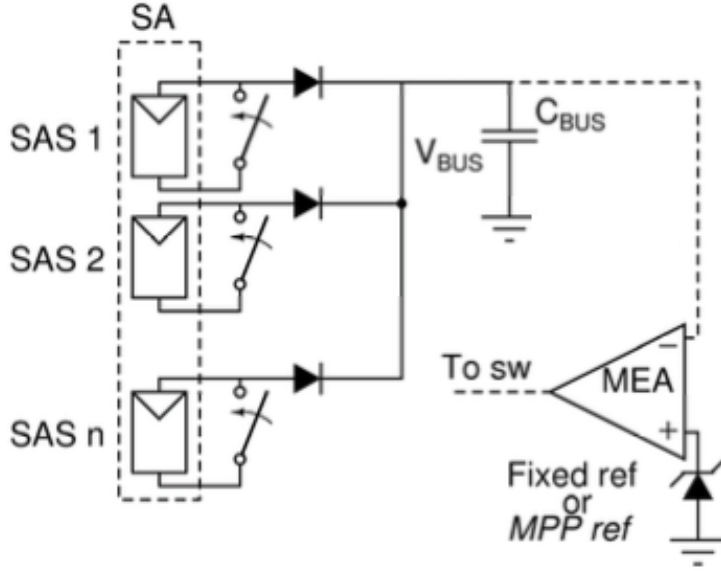


Figure 3.4: Illustration of the S3R's shunt principle, where a SA is divided in several sections (SAS).
With the courtesy of [4].

However, when the S3R is used along with very high power sources in GEO or high power LEO satellites, the BCR (battery charge controller) of the regulated bus becomes too bulky, which reduces the benefits of this topology (known for its very interesting mass/power ratio). In order to solve this problem, the S4R topology (sequential switching shunt series regulator) has been developed by the ESA. The SA is still connected to the bus through a shunt module as for the S3R, but the BCR is replaced by a series regulator between the SA and the batteries. This series switching regulator is based on the same principle as the shunt presented above, but the power flowing through the transistor goes to the batteries instead of shorting an array's section.

Series regulators

As explained in the preceding paragraph about S3R, the blocking diode has to be doubled for safety reasons. This second diode dissipates a non-negligible power because of the associated voltage drop. A topology called S2R (series switching regulator, represented in figure 3.5) has therefore been developed to replace this diode by a transistor whose voltage drop during ON state is lower than that of a diode, thereby reducing the losses. A snubber circuit is often placed in parallel with that transistor to prevent it from burning during high transients caused by the SA capacitance.

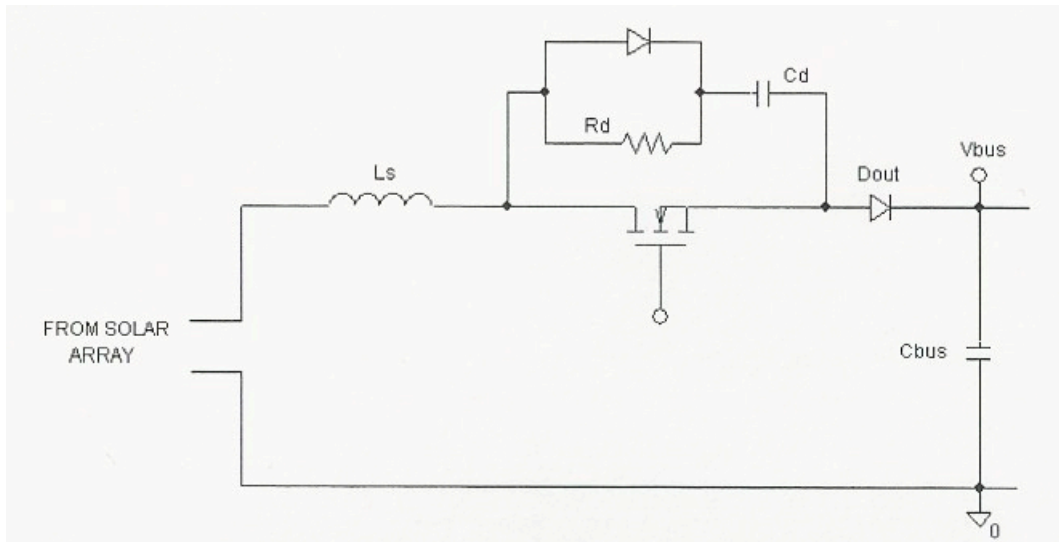


Figure 3.5: Illustration of the S2R principle (this circuit is duplicated for each section of the SA). With the courtesy of [1].

3.1.2 MPPT systems

Unlike DET systems, most MPP trackers are able to extract almost all the energy that SAs can produce, whatever the conditions (temperature, sunlight exposure, life-related SA degradations, battery state or failures). In missions where the satellite undergoes sensitive flux or temperature variations³, or when the satellite's constraints are non-negligible in terms of size and mass, the MPPT solution is often preferred to its DET counterpart; indeed, it allows to reduce the size of the SA as well as that of the batteries. Moreover, the decoupling introduced by the converter allows a greater flexibility in the components' selection, since it alleviates the matching requirements.

The main drawbacks of MPP trackers mainly correspond to the advantages of DET solutions, i.e. the system becomes more complex and the additional series elements dissipate more power, thereby lowering the converter's efficiency. In space, the problem of thermal dissipation is also a real issue since there is no natural convection nor conduction with an external medium; the only way to evacuate the heat (internally generated or due to the sun's exposition) is by radiation on the dark side of the satellite, i.e. the side which is not facing the sun. However, high temperature gradients between different parts of the satellite are also an important issue because it causes the hot parts to expand while the others do not which creates important mechanical stresses. For that reason, heat pipes with a high thermal conductivity are placed in the satellite to transport the heat from the hot spots to the dark side.

It should be noted that the MPPT does not extract the maximum power all the time. As long as the loads and batteries requirements exceed the power produced, the SA operates at its MPP; but when the needs drop below the SA's capabilities, the operating point is shifted to balance the power transfer and avoid dissipating the power difference.

Plenty of MPP tracking systems have already been developed and many patents and scientific papers are published in this area, as shown in figure 3.6. Among them, we can distinguish those that are based on simple assumptions or measurements (called "indirect MPPT") from those that really track the MPP ("direct MPPT") [10].

The first category's advantage is its simplicity but it does not really operate at MPP, it is an estimation. Therefore, important deviations from the initial model may lead to significantly lower efficiencies. Here are two common solutions:

- the operating voltage is regulated based on the measured SA temperature;
- the SA voltage is set to a constant fraction of the open-circuit voltage (the fraction depends on the technology in use) which is measured either by periodically quickly disconnecting the loads or preferably thanks to a pilot cell used for that purpose. There is also an alternative solution based on a fraction of the short-circuit current.

The other MPPTs are based on current and/or voltage measurements and are therefore able to track the actual MPP, whatever the conditions. However, it often comes at the cost of a higher complexity. Among them, we can find

- the "P&O" discussed in the previous section;
- the bus current maximization;

and many others. The following paragraphs will detail two other analog direct MPP trackers.

³Typically in LEO or in planetary missions (e.g. in the MESSENGER spacecraft launched by the NASA to orbit the Mercury planet facing temperatures from -150 to 270°C) [14].

MPPT Technique	PV Array Dependent?	True MPPT?	Analog or Digital?	Periodic Tuning?	Convergence Speed	Implementation Complexity	Sensed Parameters
Hill-climbing/P&O	No	Yes	Both	No	Varies	Low	Voltage, Current
IncCond	No	Yes	Digital	No	Varies	Medium	Voltage, Current
Fractional V_{OC}	Yes	No	Both	Yes	Medium	Low	Voltage
Fractional I_{SC}	Yes	No	Both	Yes	Medium	Medium	Current
Fuzzy Logic Control	Yes	Yes	Digital	Yes	Fast	High	Varies
Neural Network	Yes	Yes	Digital	Yes	Fast	High	Varies
RCC	No	Yes	Analog	No	Fast	Low	Voltage, Current
Current Sweep	Yes	Yes	Digital	Yes	Slow	High	Voltage, Current
DC Link Capacitor Droop Control	No	No	Both	No	Medium	Low	Voltage
Load I or V Maximization	No	No	Analog	No	Fast	Low	Voltage, Current
dP/dV or dP/dI Feedback Control	No	Yes	Digital	No	Fast	Medium	Voltage, Current
Array Reconfiguration	Yes	No	Digital	Yes	Slow	High	Voltage, Current
Linear Current Control	Yes	No	Digital	Yes	Fast	Medium	Irradiance
I_{MPP} & V_{MPP} Computation	Yes	Yes	Digital	Yes	N/A	Medium	Irradiance, Temperature
State-based MPPT	Yes	Yes	Both	Yes	Fast	High	Voltage, Current
OCC MPPT	Yes	No	Both	Yes	Fast	Medium	Current
BFV	Yes	No	Both	Yes	N/A	Low	None
LRCM	Yes	No	Digital	No	N/A	High	Voltage, Current
Slide Control	No	Yes	Digital	No	Fast	Medium	Voltage, Current

Figure 3.6: Overview and characteristics of different existing MPPT techniques. With the courtesy of [3].

Impedance matching

As early as in 1972, a MPPT concept based on impedance matching has been developed. First tested in the AEROS satellite and because of its success, it was subsequently reused in other missions such as Globalstar or Rosetta[8].

The impedance method is based on the fact that the dynamic Z_d and static Z_s impedances of the SA, defined as

$$Z_d = \frac{dV}{dI} \quad Z_s = \frac{V}{I} \quad (3.1)$$

are equal (in magnitude) at MPP: $Z_d = -Z_s$.

This relation comes from the fact that, at MPP, the slope of the P-V curve is zero. Therefore, it follows that:

$$0 = \frac{dP}{dV} = \frac{d(VI)}{dV} = I \frac{dV}{dV} + V \frac{dI}{dV} = I + \frac{V}{Z_d} \Rightarrow Z_d = -\frac{V}{I} = -Z_s \quad (3.2)$$

The circuit implementing this MPPT algorithm in Rosetta is depicted in figure 3.7. Based on two sample and hold circuits, two comparators, a flip-flop and an integrator, the circuit permanently oscillates around the MPP, and also requires the use of both current and voltage sensors. This implementation has the advantage to avoid complex calculations (such as multiplications), but still requires a non-negligible set of components, especially due to the sample and holds that have to be built based on discrete components. Moreover, the oscillating behaviour of the MPPT generates a voltage ripple causing extra (but reasonable) losses in the system.

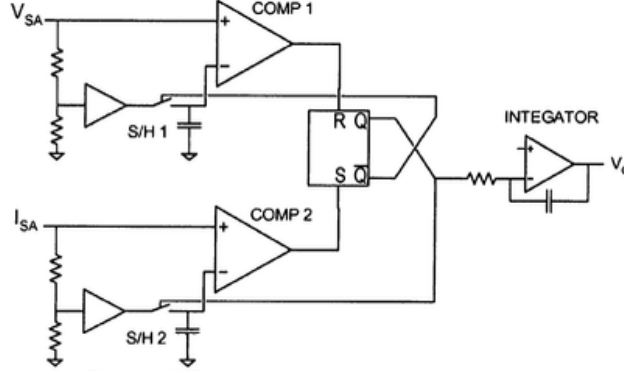


Figure 3.7: Circuit implementing the impedance matching method in Rosetta. With the courtesy of [8].

MPPT based on capacitive differentiation

A very simple MPPT technique based on capacitive differentiation has been proposed by Caldwell[1]. The principle lies here in the fact that the slope of the PV curve is equal to zero at MPP. This solution requires the SA voltage to be sensed and differentiated by a capacitor to control the converter's PWM. Let us assume that the SA starts in open-circuit conditions and that it slowly decreases towards the MPP. Once the MPP is exceeded, the sign of the derivative action will be reversed and will pull the system back to its MPP.

The simplicity of this solution makes it very attractive for space applications where the weight is an important issue. However, a major drawback of the capacitive differentiation method is that the voltage variations have to be relatively quick. Indeed, a slowly varying voltage does not generate a sufficient gradient to be detected by the capacitor and the associated control loop. This become even more a problem with the new SA technologies where the output capacitance of the array becomes more and more significant (because of a reduced number of cells in series), thereby filtering those desired voltage variations. On the contrary, the switching harmonics generated by the converter could be sensed by the control loop and interfere with the useful information. These two issues make that solution too fragile to be reliably used in a satellite; further improvements would be needed for this solution to become acceptable.

To conclude this part, we can state that the challenges inherent to the power conditioning are still far from being solved. The choice of using a DET or a MPPT system tightly depends on the mission, the budget and from the potential flight heritage of the material. It is also linked to the type of bus being selected for the mission, and this will be the topic of the next section.

3.2 Bus regulation schemes

There are three kinds of bus regulation schemes: the unregulated bus, the semi-regulated (or sunlight-regulated) bus and the fully-regulated bus. These topologies mainly differ in the implementation of the "Battery regulator" block of figure 3.1. Another type, the hybrid bus, also exists but it will not be detailed here since it is just a combination of two separate bus in parallel: one unregulated for high load transients, and one regulated devoted to "static" loads.

The choice is usually based on the mission. For instance if scientific payloads require precision or if specific loads need a thermal stability, a fully-regulated bus may be preferred. But it also depends on the power requirements of the satellite and on the user's flight heritage.

3.2.1 Unregulated bus

The so-called unregulated bus connects the bus directly to the batteries. The bus voltage therefore depends on their current state of charge. The inherent benefit of this topology is its simplicity, thereby minimizing power losses due to additional components. But on the other hand it requires more power regulation at the loads since the user usually has to tolerate up to $\pm 20\%$ of bus voltage variations[9].

The association of a DET system and this type of bus forces the SA to operate at the battery voltage, and an important issue comes at the end of the eclipse period. During eclipse, the batteries gradually discharge and the bus voltage decreases as well. At the eclipse exit, the user loads still need to be powered but batteries also need to be recharged. However the SA most probably operates far away from its MPP, therefore preventing it to produce enough energy to recharge the batteries (or at a slower rate than during the previous sun exposure). If a complete orbital period results in a significant battery discharge, after several cycles the system will stop working properly. Also, a short-circuit failure of a battery cell would cause the bus voltage to drop and then reduce the power extracted from the SAs.

When used along with a MPPT conditioning unit, this direct connection does not impact the operating point of the SA because of the switching regulator placed in between. The only drawback is that the efficiency of the converter may vary with the state of charge of the batteries.

Usually, this topology can be found in inexpensive LEO satellites (such as microsatellites, i.e. satellites ranging from 10 to 100 kg) used for Earth observation.

An unregulated bus is also particularly suited to pulsed loads since the batteries are free to discharge as quickly as they can. In the case of a regulated bus, the battery discharge controller (BDR) would require a careful design to allow such peaks to occur[9].

3.2.2 Sunlight regulated bus

Also called *partially regulated bus* or *semi-regulated bus*, this topology only regulates the bus voltage during sun exposure. This improvement is achieved thanks to a battery charge controller (BCR) placed between the bus and the batteries (see figure 3.8).

When the sunlight is available, two situations may occur:

- if the power produced by the SAs exceeds the load requirements, the bus is decoupled from the batteries by the BCR that controls the battery recharge and regulates the bus voltage.
- if the loads need more power than what the satellite is currently producing, the batteries will momentarily help the SA and supply the difference. In this situation, the BCR is bypassed and the bus voltage drops to the battery voltage; meaning that the bus is not regulated any more.

During eclipse, the BCR is deactivated and the batteries have to deliver all the power required by the loads.

If it is associated to a DET solar array regulator, this solution presents an advantage over the unregulated bus: the operating point of the SA can be selected through the bus voltage. However, this combination also suffer from the so-called *lock-up* phenomenon briefly discussed above (and in the preceding section).

If the load is momentarily asking for more power than what is currently produced, both the bus and the SA voltage will drop to the battery voltage. This will cause the SA to produce less power and then hasten the batteries discharge, thereby reducing the bus voltage even more. The only way to unlock the system is to wait until the loads require less electrical power than what the array is currently producing. If it does not happen, the power system protections will be activated and most of the loads will be disconnected

from the bus to allow the batteries to recharge up to a sufficient level.

To avoid this latch-up issue, the SAs have to be oversized; but for large power systems, these mass and costs penalties lead to the choice of a fully regulated bus.

Here again, a MPP tracker would not suffer from that problem thanks to the inherent decoupling property of the dc-dc converter.

To avoid this lock-up phenomenon, this topology is mainly used in satellites with limited load power (less than 1500 W), low bus voltage (usually from 22 to 35V), and in missions where the batteries have enough time to recharge. Such conditions can be found in highly elliptical GEO missions or sun-orbiting missions [15].

The NEAR and CONTOUR space probes have for instance used this technology to manage the on-board power.

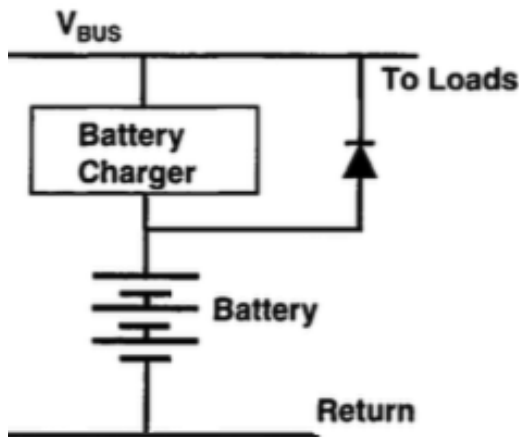


Figure 3.8: Illustration of a sun-regulated bus.
With the courtesy of [15].

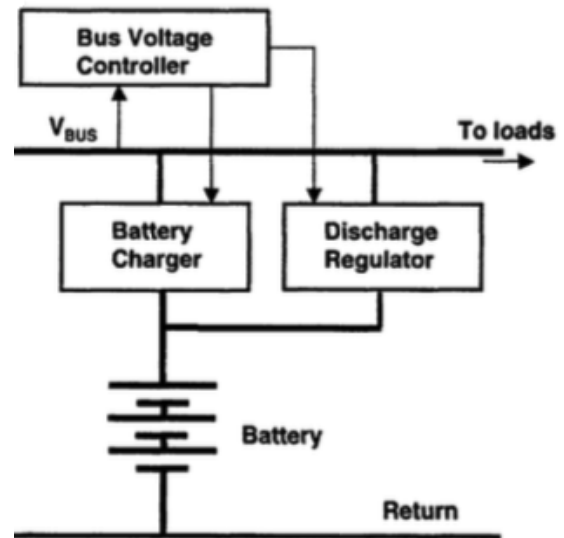


Figure 3.9: Illustration of a fully-regulated bus.
With the courtesy of [15].

3.2.3 Fully regulated bus

The most complex topology is the fully regulated-bus (see figure 3.9), since it continuously regulates the bus during the entire orbit period. The only difference with the previous topology is that it also contains a BDR instead of the discharge diodes⁴.

On the one hand, unlike the unregulated bus, a direct connection to loads lacking their own power supply is possible. And on the other hand, the constraints imposed on the filtering stage of the other loads can be alleviated since the expected bus voltage variations are usually designed to be way lower than with an unregulated bus. The size and the weight of these load's converters can then be reduced.

Thanks to the BCR and the BDR, the bus is always decoupled from the batteries, thereby leading to a more flexible battery selection process; the system is also immunised against the lock-up phenomenon present in the two other topologies.

Finally, the thermal design of the spacecraft becomes also simpler because the electric heater circuits deliver a constant heat at a fixed bus voltage[9].

⁴If used in a S4R regulated architecture, the BCR is replaced by a series regulator, as explained in section 3.1.1.

However, the two battery regulators increase the weight and the costs, and reduce the overall efficiency of the system. As a consequence, extra solar power is required (need for either more or bigger SAs). Furthermore, additional control loops have to be designed for these regulators; and the that of the BDR is especially complex to allow it to cope with the peak power demands during battery discharge periods.

Such systems equip most of the medium to very high power GEO satellites where a sufficient bus voltage is necessary to keep components relatively small and avoid thermal issues. For instance, the International Space Station (ISS) operates with several regulated busses[\[14\]](#). Nonetheless, many LEO science missions also employ regulated busses for the sake of precision.

Chapter 4

MPPT based on synchronous demodulation

This chapter will first introduce the principle of the maximum power point tracker implemented in this report. Subsequently, the equations modelling the system will be developed, and the main design trade-offs will be discussed in order to design an appropriate controller. The whole functional system will then be characterised and the chapter will finally end up with an identification of the potential issues and limitations of this solution.

4.1 Principle

As stated before, the mission of the peak power tracker is to control the converter in such a way that the solar array operates as close as possible to its maximum power point, thereby harnessing the full potential of the array.

Since the output voltage of the converter is assumed to be constant (and equal to the bus voltage), the desired solar array voltage can be selected by playing on the average duty cycle which controls the dc-dc converter (thanks to equation 2.8 for a step-down converter).

An MPPT based on synchronous demodulation adds a small perturbation (called *carrier*) on top of the average duty cycle of the converter. This will induce a similar voltage ripple at the input of the converter and then force the solar array voltage to oscillate around its current operating point. As represented in figure 4.1, this voltage oscillation will also generate power variations at the same frequency¹.

The key feature is that this power oscillation will either be in phase or in phase opposition with respect to the carrier, depending on the slope of the P-V curve:

- if the variations are in phase, it means that the slope of the P-V curve is positive. The solar array voltage is then lower than it should, and the duty cycle should be decreased.
- if the variations are in phase opposition, the slope of the P-V curve is negative. The controller should then on the contrary increase the duty cycle to reduce the solar array voltage.

Since the bus voltage is assumed to be constant, these power variations on the solar array side are also found at the output of the converter, in the bus current.

The AC component of this current is then sensed and demodulated to extract the sign of the P-V curves' slope which is sent at the input of the PID controller. Indeed, the ideal value of the demodulated signal would be 0, meaning that the solar array operates at MPP (where the slope is zero). As long as the PID input is not zero, it will modify the duty cycle to get closer to the MPP.

In other words, the carrier will modulate the slope of the the P-V curve inside the system, and this

¹This is demonstrated in appendix B.

information will be retrieved at the end of the demodulation stage. A synthetic view of the system that we just described is depicted in figure 4.2.

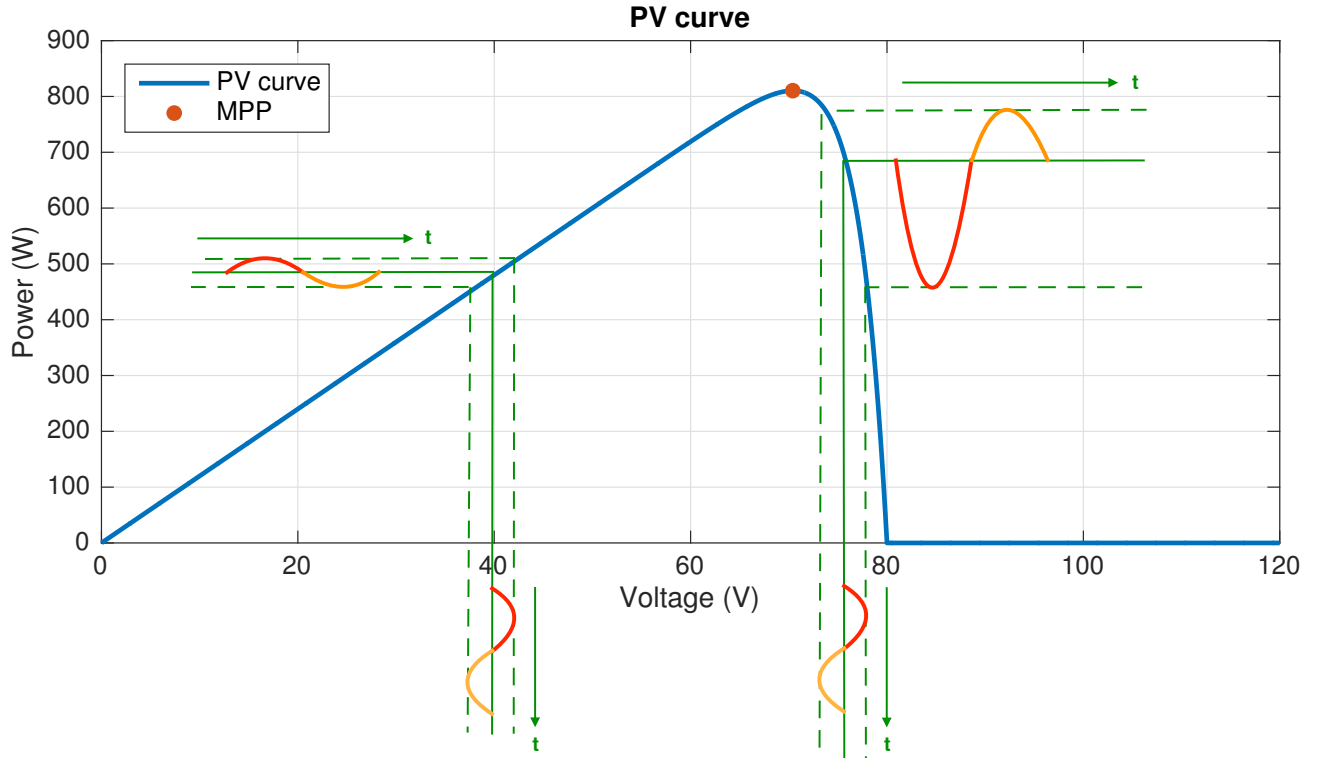


Figure 4.1: Illustration of the power variations caused by the voltage ripple on the P-V curve.

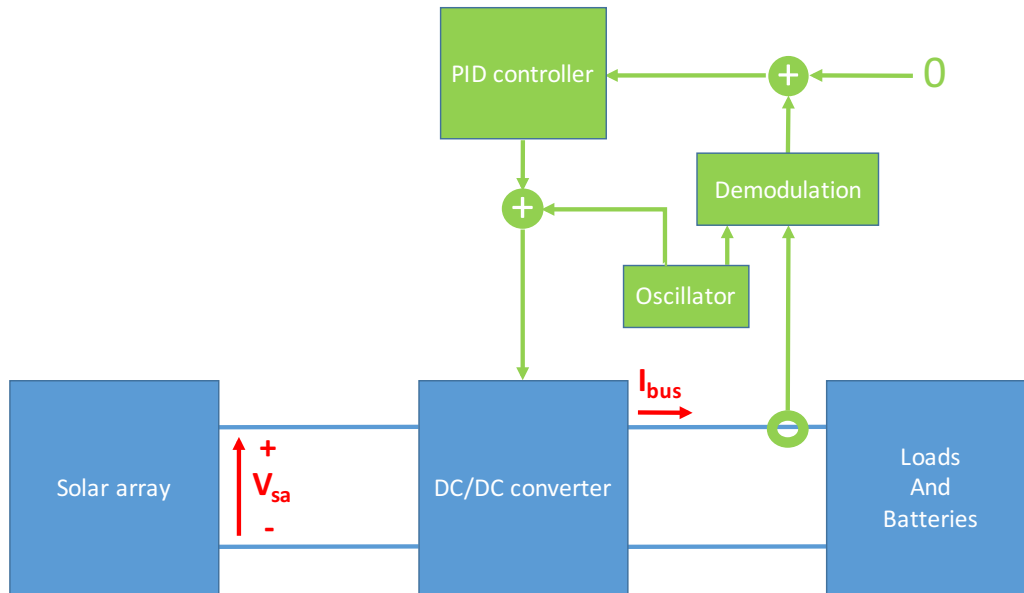


Figure 4.2: Schematic of the whole system. The electrical power system is represented in blue, while the control blocks are in green.

Main advantage

The main advantage of synchronous demodulation compared to other MPP trackers is that a single current measurement allows to control several converters (each of them being associated to a different solar array) as depicted in figure 4.3.

This comes from the fact that the information is here contained in the frequency domain. Therefore, the converters could use oscillators at different well-chosen frequencies (i.e. whose harmonics do not interfere with each other), and then demodulate the same current measurement with respect to their own carrier. In this way, each MPP tracker has the possibility to extract the information related to its own solar array. This principle is called *frequency-division multiplexing* (FDM).

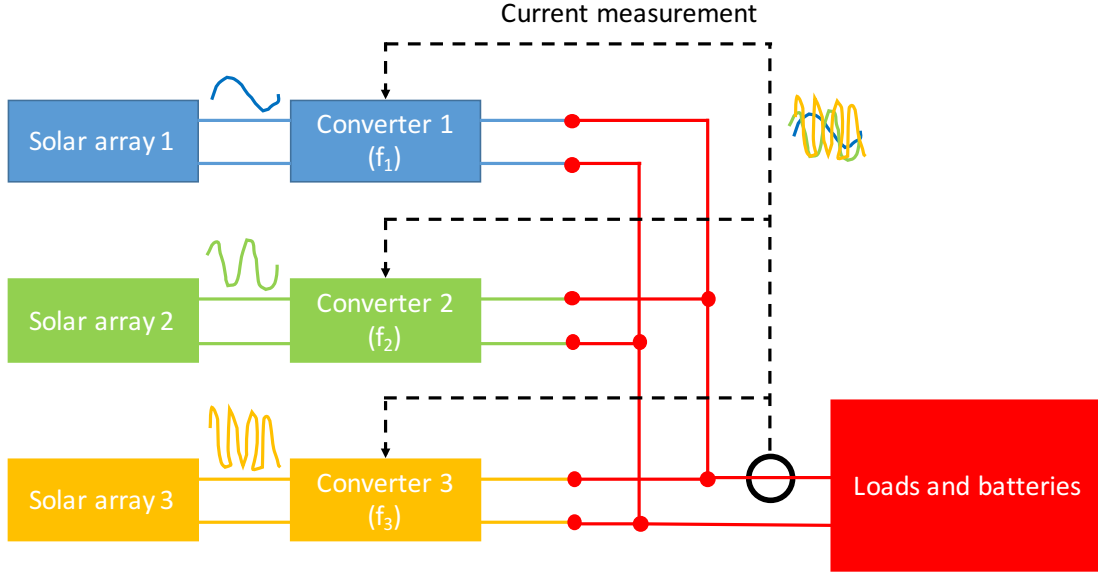


Figure 4.3: Illustration of the main advantage of synchronous demodulation in MPP tracking.

4.2 System modelling

Before entering into the details, here is the convention that will be used to label the different quantities:

- a_b represents an AC signal (without DC component);
- a_B represents the amplitude of an AC signal;
- A_B represents a DC value;
- A_b represents a complete signal, i.e. the sum of a steady-state component (A_B) and an AC signal (a_b);

The PID controller that will be designed later in this chapter will be part of a voltage-control loop. With the demodulated signal as input, it will therefore directly act on the solar array voltage V_{sa} . It will then be necessary to find the transfer function between the demodulated signal and the array voltage.

As a first step, it is required to find the relation linking the output current of the converter I_{bus} to the voltage of the solar array V_{sa} .

If we assume that the DC/DC converter is ideal (no power losses: $P_{sa} = P_{bus}$) and that the bus voltage is constant ($V_{bus} = V_{BUS}$), the current measured at the output of the converter is an image of the power delivered by the solar array:

$$I_{bus} = \frac{P_{bus}}{V_{bus}} = \frac{P_{sa}}{V_{BUS}} \quad (4.1)$$

As shown in figure 2.3, this power depends on the voltage (V_{sa}) at which the solar array operates. If we linearize the system around its operating point (V_{SA}), the voltage perturbation generated by the oscillator ($v_{sa} = v_{SA} \cos(\omega_p t)$) will cause the following output current variation:

$$\Delta I_{bus} = \frac{1}{V_{BUS}} \left[\Delta P_{sa} |_{V_{sa}=V_{SA}} \right] \quad (4.2)$$

$$= \frac{1}{V_{BUS}} \left[\frac{d(P_{SA})}{dV_{SA}} (v_{SA} \cos(\omega_p t)) \right] \quad (4.3)$$

This current perturbation is then be demodulated as follows:

1. first, the current is sensed and the information is converted in volts by a conversion factor K_{sens} [V/A] (a value of 100 [V/A] is chosen here);
2. then it is multiplied by the carrier ($v_{SA} \cos(\omega_p t)$) to bring the useful information back to DC;
3. finally it passes through a low-pass filter (LPF) whose cut-off frequency ω_c is chosen close to 0 [rad/s] to keep the DC component while reducing the potential parasitic signals at other frequencies.

Mathematically, this demodulated signal s_{demod} can be expressed as:

$$s_{demod} = LPF [\Delta I_{bus} K_{sens} v_{SA} \cos(\omega_p t)]_{\omega_c} = K_{sens} \left(\frac{v_{SA}^2}{V_{BUS}} \right) \frac{d(P_{SA})}{dV_{SA}} LPF [\cos(\omega_p t)^2]_{\omega_c} \quad (4.4)$$

$$= \frac{1}{2} K_{sens} \left(\frac{v_{SA}^2}{V_{BUS}} \right) \frac{d(P_{SA})}{dV_{SA}} LPF [1 + \cos(2\omega_p t)]_{\omega_c} \quad (4.5)$$

$$\approx \frac{1}{2} K_{sens} \left(\frac{v_{SA}^2}{V_{BUS}} \right) \frac{d(P_{SA})}{dV_{SA}} \quad (4.6)$$

This result of the equation 4.6 is the key of this MPP algorithm: all the factors are positive except for $\frac{d(P_{SA})}{dV_{SA}}$ whose sign depends on the operating voltage of the solar array. The demodulated signal will then have the same sign as the slope of the P-V curve, i.e. positive if $V_{SA} < V_{MPP}$ and negative if $V_{SA} > V_{MPP}$ (V_{MPP} being the array voltage at MPP).

4.3 Carrier design

In this section, the two degrees of freedom related to the sine carrier (frequency and amplitude) and the associated design trade-offs will be discussed.

4.3.1 Amplitude

The amplitude of the carrier plays a major role in the three following subjects: the system's gain, the cyclic power losses and the signal-to-noise ratio (often abbreviated as SNR).

Regarding the gain of the system, the equation 4.6 shows that the carrier's amplitude has a significant importance because it depends on its square (v_{SA}^2). As a consequence, if the controller is designed to reach a specific bandwidth, a modification of the carrier's amplitude would jeopardize the system dynamics.

The amplitude must therefore be chosen before the controller's design.

Furthermore, the carrier's amplitude also defines the amplitude of the movement on the I-V and P-V curves. But we should keep in mind that the wider the oscillation is, the more power is wasted every cycle. The graph drawn in figure 4.4 quantifies the losses (with respect to MPP) as a function of the carrier's amplitude. A quadratic fitting is also realized and attests that these are proportional to the square of the amplitude; this result is consistent with the fact that $P = V^2/R$ where R is the resistance of the array at MPP.

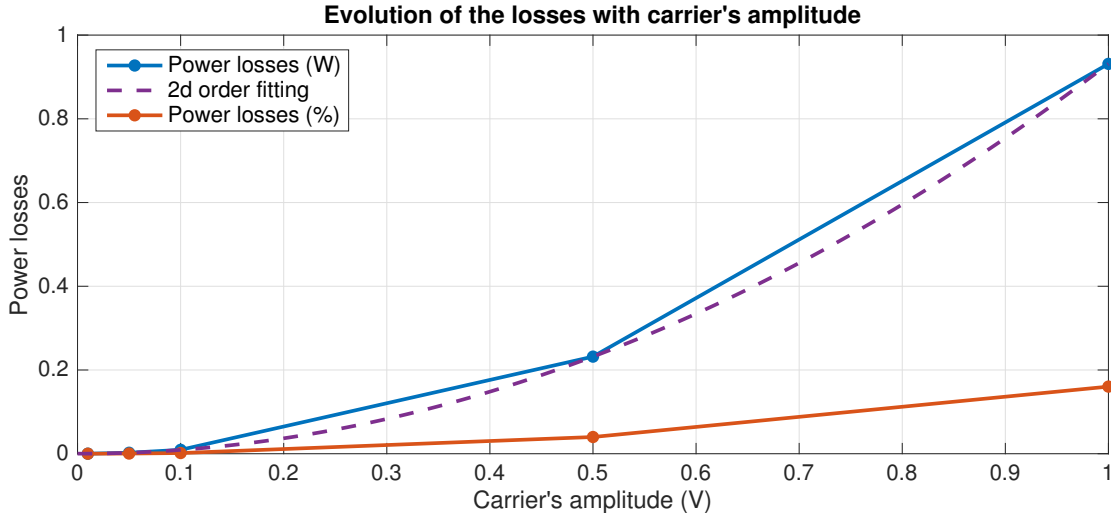


Figure 4.4: Evolution of the losses with the amplitude of the carrier at 100°C.

Last but not least, wide oscillations around MPP are not completely undesired, because it will generate larger (useful) bus current oscillations. Since the current measurement will most probably include other parasitic signals present on the bus side and interfering with the useful information, an increased useful power will be beneficial from the SNR perspective. A sufficient amplitude (and then power) is therefore required for the useful information to be distinguished from the noise in the demodulation stage.

At this stage, considering the different aspects presented above, an amplitude of

$$v_{SA} = 0.1 \text{ V} \quad (4.7)$$

is chosen, mainly to reduce the cyclic power losses.

4.3.2 Frequency

The frequency of the carrier represents the frequency where the information (i.e. the current operating point of the solar array) will be stored until reaching the demodulation stage. This frequency should therefore be carefully chosen to prevent undesirable effects from taking place. Its design will be based on the filters contained in the system and the potential perturbations.

The first elements to consider are the filters through which the carrier will have to propagate. These filters will be detailed in section 4.4.2 but we can already state that the system contains two low-pass filters (LPF): one at the input of the buck converter and the other at the output of the demodulation stage, whose cut-off frequencies are respectively 1kHz and 0.1Hz. Since the carrier signal has to reach the solar array, we can already conclude that its frequency must be smaller than 1kHz. Subsequently, the spectrum of this carrier will be split in two parts due to the product

in the demodulation stage: the first part will be located in DC and the other at twice its original frequency. Since the interesting information resides in the DC component, the other part has to be sufficiently attenuated by the filter located at the output of the demodulation stage.

Finally, it would be interesting to place the information at a frequency where external perturbations are not (or occasionally) present to avoid any interferences. In this case, the parasitic currents present on the bus are assumed to range from 40Hz up to 10kHz. It would therefore be tempting to use a frequency below 40Hz, but the double-frequency component would not be sufficiently attenuated by the output filter, resulting in a larger voltage ripple on the solar array voltage.

Based on these considerations, the carrier frequency was chosen to be

$$\boxed{f_p = 100 \text{ Hz}} \quad (4.8)$$

to benefit from a sufficient attenuation of the double-frequency component without losing the information in the system.

4.4 Controller design

This section will focus on the control loop regulating the solar array voltage. First, a global view of the system to control will be presented. Its fundamental building blocks (filters and gain) will then be discussed in more detail followed by the final PID filter's design.

4.4.1 Overview of the system

To make things simple, the system can be seen as the successive blocks that the voltage command produced at the PID's output will have to pass before reaching the PID's input. Let us here detail the path followed by this voltage command:

- At first, the converter's switch will introduce the PID's command as a virtual voltage source ΔV at the input of the converter². This voltage source will not be seen by the solar array directly, it will first have to pass the buck's input filter before modifying the solar array voltage.
- Once it has reached the solar array, this voltage source ΔV will modify the operating point of the array, and then also increment the value of its power slope (dP/dV) by a factor $\Delta(dP/dV)$. From the command's point of view, this corresponds to a gain of $[\Delta(dP/dV)]/[\Delta V] \approx d^2P/dV^2$.
- This $\Delta(dP/dV)$ will then be modulated (in amplitude) by the oscillations caused by the carrier $v_{sa} = v_{SA} \sin(\omega_p t)$, which will modify the amplitude of the power ripple ΔP by a factor $\Delta(dP/dV)v_{SA}$; it represents a gain of v_{SA} .
- Subsequently, this solar array power ripple is transformed in a current ripple at the output of the converter (gain of $1/V_{BUS}$), which is then sensed with a current transformer (gain of K_{sens}).
- In the demodulation stage, the mixer translates the measurement into a DC value (and another component at twice the carrier's frequency) with a gain of $1/2$, and the information is finally filtered to reject non-DC components before entering the PID controller.

In order to design the PID controller (see figure 4.5), we will then model the system by a constant gain (combining all the gains listed above) and two low-pass filters. These filters correspond to:

²Let us not confuse that this ΔV has nothing to do with the voltage ripple $v_{sa}(t)$ generated by the oscillator, these are completely independent.

- the LC input filter of the buck converter (2^{nd} order low-pass filter);
- the output filter of the demodulation stage (1^{st} order low-pass filter).

The system, represented in figure 4.6, also includes the saturations but these are not taken into account in the PID design.

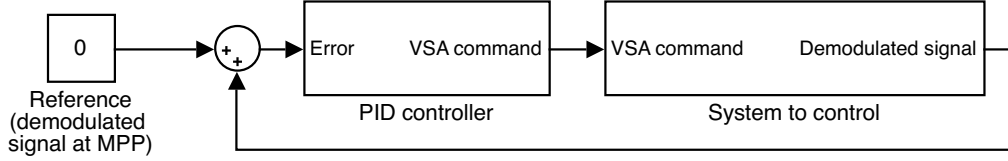


Figure 4.5: Main scheme used to design the PID filter.

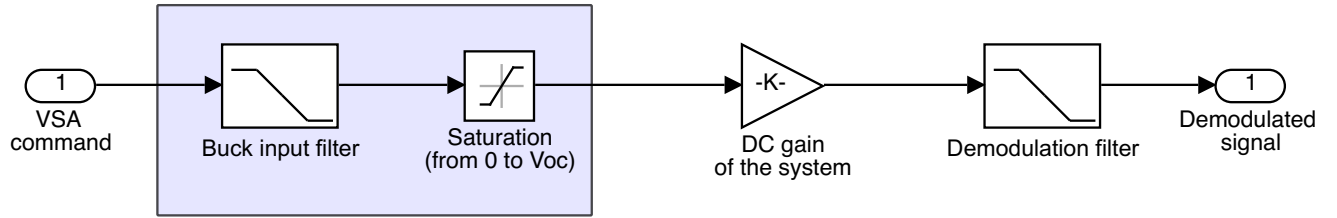


Figure 4.6: Implementation of the "system" block presented in figure 4.5.

4.4.2 Fundamental building blocks of the system

As explained in the preceding paragraph, the open-loop response of the system presents two low-pass filters and a DC gain. All of them will be detailed in the next paragraphs.

Input filter of the converter

The first filter is the one placed between the solar array and its associated converter. It ensures that the converter does not force the solar array to produce a pulsed current, because this situation would significantly reduce the average power delivered to the bus. Usually, it is a parallel-damped LC filter (as shown in figure 2.7) that presents the following transfer function:

$$\frac{v_{out}}{v_{in}} = \frac{1 + R_d C_d s}{1 + R_d C_d s + L(C + C_d)s^2 + L C C_d R_d s^3} \quad (4.9)$$

$$\approx \frac{1}{1 + \frac{L(C+C_d)}{R_d C_d} s + L C s^2} \quad (4.10)$$

$$\approx \frac{1}{1 + \left(\frac{2\zeta}{\omega_c}\right) s + \left(\frac{1}{\omega_c^2}\right) s^2} \quad (4.11)$$

As stated above, the cut-off frequency $f_c = 1/(2\pi\sqrt{LC})$ of this second-order filter has to be smaller than the switching frequency of the converter. But it should be high enough to allow the carrier (of frequency f_p) to reach the solar array. These two constraints can then be summarized as follows:

$$\boxed{f_c \ll f_{switch,conv}} \quad \text{and} \quad \boxed{f_c > f_p} \quad (4.12)$$

Usually the switching frequency of a converter ranges from tens of kHz up to several MHz. We will assume that this converter operates at 100kHz, and the cut-off frequency of the input filter is then here chosen to be $f_c = 1$ kHz.

Another important parameter is the damping factor $\zeta = L(C + C_d)/(2R_d C_d \sqrt{LC})$ of the filter, since it avoids the noise or other perturbations to be amplified at the resonance frequency. The maximum damping is achieved with $C_d = 4C$ and $R_d = \sqrt{L/C}$ as demonstrated in [17]. This leads to $\zeta = \sqrt{6}/4 = 0.612$ and the resulting bode plot is presented in figure 4.7.

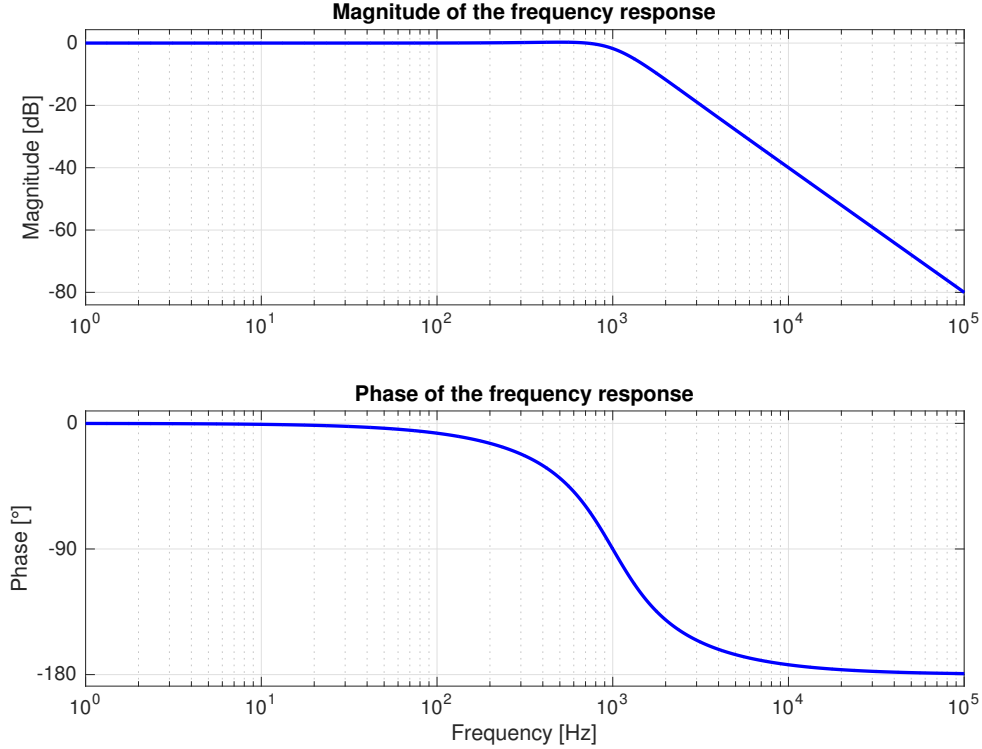


Figure 4.7: Frequency response of the buck's input filter.

Output filter of the demodulation stage

The other filter taken into account in the system dynamics is the low-pass filter placed at the output of the demodulation stage. It is responsible for removing the parasitic signals that do not contain useful information, i.e. non-DC components such as noise, high-frequency switching harmonics, potential fluctuations due to EMC aspects, etc.

Its cut-off frequency should therefore be chosen as close as possible to 0 Hz. As a consequence, the bandwidth of the system is limited and a high proportional gain will be needed to reach a decent control bandwidth. Because of this effect, a simple first-order low-pass filter is used, whose frequency response follows the relation:

$$\frac{v_{out}}{v_{in}}(s) = \frac{1}{1 + \tau s} \quad (4.13)$$

where we choose $\tau = 10/(2\pi)$ seconds, or equivalently $f_c = 1/(2\pi\tau) = 0.1$ Hz.

The bode plot of the resulting demodulation filter is drawn in figure 4.8.

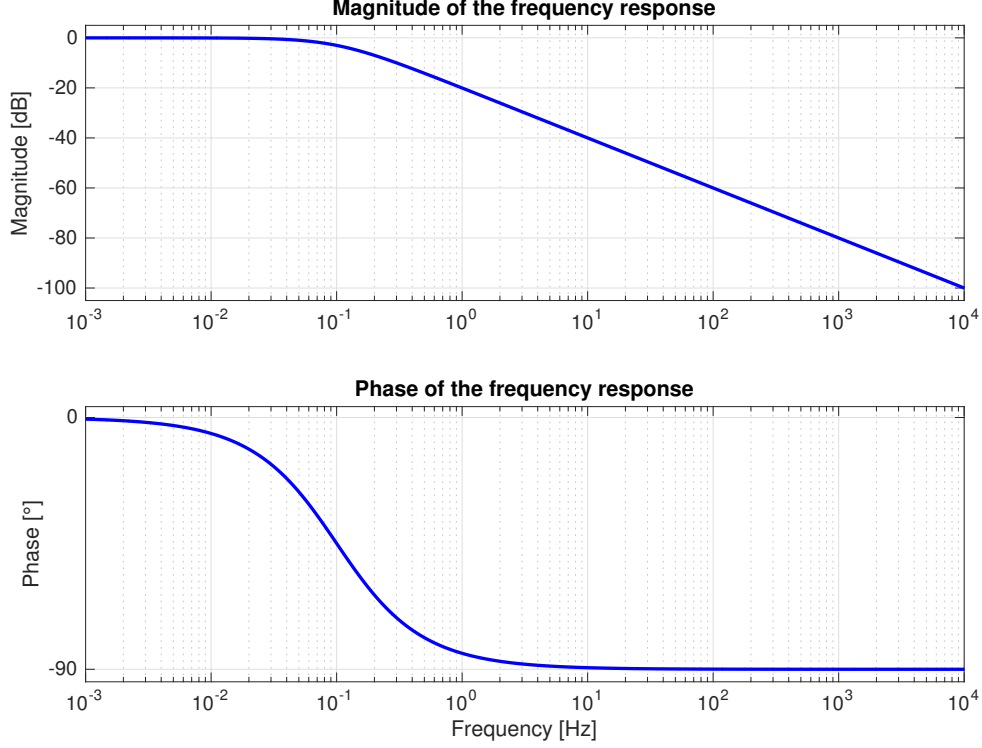


Figure 4.8: Frequency response of the filter placed at the end of the demodulation stage.

Gain of the system

The last step required in order to establish the transfer function of the system is to find the expression of its DC gain. This gain can be described as a measure of how much a voltage step from the controller will be amplified (or attenuated) at the output of the system, i.e. the demodulated signal.

If the system is currently operating at a voltage $\bar{V}_{SA}$ and that a voltage step ΔV_{SA} is suddenly applied at its input (i.e. the input goes from $V_{SA} = \bar{V}_{SA}$ to $V_{SA} = \bar{V}_{SA} + \Delta V_{SA}$), the resulting demodulated signal can be expressed as :

$$s_{demod} = \frac{1}{2} K_{sens} \left(\frac{v_{SA}^2}{V_{BUS}} \right) \frac{d(P_{SA})}{dV_{SA}} \quad (4.14)$$

$$\approx \bar{s}_{demod} + \Delta s_{demod} \quad (4.15)$$

$$\approx \frac{1}{2} K_{sens} \left(\frac{v_{SA}^2}{V_{BUS}} \right) \left(\left. \frac{d(P_{SA})}{dV_{SA}} \right|_{V_{SA}=\bar{V}_{SA}} + \frac{d^2(P_{SA})}{dV_{SA}^2} \Big|_{V_{SA}=\bar{V}_{SA}} \Delta V_{SA} \right) \quad (4.16)$$

Based on the definition of the DC gain G_{sys} given above, we obtain:

$$G_{sys} = \frac{\Delta s_{demod}}{\Delta V_{SA}} = \frac{1}{2} K_{sens} \left(\frac{v_{SA}^2}{V_{BUS}} \right) \frac{d^2(P_{SA})}{dV_{SA}^2} \Big|_{V_{SA}=\bar{V}_{SA}} \quad (4.17)$$

The analytical expression of the second derivative of the power has been computed in appendix A.2 and leads to the following relation:

$$\frac{d^2(P_{sa})}{d(V_{sa})^2} \approx \frac{1}{V_t} (I_{sa} - I_{ph}) \left(2 + \frac{V_{sa}}{V_t} \right) \quad (4.18)$$

This function is illustrated in the upper part of figure 4.9, and a zoom around the MPP voltage is presented in the lower part.

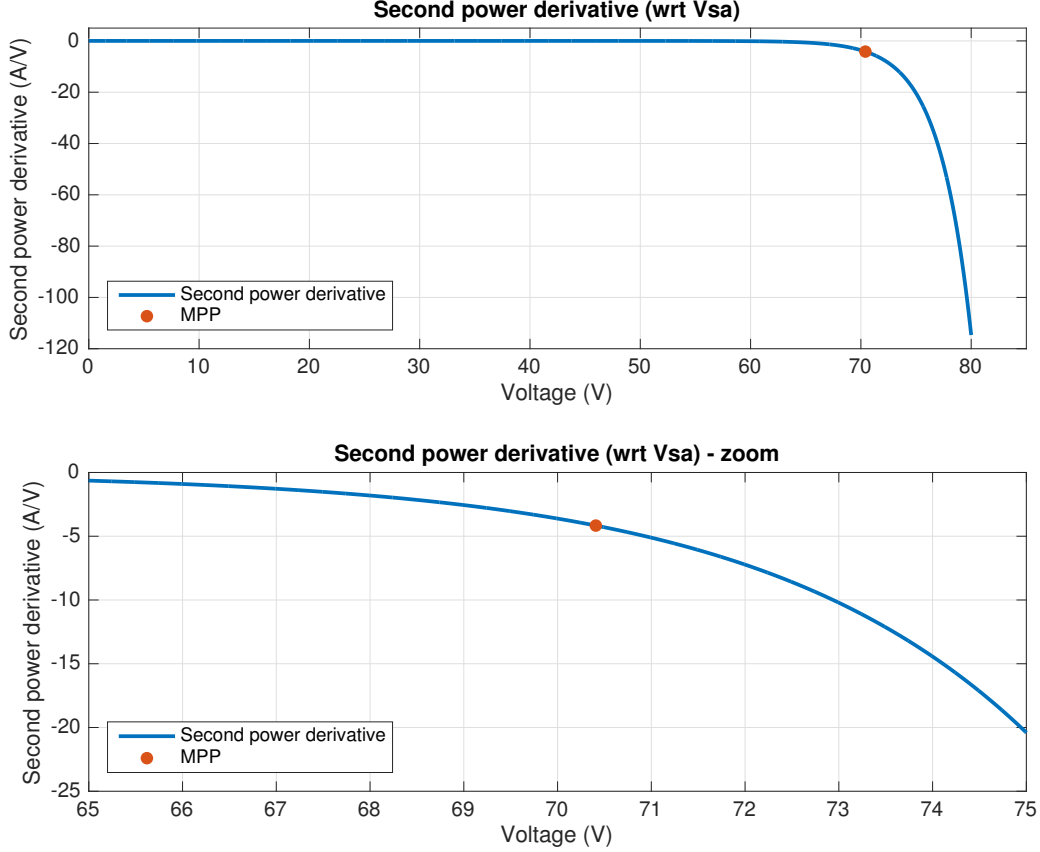


Figure 4.9: Second derivative of the power with respect to the solar array voltage (on the entire range of voltage in the upper graph, and a zoom around MPP in the lower one) at 25°C.

It should be noted that the gain of the system is *negative*, and it explains why we can see a "+" sign at the end of the feedback loop represented in figure 4.5. Indeed, the demodulated signal is here added to the reference in order to feed the PID controller with a positive error.

Another important point is that the gain of the system strongly depends on the current operating point $\bar{V}_{SA}$ of the system. The main objective being to maintain the voltage around V_{MPP} , the DC gain is then computed at that particular point:

$$G_{sys} = \frac{\Delta s_{demod}}{\Delta V_{SA}} = \frac{1}{2} K_{sens} \left(\frac{v_{SA}^2}{V_{BUS}} \right) \frac{d^2(P_{SA})}{dV_{SA}^2} \bigg|_{V_{SA}=V_{MPP}} \quad (4.19)$$

Temperature dependence of the DC gain

As stated before, the gain of the system is computed at its MPP voltage. But this voltage and the associated gain also vary with temperature. This paragraph therefore aims at analyzing the impact of temperature on this gain, and at finding a way to take it into account.

The evolution of the gain at MPP with temperature is represented in figure 4.10.

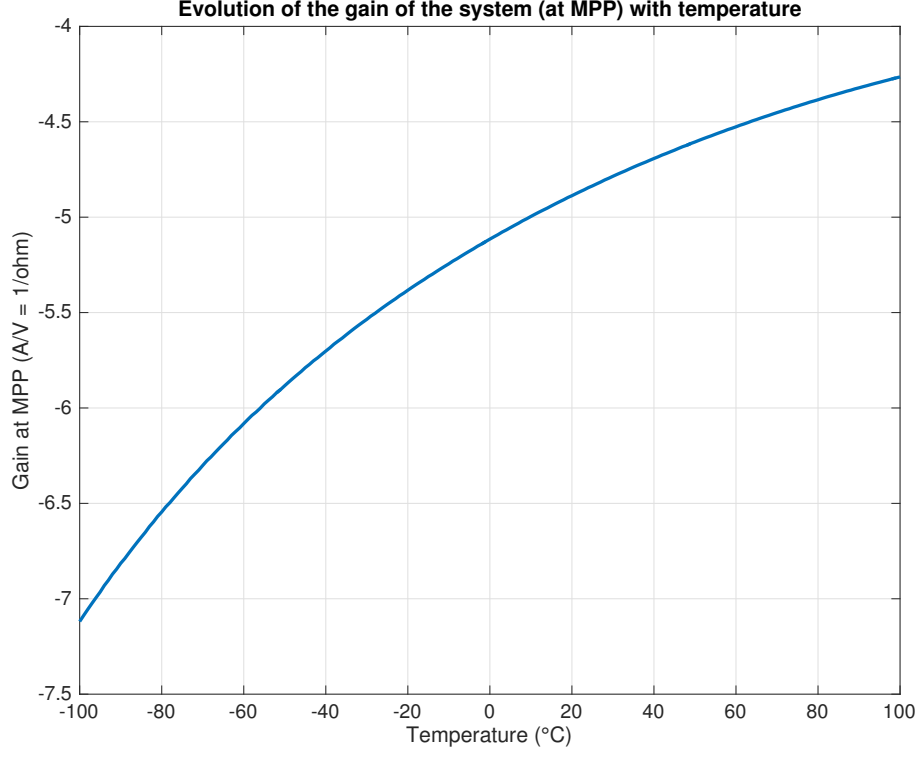


Figure 4.10: Evolution of $\left. \frac{d^2(P_{SA})}{dV_{SA}^2} \right|_{V_{SA}=V_{MPP}}$ with temperature.

Usually, the temperatures to which satellites are exposed range from -100 to 100°C. The choice made here is then to use the mean value over this range, i.e.

$$\left. \frac{d^2(P_{SA})}{dV_{SA}^2} \right|_{V_{SA}=V_{MPP}} = -5.3 \text{ [A/V]} \quad (4.20)$$

With the data listed in table 4.1, the system presents a DC gain G_{sys} of

$$G_{sys} = \frac{\Delta s_{demod}}{\Delta V_{SA}} = -0.0757 \text{ [V]} \quad (4.21)$$

The gain units appear to be in volts because of the demodulation step where a voltage is "multiplied" by another voltage. However, the way such demodulations are implemented in practice produces a simple voltage at the output. Therefore, the gain of the system has no unit in practice (or units in [V/V]).

Table 4.1: Data used to compute the DC gain of the system.

Parameter	Value
K_{sens}	100 [V/A]
V_{BUS}	35 [V]
v_{SA}	0.1 [V]

4.4.3 PID design

By combining the different elements analyzed previously, the open-loop response of the system can be drawn (see figure 4.11). Here all the graphs will assume that the system has a *positive* gain (which has an

impact on the phase of the system which is shifted by 180°), but since the feedback loop is positive, the result is the same.

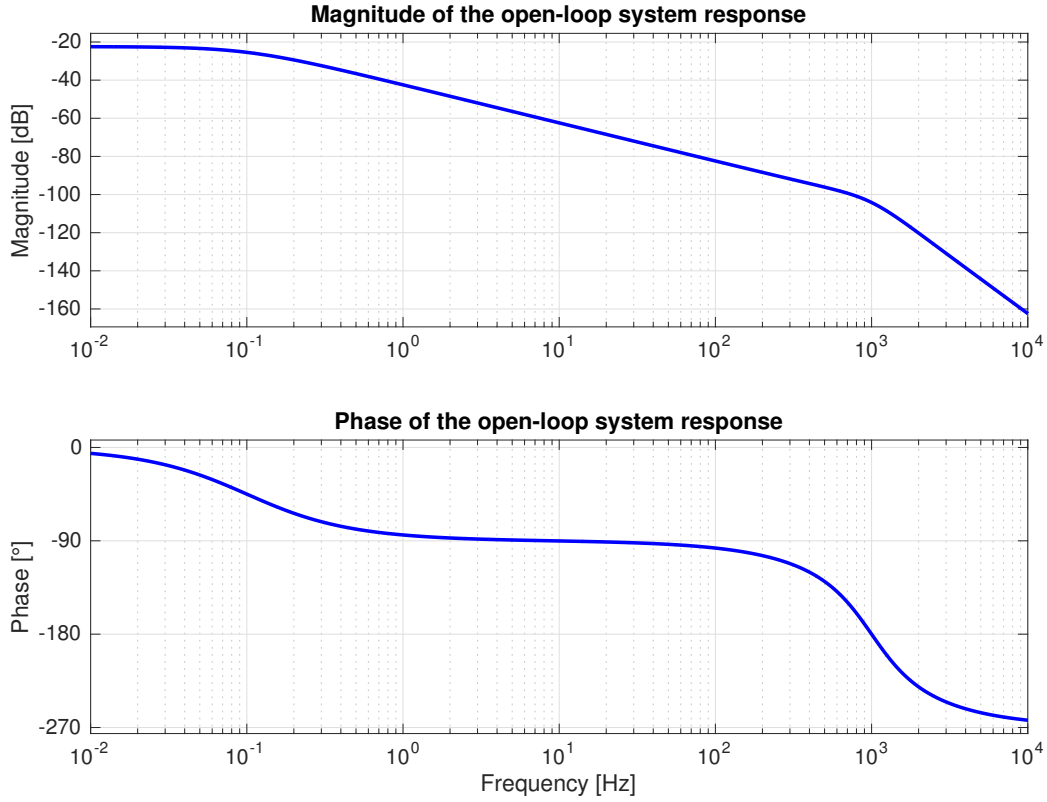


Figure 4.11: Open-loop response of the system.

The controller has to meet a set of robustness criteria to be acceptable. These criteria are summarized in table 4.2.

Table 4.2: Robustness criteria that the controller needs to fulfil.

Modulus margin³	< 6 dB
Phase margin	> 60 °
Gain margin	> 6 dB

Lots of PID tuning techniques exist in the literature, such as the Ziegler-Nicholson or Tyreus-Luyben techniques and others. In this case, we will use the loop shaping method presented in [16] because it has the advantage of being very intuitive.

Proportional action

The proportional gain of the controller is the parameter who allows to play on the bandwidth of the system. The bandwidth is defined as the frequency at which the magnitude plot of the open-loop response (including the controller) has a gain of 1 (or 0 dB).

The controller will here be designed to reach a bandwidth of approximately 300 Hz (or 1885 rad/s).

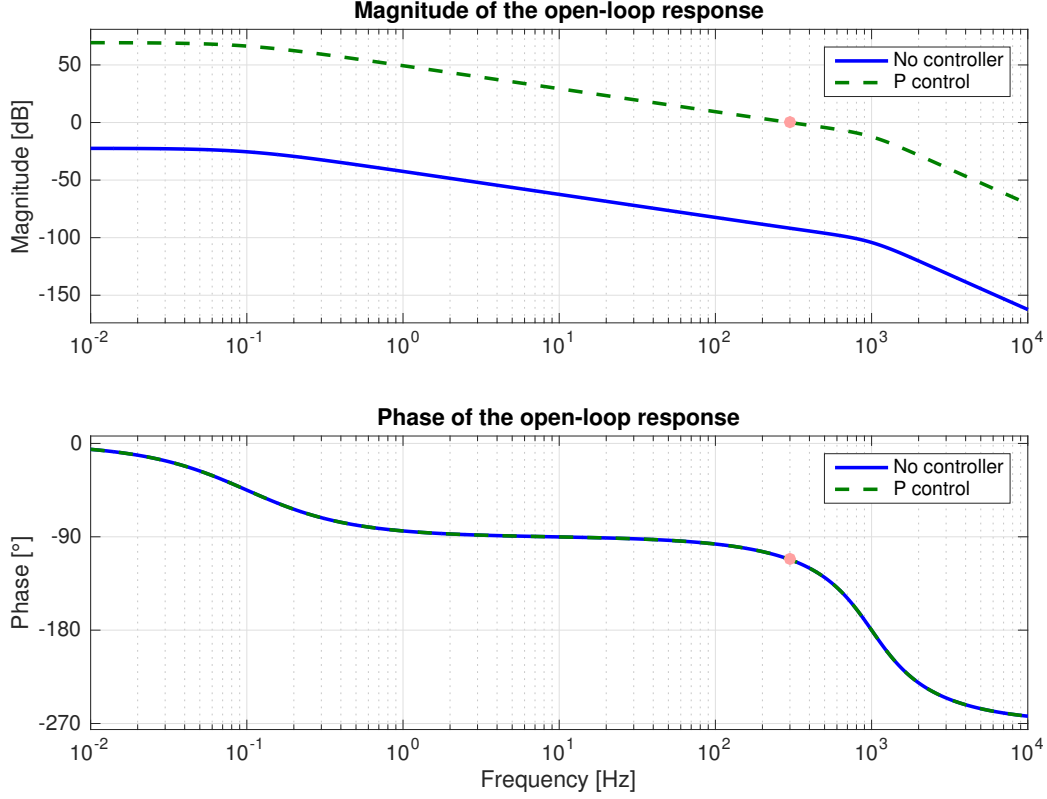


Figure 4.12: Open-loop response of the system with a simple P controller.

As discussed above, the demodulation filter highly attenuates "high" frequencies. Indeed, the system presents an attenuation of 91.8 dB at 300 Hz. In practice, such a value at the output of the system could be too small for the controller, but simple modifications could help to circumvent this problem:

- amplifying the current measurement;
- amplifying the oscillator voltage who enters the demodulation stage (but not the one applied to the solar array !);
- or increasing the cut-off frequency of the demodulation low-pass filter.

In this analysis we will consider that the current measurement amplifies the signal by a factor 100 and assume that the controller is able to cope with such a small demodulated signal, so we will not introduce extra amplifiers in the system.

In order to reach a bandwidth of $f_{bw} = 300$ Hz, the proportional gain is then set to

$$k_p = 91.8 \text{ dB} = 10^{(91.8/20)} [\text{V/V}] \quad (4.22)$$

The resulting open-loop response is depicted in figure 4.12, where the red dot represents the unity gain frequency.

Integral action

The integral action is important because it adds loop gain at low frequency, thereby allowing to reach a zero steady-state error (the gain of the controller becomes infinite at 0 Hz).

However, the integral action also adds a lag phase of 90° which could reduce the phase margin. For that reason, the I-action has to be stopped at a frequency f_i sufficiently lower than the bandwidth f_{bw} where the phase margin is computed. In order to attenuate the potential high-frequency parasitic signals, a low-pass filter is usually added one decade after the bandwidth to "continue" the integral action. In this case, the filters already present in the system eliminate the need of this additional low-pass filter.

It is a common practice to end the integral action at least one decade before the bandwidth ($f_i = f_{bw}/10$), so this guideline will be tested and compared to two controllers whose I-action are terminated earlier. Graphs in figure 4.13 show the step response performances for $f_i = 1, 10$ and 30 Hz, and the table 4.3 compares the robustness characteristics of these controllers.

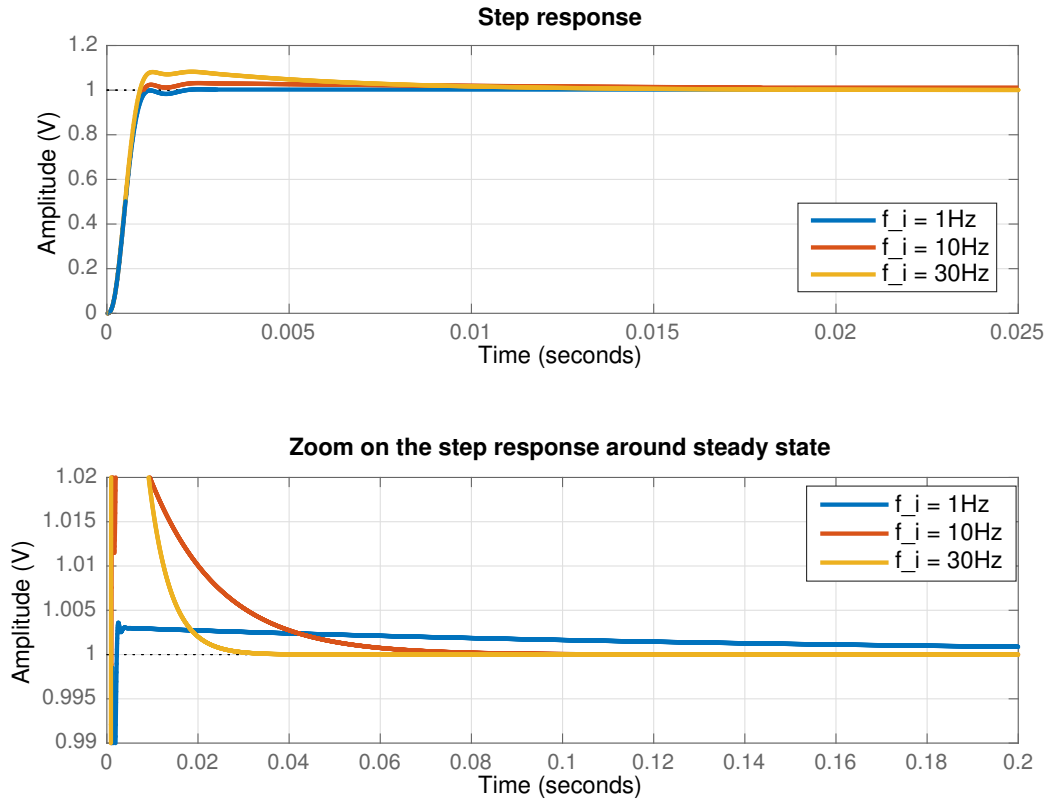


Figure 4.13: Comparison of the step response of the system with a PI controller for different values of f_i .

Table 4.3: Comparison of the system characteristics with a PI controller for different values of f_i .

	Criteria	$f_i = 1$ Hz	$f_i = 10$ Hz	$f_i = 30$ Hz
Modulus margin	< 6 dB	3.5 dB	3.5 dB	3.6 dB
Phase margin	> 60°	67.9°	66.1°	62.2°
Gain margin	> 6 dB	12.4 dB	12.3 dB	12.1 dB
Settling time (at 2%)	< 10 ms	1 ms	9.4 ms	9.2 ms

From the table, we can conclude that all three controllers easily meet the specifications, but the robustness slightly decreases when the integral action gets closer to the bandwidth.

The plots also lets appear two interesting phenomena. On the one hand, the higher f_i the more time it

takes to approach the steady state value, which is due to the inertia of the integral action. But on the other hand, the time required to fit the exact value as well as the average error (computed up to steady state) decreases when f_i gets higher.

Since we are interested in minimizing the average error and because the margins are high enough, the guideline of "1 decade below the bandwidth" will be followed here:

$$\boxed{f_i = f_{bw}/10 = 30 \text{ Hz}} \quad (4.23)$$

but at the cost of higher settling time and overshoot.

The PI controller that has been designed so far has the following transfer function:

$$C_{PI}(s) = k_p \left(\frac{s + \omega_i}{s} \right) \quad (4.24)$$

where $\omega_i = 2\pi f_i$.

(Tamed-) derivative action

The derivative action has two main purposes:

- to add phase lead around the bandwidth in order to increase the phase margin of the system
- to reduce parasitic resonance-like effects (acts like a damper)

The main purpose of a derivative action is then to improve the stability of the system.

However, because of this damping action, the derivative part of the controller tries to counteract the dynamics introduced by the proportional gain and will then increase the settling time.

Following the loop shaping design guidelines, the PID controller would have the following transfer function:

$$C_{PID}(s) = k_p \left(\frac{s + \omega_i}{s} \right) \left(\frac{1 + s/\omega_d}{1 + s/\omega_t} \right) \quad (4.25)$$

with $\omega_d = \omega_{bw}/N$ and $\omega_t = \omega_{bw} * N$.

N is usually chosen to be equal to 3 and determines how the phase lead is spread around the bandwidth:

- if N increases, the phase lead increases and is spread over a wide range of frequencies. This leads to a better robustness but the settling time increases.
- if N decreases, the phase lead is narrower but introduces a smaller delay in the system response.

It is important to note that the proportional parameter k_p has to be modified to maintain the same bandwidth. Indeed, the loop gain starts to increase at ω_d (because of the zero) and up to ω_t . To compensate for that, the proportional gain has to be divided by N :

$$k_{p,(PID)} = \frac{k_{p,(PI)}}{N} \quad (4.26)$$

The figure 4.14 compares three PID controllers with $N = 1, 2, 3$ to the PI controller designed previously, and the table 4.4 sums up their characteristics.

From the step responses, we can conclude that the PID performances are less interesting than those of the PI controller in terms of reactivity, but the derivative action could be very useful to damp the potential parasitic signals.

In table 4.4, it can be noted that the PID significantly increases the phase margin, but the modulus and gain margins are slightly less interesting than with a PI.

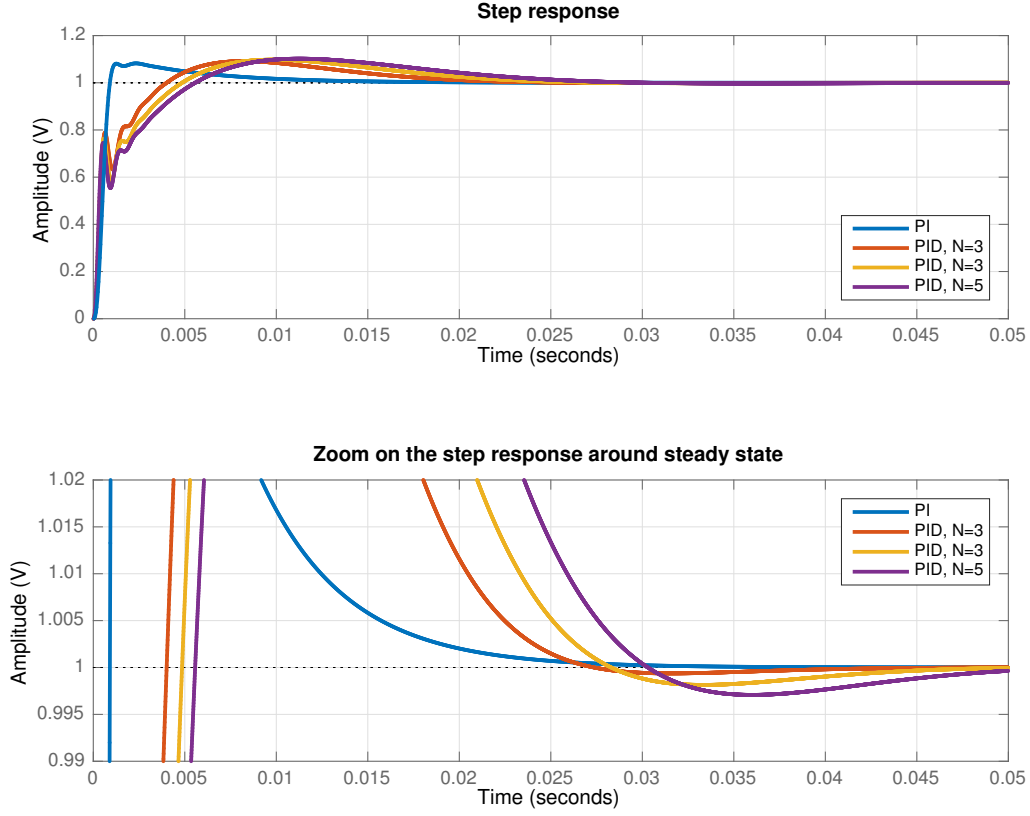


Figure 4.14: Comparison of the step response of the system using PID controllers with varying N parameters to the response using the PI controller designed previously.

Based on these considerations, we made a trade-off between reactivity and robustness: a PID controller with $N = 3$ will be implemented to control the system. The values of the parameters (from the expression 4.25) are provided in table 4.5.

Table 4.4: Comparison of the system characteristics using PID controllers with different N and using the PI designed above.

	Criteria	PI	PID, $N = 3$	PID, $N = 4$	PID, $N = 5$
Modulus margin	< 6 dB	3.6 dB	4.3 dB	4.3 dB	4.2 dB
Phase margin	$> 60^\circ$	62.6°	114.9°	123.2°	127.8°
Gain margin	> 6 dB	12.1 dB	10.9 dB	11.3 dB	11.8 dB
Settling time (at 2%)	< 10 ms	9.2 ms	18 ms	21 ms	23.5 ms

Table 4.5: Parameters of the final PID controller.

Parameter	Design guideline	Value
$\omega_{bw} \rightarrow$ bandwidth)	-	$2\pi \cdot 300 = 600\pi [rad/s]$
$G_{sys}(\omega_{bw}) \rightarrow$ system's gain at ω_{bw}	-	$-91.8 [dB]$
N	-	3
k_p	$10(G_{sys}(\omega_{bw}) /20)/N$	12 965 [V/V]
ω_i	$\omega_{bw}/10$	$60\pi [rad/s]$
ω_d	ω_{bw}/N	$200\pi [rad/s]$
ω_t	$\omega_{bw} \cdot N$	$1800\pi [rad/s]$

4.5 Characterization

The PID controller designed in the previous section is now applied to the real system (simulated in Matlab/Simulink) in order to verify that the algorithm works as expected. Subsequently, the dynamic properties of the system will be analysed and the MPP tracking performance will be quantified. Finally, the last topic of this section will be devoted to the robustness of the system.

4.5.1 MPP tracker behaviour

Before analyzing the dynamics of the system, we first verify that the MPP tracker works properly. The testing method consists in several temperature steps applied to the system to simulate varying environmental conditions. If the MPP tracker works correctly, the solar array voltage should converge towards V_{MPP} . In practice, the temperature variations have a certain inertia due to the gradual warming up of the array; the worst case occurs at the eclipse's exit when the solar arrays can start from -100° and end up at 100° in approximately 3 minutes.

Unlike temperature variations, the light power may step up almost instantaneously; however the only parameter significantly affected is the photo-generated current, the MPP staying almost at the same voltage. However, this quick variation may momentarily impact the slope seen by the controller, we will then verify that the controller designed in the previous section is sufficiently "slow" to filter out this rapid light power variation.

The figure 4.15 presents the behaviour of the system (in the lower graph) with respect to the temperature conditions (in the upper graph), and attests that the system tries to track the MPP by adapting the solar array voltage.

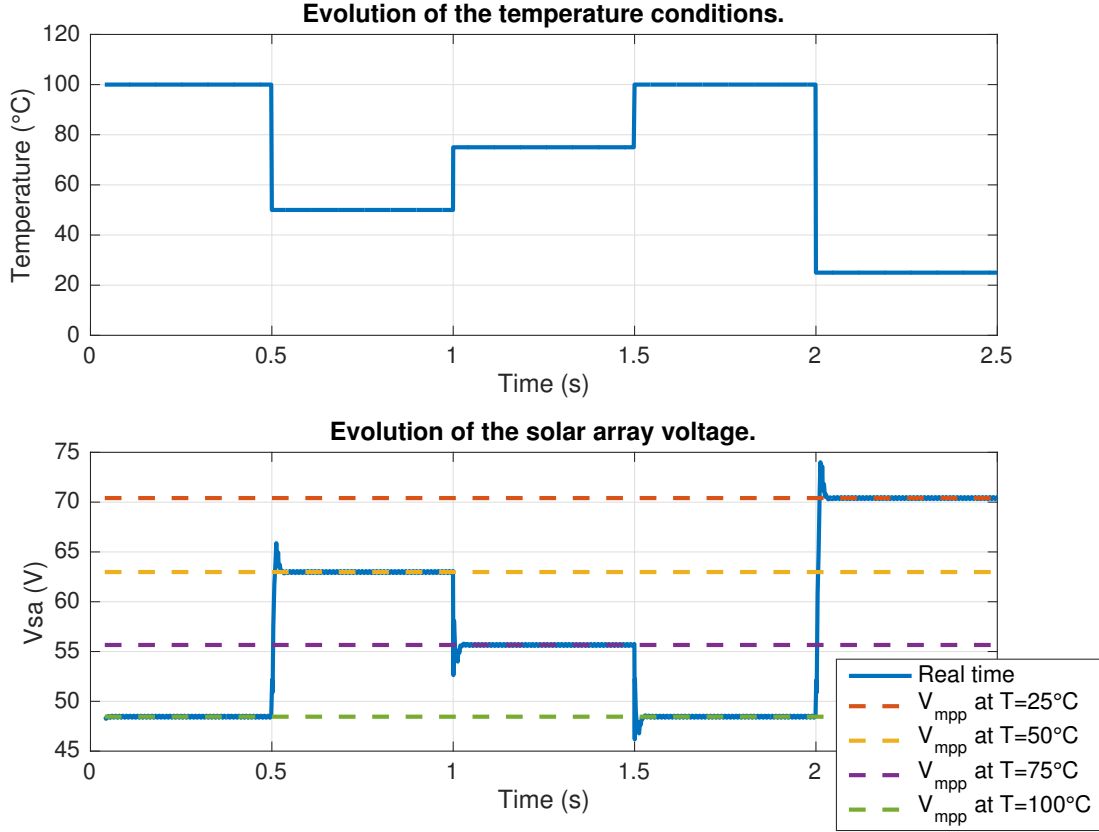


Figure 4.15: Behaviour of the system (lower graph) when the solar array temperature varies (upper graph).

The behaviour of the system in response to a temperature step (from T_1 to T_2) can also be described from the I-V and P-V curves. Here, two cases can be distinguished:

- *case 1* (illustrated in figure 4.16): at $V_{MPP,(T_1)}$, the corresponding current $I_{sa,(T_2)} = 0$.
In this situation, the current first drops to zero (meaning that the solar array temporarily does not produce any electrical power) and the system progressively reduces the voltage applied to the solar array. Once the open-circuit voltage of the "new" I-V curve is reached, the system converges towards the peak power point (here with an important overshoot).
- *case 2* (represented in figure 4.17): at $V_{MPP,(T_1)}$, the corresponding current $I_{sa,(T_2)} \neq 0$.
This situation allows the controller to switch from the initial I-V curve to the new one and to track the new maximum power point without interrupting the power production.

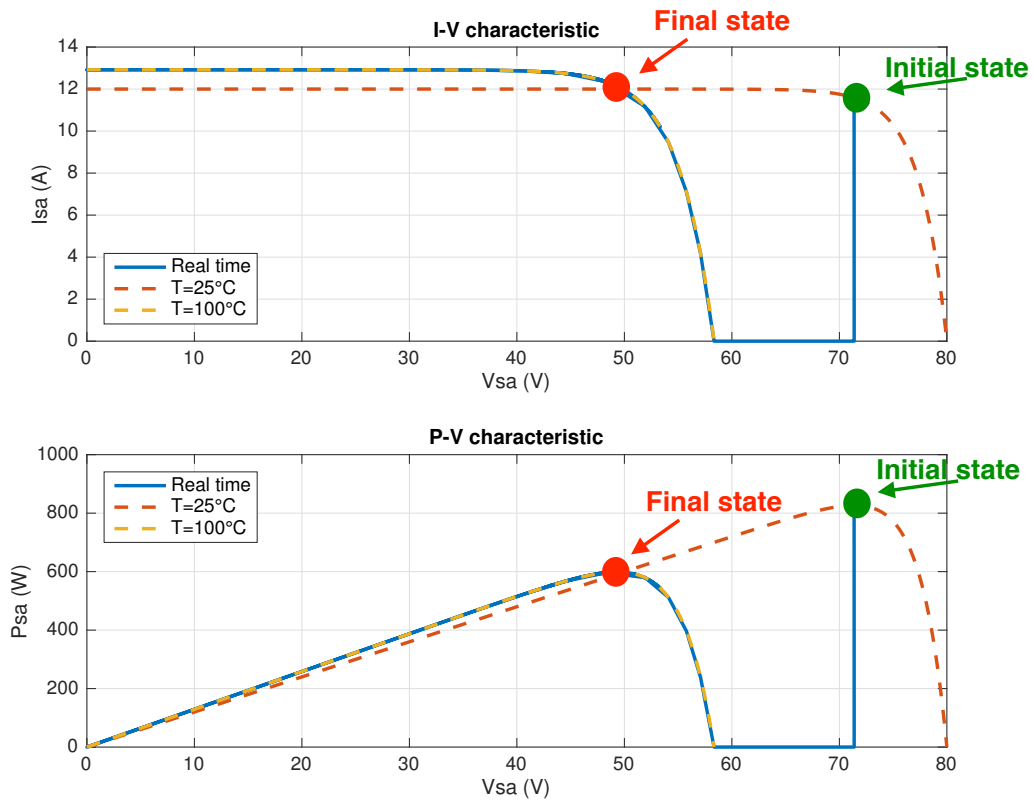


Figure 4.16: Illustration of the case 1, both on the I-V and the P-V curves.

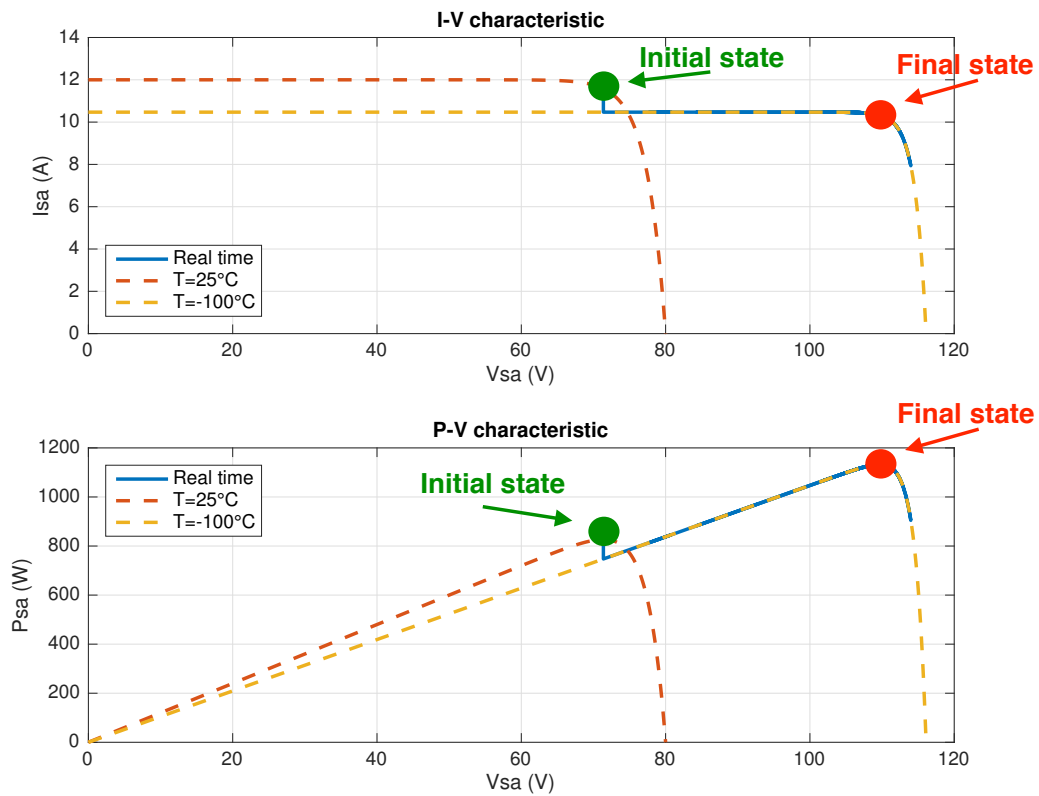


Figure 4.17: Illustration of the case 2, both on the I-V and the P-V curves.

4.5.2 System dynamics analysis

Temperature variations

In order to quantify the reactivity of the system when the temperature varies, two temperature steps (one for each case) have been applied to the system:

- a positive temperature step from 75 to 100°C (see figure 4.18);
- and a negative temperature step from 75 to 50°C (see figure 4.19).

The dynamic characteristics of the system's responses are presented in table 4.6.

A first observation is that the overshoots are quite significant. This is partly due to the decision taken during the controller design⁴ to grant higher overshoots in exchange for a quicker convergence towards the steady state value. It can also be noted that the overshoot is more significant for a temperature drop than the contrary. This is probably due to the fact that the gain of the system slightly increases when the solar array cools down.

The other remark concerns the settling time: the reactivity is slightly better for a temperature drop. As for the overshoot, this is presumably due to the solar array cooling which modifies the system's gain. Our model did not take that feature into account since the system was linearized around the MPP at 25°C. Nonetheless, less than 30 milliseconds to reach the new MPP is a satisfying result. If the time response is small enough, the most important for us is to stay close to the MPP once it has been reached. This performance indicator will be the topic of section 4.5.3.

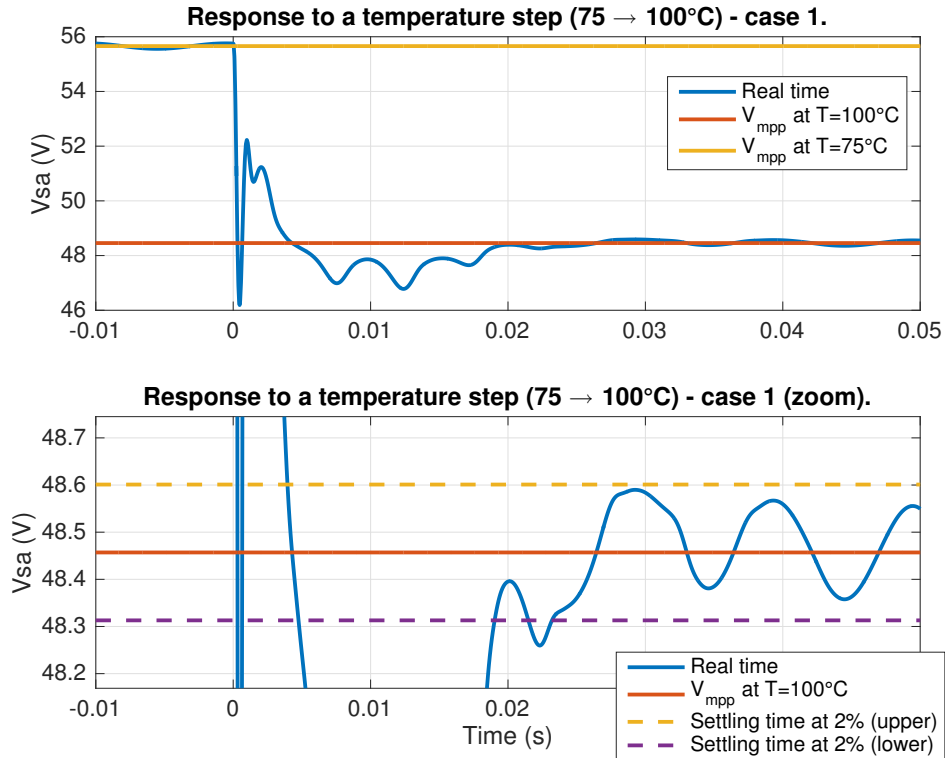


Figure 4.18: Step response of the system to a temperature step from 75 to 100°C (case 1).

⁴During the integral parameter design.

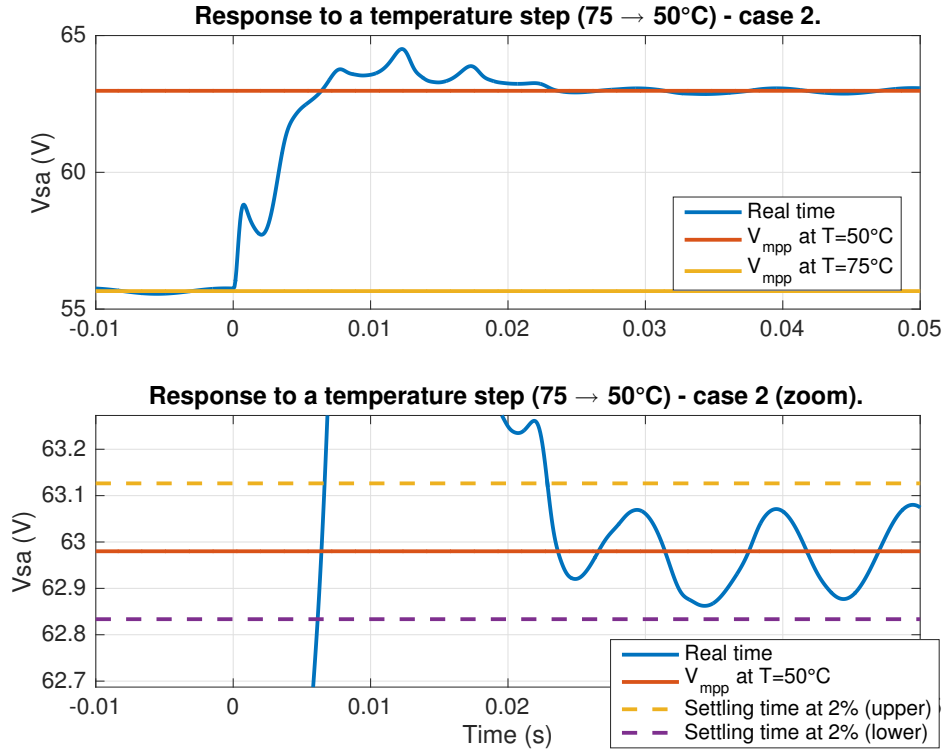


Figure 4.19: Step response of the system to a temperature step from 75 to 50°C (case 2).

Table 4.6: Dynamic characteristics of the system in response to a temperature step in each case (see figures 4.18 and 4.19).

	75°C ⇒ 100°C	75°C ⇒ 50°C
Settling time (at 2%)	23.2 ms	22.9 ms
Overshoot	20.9%	52.3%

Illumination variations

As for the temperature, a positive and a negative illumination steps are here applied to the system, and its reactions are depicted in figure 4.20.

Since the voltage ripple generated by the oscillator is too large compared to the voltage difference between the initial and final states, it is difficult to compute the value of the settling time. Therefore, we redefined the settling time as the time it takes to reach its steady state behaviour, which will overestimate the real value (at 2%). With this definition, we get the performances listed in table 4.7.

As we can see, an increased exposition takes less time for the system to reach its new MPP than an illumination drop. Also, the overshoot is not negligible compared to the voltage variation but hopefully it does not really affect the power loss since the MPP voltage difference between two different illumination conditions is quite small.

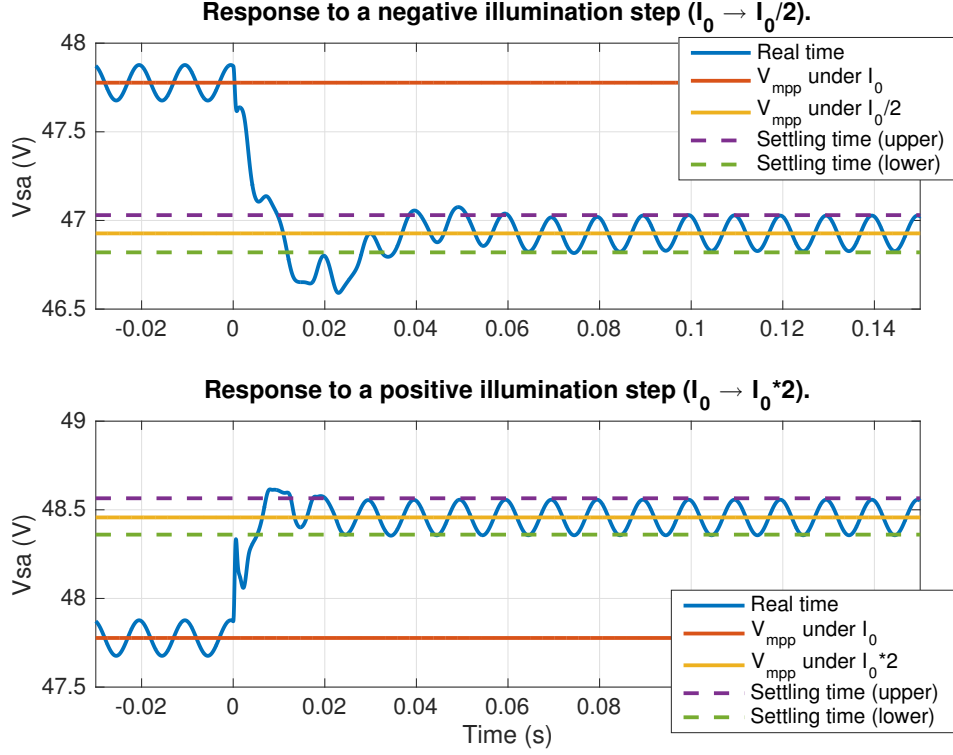


Figure 4.20: Step response of the system when exposed to a positive or a negative illumination step.

Table 4.7: Dynamic characteristics of the system in response to an illumination step (see figure 4.20).

	$I_0 \Rightarrow I_0/2$	$I_0 \Rightarrow 2I_0$
Settling time	51 ms	20.1 ms
Overshoot	39.5%	23.2%

4.5.3 MPP tracking performance in steady state

Since the goal of an MPP tracker is to follow the peak power point, a good performance indicator is to know what ratio of the available power can be extracted in steady state using this technique.

The results presented in this part come from of a simulation where the system is not disturbed by external perturbations (this situation will be treated in the next section).

The figure 4.21 illustrates the instantaneous power extracted from the array when the system operates at a temperature of 100°C. These oscillations around the MPP are a direct consequence of the MPPT based on synchronous demodulation, since a sine perturbation is voluntarily introduced in the system around the operating point. However, these results clearly reveal that the amplitude of the power ripple does not introduce significant losses in the system. Actually, the MPP tracking efficiency, defined as:

$$\eta_{mpp} = \frac{P_{extracted}}{P_{mpp}} \quad (4.27)$$

is higher than 99.99% for the whole range of temperatures (from -100 to 100°C). Of course, this efficiency does not take into account the internal losses of the dc-dc converter since it is computed on the solar array side.

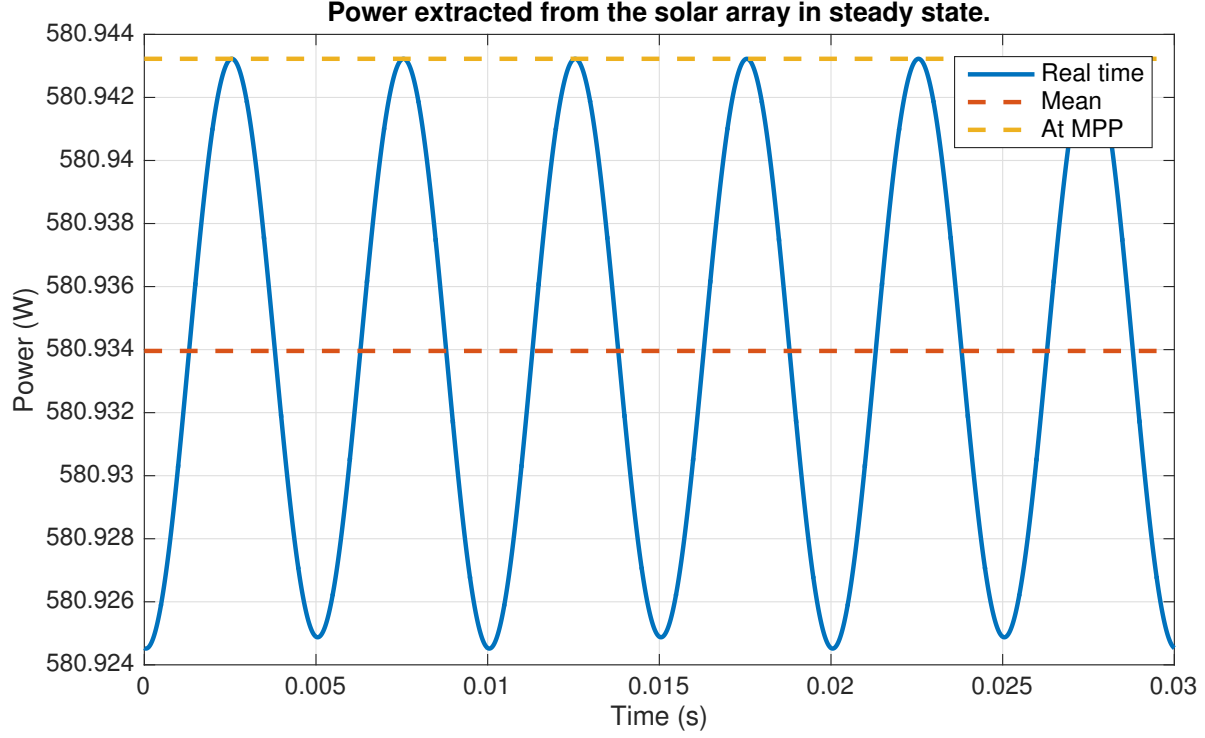


Figure 4.21: Solar array power in steady state when the system operates at 100°C.

4.5.4 Robustness analysis

Model and data

Since we are considering an unregulated bus, the bus voltage corresponds to the battery voltage which has been arbitrarily set to 35V. Furthermore, the satellite's temperature is supposed to be at its maximum (100°C).

Let us assume that a sine perturbation $v_{paras} = v_{PARAS} \sin(f_{paras}t)$ is added on top of the DC bus voltage V_{BUS} . This parasitic oscillation will cause current fluctuations in the output inductor of the converter, which will be sensed along with the useful information and then potentially cause additional power losses.

This voltage ripple is assumed to have the characteristics listed in table 4.8.

Table 4.8: Characteristics of the bus ripple voltage.

Frequency range (f_{paras})	40Hz - 10kHz
RMS amplitude (v_{PARAS})	1.5 V

The current variation i_{paras} induced in the output inductor L_{out} (whose value is designed in appendix C for a current ripple of 0.5% of its nominal value) can be expressed in the worst case⁵ as

$$i_{paras} = \frac{v_{paras}}{sL_{out}} \quad (4.28)$$

⁵When the solar array is in short-circuit, i.e when the voltage drop across the inductor is maximum.

Furthermore, it is assumed that the controller also contains an inner current control loop that attenuates these current fluctuations (see 4.22).

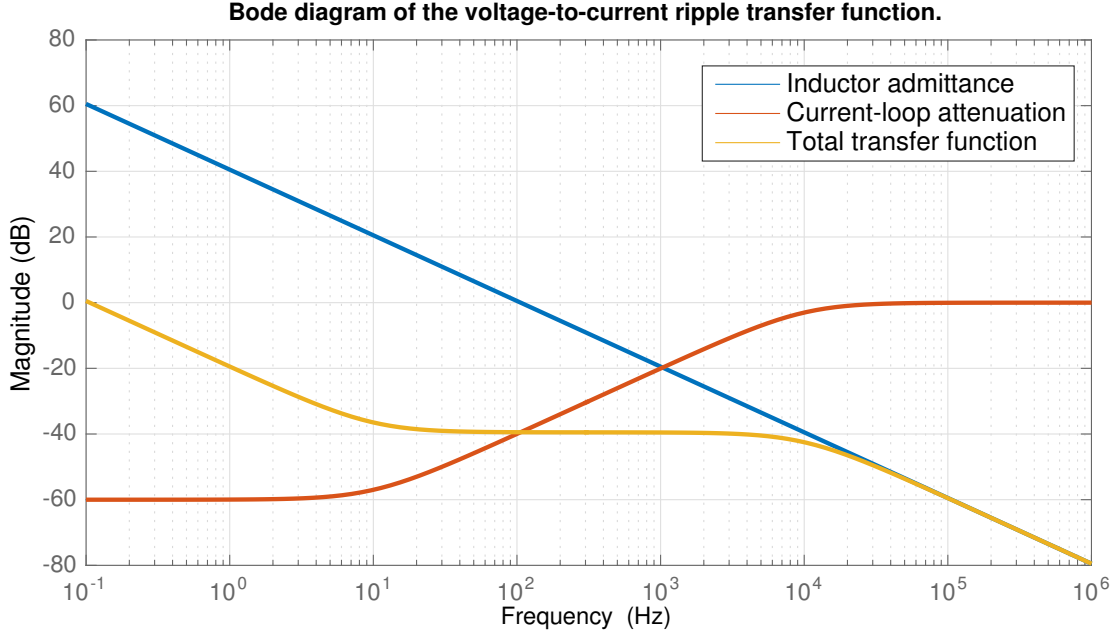


Figure 4.22: Bode plot of the transfer function from the voltage ripple to the attenuated current ripple.

Finally, the resulting transfer function from the voltage to current ripple, combining both the inductor's admittance and the current-loop attenuation factor, is represented in figure 4.22. In the range of interest, i.e. from 40Hz up to 10kHz, the voltage oscillations will then roughly be attenuated by a factor of 40 dB.

But here, the demodulation and its low-pass filter are not yet taken into account. The carrier frequency was chosen to be $f_c = 100$ Hz in this case. These parasitic signals at f_x will then be shifted towards $f_x - f_c$ and $f_x + f_c$ and subsequently enter the demodulation filter whose cut-off frequency was designed to be at $0.1Hz$. The risk will then probably come from the perturbations close to the carrier's frequency that will be shifted close to DC and then not attenuated sufficiently.

Results

In figure 4.23, the performances of the system when exposed to such bus voltage variations (at 40, 95, 100, 1k and 10kHz) have been quantified. The amplitude of the parasitic signal is fixed to $v_{PARAS} = 1.5V$ (RMS) while the carrier's amplitude is varied⁶ from 50mV up to 1V to study the impact of the SNR-like ratio v_{SA}/v_{PARAS} on the performances.

As it could be predicted from 4.22, it turns out that low-frequency bus ripples are more problematic than high-frequency perturbations, especially when the carrier's amplitude is significantly lower than that of the ripple. The other interesting observation is that when the perturbation is close but not equal to the carrier's frequency (95Hz in this case), the performances are significantly reduced. This is due to a beat phenomenon caused by the demodulation product. Indeed, the mixer brings all the frequencies close

⁶The proportional gain of the controller is scaled to keep the same bandwidth.

to that of the carrier around DC; those perturbations are then not sufficiently attenuated by the output filter and subsequently pass the PID controller. In the end, this beat appears on the solar array voltage which forces the operating point to move more than expected, thereby increasing the power losses. Again, it should be noted that this beat phenomenon can be significantly reduced by increasing the amplitude.

Finally, we can see that amplitudes lower than 100mV (orange line) should be avoided since the power losses become too important (if an efficiency of more than 99% is required). But as stated previously in the section about carrier's design, increasing the carrier's amplitude is not always a good option because of the larger oscillations created around the MPP; this is why an amplitude of 1V (the violet curve) leads to lower performances than with 0.5V (yellow).

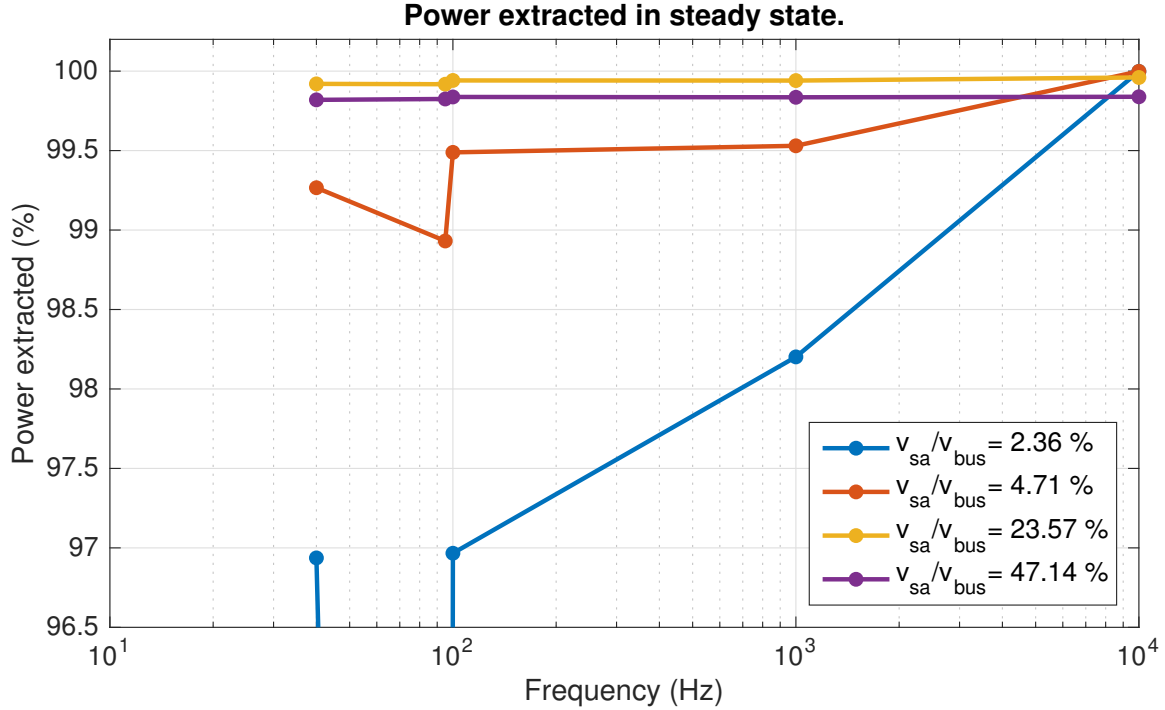


Figure 4.23: Power extracted from the solar array in steady state, when the system is exposed to sine disturbances (of 1.5V RMS) at different frequencies.

Blue: $v_{SA} = 50\text{mV}$; orange: $v_{SA} = 100\text{mV}$; yellow: $v_{SA} = 500\text{mV}$; violet: $v_{SA} = 1\text{V}$.

Based on all these considerations, it turns out that an amplitude of 0.5V would have been a better choice in terms of robustness, in case we would have to do it again.

4.6 Limitations and possible improvements

4.6.1 Highly non-linear gain

In order to design the controller, we made several assumptions to compute the DC gain of the system.

The first approximation was to consider that the voltage ripple v_{SA} across the solar array is constant, because it is a function of the operating point (as demonstrated in appendix B).

The second simplification lies in the fact that the gain of the system was computed at its MPP voltage, but it is not always the case, especially when a temperature step is applied. However, under static or slowly varying conditions, it is a good approximation.

Finally this MPP voltage also varies with temperature. Here we simplified the model by taking the mean gain of the system (at MPP) over the full range of temperatures, starting from -100°C up to 100°C .

The consequence of this highly non-linear gain is that the reactivity of the system can derive significantly from what this model established. Nonetheless, if the control loop is properly designed, the MPP tracker should still converge towards the MPP.

The choice of computing a fixed DC gain is based on the fact that most of the controllers used in space are still analog feedback loops. The parameters of the PID are therefore fixed. Depending on the equipment, we could imagine several PID controllers in parallel and a combination of switches that would select which PID to use as a function of the environmental conditions. But this solution would add an important number of components without significantly improving the performances.

4.6.2 Oscillator phase

In the simulations, the phase of the carrier was the same as that of the signal of the current measurement. However, in practice a phase delay could exist between these two signals. The consequence would be that the resulting DC component would be attenuated, since:

$$\sin(\omega t) \sin(\omega t) = \frac{1}{2} - \frac{1}{2} \cos(2\omega t) \quad (4.29)$$

$$\sin(\omega t) \sin(\omega t + \phi) = \frac{1}{2} \cos(\phi) - \frac{1}{2} \cos(2\omega t + \phi) \quad (4.30)$$

From these relations, we can conclude that the gain of the system would be multiplied by $\cos(\phi)$, where ϕ represents the phase shift between the two signals. Moreover, the noise would not suffer from this gain reduction, only the useful part of the signal (and the parasitics at that frequency) will be affected. This situation would be a serious problem since a delay of 90° would completely suppress the information, and if it exceeds 90° , it would modify the sign of the gain, leading to a positive feedback which would make the system unstable.

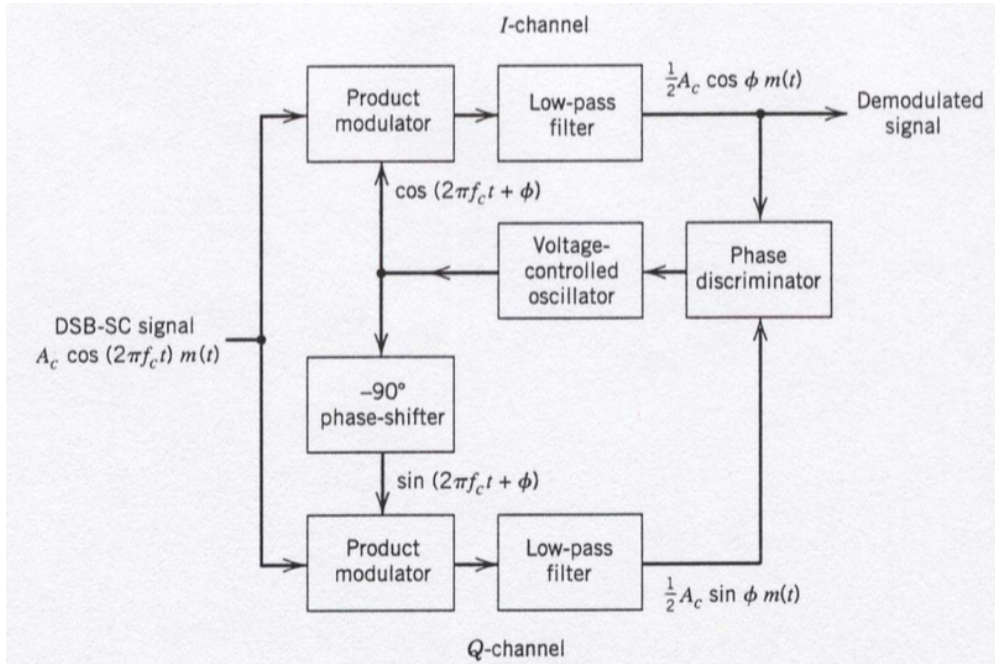


Figure 4.24: Costas receiver, with the courtesy of [6].

This problem could be addressed by a PLL-based⁷ circuit called *Costas receiver* whose role would be to synchronize the carrier with the incoming signal as represented in figure 4.24. This receiver combines two synchronous demodulators fed with the same measured signal but whose carriers' signals are in phase quadrature (90° shift).

The feedback loop included in the Costas receiver uses the fact that for small delays, $\cos(\phi) \approx 1$ and $\sin(\phi) \approx \phi$. A phase discriminator is then used to control a VCO (voltage-controlled oscillator) which corrects the phase of the carrier itself. However, the intrinsic problem is that if the signal $m(t)$ (the useful information) is zero, the phase-correction process therefore stops working until $m(t)$ goes back to a non-zero value.

Such structures are often used to demodulate DSB-SC (double side-band, suppressed carrier) waves in communication systems.

4.6.3 Single-frequency's carrier

Since the carrier is a simple sine signal, all the information is contained at a given frequency. A permanent parasitic signal located at that frequency would then virtually modify the MPP from the controller's point of view; indeed, at MPP, the demodulated signal would not be zero any more. The controller would then modify the operating point of the converter to force its input to zero; causing the system to oscillate around another point than the MPP and leading to continuous power losses.

However, this problem could be circumvented by enlarging the spectral content of the carrier, thereby spreading the information at different frequencies. For example, a combination of several sine functions at different frequencies could improve the robustness of the system. Another possibility would be to replace the sine carrier by a pseudo-random bit sequence, but it will be the topic of the next chapter so we will not go further in the detail here.

4.6.4 Beat phenomenon

Also related to the carrier's frequency, a beat phenomenon has been observed for parasitic signals whose frequency is close to that of the carrier. Indeed, these perturbations are shifted close to DC during the demodulation process. The output filter's attenuation is therefore not sufficient any more to prevent that beat to pass the PID filter and appear on the solar array voltage, leading to significant losses.

Nonetheless, at least three solutions could be implemented to reduce the effect of this phenomenon. The first solution would be to increase the inertia of the PID filter by decreasing its bandwidth down to a frequency like 1Hz. This beat phenomenon would then be limited to the remaining frequencies, i.e in a range of 1Hz around the carrier.

A second more reliable option lies in the fact that in satellites, the only perturbations present on the bus are those generated by the other equipments. We could then emit a constraint stating that the devices connected to the bus should not produce parasitic signals in a frequency range close to that of the carrier's frequency.

Finally, a third solution would be to use a highly-selective band-pass filter centred at the carrier's frequency on the measured signal, before the multiplication. This would attenuate the parasitic signals located close to the carrier's frequency, but at the cost of extra efforts in the controller design.

⁷PLL stands for phase-locked loop.

4.6.5 Input filter of the converter

As explained previously, the filter adds inertia in the system because it slows down the dynamics of the voltage command that tries to reach the SA. However, the dynamics altering the power flow from the SA to the bus current should also have been taken into account. This would add a zero in the system as well as an additional phase lag that would reduce the possible control bandwidth of the system.

4.7 Summary

This chapter presented a MPP tracker using the principle of synchronous demodulation to control a dc-dc converter. Its main advantage is that several trackers could work in parallel on the same bus based on a single current measurement, thereby saving extra sensors and their associated conditioning circuits.

Regarding the performances, the system designed in this chapter is able to track the MPP in approximately 50 milliseconds while continuously forcing the solar array to deliver more than 99% of the power that it is capable to produce, under given constraints. The steady state performances are similar to most of the trackers currently on the market, but more advanced control techniques could probably improve the system dynamics as well as its robustness's margins.

Finally, some limitations have also been identified and deserve further investigations. The first drawback of the system lies in the fact that all the information is concentrated at a single frequency. A perturbation located at that specific frequency would therefore prevent the system from working at its MPP; the system would instead stabilize around a non-MPP. The use of a carrier with a larger spectral content could however potentially attenuate this problem.

Moreover, a parasitic signal at a frequency close to that of the carrier would also introduce a beat signal that could pass the PID controller and appear on the solar array voltage. A slower controller would help to reduce this issue but the more reliable way to eradicate the two previously mentioned problems would be to forbid the on-board equipment connected to the bus to produce signals close to the selected carrier's frequency.

The last significant issue would be a phase shift between the measured signal and the carrier during demodulation. Such a situation could severely hamper the system's performances, but could be solved with a Costas loop at the cost of extra material.

Chapter 5

MPPT using PRBS modulation

This chapter is devoted to a slightly modified version of the MPP tracker presented in chapter 4. It will begin with a short introduction putting forward the motivations that led to this new approach, followed by a brief review of the underlying concepts. Some guidelines about the carrier's design will then be established before examining the performances of this type of modulation with respect to those obtained with synchronous demodulation.

5.1 Motivations

The idea to replace the sinusoidal carrier by a pseudo-random bits sequence (PRBS) came from the observation that synchronous demodulation could potentially lose the MPP when exposed to perturbations at the carrier's frequency.

Thanks to its enlarged spectrum, a PRBS is less sensitive to single-frequency disturbances; making it an interesting candidate to supplant the sinusoidal carrier. After some research, it turned out that this principle was already patented in 2011 [11].

5.2 Principle

The use of a PRBS as carrier is related to the *direct-sequence spread spectrum* (DSSS) and results in a noise-like modulated signal. The idea of spread-spectrum techniques is to transmit the information over a bandwidth which is significantly wider than the original message, thereby spreading its power similarly to a noise spectrum. Such techniques were initially developed for military applications to create secure communications. Their robustness against noise and jamming can then be particularly useful to resist to the potential bus current perturbations.

For this application, the modulation scheme can be represented as in figure 5.1: the converter modulates the slope of the PV curve with the PRBS carrier, and the resulting bus current is sensed and cross-correlated with the same carrier to retrieve the sign of the slope.

5.2.1 PRBS generation

Unipolar signal

A pseudo-random bit sequence can be generated with a linear-feedback shift register (LFSR), which is a register whose input bit results from a linear combination (using XOR gates) of bits tapped from of its previous state. This principle is illustrated in figure 5.2.

The carriers' signal is obtained by taking the last bit of the register. A clock signal of period f_{clk} sequentially modifies the state of the register and consequently the value of the carrier. If N is the number

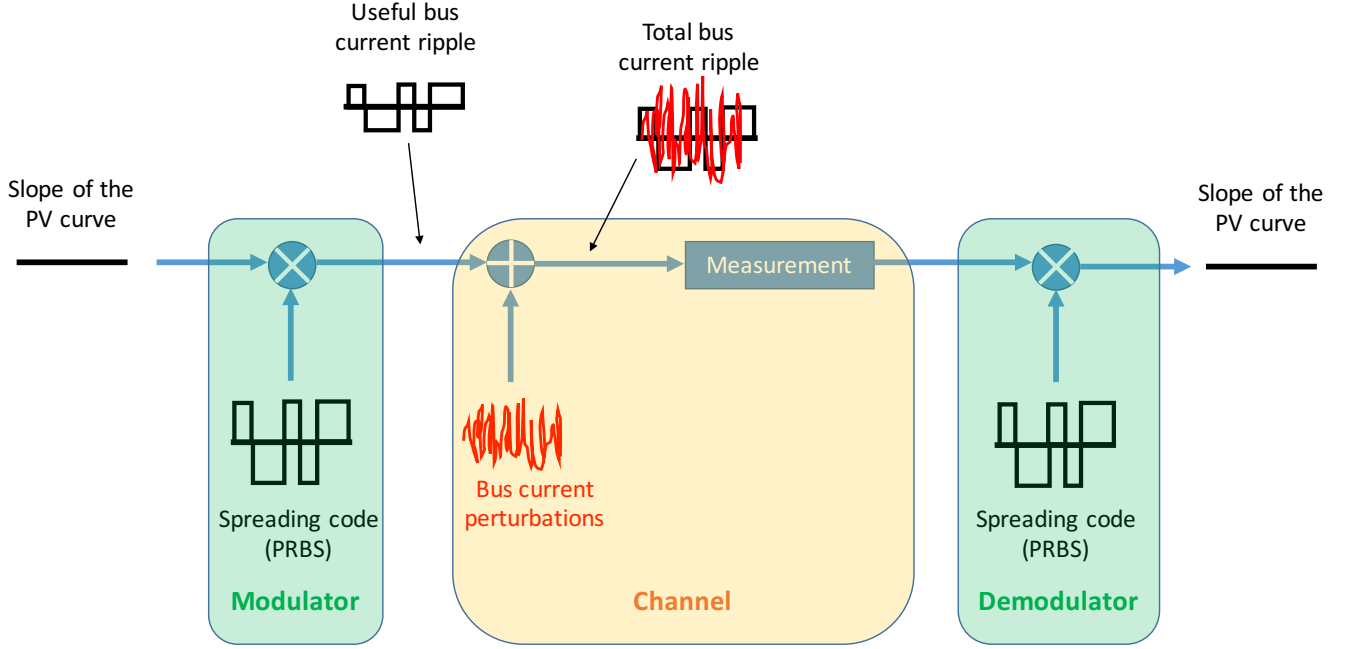


Figure 5.1: Principle of the PRBS modulation.

of bits of the register, and if the taps have been wisely chosen, the register will go through $2^N - 1$ states¹ before repeating the sequence, leading to a period of

$$T_{carrier} = \frac{2^N - 1}{f_{clk}} \quad (5.1)$$

However, this is not true for all linear combinations. Some of them, known as "non-primitive" polynomials lead to a lower periodicity than a maximum-length sequence² (MLS).

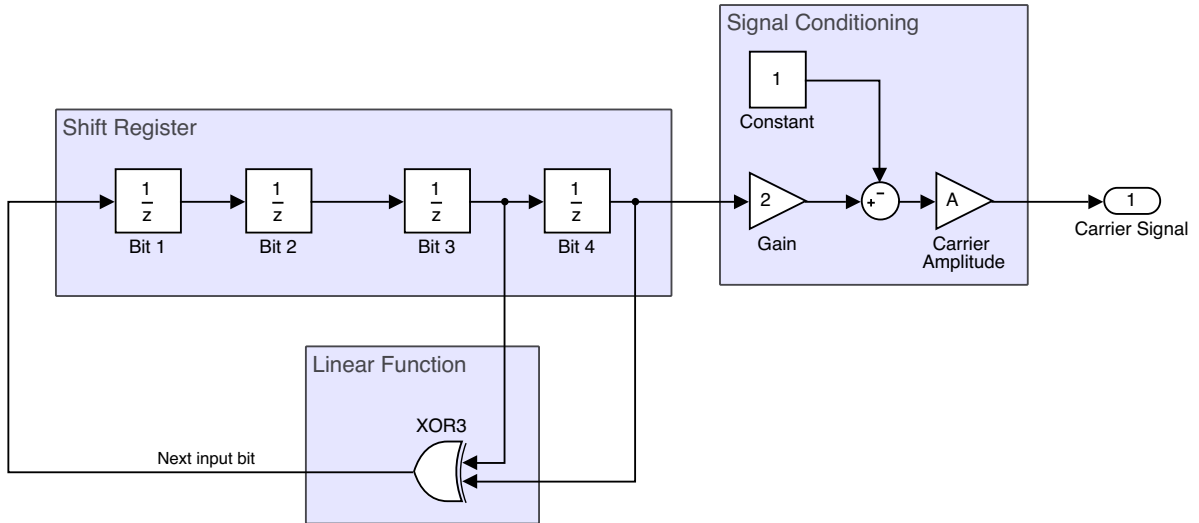


Figure 5.2: Generation of a PRBS using the LFSR principle.

¹The "-1" comes from the fact that the "full-zero" state does not occur; it cannot be used as initial condition neither because the register would be blocked in this state.

²Several combinations leading to MLS are provided in [D](#).

Since the sequence is a special kind of square-wave signal, its Fourier transform corresponds to a *sinc* function³, whose spectrum contains a set of spectral lines called harmonics (see figure 5.3). This discrete aspect is due to the "pseudo-random" character of the sequence; its period is not infinite as it would be for a truly random signal, and as a consequence the harmonics are not infinitely close.

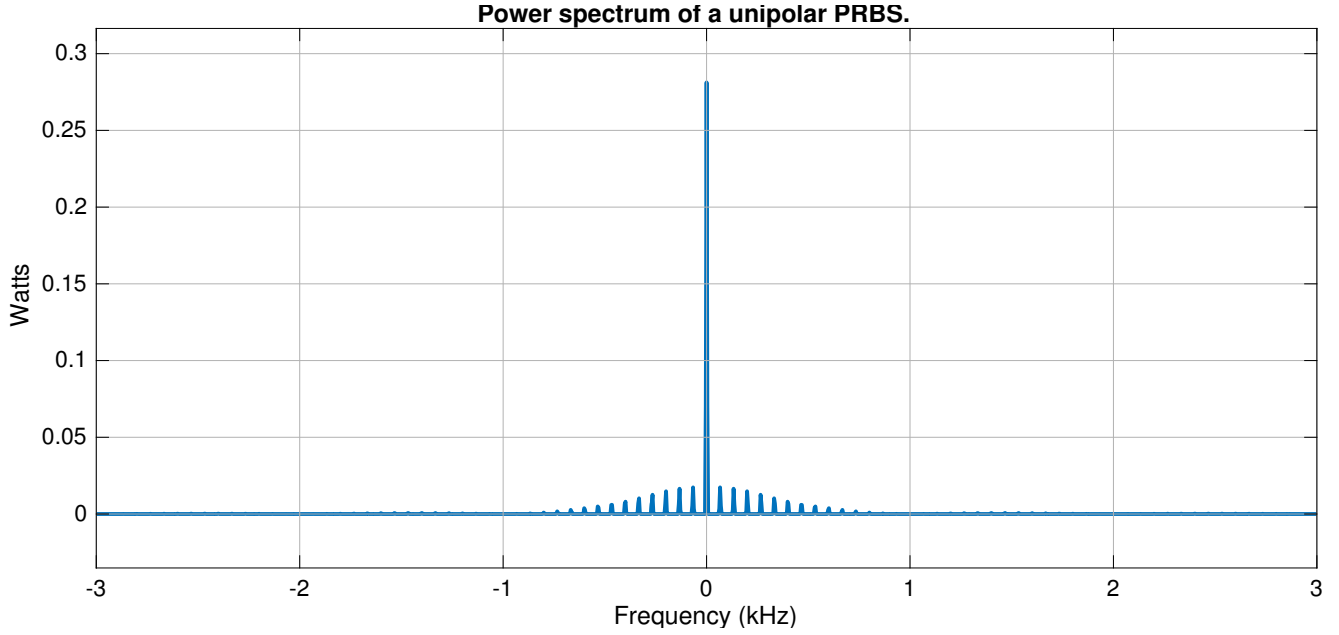


Figure 5.3: Power spectrum of an unipolar PRBS (with $f_{clk} = 1\text{kHz}$ and $N = 4$).

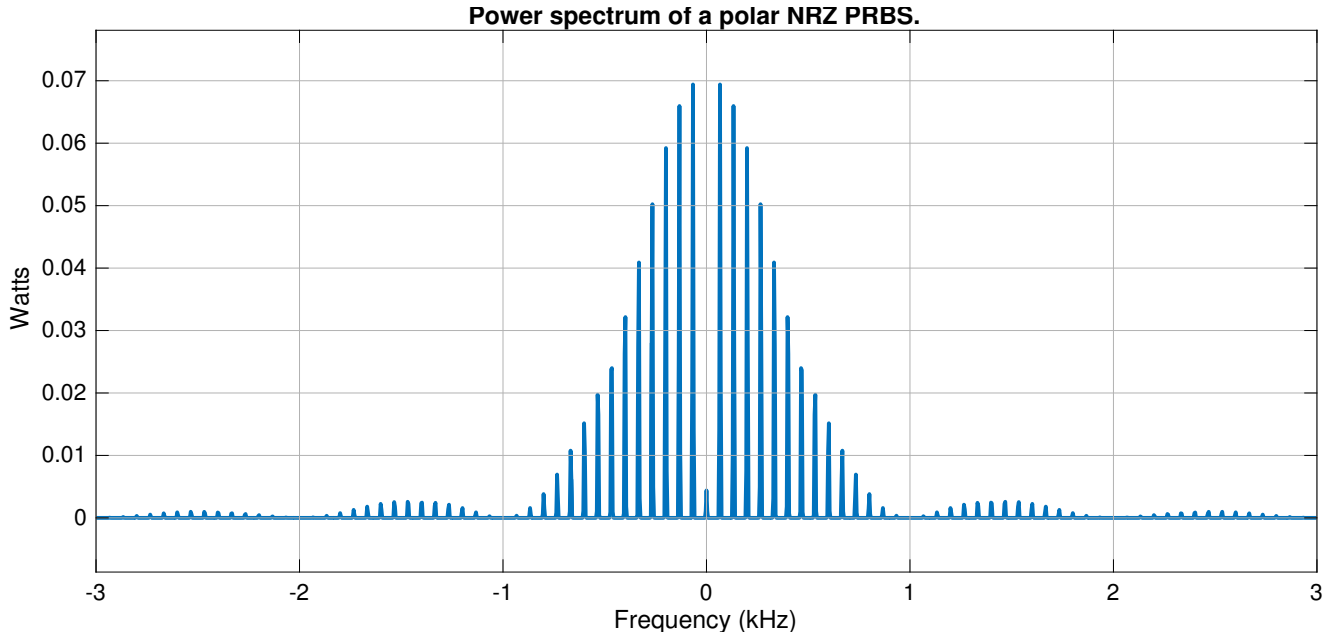


Figure 5.4: Power spectrum of a polar NRZ PRBS (with $f_{clk} = 1\text{kHz}$ and $N = 4$).

³ $\text{sinc}(x) = \frac{\sin(\pi x)}{\pi x}$

From unipolar to bipolar

The problem of the actual sequence lies in the fact that it has an important DC component that would bias the solar array voltage and result in a waste of power; this DC component is due to its *unipolar* character: the value is either 1 or 0 but never negative.

To suppress the DC component, the output of the register is modified to be around 0 (-1 or 1V) and then multiplied by a factor A which modulates the amplitude of the carrier. The resulting sequence is said to be *(bi)polar* (symmetric + and - voltages) and *NRZ* (non-return to zero, because the value is never 0). In practice however, the DC component is not completely removed since the sequence contains one more 1 than -1 (because of the impossible state full of zeros). A slight DC value of $1/(2^N - 1)$ V can then be observed, but it is negligible when the size of the register is sufficiently large.

Apart from this DC component, the first harmonic that represents the lowest frequency component of the carrier is located at $f_{(1)} = 1/T_{carrier} = f_{clk}/(2^N - 1)$; the following lines are found at every multiple of that frequency and the first lobe (called *mainlobe*) ends up at the shifting frequency $f_{(2^N-1)} = f_{clk}$ with a null amplitude. The figure 5.4 represents the spectrum of the polar and NRZ PRBS version. The envelope of its power spectrum is given by

$$\left(\frac{\sin(\pi \frac{f}{f_{clk}})}{\pi \frac{f}{f_{clk}}} \right)^2 \quad (5.2)$$

5.2.2 Autocorrelation of PRBS

The useful information is extracted in the same way as in a synchronous demodulation: the signal is multiplied by the carrier with a mixer. The only difference is that the information is spread over a wide range of frequencies and the multiplication superposes all these pieces of information into a single DC component (to reconstruct the whole message) because all the other harmonics cancel each other. However, parasitic signals will most probably affect the current measurement so the low-pass filter used with the synchronous demodulation will be kept to attenuate the potential non-DC components.

To introduce the carrier's design discussed in the next section, it is important to understand how a parasitic signal affects the spectrum after the mixer stage. To illustrate its impact, we will consider a single sinusoidal signal as perturbation. As a reminder, a multiplication in the time-domain corresponds to a convolution in the frequency domain.

To make things simple, let us dissociate the parasitic sine component (at $\pm f_p$) from the useful information. On the one hand, the correlation of this perturbation with the PRBS carrier will shift the whole PRBS spectrum around $\pm f_p$, modulated by the perturbation's amplitude; on the other hand, the autocorrelation of the PRBS with itself will result in a single DC component. Therefore, the total spectrum is obtained by summing the DC value with the two symmetric shifted sinc spectra. The figures 5.5 and 5.7 illustrate the aforementioned principle in the time-domain and in the frequency-domain, respectively; where the measured signal is modelled as a PRBS (1V of amplitude, 8 bits and 500Hz of shifting frequency) to which a parasitic sine signal is added (amplitude of 5V and frequency of 40Hz).

Finally, as represented in figure 5.6, the delay between the two PRBS sequences should be kept as small as possible to maximize the DC component. But it is an interesting property since it allows several MPPT to share exactly the same bandwidth but each being decorrelated from the others by choosing different initial conditions.

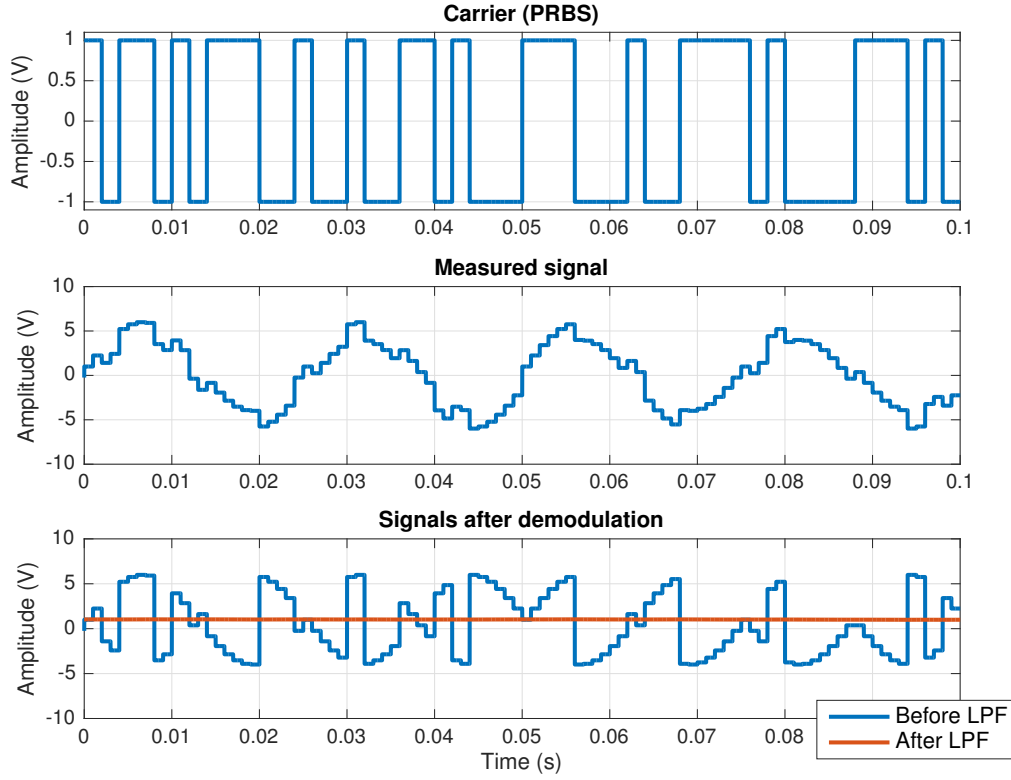


Figure 5.5: Time-domain illustration of the demodulation steps: the carrier (upper graph) is multiplied by the measured signal (middle graph) to obtain a signal (lower graph, blue) whose DC component contains the useful information (lower graph, red).

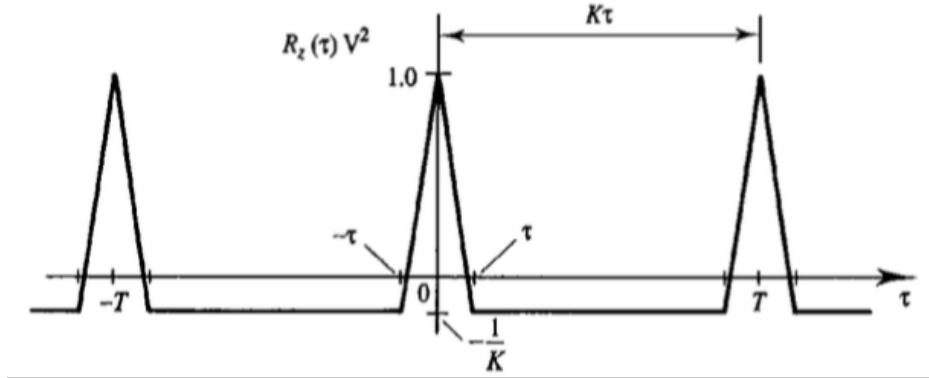


Figure 5.6: Autocorrelation function $R(\tau)$ of a PRBS of length $K = 2^N - 1$ and period $T = 1/f_{(1)}$, as a function of the delay τ between the two PRBS being correlated. With the courtesy of [5].

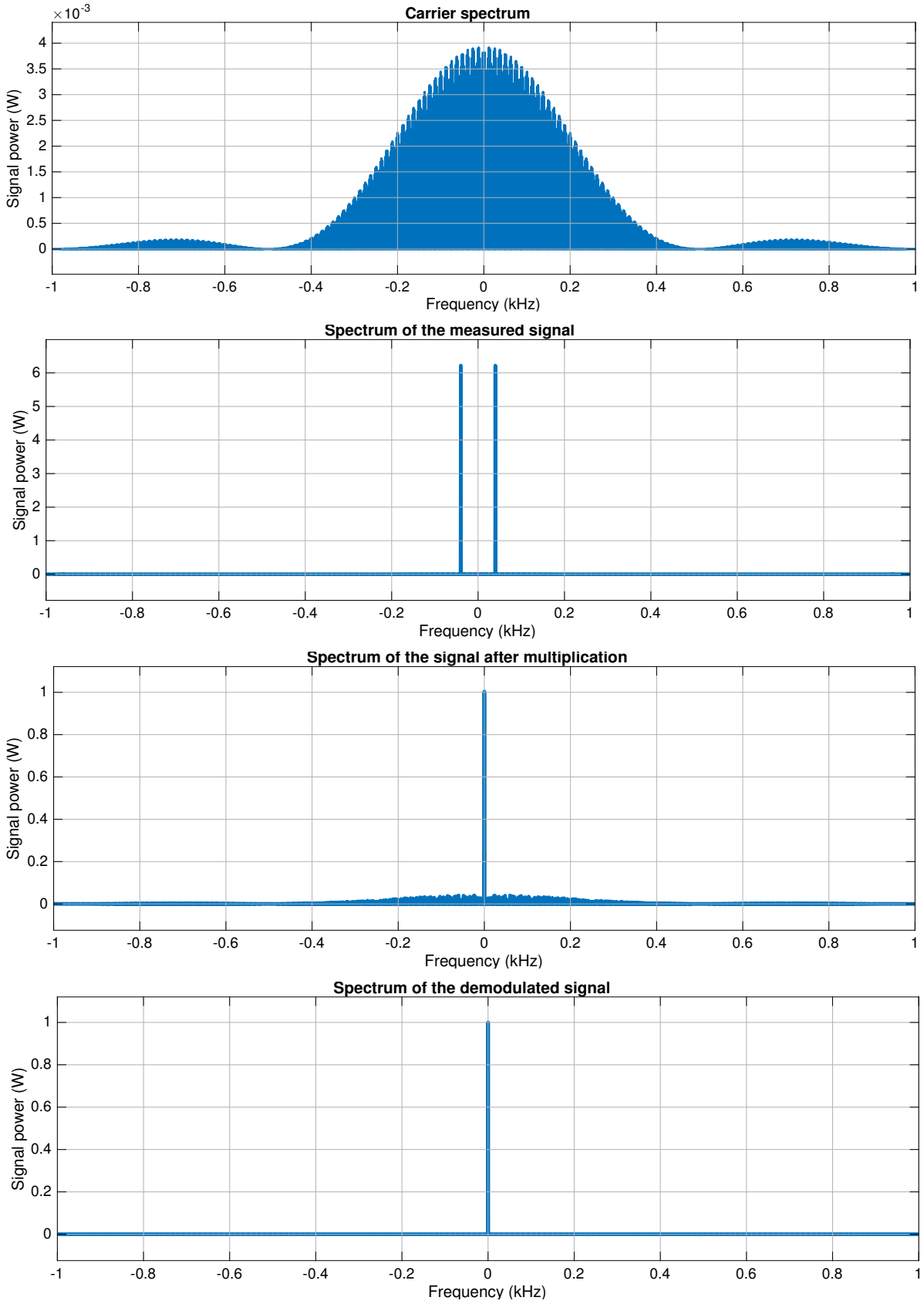


Figure 5.7: Frequency-domain illustration of the demodulation steps: the carrier spectrum (first graph) is convoluted with the spectrum of the measured signal (second graph) to obtain a spectrum (third graph) whose DC component contains the useful information (fourth graph).

5.3 Gibbs phenomenon

5.3.1 Clock's frequency

In theory, the *sinc* function has an infinitely wide spectrum. Since the carrier introduced in the system will have to pass in the buck's input filter, the information contained at high frequencies (i.e. above 1kHz) will be lost. The impact of such a situation is represented in figure 5.8. The power loss associated to sidelobes filtering can be observed in the shape of the time-domain waveform, where the input's filter frequency is varied to keep one, two or three lobes of the *sinc* function. This is known as the *Gibbs phenomenon*: the amplitude of the time-domain overshoot does not vary with the number of unfiltered sidelobes⁴, but the time response does. The autocorrelation of the PRBS is therefore partially reduced (see the lower graph) which modifies the gain of the system.

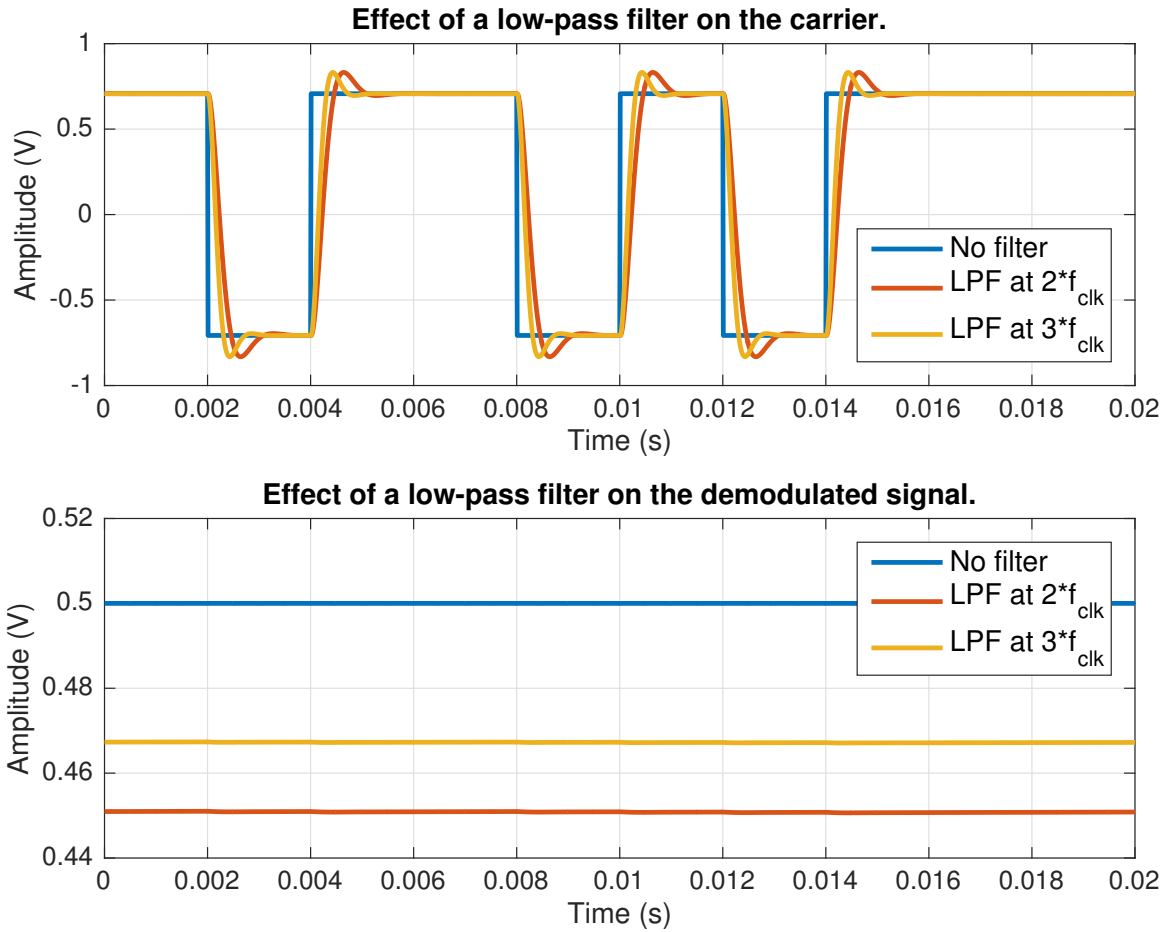


Figure 5.8: Effect of the information loss if we keep two (LPF at 1kHz) or three (LPF at 1.5kHz) lobes of the *sinc* function compared to ideal case (no LPF).

⁴The only way to prevent these oscillations from happening is to keep the whole spectrum.

5.3.2 Carrier's amplitude

In order to reuse the same controller as for the sine-based demodulation, the gain of the system must remain the same. As a reminder, its expression was:

$$G_{sys} = \frac{\Delta s_{demod}}{\Delta V_{SA}} = \frac{1}{2} K_{sens} \left(\frac{v_{SA}^2}{V_{BUS}} \right) \frac{d^2(P_{SA})}{dV_{SA}^2} \Big|_{V_{SA}=\bar{V}_{SA}} \quad (5.3)$$

The factor 1/2 came from the fact that half of the carrier's power was lost due to the filtered double-frequency component. At first sight, the amplitude of the PRBS should then fixed to

$$v_{SA} = \frac{1}{\sqrt{2}} \quad (5.4)$$

to keep the same 1/2 factor in the system's gain seen by the controller.

However, because of the Gibbs phenomenon, the sidelobes filtered out by the buck's input filter represent a power loss. Based on simulations, we have determined the percentage of power remaining after the filter, for different values of the ratio $\frac{f_{clk}}{f_c}$ (f_c is the cut-off frequency of the input filter). The results are listed in table 5.1. It is important to keep in mind that the number of harmonics contained in a single lobe has no effect on these results.

Table 5.1: Power remaining in the signal when the number of lobes kept by the filter varies (with $f_c = 1\text{kHz}$).

f_{clk}	Number of remaining lobes	Remaining power percentage
100 Hz	10	98%
200 Hz	5	96%
333 Hz	3-4	93%
500 Hz	2	90%
1 kHz	1	80%

5.4 Robustness

Since the system is the same as in the previous chapter, and since we took the precautions to keep the same gain values, their dynamic behaviour are very similar. What is interesting here is to test whether a PRBS modulation is really able to improve the robustness of the system. The system will then be tested against parasitic signals presenting the same characteristics as those introduced in the previous chapter, i.e. a ripple voltage of 1.5 V (RMS) ranging from 40Hz to 10kHz.

For this analysis, the PRBS's parameters (frequency, amplitude and register size) will be varied in order to look at the way the system reacts against each of them, and the best configuration will then be compared to the results obtained by synchronous demodulation.

5.4.1 Impact of the clock's frequency

To analyze the effect of the clock's frequency, the register size is fixed to $N = 4$ and the amplitude will be adapted to the number of unfiltered lobes (see table 5.1) to maintain the same gain in the system. Three shift frequencies have been tested, namely 10Hz, 100Hz and 1kHz and the resulting steady state

performance of the MPP tracker are represented in figure 5.9. In the following paragraph, the three cases will be identified by the letters $\alpha = 10\text{Hz}$, $\beta = 100\text{Hz}$ and $\gamma = 1\text{kHz}$.

From these results, it appears that a clock's frequency of 1kHz (γ) leads globally to better results than the two other options tested; it is the only configuration keeping an extraction ratio higher than 99% whatever the frequency of the parasitic signal present on the bus. For low-frequency disturbances, the beat effect is not very significant with γ since the PRBS spectrum shifted around the perturbation frequency has less harmonics close to DC than the two other cases⁵. At 1kHz however, the two slower sequences α and β do not suffer from that beat effect any more and achieve similar performances than that of γ . Finally, the results against the perturbations at 10kHz can be explained by the fact that the correlation of the carrier with a filtered version of itself does not result in a single DC component any more, but also generate harmonics which are especially important at the multiples of the clock's frequency. For that reason, γ presents better performances than its opponents since these parasitic harmonics are first attenuated by the output demodulation filter and then even more by the input filter of the converter.

For theses reasons, the following tests will be performed with a clock's frequency of 1kHz.

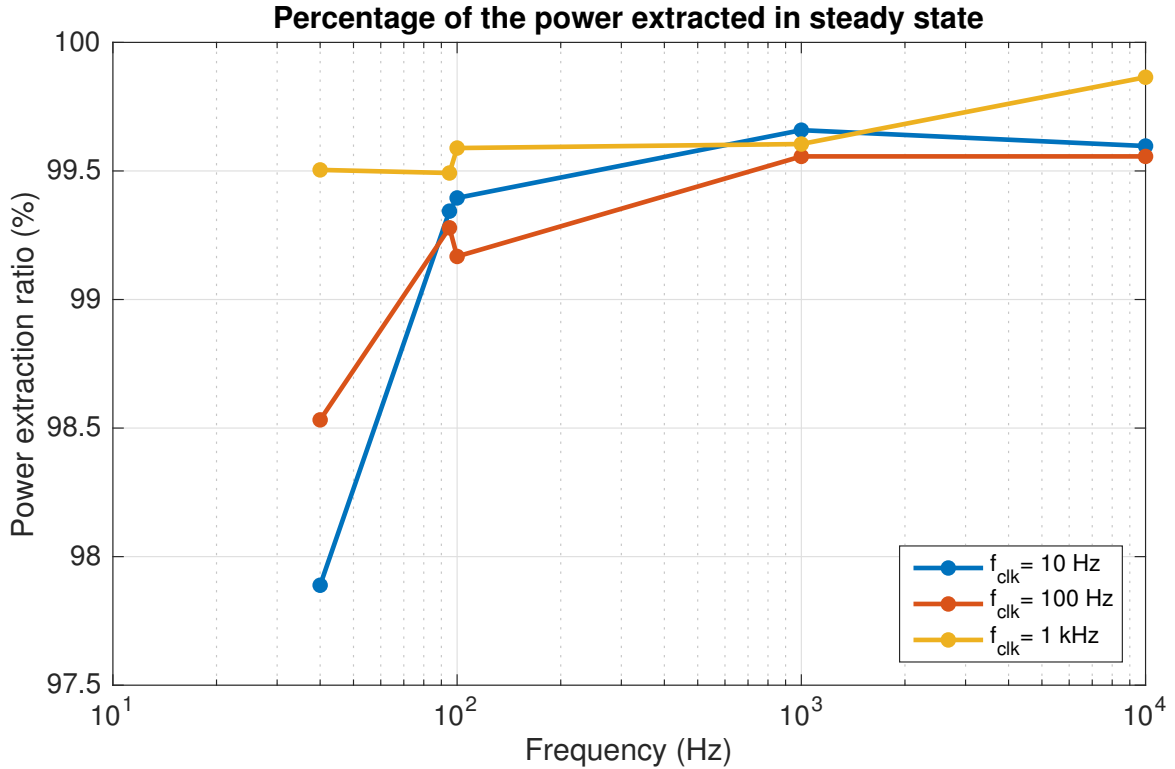


Figure 5.9: Effect of f_{clk} on the steady state performances of the MPPT.

5.4.2 Impact of the register size

In order to understand how the harmonics' density affect the system's robustness, several tests have been performed with different sizes: 4, 8 and 16 bits. The performances achieved by each of these configurations are depicted in figure 5.10. According to what we saw in the previous section about the harmonics' spacing, we can expect that a reduced number of bits will lead to better performances than very large registers.

⁵The space between harmonics increases with the clock's frequency.

Compared to the clock's frequency, the register size seems to have a lower influence on the performances of the system. Nonetheless, the results confirm that smaller register sizes allow to extract a bigger portion of the power that the SA is able to produce. As explained above, this is due to the fact that a denser PRBSs' spectrum will bring more harmonics close to DC.

Here also, the bigger performance variability between the tested configurations occur under low frequency perturbations; the beat effect discovered in the previous chapter still seem to cause efficiency problems by preventing undesirable signals to be attenuated.

For the last analysis about the carrier's amplitude, a register size of $N = 4$ will then be maintained.

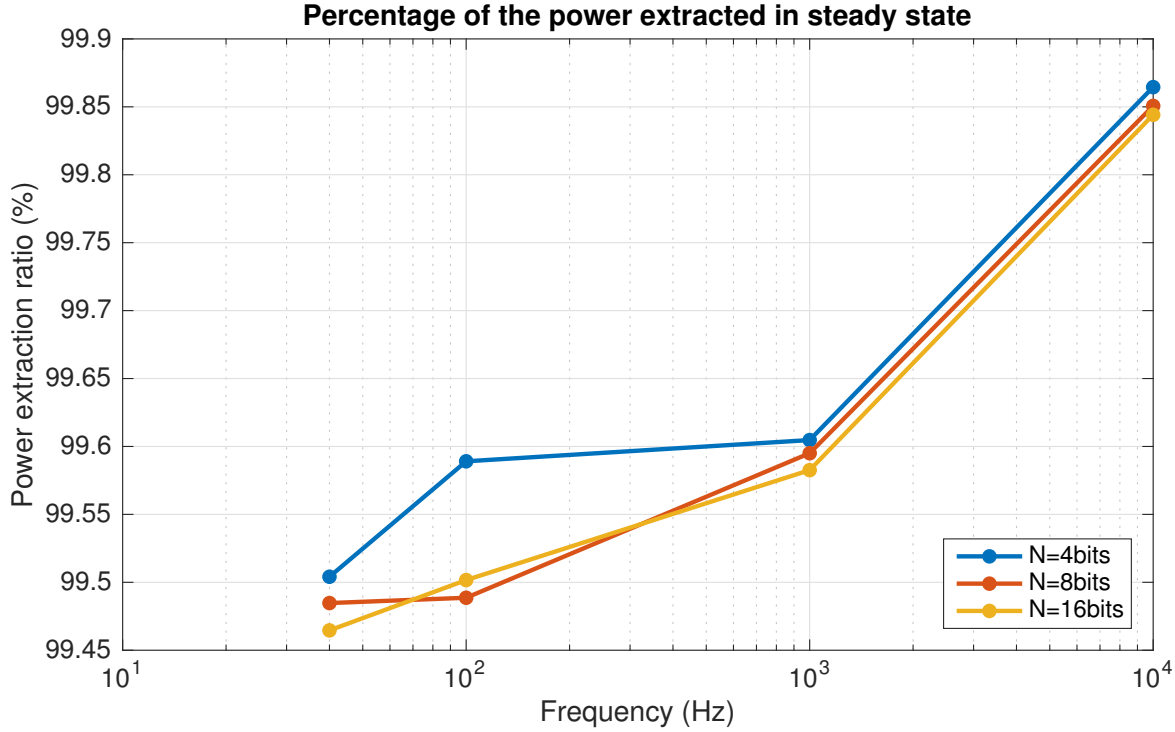


Figure 5.10: Effect of the register size N on the steady state performances of the MPPT.

5.4.3 Impact of the carrier's amplitude

The last parameter to play with is the carrier's amplitude. The amplitudes tested are given by

$$v_{SA} = K \frac{1}{\sqrt{2}} \frac{1}{0.8} \quad (5.5)$$

with the following values of K : 50mV, 100mV, 500mV and 1V. The factors $1/\sqrt{2}$ and $1/0.8$ are there to keep the same gain as for synchronous demodulation; the first factor has been explained before and the second takes into account that the carrier introduced in the converter loses all its sidelobes (keeps its mainlobe only) due to the buck's input filter.

The results, presented in figure 5.11, could have been predicted from what we saw in the synchronous demodulation: if the amplitude is too small, the impact of the perturbations becomes more important. However, from a given value (above 500mV in this case), the losses generated by the "desired" oscillations exceed those that were caused by the perturbations, thereby reducing the overall efficiency. As for the synchronous demodulation, there is a trade-off to make between the "desired" and undesired losses; an

amplitude of 500mV seems here to be the best compromise among the tested configurations.

It should be noted that, above a certain amplitude, the PRBS does not show a strong dependence with the perturbations' frequency. It comes from the fact that the power associated to the DC component increases with the square of the carrier's amplitude; the harmonics then become less significant in comparison to the other cases. This effect was also present in the sine-based modulation.

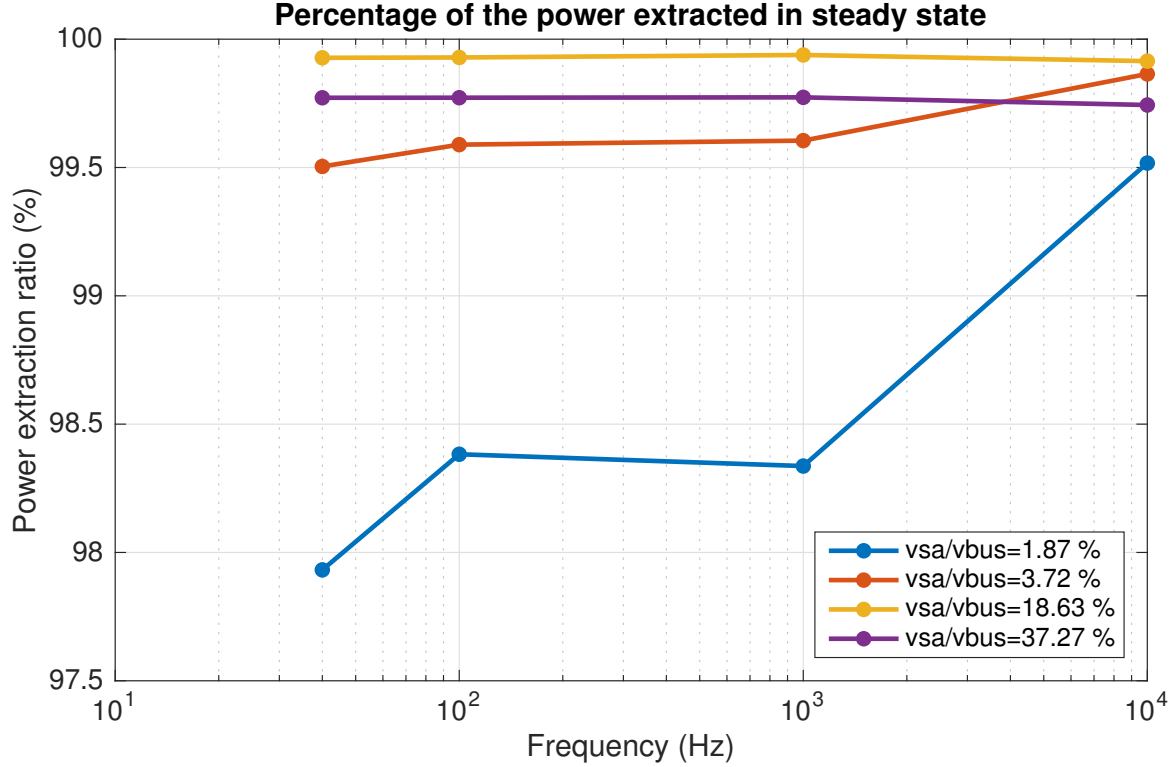


Figure 5.11: Effect of the amplitude v_{SA} on the steady state performances of the MPPT.

5.5 Comparison of both techniques

Finally, both techniques (synchronous demodulation and PRBS modulation) are compared to see whether the PRBS really improved the performances. For both cases, an amplitude of 500mV was chosen since it is the value that lead to the best results in the two situations⁶. The graph comparing the best performances of both types of modulation is depicted in figure 5.12.

As we can see, with these amplitudes, both systems are able to extract more than 99.9% of the power, regardless of the frequency of the bus' perturbations.

When looking at low-frequencies, the PRBS reaches better performances than its sine counterpart. This is due to the fact that the few harmonics that are transported close to DC have a much lower amplitude than that of the sine carrier; the reduced amplitude of the parasitic components remaining after the output filter therefore lead to a lower voltage ripple on the solar array.

On the contrary, when the perturbations present on the bus have a higher frequency, the sine components are sent far away from DC which result in a high attenuation of the parasitics. Unlike the sine

⁶The PRBS also includes the two correction factors previously discussed.

carrier, the PRBS's shifted spectrum still presents some harmonics at low frequencies thereby causing a small beat effect. This beat is more important for disturbances at 10kHz than at 1kHz since the PRBS's spectrum is null at the clock's frequency (1kHz) being shifted to DC, and the surrounding harmonics have a smaller amplitude than in the middle of the mainlobe.

As a conclusion, the PRBS slightly improves the performances at low frequencies but causes more important losses when the bus is subject to high-frequency parasitic signals.

However, another important consideration should not be forgotten. With PRBS, several MPP trackers can share the same frequency band without significantly interfering between each other by simply using different initial conditions (that can be assimilated to a delay of more than $1/f_{clk}$); the sine-based modulation requires on the contrary to carefully choose the different frequencies at which they will operate. Moreover, the PSD of a PRBS is also significantly lower than that of a sine with the same amplitude, making it more suited in applications with stronger EMC requirements.

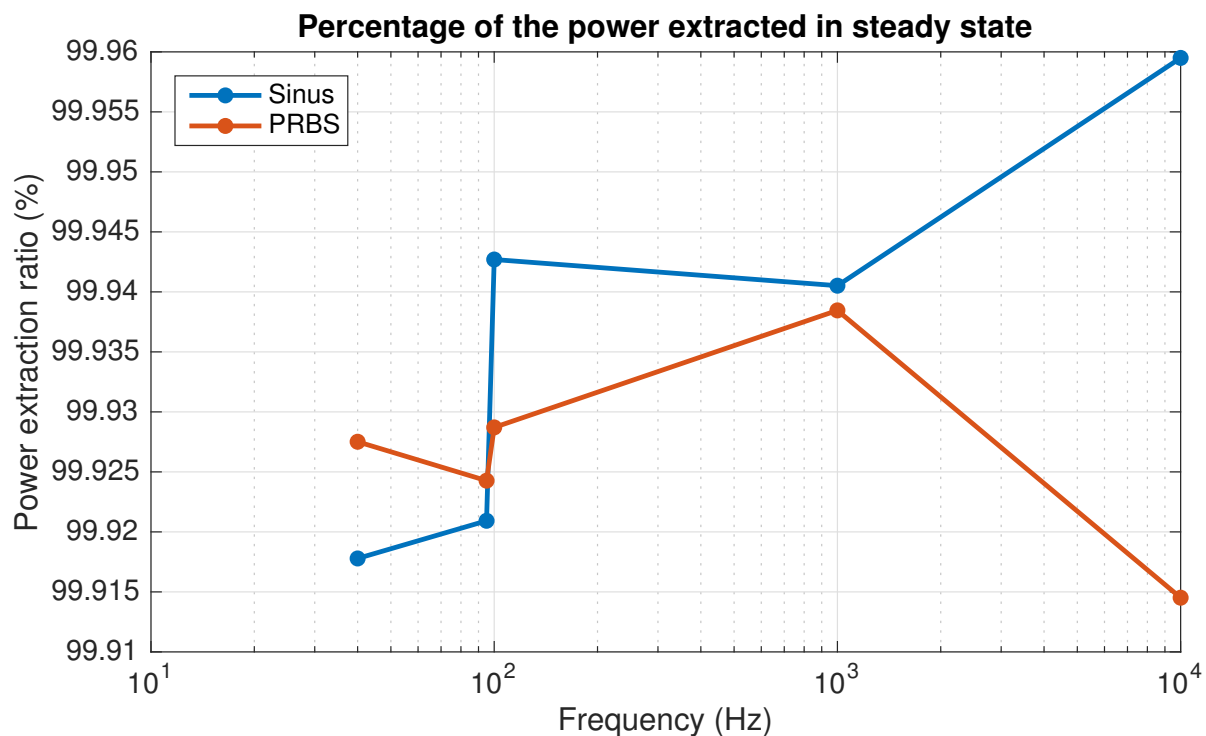


Figure 5.12: Comparison of the two best configurations in sine-based and PRBS modulations.

5.6 Limitations and possible improvements

5.6.1 Input filter of the converter

Because of the buck's input filter, the bandwidth available to spread the PRBSs' spectrum is significantly reduced. A higher cut-off frequency would allow to add even more space between the harmonics, thereby improving the robustness performances against the bus perturbations that could affect the system.

This technique would then benefit from applications with converters' switching frequencies of several MHz for which a higher cut-off frequency would be possible.

Of course, we should keep in mind that all these modulations add their own perturbations on the bus and could potentially disturb other equipments connected to that bus. For that reason, this solution asks

for a prior information over the EMC requirements of the bus to know whether it would be suitable for this application.

5.6.2 Time delays

As for the sine-based modulation, a time delay could severely hamper the performances of the system because the DC component resulting from the autocorrelation would be affected, thereby modifying the gain of the system. Moreover, this time delay could potentially interfere with the other trackers working on the same bus if the initial conditions of the LFSRs were badly chosen, especially if their size is small.

However, as for the synchronous demodulation, a Costas loop could be used to synchronise the sequences. Other solutions based on learning sequences also exist, but the implementation details exceed the scope of this work.

Chapter 6

Conclusion

This paper presented a MPP tracker making use of the correlation principle to control a dc-dc converter. The main advantage of this algorithm lies in the fact that several trackers are able to work in parallel on the same bus, based on a single and identical current measurement. As a consequence, this solution allows to save the costs of the potential sensors that would have been used instead, as well as the cost related to their conditioning circuits.

With regard to the performances, the system designed in this paper achieves a reasonable dynamic behaviour; in case of a modification of the temperature or illumination conditions, the MPPT brings the system back to the MPP in approximately 50 milliseconds. For most applications, such a reactivity is maybe not necessary and could instead be traded against robustness.

In terms of static performances, the two MPPT versions, namely the sine-based and the PRBS-based, are able to extract more than 99.9% of the available power, which is a promising result. It should however be noted that this value does not take into account the power necessary to feed the external circuit nor the losses generated inside the dc-dc converter.

The two methods tested lead to relatively similar results; the PRBS is slightly more robust against low-frequency bus perturbations ($< 1\text{kHz}$) but becomes less performing when their frequency increases. Another important consideration is that PRBSs generate bus perturbations over a wider spectrum but with a reduced power spectral density compared to the sine-based solution. The appropriate technique should then be determined based on the bus EMC requirements.

Finally, some limitations have also been identified and deserve further investigations. The greatest danger that would severely impact both solutions would be a delay during the correlation. Such a situation could in the best case only reduce the system's reactivity and robustness, but could also lead to an unstable control loop. Several solutions exist to synchronise two signals together; among them, we presented the well-known Costas loop often used in DSB-SC modulations. The other problem observed was the sensibility of the sine-based modulation to the bus perturbations with a similar frequency. If the frequency is exactly the same, the SA operating point is slightly shifted from the MPP but not enough to significantly impact the performances; if the frequency is however close to it but exactly equal, a way less desirable beat phenomenon occurs which amplifies the oscillations around the MPP. Hopefully, it appeared that increasing the carrier's amplitude significantly reduced the problem. Another solution could have been to enlarge the frequency spectrum of the carrier to desensitize the system from the perturbations' frequency. This is the reason why a PRBS-based modulation has then been implemented, and it appeared to solve the problem at low-frequency but introduced another at higher frequencies, leading to similar performances.

As a conclusion, these two methods have lead to quite promising results but would require a practical implementation to verify that the performances can be as high as those obtained from these simulations.

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Appendices

A System modeling - Analytical expressions

A.1 First derivative of the solar array power

The analytical expression of the first derivative of the solar array power (with respect to the voltage) can be expressed as

$$\frac{d(P_{sa})}{dV_{sa}} = \frac{d(V_{sa}I_{sa})}{dV_{sa}} \quad (\text{A.1})$$

$$= \frac{d(V_{sa})}{dV_{sa}} I_{sa} + V_{sa} \frac{d(I_{sa})}{dV_{sa}} \quad (\text{A.2})$$

$$= \left(I_{sa} + \frac{V_{sa}}{R_{sa}} \right) \quad (\text{A.3})$$

It can already be noted here that the second term is negative, because the slope of the I-V curve is always negative and is equal to the inverse of the solar array resistance $1/R_{sa}$.

But this expression can be further developed since

$$\frac{1}{R_{sa}} = \frac{d(I_{sa})}{dV_{sa}} \quad (\text{A.4})$$

$$= \frac{d \left(I_{sc} - I_o \left(\exp \left(\frac{V_{sa}}{V_t} \right) - 1 \right) \right)}{d(V_{sa})} \quad (\text{A.5})$$

$$= \frac{1}{V_t} \left(-I_o \exp \left(\frac{V_{sa}}{V_t} \right) \right) \quad (\text{A.6})$$

$$= \frac{1}{V_t} (I_{sa} - I_{sc} + I_o) \quad (\text{A.7})$$

$$\approx \frac{1}{V_t} (I_{sa} - I_{sc}) \quad (\text{A.8})$$

We can then finally write

$$\boxed{\frac{d(P_{sa})}{dV_{sa}} \approx I_{sa} + \frac{V_{sa}}{V_t} (I_{sa} - I_{sc})} \quad (\text{A.9})$$

A.2 Second derivative of the solar array power

Starting from the relation A.9 computed in the previous section, it is possible to derive the expression of the second derivative of the power with respect to the voltage :

$$\frac{d^2(P_{sa})}{d(V_{sa})^2} = \frac{d \left(I_{sa} + \frac{V_{sa}}{V_t} (I_{sa} - I_{sc}) \right)}{d(V_{sa})} \quad (\text{A.10})$$

$$= \frac{d(I_{sa})}{dV_{sa}} + \frac{1}{V_t} \left(\frac{d(P_{sa})}{dV_{sa}} - \frac{d(V_{sa})}{dV_{sa}} I_{sc} \right) \quad (\text{A.11})$$

$$= \frac{1}{R_{sa}} + \frac{1}{V_t} \left(I_{sa} + \frac{V_{sa}}{R_{sa}} - I_{sc} \right) \quad (\text{A.12})$$

$$= \frac{1}{R_{sa}} \left(2 + \frac{V_{sa}}{V_t} \right) \quad (\text{A.13})$$

And if we combine this result with the equation A.8, it leads to:

$$\boxed{\frac{d^2(P_{sa})}{d(V_{sa})^2} \approx \frac{1}{V_t} (I_{sa} - I_{sc}) \left(2 + \frac{V_{sa}}{V_t} \right)} \quad (\text{A.14})$$

B Output current of the converter

In order to analyze the output current, we will sequentially develop the expressions of the solar array voltage and current, and finally combine them.

B.1 Solar array voltage

In this method, the duty cycle θ applied to the converter is the sum of an average component Θ regulating the operating point of the array and a small oscillating perturbation $\tilde{\theta} \cos(\omega_p t)$. If we combine that with the relation 2.8 that we established previously, we can write

$$V_{sa} = \frac{V_{BUS}}{\theta} \quad (\text{B.15})$$

$$= \frac{V_{BUS}}{\Theta + \tilde{\theta} \cos(\omega_p t)} \quad (\text{B.16})$$

By using a 2^{nd} order Taylor development, we can approximate V_{sa} by the relation:

$$V_{sa} \approx \frac{V_{BUS}}{\Theta} \left(1 - \left(\frac{\tilde{\theta}}{\Theta} \right) \cos(\omega_p t) + \left(\frac{\tilde{\theta}}{\Theta} \right)^2 \cos^2(\omega_p t) \right) \quad (\text{B.17})$$

$$\approx V_{SA} (1 - \theta_r \cos(\omega_p t) + \theta_r^2 \cos^2(\omega_p t)) \quad (\text{B.18})$$

where $V_{SA} = \frac{V_{BUS}}{\Theta}$ and $\theta_r = \frac{\tilde{\theta}}{\Theta}$.

Since $\theta_r \ll 1$, the first order approximation is already sufficient

$$\boxed{V_{sa} \approx V_{SA} (1 - \theta_r \cos(\omega_p t)) = V_{SA} - v_{sa} \cos(\omega_p t)} \quad (\text{B.19})$$

with $v_{sa} = V_{SA} \theta_r$

The ripple voltage reaching the solar array is therefore a sinusoidal signal at the same frequency as that generated by oscillator.

B.2 Solar array current

If we put the previous result (equation B.19) in the current expression of the solar array (equation 2.3), it leads to:

$$I_{sa} \approx I_{sc} - I_o \left(\exp \left[\frac{V_{SA}}{V_t} (1 - \theta_r \cos(\omega_p t)) \right] - 1 \right) \quad (\text{B.20})$$

$$\approx I_{sc} - I_o \left(\exp \left[\frac{V_{SA}}{V_t} \right]^{[1 - \theta_r \cos(\omega_p t)]} - 1 \right) \quad (\text{B.21})$$

$$\approx I_{sc} - I_o \left(\exp \left[\frac{V_{SA}}{V_t} \right] \left(1 - \frac{V_{SA}}{V_t} \theta_r \cos(\omega_p t) \right) - 1 \right) \quad (\text{B.22})$$

$$\approx I_{SA} + \left(I_o \exp \left[\frac{V_{SA}}{V_t} \right] \frac{V_{SA}}{V_t} \theta_r \right) \cos(\omega_p t) \quad (\text{B.23})$$

$$\approx I_{SA} + \left(\frac{I_o}{V_t} \exp \left[\frac{V_{SA}}{V_t} \right] \right) v_{sa} \cos(\omega_p t) \quad (\text{B.24})$$

$$\approx I_{SA} + \left(\frac{-1}{R_{SA}} \right) v_{sa} \cos(\omega_p t) \quad (\text{B.25})$$

And then

$$\boxed{I_{sa} \approx I_{SA} - i_{sa} \cos(\omega_p t)} \quad (\text{B.26})$$

where $I_{SA} = I_{sa}(V_{sa} = V_{SA})$ is the DC component of the current and $i_{sa} = \frac{v_{sa}}{R_{SA}}$ is the peak-to-peak amplitude of the alternating component. The current ripple is then in phase opposition with the voltage ripple.

B.3 Bus current

Finally, if we assume the converter to be ideal, the SA power is entirely transferred to the bus. If the bus voltage V_{BUS} is fixed, we can then write that:

$$I_{bus} = \frac{1}{V_{BUS}} V_{sa} I_{sa} \quad (\text{B.27})$$

$$\approx \frac{1}{V_{BUS}} (V_{SA} - v_{sa} \cos(\omega_p t)) (I_{SA} - i_{sa} \cos(\omega_p t)) \quad (\text{B.28})$$

$$\approx \frac{1}{V_{BUS}} (V_{SA} I_{SA} - (V_{SA} i_{sa} + v_{sa} I_{SA}) \cos(\omega_p t) + v_{sa} i_{sa} \cos(\omega_p t)^2) \quad (\text{B.29})$$

Since the ripples are supposed to be way smaller than the DC value, the 2nd order term can be neglected, resulting in small-signal bus current component of:

$$\boxed{i_{bus} = \frac{-1}{V_{BUS}} (V_{SA} i_{sa} + v_{sa} I_{SA}) \cos(\omega_p t)} \quad (\text{B.30})$$

Since at MPP, the dynamic impedance of the SA (v_{sa}/i_{sa}) is equal to the opposite of its static impedance (V_{SA}/I_{SA}); the ripple's amplitude is then zero at MPP.

C Output inductor dimensioning

The size of the output inductor L_o of a buck converter determines the current ripple allowed at the output. For this application, let's assume that the output ripple ΔI_{bus} has to be lower than 0.5% of the average current I_{BUS} (at MPP and at 25°C).

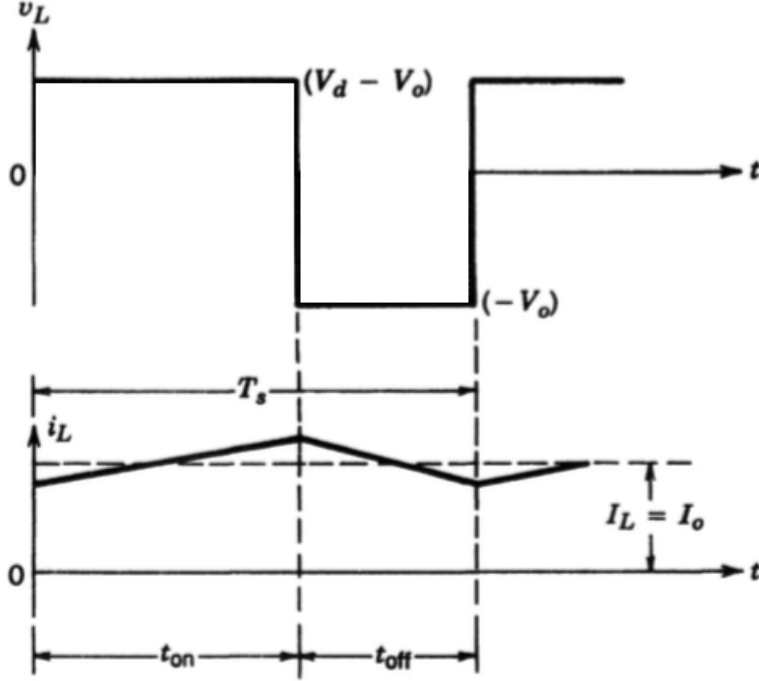


Table C.1: Data used to dimension the output inductor of the buck converter.

P_{SA}	800 W
V_{SA}	70 V
V_{BUS}	35 V
θ	0.5
f_{sw}	50 kHz

Figure C.1: Illustration of the voltage v_L across the inductor and of the current i_L flowing through it. V_d and V_o respectively correspond to V_{SA} and V_{BUS} . With the courtesy of [12].

From figure C.1, from the buck's equation $V_{SA}\theta = V_{BUS}$ and from the inductor's fundamental equation $v_L = L(di_L/dt)$, the half of the peak-to-peak amplitude of the current ripple can be expressed as:

$$\Delta I_{bus} = \frac{1}{2} \frac{(V_{SA} - V_{BUS})}{L_o} \theta T_{sw} \quad (C.31)$$

$$= \frac{1}{2} \frac{V_{BUS}}{L_o f_{sw}} (1 - \theta) \quad (C.32)$$

If we assume that the converter is ideal, i.e. that it does not dissipate any energy, and that the solar array operates at MPP at a temperature of 25°C, we can express the average current as:

$$I_{BUS} = \frac{P_{SA}}{V_{BUS}} \quad (C.33)$$

The equation used to dimension the inductor is then given by:

$$\frac{\Delta I_{bus}}{I_{BUS}} = \frac{1}{2} \frac{V_{BUS}^2}{L_o f_{sw} P_{SA}} (1 - \theta) \quad (C.34)$$

For a ripple current of 0.5% with the data¹ listed in table C.1, an inductor of

$$\boxed{L_o = 1.5mH} \quad (C.35)$$

is required.

¹All the data are computed at MPP and at 25°C.

D Maximum-length sequences

For a PRBS to reach a periodicity of $2^N - 1$ and be considered as a MLS (maximum-length sequence), the XOR gates of the feedback loop have to combine the right bits. For certain register sizes, it is possible to achieve a maximum periodicity thanks to a single XOR gate. The figure D.2 lists which tap index n has to be selected as a function of the register size m (for the configurations where a single-tap is sufficient).

Since we are dealing with binary numbers, it is common to select a multiple of 8 (a byte). The table provided in figure D.3 therefore lists possible taps combinations leading to a MLS.

Table 13.14 Single-tap LFSRs

m	n	length	m	n	length	m	n	length
3	2	7	49	40	5.6e14	108	77	3.2e32
4	3	15	52	49	4.5e15	111	101	2.6e33
5	3	31	55	31	3.6e16	113	104	1.0e34
6	5	63	57	50	1.4e17	118	85	3.3e35
7	6	127	58	39	2.9e17	119	111	6.6e35
9	5	511	60	59	1.2e18	121	103	2.7e36
10	7	1023	63	62	9.2e18	123	121	1.1e37
11	9	2047	65	47	3.7e19	124	87	2.1e37
15	14	32767	68	59	3.0e20	127	126	1.7e38
17	14	1.3e5	71	65	2.4e21	129	124	6.8e38
18	11	2.6e5	73	48	9.4e21	130	127	1.4e39
20	17	1.0e6	79	70	6.0e23	132	103	5.4e39
21	19	2.1e6	81	77	2.4e24	134	77	2.2e40
22	21	4.2e6	84	71	1.9e25	135	124	4.4e40
23	18	8.4e6	87	74	1.5e26	137	116	1.7e41
25	22	3.4e7	89	51	6.2e26	140	111	1.4e42
28	25	2.7e8	93	91	9.9e27	142	121	5.6e42
29	27	5.3e8	94	73	2.0e28	145	93	4.5e43
31	28	2.1e9	95	84	4.0e28	148	121	3.6e44
33	20	8.6e9	97	91	1.6e29	150	97	1.4e45
35	33	3.4e10	98	87	3.2e29	151	148	2.9e45
36	25	6.9e10	100	63	1.3e30	153	152	1.1e46
39	35	5.5e11	103	94	1.0e31	159	128	7.3e47
41	38	2.2e12	105	89	4.1e31	161	143	2.9e48
47	42	1.4e14	106	91	8.1e31	167	161	1.9e50

Figure D.2: Tap index n leading to a MLS ($2^m - 1$) when a single XOR is used. With the courtesy of [7].

Table 13.15 Multiple-of-8 LFSRs

m	taps	length	m	taps	length
8	4, 5, 6	255	96	47, 49, 94	7.9e28
16	4, 13, 15	64K	104	93, 94, 103	2.0e31
24	17, 22, 23	16M	112	67, 69, 110	5.2e33
32	1, 2, 22	4G	120	2, 9, 113	1.3e36
40	19, 21, 38	1.1e12	128	99, 101, 126	3.4e38
48	20, 21, 47	2.8e14	136	10, 11, 135	8.7e40
56	34, 35, 55	7.2e16	144	74, 75, 143	2.2e43
64	60, 61, 63	1.8e19	152	86, 87, 151	5.7e45
72	19, 25, 66	4.7e21	160	141, 142, 159	1.5e48
80	42, 43, 79	1.2e24	168	151, 153, 166	3.7e50
88	16, 17, 87	3.1e26			

Figure D.3: Tap indices leading to a MLS ($2^m - 1$) when the size is a multiple of 8. With the courtesy of [7].

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